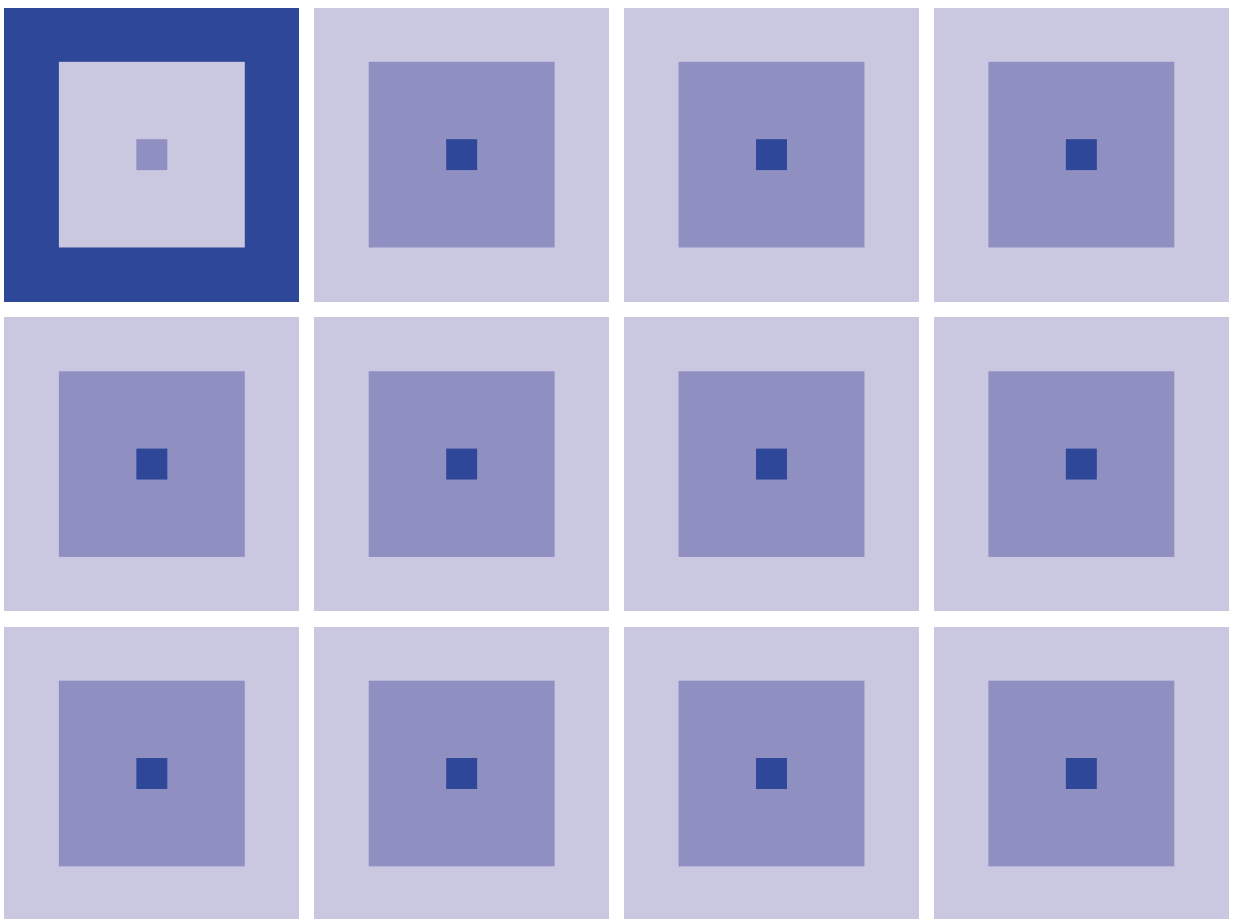
MF924-02

EPSON

GATE ARRAY

S1L35000 Series
DESIGN GUIDE



ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

NOTICE

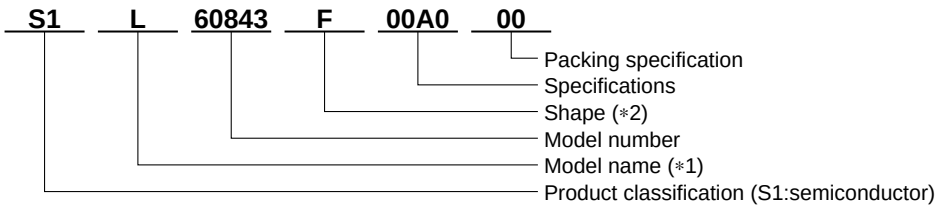
No part of this material may be reproduced or duplicated in any from or by any means without the written permission of EPSON. EPSON reserves the right to make changes to this material without notice. EPSON does not assume any liability of any kind arising out of any inaccuracies contained in this material or due to its application or use in any product or circuit and, further, there is no representation that this material is applicable to products requiring high level reliability, such as, medical products. Moreover, no license to any intellectual property rights is granted by implication or otherwise, and there is no representation or warranty that anything made in accordance with this marerial will be free from any patent or copyright infringement of a third party. This material or portions there of may contain techology or the subject relating to strategic products under the control of the Forign Exchange and Foreign Trade Law of Japan and may require an export license from the Ministry of international Trade and Industry or other approval from another government agency.

The information of the product number change

Starting April 1, 2001 the product number will be changed as listed below. To order from April 1, 2001 please use the new product number. For further information, please contact Epson sales representative.

Configuration of product number

●DEVICES



*1: Model name

K	Standard Cell
L	Gate Array
X	Embedded Array

*2: Shape

B	Assembled on board, COB, BGA
C	Plastic DIP
D	Bare Chip
F	Plastic QFP
H	Ceramic DIP
L	Ceramic QFP

M	Plastic SOP
R	TAB–QFP
T	Tape Carrier (TAB)
2	TSOP (Standard Bent)
3	TSOP (Reverse Bent)

Comparison table between new and previous number

Previous number	New Number
SLA35000 series	S1L35000 series
SLA3504	S1L35043
SLA3506	S1L35063
SLA3509	S1L35093
SLA3516	S1L35163

S1L35000 Series Table of Contents

Chapter 1 Overview

The S1L35000 Series is a family of ultra high-speed VLSI CMOS gate arrays utilizing a 0.6 micron "sea-of-gates" architecture.

1.1 Features of the S1L35000 Series

• Integration	A Max. of 161,841 gates (2 input NAND gate equivalent)
• Operating Speed	Internal gates:0.30 ns (5.0 V Typ.), 0.4 ns (3.3 V Typ.) (2-input power NAND, F/O = 2, Al = 2 mm) Input buffer: 0.48 ns (5.0 V Typ.), 0.63 ns (3.3 V Typ.) (F/O = 2, Al = 2 mm) Output buffer: 2.08 ns (5.0 V Typ.), 2.86 ns (3.3 V Typ.) (C_L = 50 pF)
• Process	CMOS 0.6 µm Al 3 interconnect layers
• I/F Levels	Input/Output TTL/CMOS compatible
• Input Modes	TTL, CMOS, TTL Schmitt, CMOS Schmitt Pull-up and pull-down resistors can be equipped internally (2 types for each resistor value)
• Output Modes	Normal, 3-state, bi-directional
• Output Drive	I_{OL} = 1, 4, 8, 12 mA, selectable (at 5.0 V) I_{OL} = 0.5, 2, 4, 6 mA, selectable (at 3.3V)
• RAM	Asynchronous 1-port, asynchronous 2-port

1.2 Master Structure of the S1L35000 Series

The S1L35000 Series comprises 4 types of masters, from which the customer is able to select the master most suitable.

Table 1-1 Overview of the S1L35000 Series

Master	BC Total	Number of Pads	Number of Columns (X)	Number of Rows (Y)	Cell use ratio (U) *1
S1L35043	41417	110	499	83	65%
S1L35063	64320	130	480	134	60%
S1L35093	95760	162	570	168	55%
S1L35163	161841	210	739	219	50%

NOTE: *1: This is the value when there are no cells, such as RAM cells. The cell use effciency is dependent not only on the scope of the circuits, but also on the number of signals, the number of branches per signal, etc.; thus, use the values in this table only as an estimate.

1.3 Electrical Characteristics and Specifications of the S1L35000 Series

Table 1-2 S1L35000 Absolute Max. Ratings
(V_{SS} = 0 V)

Item	Symbol	Limits	Unit
Power Supply Voltage	V_{DD}	-0.3 to 6.0	V
Input Voltage	V_I	-0.3 to V_{DD} + 0.5	V
Output Voltage	V_O	-0.3 to V_{DD} + 0.5	V
Output Current/Pin	I_{OUT}	± 25	mA
Storage Temperature	T_{STG}	-65 to 150	^oC

Table 1-3 Recommended Operating Conditions for the S1L35000 Series
(For Single Power Supplies)

Item	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	2.70 3.00 4.75 4.50	3.00 3.30 5.00 5.00	3.30 3.60 5.25 5.50	V
Input Voltage	V_I	V_{SS}	--	V_{DD}	V
Operating Temperature	Topr	0 -40	25 25	70 85	^oC ^oC
Normal Input Rising Time	t_{ri}	--	--	50	ns
Normal Input Falling Time	t_{fa}	--	--	50	ns
Schmitt Input Rising Time	t_{ri}	--	--	5	ms
Schmitt Input Falling Time	t_{fa}	--	--	5	ms

Table 1-4 Electrical Characteristics of the S1L35000 Series
(V_{DD} = 5 V, V_{SS} = 0 V, Ta = -40 to 85°C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Quiescent Current	I_{DDS}	Quiescent Conditions		--	--	400	µA
Input Leakage Current	I_{LI}	--		-1	--	1	µA
Off State Leakage Current	I_{OZ}	--		-1	--	1	µA
High Level Output Voltage	V_{OH}	I_{OH} = -1 mA (Type M), -4 mA (Type 1) -8 mA (Type 2), -12 mA (Type 3) V_{DD} = Min.		V_{DD} -0.4	--	--	V
Low Level Output Voltage	V_{OL}	I_{OL} = 1 mA (Type M), 4 mA (Type 1), 8 mA (Type 2), 12 mA (Type 3) V_{DD} = Min.		--	--	0.4	V
High Level Input Voltage	V_{IH1}	CMOS Level, V_{DD} = Max.		3.5	--	--	V
Low Level Input Voltage	V_{IL1}	CMOS Level, V_{DD} = Min.		--	--	1.0	V
High Level Input Voltage	V_{T1+}	CMOS Schmitt, V_{DD} = 5.0 V		--	--	4.0	V
Low Level Input Voltage	V_{T1-}	CMOS Schmitt, V_{DD} = 5.0 V		0.8	--	--	V
Hysteresis Voltage	V_{H1}	CMOS Schmitt, V_{DD} = 5.0 V		0.3	--	--	V
High Level Input Voltage	V_{IH2}	TTL Level, V_{DD} = Max.		2.0	--	--	V
Low Level Input Voltage	V_{IL2}	TTL Level, V_{DD} = Min.		--	--	0.8	V
High Level Input Voltage	V_{T2+}	TTL Schmitt, V_{DD} = 5.0 V		--	--	2.4	V
Low Level Input Voltage	V_{T2-}	TTL Schmitt, V_{DD} = 5.0 V		0.6	--	--	V
Hysteresis Voltage	V_{H2}	TTL Schmitt, V_{DD} = 5.0 V		0.1	--	--	V
Pull-up Resistance	R_{PU}	V_I = 0 V	Type 1	25	50	100	kΩ
			Type 2	50	100	200	
Pull-down Resistance	R_{PD}	V_I = V_{DD}	Type 1	25	50	100	kΩ
			Type 2	50	100	200	
Input Terminal Capacitance	C_I	f = 1 MHz, V_{DD} = 0 V		--	--	12	pF
Output Terminal Capacitance	C_O	f = 1 MHz, V_{DD} = 0 V		--	--	12	pF
Input/Output Terminal Capacitance	C_{IO}	f = 1 MHz, V_{DD} = 0 V		--	--	12	pF

Table 1-5 Electrical Characteristics of the S1L35000 Series
(V_{DD} = 3 V ± 0.3 V, V_{SS} = 0 V, Ta = -40 to 85 ^{o}C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Quiescent Current	I_{DDS}	Quiescent Conditions		--	--	260	µA
Input Leakage Current	I_{LI}	--		-1	--	1	µA
Off State Leakage Current	I_{OZ}	--		-1	--	1	µA
High Level Output Voltage	V_{OH}	I_{OH} = -0.5 mA (Type M), -1.8 mA (Type 1) -3.5 mA (Type 2), -5 mA (Type 3) V_{DD} = Min.		V_{DD} -0.3	--	--	V
Low Level Output Voltage	V_{OL}	I_{OL} = 0.5 mA (Type M),1.8 mA (Type 1), 3.5 mA (Type 2), 5 mA (Type 3) V_{DD} = Min.		--	--	0.3	V
High Level Input Voltage	V_{IH1}	CMOS Level, V_{DD} = Max.		2.0	--	--	V
Low Level Input Voltage	V_{IL1}	CMOS Level, V_{DD} = Min.		--	--	0.8	V
High Level Input Voltage	V_{T1+}	CMOS Schmitt, V_{DD} = 3.0 V		--	--	2.3	V
Low Level Input Voltage	V_{T1-}	CMOS Schmitt, V_{DD} = 3.0 V		0.5	--	--	V
Hysteresis Voltage	V_{H1}	CMOS Schmitt, V_{DD} = 3.0 V		0.1	--	--	V
Pull-up Resistance	R_{PU}	V_I = 0 V	Type 1	50	100	200	kΩ
			Type 2	100	200	400	
Pull-down Resistance	R_{PD}	V_O = V_{DD}	Type 1	50	100	200	kΩ
			Type 2	100	200	400	
Input Terminal Capacitance	C_I	f = 1 MHz, V_{DD} = 0 V		--	--	12	pF
Output Terminal Capacitance	C_O	f = 1 MHz, V_{DD} = 0 V		--	--	12	pF
Input/Output Terminal Capacitance	C_{IO}	f = 1 MHz, V_{DD} = 0 V		--	--	12	pF

Table 1-6 Electrical Characteristics of the S1L35000 Series
(V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = -40 to 85 ^{o}C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Quiescent Current	I_{DDS}	Quiescent Conditions		--	--	290	µA
Input Leakage Current	I_{LI}	--		-1	--	1	µA
Off State Leakage Current	I_{OZ}	--		-1	--	1	µA
High Level Output Voltage	V_{OH}	I_{OH} = -0.5 mA (Type M), -2 mA (Type 1), -4 mA (Type 2), -6 mA (Type 3) V_{DD} = Min.		V_{DD} -0.3	--	--	V
Low Level Output Voltage	V_{OL}	I_{OL} = 0.5 mA (Type M),2 mA (Type 1), 4 mA (Type 2), 6 mA (Type 3) V_{DD} = Min.		--	--	0.3	V
High Level Input Voltage	V_{IH1}	CMOS Level, V_{DD} = Max.		2.2	--	--	V
Low Level Input Voltage	V_{IL1}	CMOS Level, V_{DD} = Min.		--	--	0.8	V
High Level Input Voltage	V_{T1+}	CMOS Schmitt, V_{DD} = 3.3 V		--	--	2.4	V
Low Level Input Voltage	V_{T1-}	CMOS Schmitt, V_{DD} = 3.3 V		0.6	--	--	V
Hysteresis Voltage	V_{H1}	CMOS Schmitt, V_{DD} = 3.3 V		0.1	--	--	V
Pull-up Resistance	R_{PU}	V_I = 0 V	Type 1	45	90	180	kΩ
			Type 2	90	180	360	
Pull-down Resistance	R_{PD}	V_I = V_{DD}	Type 1	45	90	180	kΩ
			Type 2	90	180	360	
Input Terminal Capacitance	C_I	f = 1 MHz, V_{DD} = 0 V		--	--	12	pF
Output Terminal Capacitance	C_O	f = 1 MHz, V_{DD} = 0 V		--	--	12	pF
Input/Output Terminal Capacitance	C_{IO}	f = 1 MHz, V_{DD} = 0 V		--	--	12	pF

1.4 Overview of Gate Array Development Flow

Gate arrays are developed jointly by the customer and EPSON. System design, circuit design, and test pattern design is performed by the customer, based on various reference materials, including the cell libraries provided to the customer by EPSON.

Various modes of interface, listed below, are possible between the customer and EPSON during design, depending on the stage in gate array development wherein the customer interfaces with EPSON.

When interfacing with EPSON, the customer is to provide the necessary data and documents to EPSON.

The customer performs schematic capture, logic synthesis and simulation using EDA software and Auklet* supported by EPSON. Place and route is performed by EPSON. Both the customer and EPSON are responsible for final sign-off simulations.

Note) * : Auklet is the EPSON's ASIC desgin support system that can run on a personal computer- OS : MS-Windows 95/98, NT platform.

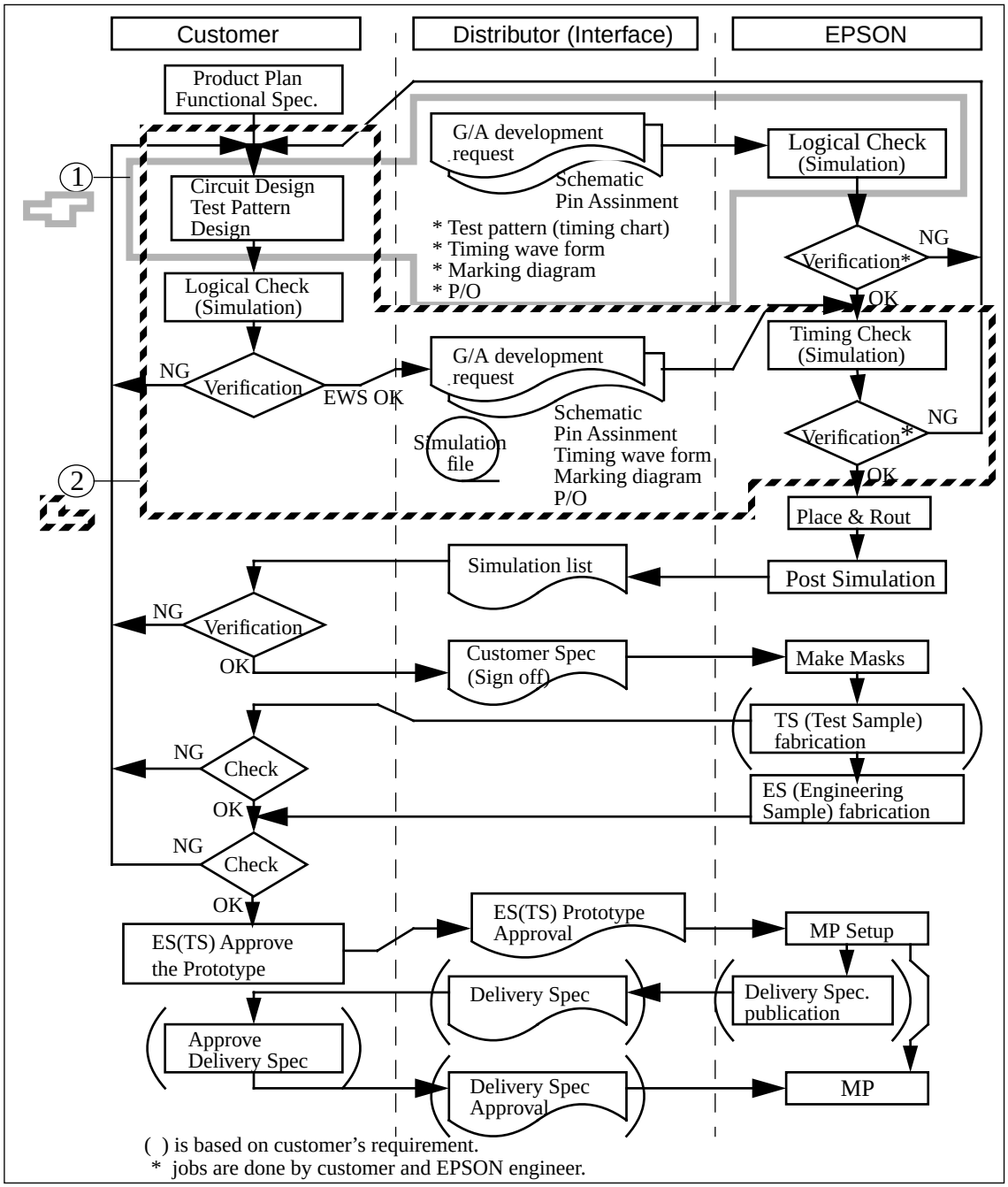
The simulation is currently supported by the following EDA software:

- Verilog-XL (*1)
- VSS (*2)
- ModelSim (*3)

Note) *1 : Verilog-XL is a registered trademark of Cadence Desgin Systems Corporation, USA.
*2 : VSS is a registered trademark of Synopsys Inc., USA.
*3 : ModelSim is a registered trademark of Model Technology Corp., USA.

For more information, refer to the Gate Array Technical Guide or contact to our sales office for technical support.

The process flow of the gate array development process is shown below:



NOTE: When the customer performs all tasks to the point of logical simulations and delay simulations on engineering workstations, etc., the route taken is (2). When EPSON performs the logical simulations, the route taken is (1).

Chapter 2 Estimating Gate Density and Selecting the Master

Methods and guidelines are described below to assist in defining the logic which will be integrated into a gate array, estimating the array requirements, and determining the appropriate master for a given application.

2.1 Dividing up Logic between Chips

When extracting logic, which is to be integrated into gate arrays from the system being created by the user, the logic should be selected with the following criteria in mind.

• Integration Criteria

(1) Quantity of logic to integrate
(2) Quantity of input, output and bi-directional signals required
(3) Package to be used
(4) Power consumption

Generally, the larger the gate density, the more power is consumed, and the more input and output terminals required. Because of this, it may be better, from the perspective of total cost or from the perspective of power consumption, etc., to divide the circuit into multiple chips, rather than forcing them into a single chip.

2.2 Determining Gate Density

In the case of gate arrays, the scope of the array is defined as the sum of gates or basic cells (BCs) used. One gate or basic cell is typically defined as being equivalent to one two-input NAND gate (or four transistors). The "Gate Array S1L35000 Series MSI Cell Library" can be used as reference to facilitate gate count estimation.

2.3 Estimating the Number of Input/Output Terminals

Defining the number of I/O signals, test signals and power pins required for a given application has a bearing on the array member suitable for that application. The appropriate number of I/O pads must be available on the array member to satisfy the application signal requirements. Estimate the number of power supply pins using the method discussed in Chapter 10.

2.4 Selecting the Master

Select the appropriate master from the CMOS Device Catalog S1L35000 Series tables, based on the estimated number of BCs, the number of required input and output pins (including power supply pins) and the package to be used.

The actual number of BCs (BC_A) which can be used for each device type is estimated using the following formula from the gross number of BCs (BC_G) loaded on each master (shown in Table 1-1 of the previous chapter) and the cell utilization ratio (U).

$$BC_A = U \times BC_G$$

where U = 0.50 to 0.65

NOTE: When a RAM circuit is included, this estimate should be made after refering to the following section and after refering to Chapter 5.

2.5 Estimating the BCs That can be Used in Circuits Which Include RAM

RAM blocks, in comparison to MSI cells, are extremely large and have fixed shapes (defined vertical and horizontal dimensions). Because of this, some RAM blocks which may appear to fit on the chip because of calculations based on the number of BCs may, in actuality, not be placable on a given master. Thus, the first decision is that of whether or not the RAM configuration is available on a given master. Please refer to Chapter 5.

Once the masters which can accommodate the RAM have been selected, it becomes possible to estimate the number of BCs (BC_{AWR}) of random logic (excluding RAM) available using the formula below.

$$BC_{AWR} = 0.9 \times U \times (BC_G - BC_{RAM})$$

where BC_{AWR} is the number of BCs available for random logic
BC_G is the gross BCs available on a mater (raw gates)
BC_{RAM} is the BC use of RAM(s) (See Chapter 5 for BC calculation)
U is the utilization ratio

NOTE: Actual BCs available (BC_{AWR}) is design dependent.
Use the formula above for estimation purposes only.
Please consult EPSON for design specific information.

Chapter 3 Cautions and Notes Regarding Circuit Design

3.1 Inserting Input/Output Buffers

When designing your circuit using gate arrays, always be sure to use input/output buffers to exchange signals with external devices. Due to CMOS IC's extreme vulnerability to electrical static discharge (ESD), protection circuitry has been incorporated within the input/output buffers. In addition, due to limitations on chip layout, be sure to insert input or output buffers between external terminals and internal cells.

3.2 The Use of Differentiating Circuits is Forbidden

In LSIs, the propagation delay (tpd) of each gate varies depending on process variance during mass production and on the operating environment. Therefore, depending on the process dispersions and operating conditions, differentiating circuits using the relative time difference of tpd, like the one shown in Figure 3-1, may not be able to obtain a sufficient pulse width, causing the circuit to operate erratically.

When using a differentiating circuit, be sure to use one that utilizes flip-flops, and not the one shown in Figure 3-1.

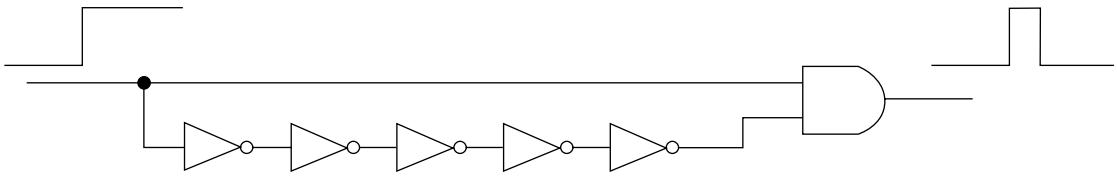


Figure 3-1 Example of a Differentiating Circuit

3.3 Wired Logic is Forbidden

Because the S1L35000 uses CMOS transistors, wired logic as in bipolar transistors cannot be configured. Consequently, cell output terminals cannot be wired together, as shown in Figure 3-2. It is only in a bus-circuit configuration that output terminals can be connected together.

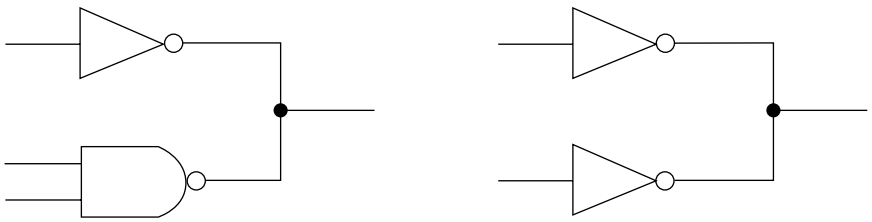


Figure 3-2 Example of Forbidden Wired Logic

3.4 Hazard Countermeasures

In circuits or decoder cells configured by combining gates such as NAND or NOR gates, an extremely short pulse may be generated due to the difference in delay times between gates. This short pulse is known as a "hazard" and, when fed into the clock or reset terminals of flip-flops, causes malfunction.

Therefore, circuits in which such a hazard is likely to occur must be configured so as to prevent the hazard from propagating. Alternately, for decoders, it may be necessary to use one that has an enable terminal.

3.5 Fan-Out Constraints

The tpd of a logic gate is determined by the load capacitance of its output terminal. An excessively large load capacitance may not only cause the tpd to become large, but may also cause malfunction. Therefore, the output terminals of each logic gate are subject to limitations on the number of loads that can be connected. These are known as "fan-out constraints."

The input-terminal capacitance of each logic gate, on the other hand, tends to differ for each logic-gate input. The input capacitance of each logic gate, as referenced to the input capacitance of an inverter (INI) = 1, is known as the "fan-in."

In the design of your circuit, confirm that the sum total of fan-ins connected to the output terminals of each logic gate will not exceed the fan-out constraints of those output terminals.

Furthermore, for logic gates operating at high speed such as high-speed clock lines (fmax = 40 MHz or more), confirm that the output-terminal capacitance of those gates is approximately half of the fan-out constraints.

3.6 Bus Circuits

A bus circuit is configured with 3-state logic circuits, so that one of the outputs connected to the bus is driven active (while the other outputs are placed in the high-impedance state) by turning the bus control signals on or off. In this way, one transmission signal line on the bus is shared by dividing its use time.

Although bus circuits are very effective for logic design, note the following when using a bus circuit.

Notes Regarding the Use of Bus Circuits

(1) Bus cells can only be used for bus circuits (for the S1L35000 series bus cells, see Table 3-1).

(2) When using bus cells, add bus definition cells BLT to the bus when configuring your circuit.

(3) Up to 32 bus cells can be connected to one length of bus.

(4) Of the bus cells connected to one length of bus, only one output can be active (0 or 1) at one time, and all other bus-cell outputs must be placed in the high-impedance state (Z).

(5) Even when all of the bus cells connected to one length of bus are in the high-impedance state (Z), data may be retained by a bus latch cell. However, leave the retained data floating, and do not use it as a logic signal.

(6) In the creation of your test pattern, make sure the bus's initial state will be easily settled to provide improved testability. In addition, add one or more test terminals to make the bus easily controllable.

(7) The bus control signals within the same event rate can be switched only once.

(8) An excessive fan-out of the bus circuit may cause the propagation delay time to increase, making high-speed operation difficult.

The usable bus cells in the S1L35000 series are listed in Table 3-1.

Table 3-1 Table of S1L35000 Series Bus Cells

Cell Type	Cell Name		
	1 Bit	4 Bit	8 Bit
Bus latches	XBLT 1	XBLT 4	XBLT 8
Bus drier	XTSB, XTSBP	XT244H	XT244
Inverting bus driver	XTSV, XTSVP	XT240H	XT240
Transparent latches with reset and 3-state output	–	XT373H	XT373
D-flip flops with rest and 3-state output	–	XT374H	XT374
1-bit RAM	XRM1	–	–

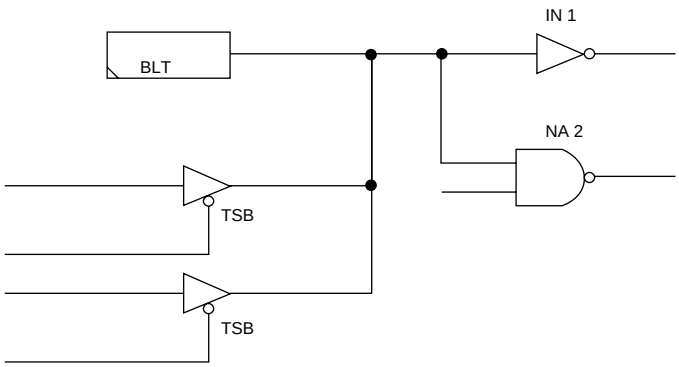


Figure 3-3 Typical Configuration of a Bus Cell Circuit

3.7 Schematic Capture Guidelines

Please adhere to the following conventions when designing an ASIC via manual schematic entry:

- Use logic cells found in Gate Array S1L35000 Series MSI Cell Library.
- Use orthogonal (not oblique) connections when wiring logic cells to one another.
- Primary uni-directional I/O and bi-directional I/O signal names must be 2 to 32 characters in length, and must begin with an alphabetic character.

3.8 Clock Tree Synthesis

(1) Overview

Clock Tree Synthesis is a support that automatically inserts the ClockTree into the buffer group that optimizes the skew and delay time of “Clock Line”. If a customer has a program to insert ClockTree to adjust the Fan-out of “ClockLine”, clock skew may be large, so the P & R tool is started and the placing and routing for designing the gate array are executed voluntarily. Also, the propagation delay time may be longer than estimated because there are many cases it is difficult to maintain a good balance between the wire interconnecting load and the intrinsic cell delay. The Clock Tree Synthesis is used to solve this problem. Refer to the actual results to use the Clock Tree Synthesis as follows:

(2) How to Examine the Clock Tree Synthesis

When the clock tree is inserted automatically, the customer must insert the special buffer to the Clock Line for the following three purposes.

- Judging the place to insert the Clock Tree Synthesis.
- Estimating the delay time of the Clock Tree inserted and execute the simulation of virtual wire interconnecting level (pre-simulation).
- Back annotate the delay time of the inserted Clock Tree to accurately estimate the post-simulation.

Select the special buffer for the Clock Tree Synthesis in the table of special buffers mentioned later.Then insert the special buffer selected from the table into the Clock Line taking into consideration the restriction or notes mentioned later and the same placing as the normal cells. Otherwise, if the logic are designed by HDL, as the special buffer can not insert automatically the Clock Line, assign directly the HDL of the content using the script language. Note that another buffer is not combined in the clock Line inserted in the special buffer, and execute the following command:

set_dont_touch_net *net_name*

[The special buffer]

Select the special buffer from the table below corresponding to the estimated number of fan-outs.

S1L9000F, S1L30000, S1L50000 Series		
Cell Name	To Max. (ns)	Estimated number of fan-out
CRBF2	2.00	0 to 500
CRBF3	3.00	500 to 3000
CRBF4	4.00	3000 to 10000
CRBF5	5.00	Over 10000
CRBF6	6.00	
CRBF7	7.00	
CRBF8	8.0	

S1L35000 Series		
Cell Name	To Max. (ns)	Estimated number of fan-out
XCRBF2	2.00	0 to 500
XCRBF3	3.00	500 to 3000
XCRBF4	4.00	3000 to 10000
XCRBF5	5.00	Over 10000
XCRBF6	6.00	
XCRBF7	7.00	
XCRBF8	8.0	

Note 1: The value “K” (load delay of fan-out) of these cells is set “0” at the pre-simulation.

Note 2: The number of fan-outs of these cells is set to the infinity.

Note 3: Please consider that the load delay for the number of fan-outs is not accurately and only estimated.

[Restriction and Notes]

- Target series: S1L9000F, S1L30000, S1L35000, S1L50000
- The special buffer can not be used for any purpose other than the Clock Tree Synthesis.
- The Clock Tree Synthesis can also be used for data line and other control signals. However, when the nets used in the synthesis are increased, the skew and propagation delay also became larger. Therefore, the number of nets to be used in the synthesis is less than 10 and the net which has a critical and large fan-out should be used.
- If a net which has a small fan-out is used for the Clock Tree Synthesis, the propagation delay and skew may be larger. The target net with fan-out should be used more than scores.
- As there are cases corresponding to the skew adjustment between multiple Clock lines, contact EPSON for handing in the detail schematic (the clock line configuration is described very clearly) to be checked.
- For the Clock group separated into multiple Clock Lines with the same Root of Clock by the gates, contact EPSON to obtain the materials of “Gated Clock Tree Synthesis Explanations”.

[Necessary Information from a Customer]

Send the following information until the data is released, because the Clock Tree Synthesis is used efficiently.

Instance name of CRBF*	Target skew value	Target propagation delay (Min./Max.)

Note 1: The target values on the table are needed to estimate to use the Synthesis. The target values are not always satisfied.

Note 2: If there is no target values, write the comments for each item in the table.
Example: As smaller as possible

[Imaging schematic]

The schematic created by a customer and the layout schematic after executing the Clock Tree Synthesis in EPSON are shown as follows:

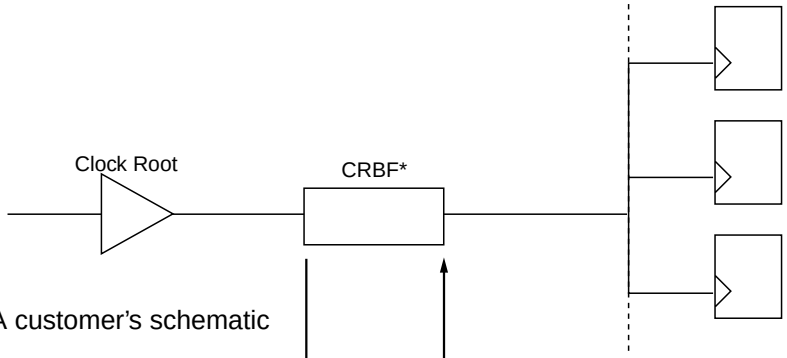


Figure 3-4 A customer's schematic

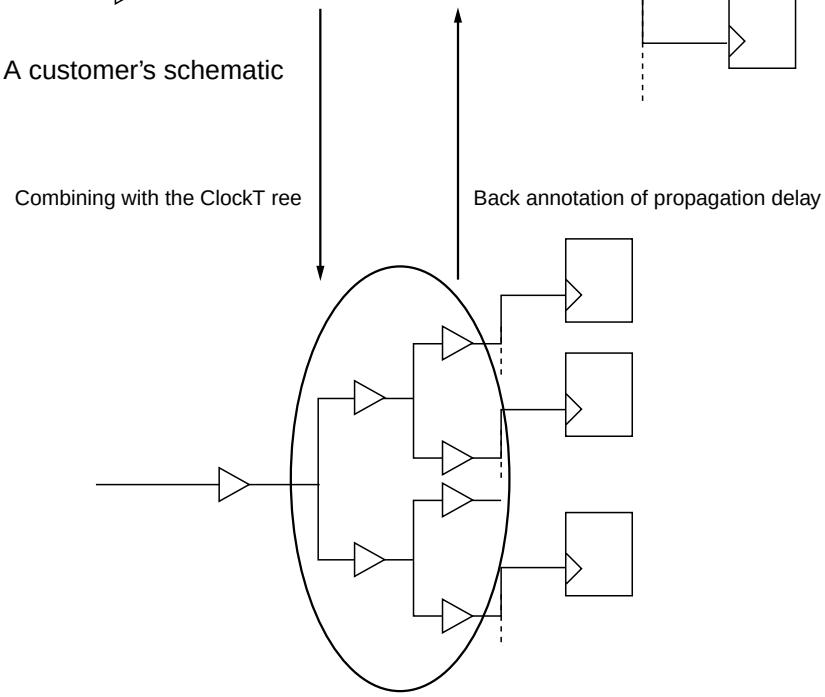


Figure 3-5 Layout schematic after executing the Clock Tree Synthesis in EPSON

3.9 Restrictions and Constraints on VHDL/Verilog-HDL Netlist

The VHDL/Verilog-HDL net list to be interfaced to EPSON shall be a pure gate-level net list (not containing description of operation). The restrictions and constraints in developing EPSON ASIC using VHDL/Verilog HDL are as follows.

3.9.1 Common Restrictions and Constraints

(1) Names of External Terminal (I/O Terminal)

- Use only upper-case letters.
- Number of characters: 2 to 32
- Usable characters : Alphanumeric characters and "_." Use an alphabetical letter at the head.
- Examples of prohibited character strings :

  2 INPUT : A digit is at the head.
  \2INPUT : "\" is at the head.
  InputA : Lower-case letters are included.
  INPUTA : "" is at the head.
  TNA[3:0] : A bus is used for the name of the external terminal.
  INA[3] : A bus is used for the name of the external terminal.

(2) Names of Internal Terminal (including bus net names)

- Upper-and lower-case letters can be used in combination, except the following. Combinations of the same words expressed in upper-and lower-case letters, such as "_RESET_" and "_Reset_."
- Number of characters : 2 to 32
- Usable characters :Alphanumeric characters, "_," "_[ ]_" (Verilog bus blanket), and "_()_" (VHDL bus blanket) with an alphabetical letter at the head.

(3) Bus description is prohibited at the most significant place of the module.

Examples: DATA [0:3], DATA [3], and DATA [2] are prohibited.DATA0, DATA1, and DATA2 are all allowed.

(4) You can use I/O cells of the same library series, but cannot combine those of different series.

(5) It is not possible to describe operations in behaviors or in the C language. Such descriptions existing in the net list are invalid.

(6) Precision of the time scale of the library of each series is 1 ps.

3.9.2 Restrictions and Constraints for Verilog Netlist

(7) Descriptions using the functions "assign" and "tran" are prohibited in the gate-level Verilog net list.

(8) Descriptions of connection with cell pin names are recommended in the Verilog net list.

Example: Connection with pin names: IN2 inst_1 (.A(inst_2),.X(inst_3)); Recommended Connection with net names: IN2 inst_1(net1, net2):

(9) You cannot use the Verilog command “force” as a description of flip-flop operation. (Example: force logic .singal = 0;)

(10) The time scale description is added at the head of the gate-level net list generated by the Synopsys design compiler.
Set it at the value described in the EPSON Verilog library. See (6) for the time scale of each series.

Example: 'timescale 1ps/1ps

(11) EPSON prohibits combination of a bus single port name and a name that includes “__”, such as the following, in the same module.

input A [0];

wire \A [0];

(12) The following letter strings are reserved for Verilog, which cannot be used as a user-defined name.

always, and, assign, begin, buf, bufif0, bufif1, case, design,default, defparam, disable, else, end, endcase, endfunction, endmodule, endtask, event, for, force, forever, fork, function, highz0, highz1, if, initial, inout, input, integer, join, large, medium, module, nand, negedge, nor, not, notif0, notif1, or, output, parameter, posedge, pull0, pull1, reg, release, repeat, scalared, small, specify, strong0, strong1, supply0, supply1, task, time, tri, tri0, tri1, trinand, trior, trireg, vectored, wait, wand, weak0, weak1, while, wire, wor, xor, xnor

3.9.3 Restrictions and Constraints on VHDL Netlist

(13) In addition to the constraints in (1), the following letter strings are also prohibited.

INPUTA_	:	“_” is used at the end.
INPUT_ _A	:	“_” is used twice or more in succession.
read	:	Used in the system.
write	:	Used in the system.

(14) The following letter strings are reserved for VHDL, which cannot be used as a user-defined name.

abs, access, after, alias, all, and, architecture, array, assert, attribute, begin, block, body, buffer, bus, case, component, configuration, constant, disconnect, downto, else, elsif, end, entity, exit, file, for, function, generate, generic, guarded, if, in, inout, is, label, library, linkage, loop, map, mod, nand, new, next, nor, not, null, of, on, open, or, others, out, package, port, procedure, process, range, record, register, rem, report, return, select, severity, signal, subtype, then, to, transport, type, units, until, use, variable, wait, when, while, with, xor

(15) To use EPSON utilities and tools, it is necessary to change the VHDL format into the Verilog format. Therefore, the letter strings reserved for Verilog in (12) are also prohibited.

Chapter 4 Input/Out Buffer and Their Use

4.1 Types of Input/Output Buffer in the S1L35000 Series

Various I/O buffers types of the S1L35000 Series are available according to the input interface level, output drive capacity, use or no use of pull-up and pull-down resistors, and the pull-up and pull-down resistors. You can select the ones appropriate to your needs.

4.1.1 Selecting I/O Buffer

The S1L35000 series provides a wide range of input / output buffers. You can select buffer parameters, including input interface level, schmitt trigger input or not, output drive capabil-ity and a pull-up or pull-down resistance. This allows you to select the most suitable buffer for each application.b) Is a schmitt trigger input necessary? (Are hysteresis characteristics necessary?)

(1) Selecting the Input Cell
   a) Is the required interface level a CMOS level or a TTL level?
   b) Is a schmitt trigger input necessary? (Are hysteresis characteristics necessary?)
   c) Is it necessary to add pull-up/pull-down resistors?

(2) Selecting the Output Cell
   a) How much output current must be driven?(I_{OL} / I_{OH})
   b) Are noise countermeasures necessary?

(3) Selecting Bi-directional Cells
   Select the bi-directional cells by examining both sets of criteria for selecting the input cells and selecting the output cells.

   • I/O Interface Level

   1) 5.0V system single power supply
      Input level
         TTL level, CMOS level, TTL Schmitt, CMOS Schmitt
      Output level
         CMOS level

   2) 3.0 V system single power supply
      Input level
         TTL Schmitt, CMOS Schmitt
      Output level
         CMOS level

NOTE 1 :The 3.0 V/ 3.3 V system CMOS level is about the same value as the 5.0V system TTL level. When a single 3.0 / 3.3 V power supply is used, TTL level input cannot be used.

   • Output Drive Capability
     See the electrical characteristics (Tables 1.4 to 1.6).
   • Pull-up/Pull-down Resistance
     See the electrical characteristics (Tables 1.4 to 1.6).

Some I/O buffers of the S1L35000 series need to use a combination of I/O cells and internal interface cells.

The input buffer, output buffer, and bi-directional buffer configuration for single power supplies are expained in detail biginning with Section 4.2.

4.2 I/O Buffer Configurations with a Single Power Supply

When using a single power supply, the power supply voltage (V_{DD}) may be either 5.0V, 3.3V or 3.0V.

Also, I/O buffer can be used either 5.0V, 3.3V or 3.0V. I/O buffer configurations with a single power supply either 3.0V or 5.0V are explained below.

4.2.1 I/O Buffer Configurations with a Single 5.0V Power Supply

4.2.1.1 Input Buffer Configurations with a Single 5.0V Power Supply

The input buffer function is structured of input cells only.

Table 4-1 Input Cell (combinations of I/O cells)

Cell Name	Input Level	Function	Pull-up/Pull-down Resistance
XIBT	TTL	Buffer	None
XIBTP*	TTL	Buffer	Pull-up resistance (50 kΩ, 100 kΩ)
XIBTD*	TTL	Buffer	Pull-down resistance (50 kΩ, 100 kΩ)
XIBC	CMOS	Buffer	None
XIBCP*	CMOS	Buffer	Pull-up resistance (50 kΩ, 100 kΩ)
XIBCD*	CMOS	Buffer	Pull-down resistance (50 kΩ, 100 kΩ)
XIBS	TTL Schmitt	Buffer	None
XIBSP*	TTL Schmitt	Buffer	Pull-up resistance (50 kΩ, 100 kΩ)
XIBSD*	TTL Schmitt	Buffer	Pull-down resistance (50 kΩ, 100 kΩ)
XIBH	CMOS Schmitt	Buffer	None
XIBHP*	CMOS Schmitt	Buffer	Pull-up resistance (50 kΩ, 100 kΩ)
XIBHD*	CMOS Schmitt	Buffer	Pull-down resistance (50 kΩ, 100 kΩ)

NOTE: When * value is 1 or 2, pull-up/pull-down resistance values correspond to 1:50 kΩ., 2:100 kΩ respectively.

4.2.1.2 Output Buffer Configurations with a Single 5.0V Power Supply

Please configure the output buffers using pre-drivers (such as XPDV1T, XPDV1AT, XPDV1BT, XPDV2T, XPDV2AT, XPDV2BT, etc.), and output cells (such as XUOM to XUO3). See Figure 4-1 for connectivity and reference Table 4-2 below regarding the pre-driver and output cell combinations.

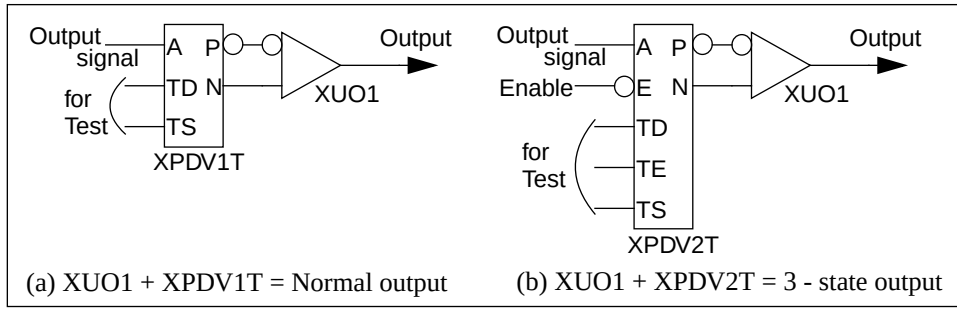


Figure 4-1 Examples of Pre-driver and Output Cell Configurations

Table 4-2 Combinations of Pre-drivers and Output Cells

Function	I_{OL}* / I_{OH}**	Cell Structure***
Normal output for low noise	1mA/-1mA 4mA/-4mA 8mA/-8mA 12mA/-12mA	XUOM+XPDV1T XUO1+XPDV1T XUO2+XPDV1T XUO3+XPDV1T
Normal output for high speed	1mA/-1mA 4mA/-4mA 8mA/-8mA 12mA/-12mA	XUOM+XPDV1AT XUO1+XPDV1AT XUO2+XPDV1AT XUO3+XPDV1AT
Normal output with slew rate control	1mA/-1mA 4mA/-4mA 8mA/-8mA 12mA/-12mA	XUOM+XPDV1BT XUO1+XPDV1BT XUO2+XPDV1BT XUO3+XPDV1BT
Normal output with slew rate control for falling edge only	12mA/-12mA	XUO3L+XPDV3T
3-state output for low noise	1mA/-1mA 4mA/-4mA 8mA/-8mA 12mA/-12mA	XUOM+XPDV2T XUO1+XPDV2T XUO2+XPDV2T XUO3+XPDV2T
3-state output for high speed	1mA/-1mA 4mA/-4mA 8mA/-8mA 12mA/-12mA	XUOM+XPDV2AT XUO1+XPDV2AT XUO2+XPDV2AT XUO3+XPDV2AT
3-state output with low slew rate control	1mA/-1mA 4mA/-4mA 8mA/-8mA 12mA/-12mA	XUOM+XPDV2BT XUO1+XPDV2BT XUO2+XPDV2BT XUO3+XPDV2BT
3-state output with slew rate control for falling edge only	12mA/-12mA	XUO3L+XPDV4T

NOTES: * V_{OL} = 0.4 V (V_{DD} = 5.0 V)

** V_{OH} = V_{DD} - 0.4 V (V_{DD} = 5.0 V)

*** In addition to the configurations in Table 4-2, the output buffers may be configured with pre-drivers which do not have test terminals. Customers desiring to use such structures should direct inquiries to EPSON.

As is shown in Table 4-2, the combination with XUO3L and XPDV3T can be output more than normal slew rate for falling edge only . Also, both XPDV1BT and XPDV2BT are output more than normal slew rate for falling and rising edges. Usually, they are used in combination with XUO3.

• XODN (Open Drain Output Cell) Usage

As is shown in Table 4-3, configure open drain output functionality using the XODNx output cell and pre-driver combinations with the N terminal connection only. Do not connect the P terminal of the pre-driver output. (See Figure 4-2)

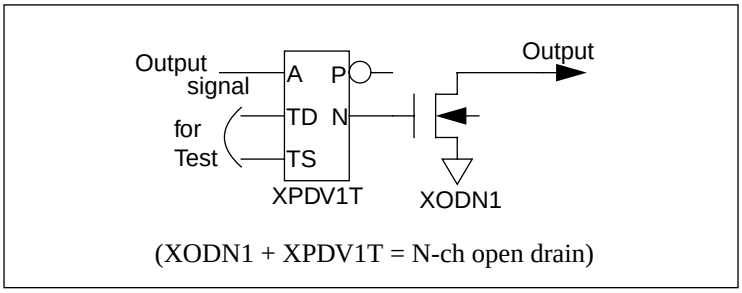


Figure 4-2 Example of XODN Configuration

Table 4-3 Combinations of Pre-drivers and XODN Cell Usage

Function	I_{OL}*	Cell Structure**
Normal output for low noise	1mA 4mA 8mA 12mA	XODNM+XPDV1T XODN1+XPDV1T XODN2+XPDV1T XODN3+XPDV1T
Normal output for high speed	1mA 4mA 8mA 12mA	XODNM+XPDV1AT XODN1+XPDV1AT XODN2+XPDV1AT XODN3+XPDV1AT
Normal output with slew rate control	12mA	XODN3L+XPDV3T

NOTES: * V_{OL} = 0.4 V (V_{DD} = 5 V)

** In addition to the configurations on Table 4-3, the output buffers may be configured with pre-drivers which do not have test terminals. Customers desiring to use such structures should direct inquiries to EPSON.

4.2.1.3 Bi-directional Buffer Configurations with a Single 5.0V Power Supply

Bi-directional buffers are configured from combinations of pre-drivers (with enable terminals) and bi-directional cells. (See Figure 4-3.)

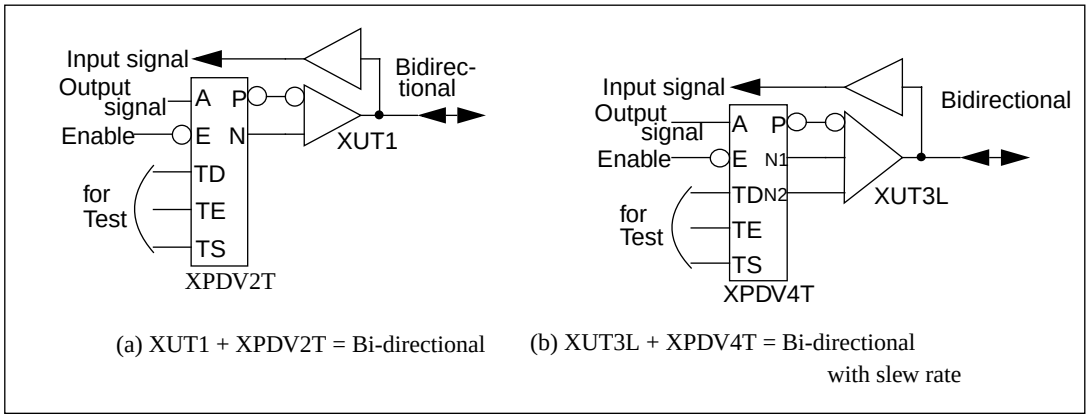


Figure 4-3 Examples of Pre-driver and Bi-directional Cell Configurations

Table 4-4 Combinations of Pre-drivers and Bi-directional Cells (1/2)

Input Level	Function	I_{OL}*/I_{OH}**	Cell Structure***
TTL	Bi-directional for low noise output	1mA/-1mA 4mA/-4mA 8mA/-8mA 12mA/-12mA	XUTM+XPDV2T XUT1+XPDV2T XUT2+XPDV2T XUT3+XPDV2T
TTL	Bi-directional for high speed output	1mA/-1mA 4mA/-4mA 8mA/-8mA 12mA/-12mA	XUTM+XPDV2AT XUT1+XPDV2AT XUT2+XPDV2AT XUT3+XPDV2AT
TTL	Bi-directional with low slew rate control output	1mA/-1mA 4mA/-4mA 8mA/-8mA 12mA/-12mA	XUTM+XPDV2BT XUT1+XPDV2BT XUT2+XPDV2BT XUT3+XPDV2BT
TTL	Bi-directional with slew rate control output for falling edge only	12mA/-12mA	XUT3L+XPDV4T
CMOS	Bi-directional for low noise output	1mA/-1mA 4mA/-4mA 8mA/-8mA 12mA/-12mA	XUCM+XPDV2T XUC1+XPDV2T XUC2+XPDV2T XUC3+XPDV2T
CMOS	Bi-directional for high speed output	1mA/-1mA 4mA/-4mA 8mA/-8mA 12mA/-12mA	XUCM+XPDV2AT XUC1+XPDV2AT XUC2+XPDV2AT XUC3+XPDV2AT
CMOS	Bi-directional with low slew rate control output	1mA/-1mA 4mA/-4mA 8mA/-8mA 12mA/-12mA	XUCM+XPDV2BT XUC1+XPDV2BT XUC2+XPDV2BT XUC3+XPDV2BT
CMOS	Bi-directional with slew rate control output for falling edge only	12mA/-12mA	XUC3L+XPDV4T

Table 4-4 Combinations of Pre-drivers and Bi-directional Cells (2/2)

Input Level	Function	I_{OL}*/I_{OH}**	Cell Structure
TTL Schmitt	Bi-directional for low noise output	1mA/-1mA 4mA/-4mA 8mA/-8mA 12mA/-12mA	XUSM+XPDV2T XUS1+XPDV2T XUS2+XPDV2T XUS3+XPDV2T
TTL Schmitt	Bi-directional for high speed output	1mA/-1mA 4mA/-4mA 8mA/-8mA 12mA/-12mA	XUSM+XPDV2AT XUS1+XPDV2AT XUS2+XPDV2AT XUS3+XPDV2AT
TTL Schmitt	Bi-directional with low slew rate control output	1mA/-1mA 4mA/-4mA 8mA/-8mA 12mA/-12mA	XUSM+XPDV2BT XUS1+XPDV2BT XUS2+XPDV2BT XUS3+XPDV2BT
TTL Schmitt	Bi-directional with slew rate control output for falling edge only	12mA/-12mA	XUS3L+XPDV4T
CMOS Schmitt	Bi-directional for low noise output	1mA/-1mA 4mA/-4mA 8mA/-8mA 12mA/-12mA	XUHM+XPDV2T XUH1+XPDV2T XUH2+XPDV2T XUH3+XPDV2T
CMOS Schmitt	Bi-directional for high speed output	1mA/-1mA 4mA/-4mA 8mA/-8mA 12mA/-12mA	XUHM+XPDV2AT XUH1+XPDV2AT XUH2+XPDV2AT XUH3+XPDV2AT
CMOS Schmitt	Bi-directional with low slew rate control output	1mA/-1mA 4mA/-4mA 8mA/-8mA 12mA/-12mA	XUHM+XPDV2BT XUH1+XPDV2BT XUH2+XPDV2BT XUH3+XPDV2BT
CMOS Schmitt	Bi-directional with slew rate control output for falling edge only	12mA/-12mA	XUH3L+XPDV4T

NOTES: * V_{OL} = 0.4 V (V_{DD} = 5.0 V)
** V_{OH} = V_{DD} - 0.4 V (V_{DD} = 5.0 V)
*** In addition to the configurations in Table 4-4, bi-directional buffers may be configured with pre-drivers which do not have test terminals. Most bi-directional buffers have two types of pull-up resistance options and two types of pull-down resistance options. Customers desiring such should direct inquiries to EPSON.

4.2.2 I/O Buffer Configurations with a Single 3.0/3.3 V Power Supply

4.2.2.1 Input Buffer Configurations with a Single 3.0/3.3 V Power Supply

Table 4-5 Input Cells

Cell Name	Input Level**	Function	Pull-up/Pull-down Resistance
XIBC	CMOS	Buffer	None
XIBCP*	CMOS	Buffer	Pull-up Resistance (90 kΩ, 180 kΩ)
XIBCD*	CMOS	Buffer	Pull-down Resistance (90 kΩ, 180 kΩ)
XIBH	CMOS Schmitt	Buffer	None
XIBHP*	CMOS Schmitt	Buffer	Pull-up Resistance (90 kΩ, 180 kΩ)
XIBHD*	CMOS Schmitt	Buffer	Pull-down Resistance (90 kΩ, 180 kΩ)

NOTES:When * value is 1 or 2, pull-up/pull-down resistance values correspond to 1:90 kΩ., 2:180 kΩ respectively.
** In a 3.0 V/3.3 V single power supply TTL level input cannot be used.

XIDC (Input Cells)

The XIDC is a 5.0 V tolerant input buffer which can be used in a 3.0 V/3.3 V only ASIC application to satisfy mixed-voltage system requirements.

Table 4-6 Table of Input Level Shifters

Cell Name	Input Level	Function	Pull-up/Pull-down Resistance
XIDC	TTL	Buffer	None
XIDCD*	TTL	Buffer	Pull-down Resistance (90 kΩ, 180 kΩ)

NOTE: When * value is 1 or 2, pull-down resistance value correspond to 1:90 kΩ and 2:180 kΩ respectively.

4.2.2.2 Output Buffer Configurations with a Single 3.0/3.3V Power Supply

When structuring the output buffer, use a combination of pre-drivers (such as XPDV1T, XPDV1AT, XPDV2T, XPDV2AT, etc.), which are structured of internal cells and output cells (such as XUOM to XUO3). See Table 4-7 below, regarding these combinations.

Table 4-7 Combinations of Pre-drivers and Output Cells

Function	I_{OL}*/I_{OH}**	Cell Structure***
Normal output for low noise	0.5mA/-0.5mA 2mA/-2mA 4mA/-4mA 6mA/-6mA	XUOM+XPDV1T XUO1+XPDV1T XUO2+XPDV1T XUO3+xPDV1T
Normal output for high speed	0.5mA/-0.5mA 2mA/-2mA 4mA/-4mA 6mA/-6mA	XUOM+XPDV1AT XUO1+XPDV1AT XUO2+XPDV1AT XUO3+XPDV1AT
Normal output with low slew rate control	0.5mA/-0.5mA 2mA/-2mA 4mA/-4mA 6mA/-6mA	XUOM+XPDV1BT XUO1+XPDV1BT XUO2+XPDV1BT XUO3+XPDV1BT
Normal output with slew rate control for fallling edge only	6mA/-6mA	XUO3L+XPDV3T
3-state output for low noise	0.5mA/-0.5mA 2mA/-2mA 4mA/-4mA 6mA/-6mA	XUOM+XPDV2T XUO1+XPDV2T XUO2+XPDV2T XUO3+XPDV2T
3-state output for high speed	0.5mA/-0.5mA 2mA/-2mA 4mA/-4mA 6mA/-6mA	XUOM+XPDV2AT XUO1+XPDV2AT XUO2+XPDV2AT XUO3+XPDV2AT
3-state output with low slew rate control	0.5mA/-0.5mA 2mA/-2mA 4mA/-4mA 6mA/-6mA	XUOM+XPDV2BT XUO1+XPDV2BT XUO2+XPDV2BT XUO3+XPDV2BT
3-state output with slew rate control for falling edge only	6mA/-6mA	XUO3L+XPDV4T

NOTES: * V_{OL} = 0.3 V (V_{DD} = 3.3 V) Refer to Table 1-5 about the standard of I_{OL} in V_{DD} = 3.0V.
** V_{OH} = V_{DD} - 0.3 V (V_{DD}= 3.3 V) Refer to Table 1-5 about the standard of I_{OH} in V_{DD} = 3.0V.
*** In addition to the configurations in Table 4-7, the output buffers may be configured with pre-drivers which do not have test terminals. Customers desiring to use such structures should direct inquiries to EPSON.

• XODN (Open Drain Output Cell) Usage

As is shown in Table 4-8, configure open drain output functionality using the XODN output cell and pre-driver combinations with the N terminal connection only. Do not connect the P terminal of the pre-driver output. (See Figure 4-2).

Table 4-8 Combinations of Pre-drivers and the XODN System Cells

Function	I_{OL}*	Cell Structure**
Normal output for low noise	0.5mA 2mA 4mA 6mA	XODNM+XPDV1T XODN1+XPDV1T XODN2+XPDV1T XODN3+XPDV1T
Normal output for high speed	0.5mA 2mA 4mA 6mA	XODNM+XPDV1AT XODN1+XPDV1AT XODN2+XPDV1AT XODN3+XPDV1AT
Normal output with slew rate control	6mA	XODN3L+XPDV3T

NOTES * V_{OL} = 0.3 V (V_{DD}= 3.3 V) Refer to Table 1-5 about the standard of I_{OL} in V_{DD} = 3.0V.

** In addition to the structuring methods of Table 4-8, the output buffers may be configured with pre-drivers which do not have test terminals. Customers desiring to use such structures should direct inquiries to EPSON .

4.2.2.3 Bi-directional Buffer Configurations with a Single 3.0/3.3 V Power Supply

Bi-directional buffers are configured from combinations of pre-drivers (with enable terminals) and bi-directional cells. (See Figure 4-3.)

Table 4-9 Combinations of Pre-drivers and Bi-directional Cells

Input Level	Function	I_{OL}*/I_{OH}**	Cell Structure
CMOS	Bi-directional for low noise output	0.5mA/-0.5mA 2mA/-2mA 4mA/-4mA 6mA/-6mA	XUCM+XPDV2T XUC1+XPDV2T XUC2+XPDV2T XUC3+XPDV2T
CMOS	Bi-directional for high speed output	0.5mA/-0.5mA 2mA/-2mA 4mA/-4mA 6mA/-6mA	XUCM+XPDV2AT XUC1+XPDV2AT XUC2+XPDV2AT XUC3+XPDV2AT
CMOS	Bi-directional with low slew rate control output	0.5mA/-0.5mA 2mA/-2mA 4mA/-4mA 6mA/-6mA	XUCM+XPDV2BT XUC1+XPDV2BT XUC2+XPDV2BT XUC3+XPDV2BT
CMOS	Bi-directional with slew rate control output for falling edge only	6mA/-6mA	XUC3L+XPDV4T
CMOS Schmitt	Bi-directional for low noise output	0.5mA/-0.5mA 2mA/-2mA 4mA/-4mA 6mA/-6mA	XUHM+XPDV2T XUH1+XPDV2T XUH2+XPDV2T XUH3+XPDV2T
CMOS Schmitt	Bi-directional for high speed output	0.5mA/-0.5mA 2mA/-2mA 4mA/-4mA 6mA/-6mA	XUHM+XPDV2AT XUH1+XPDV2AT XUH2+XPDV2AT XUH3+XPDV2AT
CMOS Schmitt	Bi-directional with low slew rate control output	0.5mA/-0.5mA 2mA/-2mA 4mA/-4mA 6mA/-6mA	XUHM+XPDV2BT XUH1+XPDV2BT XUH2+XPDV2BT XUH3+XPDV2BT
CMOS Schmitt	Bi-directional with slew rate control output for falling edge only	6mA/-6mA	XUH3L+XPDV4T

NOTES: * V_{OL} = 0.3 V (V_{DD}= 3.3 V) Refer to Table 1-5 about the standard of I_{OL} in V_{DD} = 3.0V.

** V_{OH} = V_{DD} - 0.3 V (V_{DD}= 3.3 V) Refer to Table 1-5 about the standard of I_{OH} in V_{DD} = 3.0V.

*** In addition to the configurations on Table 4-9, bi-directional buffers may be configured with pre-drivers which do not have test terminals. Most bi-directional buffers have two types of pull-up resistance options and two types of pull-down resistance options. Customers desiring to use a pre-driver without test terminals should direct inquiries to EPSON.

**** TTL input levels are not available when using a 3.0 V/3.3 V single power supply.

• XBDC, XBDH System Cells (Bi-directional Cells)

XBDC and XBDH system cells are bi-directional cells which are constructed by combining XIDC (5-volt tolerant input cells) and XODN (open drain output cells). Table 4-10 gives combinations of pre-drivers and XBDC, XBDH system cells.

Table 4-10 Combinations of Pre-drivers and XBDC/XBDH System Cells

Input Level	Function	I_{OL}*	Cell Structure
CMOS	Bi-directional for low noise output	0.5mA 2mA 4mA 6mA	XBDCM+XPDV2T XBDC1+XPDV2T XBDC2+XPDV2T XBDC3+XPDV2T
CMOS	Bi-directional for high speed output	0.5mA 2mA 4mA 6mA	XBDCM+XPDV2AT XBDC1+XPDV2AT XBDC2+XPDV2AT XBDC3+XPDV2AT
CMOS	Bi-directional with low slew rate control output	0.5mA 2mA 4mA 6mA	XBDCM+XPDV2BT XBDC1+XPDV2BT XBDC2+XPDV2BT XBDC3+XPDV2BT
CMOS	Bi-directional with slew rate control output	6mA	XBDC3L+XPDV4T
CMOS Schmitt	Bi-directional for low noise output	0.5mA 2mA 4mA 6mA	XBDHM+XPDV2T XBDH1+XPDV2T XBDH2+XPDV2T XBDH3+XPDV2T
CMOS Schmitt	Bi-directional for high speed output	0.5mA 2mA 4mA 6mA	XBDHM+XPDV2AT XBDH1+XPDV2AT XBDH2+XPDV2AT XBDH3+XPDV2AT
CMOS Schmitt	Bi-directional with low slew rate control output	0.5mA 2mA 4mA 6mA	XBDHM+XPDV2BT XBDH1+XPDV2BT XBDH2+XPDV2BT XBDH3+XPDV2BT
CMOS Schmitt	Bi-directional with slew rate control output	6mA	XBDH3L+XPDV4T

NOTES: * V_{OL} = 0.3 V (V_{DD}= 3.3 V) Refer to Table 1-5 about the standard of I_{OL} in V_{DD} = 3.0V.

** In addition to the configurations in Table 4-10, bi-directional buffers may be configured with pre-drivers which do not have test terminals. Most bi-directional buffers have two types of pull-up resistance options and two types of pull-down resistance options. Customers desiring to use structures without test terminals should direct inquiries to EPSON .

4.3 Oscillation Circuit

4.3.1 Oscillation Circuit Configurations

Oscillation circuits should be configured, as shown in Figure 4-4. Both standard and gated oscillator circuit configurations are supported as shown.

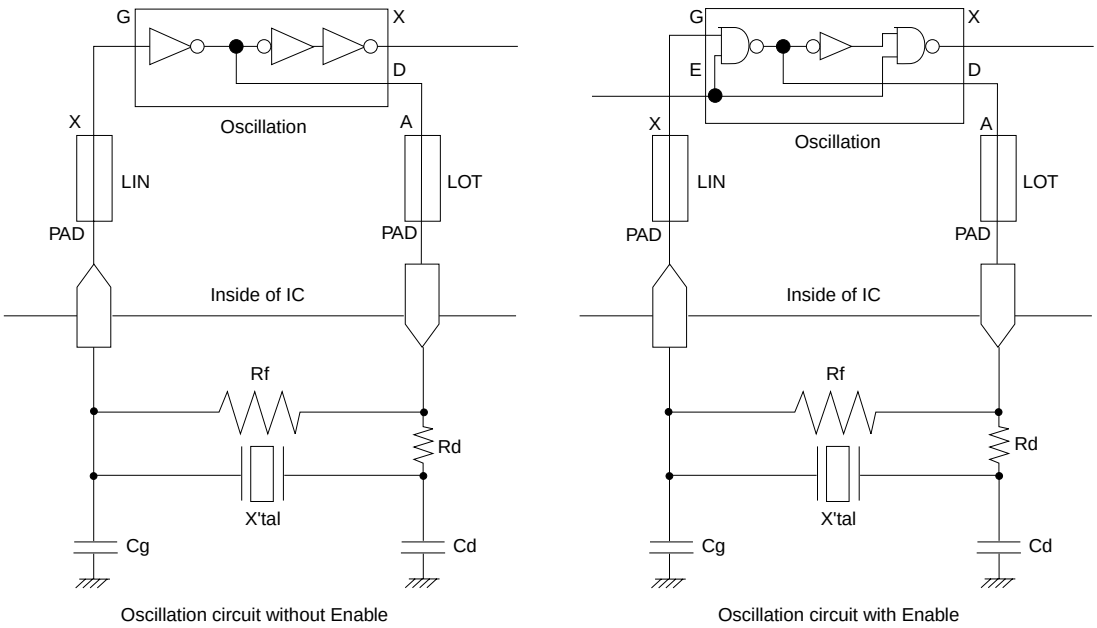


Figure 4-4 Method of Structuring the Oscillator Circuit

4.3.2 Oscillator Circuit Considerations

(1) Pin Layout

The inputs and outputs of the oscillator circuits should be positioned on adjacent pins, and should be located between power supply pins (V_{DD}, V_{SS}). Do not locate high drive output pins near the input/output pins of the oscillator circuit. Be especially careful to locate any outputs having the same phase or the opposite phase of the oscillating wave form as far as possible from the oscillator circuit input/output pins. Whenever possible, locate the input/output pins of the oscillator circuit near the center of the edge of the package.

(2) Oscillator Cell Selection Criteria

The frequency at which oscillation is possible is approximately several 10 KHz to mega-hertz (MHz). For details, please direct inquiries to EPSON.

.

(3) Selecting the Values for the Resistances and Capacitors to be Attached

The characteristics of oscillation depends on the capacitive and resistive biasing elements. Because of this, the capacitive and resistive values must be adjusted, depending on the crystal which will be used on the actual board. Consequently, the optimal values should be chosen through spending adequate time evaluating available engineering samples.

(4) Assurance Levels

EPSON is unable to guarantee the function or characteristics of the oscillation. EPSON can warrantee only the oscillator cell. Because of this, it is necessary for the customer to spend adequate time evaluating the engineering samples in terms of their oscillation characteristics.

(5) Discerning between XLOT and XLOT2

XLOT and XLOT2 are protected yet unbuffered line output cells. XLOT2 is a low-impedance type XLOT, used for situations where the oscillation frequency is high (>25 MHz). The selection of XLOT vs. XLOT2 is done in combination with the oscillator cell. Direct inquiries for details to EPSON.

Chapter 5 RAM

The S1L35000 Series supports 1 port RAM and 2 port RAM.

5.1 Features

(1) 1-Port RAM

- Asynchronous
- Static operation
- 1 read/write address port, 1 input data port, 1 output data port
- RAM configurations supported: Word Depth =16,32,64,96,128,192,256
  Bit Width = 1 to 32 (incremental by 1 bit)
- 3.0 V operation available

(2) 2-Port RAM

- Asynchronous
- Static operation
- 1 read address port, 1 write address port, 1 input data port, 1 output data port
- RAM configurations supported: Word Depth =16,32,64,96,128,192,256
  Bit Width = 1 to 32 (incremental by 1 bit)
- 3.0 V operation available

5.2 RAM Configuration and Simulation Model Selection

RAM delay parameters change depending on the word/bit structure. Six simulation models (three 1-port RAM models and three 2-port RAM models) have been prepared using performance characteristics indicative to the RAM word/bit configuration.

The 1-port RAM and 2-port RAM word/bit structure simulation models are shown in Table 5-1 and 5.2 respectively .

For RAM with word/bit structures exceeding the limitations in the tables below, use combinations of multiple RAMs.

Table 5-1 Simulation Model Selection Chart (1-Port RAM Word/Bit Structure)

Number of words/bits	1 to 8	9 to 16	17 to 32
16, 32	XRAM4	XRAM5	XRAM6
64	XRAM5	XRAM5	XRAM6
96, 128	XRAM6	XRAM6	XRAM6
192, 256	XRAM7	XRAM7	———

NOTE: Although each simulation model supports a variety of RAM configurations, the customer specified RAM configuration will be used during layout.

Table 5-2 Simulation Model Selection Chart (2-Port RAM Word/Bit Structure)

Number of words/bits	1 to 8	9 to 16	17 to 32
16, 32	XRAM2P4	XRAM2P5	XRAM2P6
64	XRAM2P5	XRAM2P5	XRAM2P6
96, 128	XRAM2P6	XRAM2P6	XRAM2P6
192, 256	XRAM2P7	XRAM2P7	————

NOTE: Although each simulation model supports a variety of RAM configurations, the customer specified RAM configuration will be used during layout.

5.3 RAM Size

The X-direction size, Y-direction size, and number of BCs used in the RAM are calculated using the formulas below. The formulas below include the interconnect region contained in the RAM. Use these formulas when investigating master selection when RAM is included (see Section 2.5).

(1) 1-Port RAM

a) For XRAM4, XRAM5, or XRAM6

Size in the X direction: RX = 3 x word/2+J

Here,

J=32; 1 ≤ Bit ≤ 8
J=37; 9 ≤ Bit ≤ 16
J=39; 17≤ Bit ≤ 24
J=44; 25≤ Bit ≤ 32

Size in the Y direction: RY = 2 x Bit + K

Here,

K=12; Word = 16
K=13; Word = 32
K=17; Word ≥ 64

Number of BCs:BC_{RAM} = RX x RY

Table 5-3 An Example of the Structure of 1-Port RAM

Word/Bit	4	8	16	32
16	1120 (56x20)	1568 (56x28)	2684 (61x44)	5168 (68x76)
32	1680 (80x21)	2320 (80x29)	3825 (85x45)	7084 (92x77)
64	3200 (128x25)	4224 (128x33)	6517 (133x49)	11340 (140x81)
96	4400 (176x25)	5808 (176x33)	8869 (229x49)	15228 (188x81)
128	5600 (224x25)	7392 (224x33)	11221 (325x49)	19116 (236x81)
192	8000 (320x25)	10560 (320x33)	15925 (325x49)	————
256	10400 (416x25)	13728 (416x33)	20629 (421x49)	————

NOTE: The numbers within this chart indicate BC_{RAM} (RX x RY) which includes interconnect area.

(2) 2-Port RAM

Size in the X direction: RX = 3 x Word /2+J

Here,

J=32; $1 \leq Bit \leq 8$

J=37; $9 \leq Bit \leq 16$

J=39; $17 \leq Bit \leq 24$

J=44; $25 \leq Bit \leq 32$

Size in the Y direction: RY = 2 x Bit + K

Here,

K=14; Word = 16

K=15; Word = 32

K=21; Word ≥ 64

Number of BCs: BC_{RAM} = RX x RY

Table 5-4 An Example of the Structure of 2-Port RAM

Word/Bit	4	8	16	32
16	1232 (56x22)	1680 (56x30)	2806 (61x46)	5304 (68x78)
32	1840 (80x23)	2480 (80x31)	3995 (85x47)	7268 (92x79)
64	3712 (128x29)	4736 (128x37)	7049 (133x53)	11900 (140x85)
96	5104 (176x29)	6512 (176x37)	9593 (181x53)	15980 (188x85)
128	6496 (224x29)	8288 (224x37)	12137 (229x53)	20060 (236x85)
192	9280 (320x29)	11840 (320x37)	17225 (325x47)	———
256	12064 (416x29)	15392 (416x37)	22313 (410x47)	———

NOTE: The numbers within this chart indicate BC_{RAM} (RX x RY), which includes interconnect area.

5.4 Investigating RAM Placement on Master Slice

When investigating RAM placement on a master slice, please insure that sufficient area is available in both the X direction (column) and the Y direction (row). When loading RAM onto a chip, it is necessary to insure that the capacity of the master exceeds the required RAM area in both the X and Y directions.

When multiple RAMs are used, RAM blocks are placed adjacent to each other either horizontally or vertically; the decision regarding master slice selection is based simply on RX and RY. Please see Table 1-1 of Chapter 1 regarding the number of columns (X-direction) and number of rows (Y-direction).

For example, if five 256word x 4 bit 1-port RAMs are required.

As shown in Figure 5-1, the total RAM layout area would be:

X direction: 416 BCs
Y direction: 125 BCs (25 x 5)

Because of this,

S1L35043 is (X, Y) = (499, 83) is impossible due to area constraints, however,
S1L35063 is (X, Y) = (480, 134) is possible.

See Section 2.5 pertaining to estimating the number of gates, BC_{AWR}, which can be used for random logic.

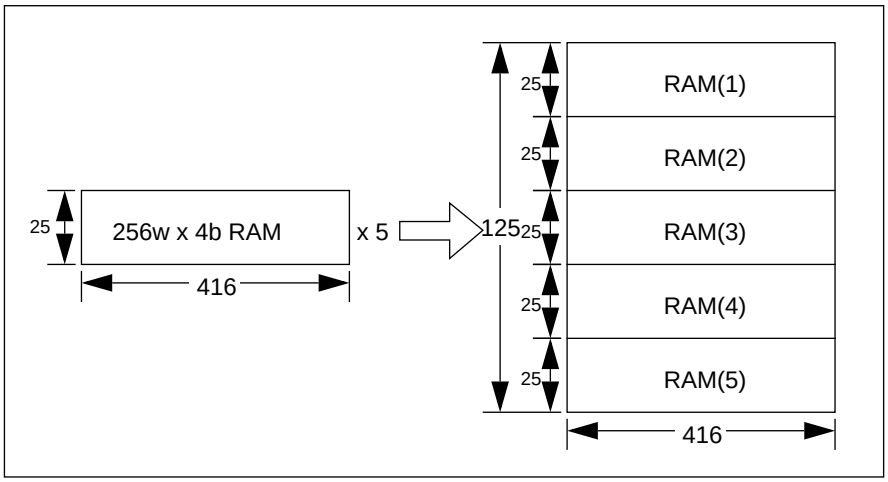


Figure 5-1 Example of RAM Layout

5.5 Explanation of Functions

(1) 1-Port RAM

Table 5-5 1-Port RAM Signals

Signal Name	I/O	Function	Notes
CS	IN	Chip select signal, H: RAM active	FI = 1LU
RW	IN	Read/write signal, H: Read, L: Write	FI = 1LU
A0, A1 ... A(m-1)	IN	Read/write address port, A0: LSB	FI = 1LU
D0, D1 ... D(n-1)	IN	Data input port, D0: LSB	FI = 2LU
Y0, Y1 ... Y(n-1)	OUT	Data output port, Y0: LSB	FO = 49LU corresponds to K:IN2

Table 5-6 1-Port RAM Truth Table

CS	RW	A0, A1 ... A(m-1)	Y0, Y1 ... Y(n-1)	Mode
0	X	X	Unknown	Wait
1	0	Stable	Unknown	Write
1	1	Stable	Read Data	Read

X: “H” or “L”

• Data Read
The data is read by holding CS at “H” and RW at “H” and setting the address.

• Data Write
The data can be written in either of the following two ways:
(1) Holding CS at “H”, setting the address, and sending a negative pulse to RW.
(2) Holding RW at “L”, setting the address, and sending a positive pulse to CS.

When either method is used, the data is latched to the RAM at the trailing edge of the pulse.

• The Wait State
When CS is “L”, the 1 port RAM enters a wait state and only maintains the data. The current consumed by the RAM is merely the leakage current, and is almost zero.

(2) 2-Port RAM

Table 5-7 2-Port RAM Signals

Signal Name	I/O	Function	Notes
CS	IN	Chip select signal, H: RAM active	FI = 1LU
RD	IN	Read signal, H: Read enable	FI = 1LU
WR	IN	Write signal, H: Write enable	FI = 1LU
RA0, . . . RA(m-1)	IN	Read address port, RA0: LSB	FI = 1LU
WA0, . . . WA(m-1)	IN	Write address port, WA0: LSB	FI = 1LU
D0, D1, . . . D(n-1)	IN	Data input port, D0: LSB	FI = 2LU
Y0, Y1, . . . Y(n-1)	OUT	Data output port, Y0: LSB	F0 = 49LU corresponds to K:IN2

Table 5-8 2-Port RAM Truth Table

CS	RD	WR	RA0, ... RA(n-1)	WA0, ...WA(m-1)	Y0, ... Y(n-1)	Mode
0	X	X	X	X	Unknown	Wait
1	0	0	X	X	Unknown	Wait
1	0	1	X	Stable	Unknown	Write
1	1	0	Stable	X	Read Data	Read
1	1	1	Stable	Stable	Read Data	Read & Write

X: “H” or “L”

• Data Read

The data is read by holding CS at “H” and RD at “H” and setting the read address.

• Data Write

The data can be written in either of the following two ways:

(1)Holding CS at “H”, setting the write address, and sending a positive pulse to WR.

(2)Holding WR at “H”, setting the write address, and sending a positive pulse to CS.

• Data Read/Write

When reading is done at the same time as writing, it is possible by performing the respective methods simultaneously. However, these two operations cannot be performed simultaneously on the same address. The read cycle access time applies to data for which the writing has already been completed.

• The Wait State

When CS is "L" ,the 1 port RAM enters a wait state and only maintains the data. The current consumed by the RAM is merely the leakage current, and is almost Zero.

5.6 Delay Parameters

(1) 3.0 V Specifications (V_{DD} = 2.7 to 3.3V ; Ta = -40 to 85°C)

Table 5-9 1-Port RAM Read Cycle

Parameter	Signal	XRAM 4		XRAM 5		XRAM 6		XRAM 7		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	11.92	–	15.37	–	24.15	–	33.87	–	ns
Address access time	t_{ACC}	–	11.92	–	15.37	–	24.15	–	33.87	
CS access time	t_{ACS}	–	11.47	–	14.77	–	23.25	–	32.71	
R/W access time	t_{ARW}	–	10.20	–	13.80	–	21.45	–	30.26	
CS active time	t_{RCS}	11.92	–	15.37	–	24.15	–	33.87	–	
Output hold time after address change	t_{OH}	0.32	–	0.39	–	0.52	–	0.52	–	
Output hold time after CS disable	t_{OHCS}	0.32	–	0.39	–	0.52	–	0.52	–	
Output hold time after R/W disable	t_{OHRW}	0.33	–	0.45	–	0.52	–	0.52	–	

Table 5-10 1-Port RAM Write Cycle

Parameter	Signal	XRAM 4		XRAM 5		XRAM 6		XRAM 7		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	13.27	–	15.45	–	21.45	–	21.45	–	ns
Write pulse width	t_{WP}	9.07	–	10.72	–	15.60	–	15.60	–	
CS active time	t_{WCS}	9.07	–	10.72	–	15.60	–	15.60	–	
Address setup time	t_{AS}	1.87	–	2.17	–	2.70	–	2.70	–	
Address hold time	t_{AH}	2.32	–	2.62	–	3.15	–	3.15	–	
Data setup time	t_{DS}	2.92	–	3.30	–	4.20	–	4.20	–	
Data hold time	t_{DH}	4.05	–	6.60	–	9.30	–	9.30	–	

Table 5-11 2-Port RAM Read Cycle

Parameter	Signal	XRAM 2P4		XRAM 2P5		XRAM 2P6		XRAM 2P7		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	11.92	–	15.37	–	24.15	–	33.87	–	ns
Address access time	t_{ACC}	–	11.92	–	15.37	–	24.15	–	33.87	
CS access time	t_{ACS}	–	11.47	–	14.77	–	23.25	–	32.71	
RD access time	t_{ARW}	–	10.20	–	13.80	–	21.45	–	30.26	
CS active time	t_{RCS}	11.92	–	15.37	–	24.15	–	33.87	–	
Output hold time after address change	t_{OH}	0.32	–	0.39	–	0.52	–	0.52	–	
Output hold time after CS disable	t_{OHCS}	0.32	–	0.39	–	0.52	–	0.52	–	
Output hold time after RD disable	t_{OHRW}	0.33	–	0.45	–	0.52	–	0.52	–	

Table 5-12 2-Port RAM Write Cycle

Parameter	Signal	XRAM 2P4		XRAM 2P5		XRAM2P6		XRAM2P7		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	13.27	–	15.45	–	21.45	–	21.45	–	ns
Write pulse width	t_{WP}	9.07	–	10.72	–	15.60	–	15.60	–	
CS active time	t_{WCS}	9.07	–	10.72	–	15.60	–	15.60	–	
Address setup time	t_{AS}	1.87	–	2.17	–	2.70	–	2.70	–	
Address hold time	t_{AH}	2.32	–	2.62	–	3.15	–	3.15	–	
Data setup time	t_{DS}	2.92	–	3.30	–	4.20	–	4.20	–	
Data hold time	t_{DH}	4.05	–	6.60	–	9.30	–	9.30	–	

(2) 3.3 V Specifications (V_{DD} = 3.0 to 3.6V ; Ta = -40 to 85°C)

Table 5-13 1-Port RAM Write Cycle

Parameter	Signal	XRAM 4		XRAM 5		XRAM 6		XRAM 7		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	10.42	–	13.50	–	21.22	–	30.35	–	ns
Address access time	t_{ACC}	–	10.42	–	13.50	–	21.22	–	30.35	
CS access time	t_{ACS}	–	10.05	–	12.97	–	20.40	–	29.19	
R/W access time	t_{ARW}	–	8.92	–	12.15	–	18.82	–	27.61	
CS active time	t_{RCS}	10.42	–	13.50	–	21.22	–	30.35	–	
Output hold time after address change	t_{OH}	0.29	–	0.36	–	0.50	–	0.50	–	
Output hold time after CS disable	t_{OHCS}	0.29	–	0.36	–	0.50	–	0.50	–	
Output hold time after R/W disable	t_{OHRW}	0.30	–	0,42	–	0.53	–	0.53	–	

Table 5-14 1-Port RAM Write Cycle

Parameter	Signal	XRAM 4		XRAM 5		XRAM 6		XRAM 7		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	11.62	–	13.57	–	18.82	–	18.82	–	ns
Write pulse width	t_{WP}	7.95	–	9.37	–	13.65	–	13.65	–	
CS active time	t_{WCS}	7.95	–	9.37	–	13.65	–	13.65	–	
Address setup time	t_{AS}	1.65	–	1.95	–	2.40	–	2.40	–	
Address hold time	t_{AH}	2.02	–	2.25	–	2.77	–	2.77	–	
Data setup time	t_{DS}	2.55	–	2.92	–	3.67	–	3.67	–	
Data hold time	t_{DH}	3.52	–	5.77	–	8.17	–	8.17	–	

Table 5-15 2-Port RAM Read Cycle

Parameter	Signal	XRAM 2P4		XRAM 2P5		XRAM 2P6		XRAM 2P7		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	10.42	–	13.50	–	21.22	–	30.35	–	ns
Address access time	t_{ACC}	–	10.42	–	13.50	–	21.22	–	30.35	
CS access time	t_{ACS}	–	10.05	–	12.97	–	20.40	–	29.19	
RD access time	t_{ARW}	–	8.92	–	12.15	–	18.82	–	27.61	
CS active time	t_{RCS}	10.42	–	13.50	–	21.22	–	30.35	–	
Output hold time after address change	t_{OH}	0.29	–	0.36	–	0.50	–	0.50	–	
Output hold time after CS disable	t_{OHCS}	0.29	–	0.36	–	0.50	–	0.50	–	
Output hold time after RD disable	t_{OHRW}	0.30	–	0.42	–	0.53	–	0.53	–	

Table 5-16 2-Port RAM Write Cycle

Parameter	Signal	XRAM 2P4		XRAM 2P5		XRAM2P6		XRAM2P7		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	11.62	–	13.57	–	18.82	–	18.82	–	ns
Write pulse width	t_{WP}	7.95	–	9.37	–	13.65	–	13.65	–	
CS active time	t_{WCS}	7.95	–	9.37	–	13.65	–	13.65	–	
Address setup time	t_{AS}	1.65	–	1.95	–	2.40	–	2.40	–	
Address hold time	t_{AH}	2.02	–	2.25	–	2.77	–	2.77	–	
Data setup time	t_{DS}	2.55	–	2.92	–	3.67	–	3.67	–	
Data hold time	t_{DH}	3.52	–	5.77	–	8.17	–	8.17	–	

(3) 5.0 V ± 5% Specifications (V_{DD} = 4.75 to 5.25V; Ta = 0 to 70°C)

Table 5-17 1-Port RAM Read Cycle

Parameter	Signal	XRAM 4		XRAM 5		XRAM 6		XRAM 7		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	5.92	–	7.57	–	11.70	–	16.74	–	ns
Address access time	t_{ACC}	–	5.92	–	7.57	–	11.70	–	16.74	
CS access time	t_{ACS}	–	5.70	–	7.27	–	11.17	–	15.79	
R/W access time	t_{ARW}	–	5.32	–	6.75	–	10.12	–	13.96	
CS active time	t_{RCS}	5.92	–	7.57	–	11.70	–	16.74	–	
Output hold time after address change	t_{OH}	0.26	–	0.32	–	0.44	–	0.44	–	
Output hold time after CS disable	t_{OHCS}	0.27	–	0.33	–	0.45	–	0.45	–	
Output hold time after R/W disable	t_{OHRW}	0.27	–	0.33	–	0.45	–	0.45	–	

Table 5-18 1-Port RAM Write Cycle

Parameter	Signal	XRAM 4		XRAM 5		XRAM 6		XRAM 7		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	8.02	–	9.22	–	11.92	–	11.92	–	ns
Write pulse width	t_{WP}	5.55	–	6.52	–	8.40	–	8.40	–	
CS active time	t_{WCS}	5.55	–	6.52	–	8.40	–	8.40	–	
Address setup time	t_{AS}	1.12	–	1.20	–	1.50	–	1.50	–	
Address hold time	t_{AH}	1.35	–	1.50	–	2.02	–	2.02	–	
Data setup time	t_{DS}	1.65	–	1.87	–	2.32	–	2.32	–	
Data hold time	t_{DH}	2.85	–	3.60	–	5.10	–	5.10	–	

Table 5-19 2-Port RAM Read Cycle

Parameter	Signal	XRAM 2P4		XRAM 2P5		XRAM 2P6		XRAM 2P7		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	5.92	–	7.57	–	11.70	–	16.74	–	ns
Address access time	t_{ACC}	–	5.92	–	7.57	–	11.70	–	16.74	
CS access time	t_{ACS}	–	5.70	–	7.27	–	11.17	–	15.79	
RD access time	t_{ARW}	–	5.32	–	6.75	–	10.12	–	13.96	
CS active time	t_{RCS}	5.92	–	7.57	–	11.70	–	16.74	–	
Output hold time after address change	t_{OH}	0.26	–	0.32	–	0.44	–	0.44	–	
Output hold time after CS disable	t_{OHCS}	0.27	–	0.33	–	0.45	–	0.45	–	
Output hold time after RD disable	t_{OHRW}	0.27	–	0.33	–	0.45	–	0.45	–	

Table 5-20 2-Port RAM Write Cycle

Parameter	Signal	XRAM 2P4		XRAM 2P5		XRAM2P6		XRAM2P7		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	8.02	–	9.22	–	11.92	–	11.92	–	ns
Write pulse width	t_{WP}	5.55	–	6.52	–	8.40	–	8.40	–	
CS active time	t_{WCS}	5.55	–	6.52	–	8.40	–	8.40	–	
Address setup time	t_{AS}	1.12	–	1.20	–	1.50	–	1.50	–	
Address hold time	t_{AH}	1.35	–	1.50	–	2.02	–	2.02	–	
Data setup time	t_{DS}	1.65	–	1.87	–	2.32	–	2.32	–	
Data hold time	t_{DH}	2.85	–	3.60	–	5.10	–	5.10	–	

(4) 5.0V ± 10% Specifications (V_{DD} = 4.5 to 5.5V ; Ta = -40 to 85°C)

Table 5-21 1-Port RAM Read Cycle

Parameter	Signal	XRAM 4		XRAM 5		XRAM 6		XRAM 7		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	6.30	–	8.10	–	12.52	–	17.85	–	ns
Address access time	t_{ACC}	–	6.30	–	8.10	–	12.52	–	17.85	
CS access time	t_{ACS}	–	6.08	–	7.80	–	12.00	–	16.90	
R/W access time	t_{ARW}	–	5.70	–	7.20	–	10.87	–	15.04	
CS active time	t_{RCS}	6.30	–	8.10	–	12.52	–	17.85	–	
Output hold time after address change	t_{OH}	0.23	–	0.28	–	0.39	–	0.39	–	
Output hold time after CS disable	t_{OHCS}	0.24	–	0.28	–	0.39	–	0.39	–	
Output hold time after R/W disable	t_{OHRW}	0.24	–	0.29	–	0.39	–	0.39	–	

Table 5-22 1-Port RAM Write Cycle

Parameter	Signal	XRAM 4		XRAM 5		XRAM 6		XRAM 7		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	8.62	–	9.90	–	12.80	–	12.80	–	ns
Write pulse width	t_{WP}	6.00	–	6.97	–	9.00	–	9.00	–	
CS active time	t_{WCS}	6.00	–	6.97	–	9.00	–	9.00	–	
Address setup time	t_{AS}	1.20	–	1.35	–	1.65	–	1.65	–	
Address hold time	t_{AH}	1.42	–	1.57	–	2.17	–	2.17	–	
Data setup time	t_{DS}	1.80	–	2.02	–	2.55	–	2.55	–	
Data hold time	t_{DH}	3.07	–	3.90	–	5.47	–	5.47	–	

Table 5-23 2-Port RAM Read Cycle

Parameter	Signal	XRAM 2P4		XRAM 2P5		XRAM 2P6		XRAM 2P7		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	6.30	–	8.10	–	12.52	–	17.85	–	ns
Address access time	t_{ACC}	–	6.30	–	8.10	–	12.52	–	17.85	
CS access time	t_{ACS}	–	6.08	–	7.80	–	12.00	–	16.90	
RD access time	t_{ARW}	–	5.70	–	7.20	–	10.87	–	15.04	
CS active time	t_{RCS}	6.30	–	8.10	–	12.52	–	17.85	–	
Output hold time after address change	t_{OH}	0.23	–	0.28	–	0.39	–	0.39	–	
Output hold time after CS disable	t_{OHCS}	0.24	–	0.28	–	0.39	–	0.39	–	
Output hold time after RD disable	t_{OHRW}	0.24	–	0.29	–	0.39	–	0.39	–	

Table 5-24 2-Port RAM Write Cycle

Parameter	Signal	XRAM 2P4		XRAM 2P5		XRAM2P6		XRAM2P7		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	8.62	–	9.90	–	12.80	–	12.80	–	ns
Write pulse width	t_{WP}	6.00	–	6.97	–	9.00	–	9.00	–	
CS active time	t_{WCS}	6.00	–	6.97	–	9.00	–	9.00	–	
Address setup time	t_{AS}	1.20	–	1.35	–	1.65	–	1.65	–	
Address hold time	t_{AH}	1.42	–	1.57	–	2.17	–	2.17	–	
Data setup time	t_{DS}	1.80	–	2.02	–	2.55	–	2.55	–	
Data hold time	t_{DH}	3.07	–	3.90	–	5.47	–	5.47	–	

5.7 Timing Charts

(1) 1-Port RAM

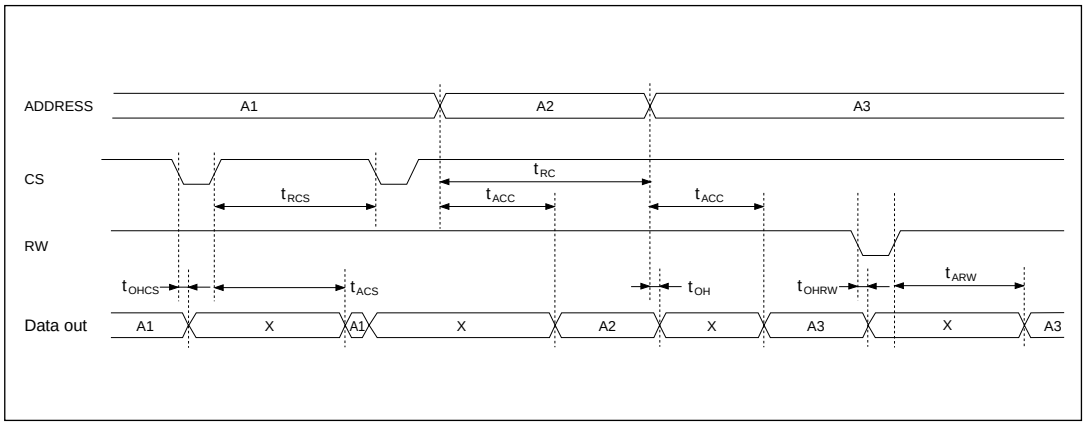


Figure 5-2 Read Cycle

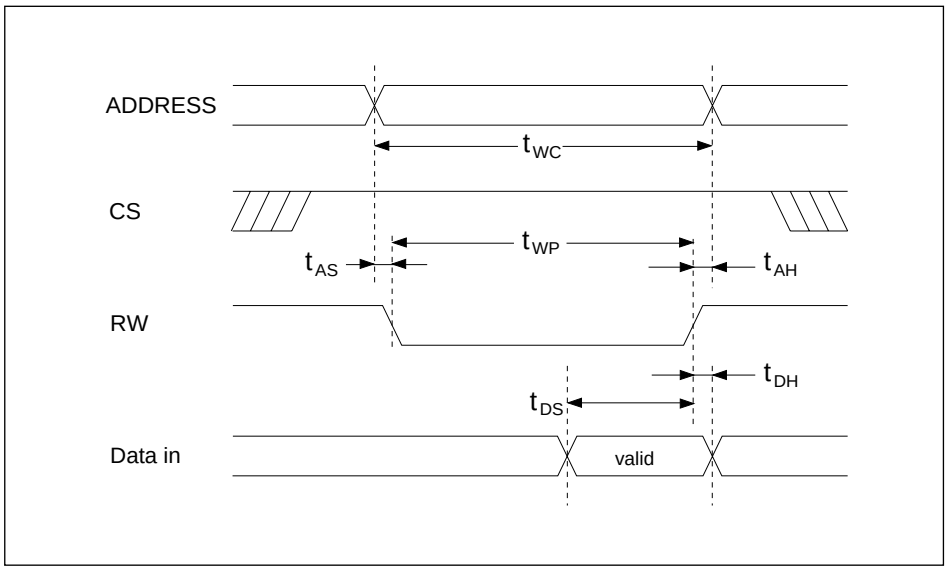


Figure 5-3 Write Cycle (R/W Control)

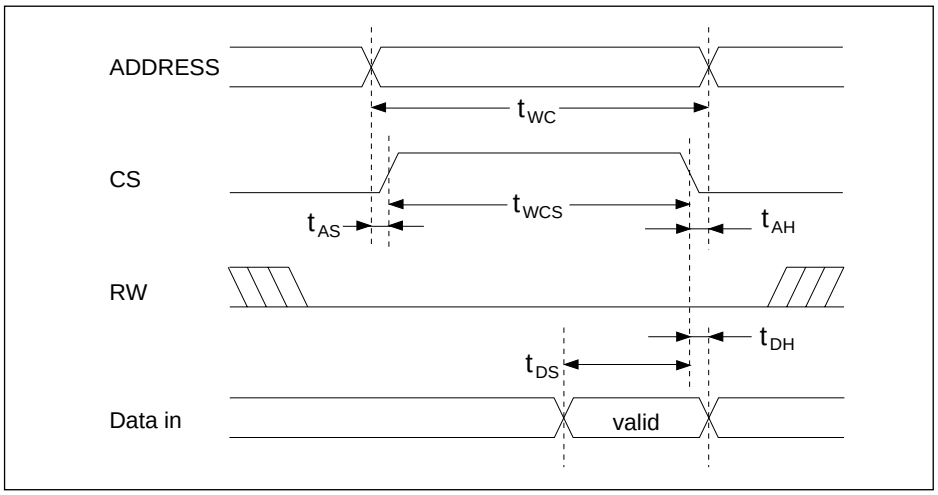


Figure 5-4 Write Cycle (CS Control)

(2) 2-Port RAM

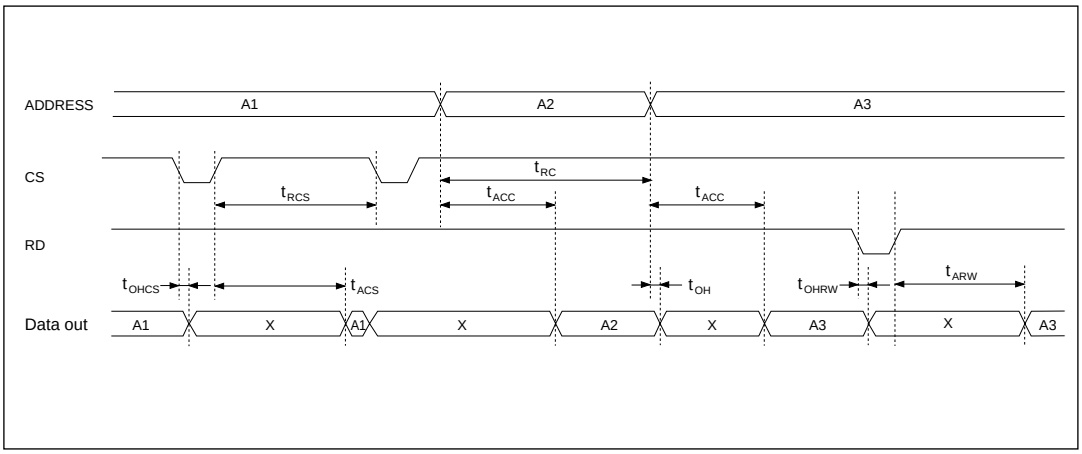


Figure 5-5 Read Cycle

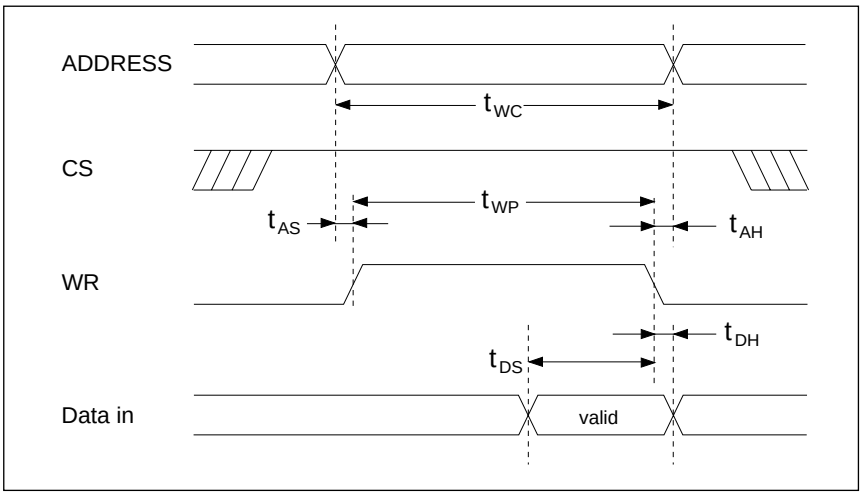


Figure 5-6 Write Cycle (Write Control)

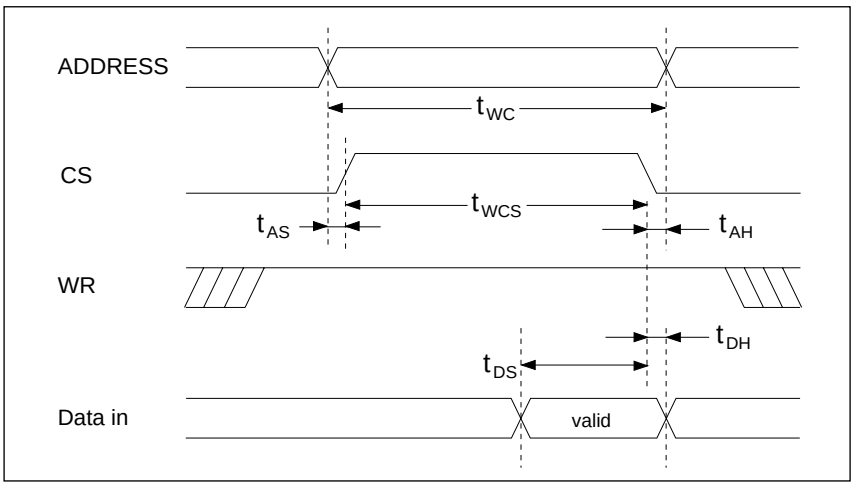


Figure 5-7 Write Cycle (CS Control)

5.8 RAM Test Method

When it comes to internal RAM, specialized tests are performed corresponding to the RAM, separate from the ramdom logic. Please structure test circuits which facilitate direct access to the internal RAM from external pins for this purpose. See Section 6.3 of Chapter 6 regarding the method of structuring the RAM test circuits.

Also, although EPSON will generate an independent test pattern for the RAM, the customer should provide test patterns for the remaining random logic, in addition to a RAM test pattern template, as shown in Section 6.3.1.

5.9 Estimating RAM Current Consumption

The method for estimating the current consumption at V_{DD} (Typ.) = 5.0 V is given below.

Moreover, for V_{DD} (Typ.) = 3.0 V or 3.3 V, the value is approximately 0.6 (60%) of the value which is calculated using the method shown below.

At standby (CS = 0) : 0 [µA/Bit]
During operation (CS = 1) : $[(-1.5x^2 + 832x) * 10^{-4} + 2.0y + 6.075] * f$

x : Words
y : Bits
f : MH_Z (average access cycles)

5.10 RAM Symbols and How They are Used

When the 1 port RAM uses a 32 word x 8 bit structure, the use of symbols is as given in Figure 5-8. This structure requires 5 address pins and 8 data input pins. As is shown in Figure 5-8, any unused address pins or data input pins should be tied to “L” or “H” beginning with the most significant bits.
Furthermore, if multiple RAMs are used, the circuit shoud be configured by using the same numbers of symbols as RAMs.

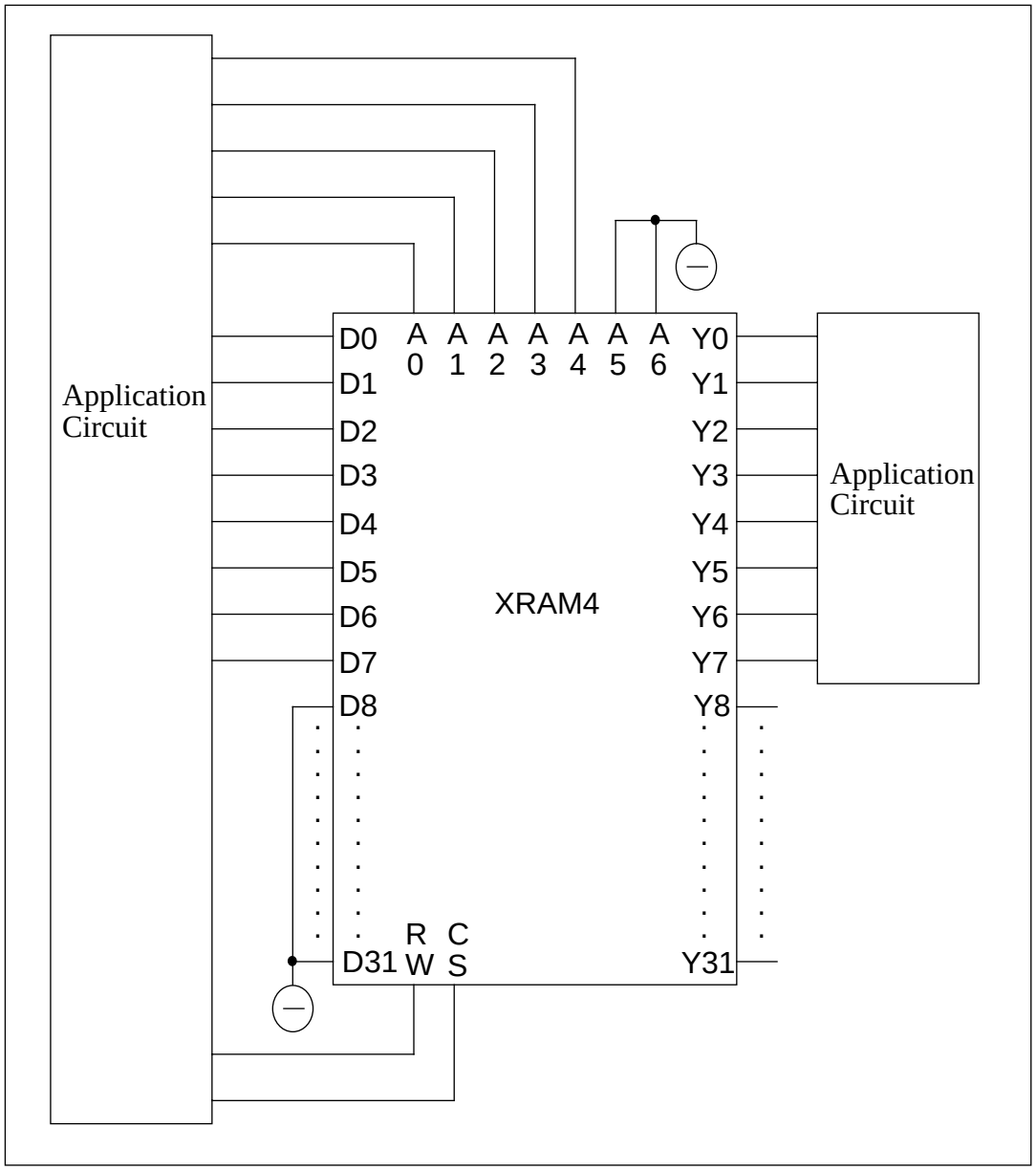


Figure 5-8 Example of the Use of RAM Symbols (XRAM4: 32 words x 8 Bits)

Chapter 6 Circuit Design Taking Testability Into Account

Before a gate array is shipped the product is tested using an LSI tester. It is necessary to design the circuit keeping testability in mind to facilitate this testing. When designing the circuit, the following points should be carefully considered.

6.1 Considerations Regarding Circuit Initialization

When testing ICs using an LSI tester, or when verifying circuit functionality using a software simulator, the initial state of all sequential element is X (unknown). Consequently, very large test patterns may be necessary, depending on the circuit structure, to initialize the sequential elements or it may not be possible to initialize the circuits at all. Because of this, the circuits should be structured to facilitate easy initialization when they are designed (for example, by using sequential elements which have reset, set or preset functions).

6.2 Considerations Regarding Compressing the Test Patterns

As the gate densities of circuits increase, there is a tendency for test patterns to become larger as well. However, one must understand that there are constraints, such as shown below, to the LSI device tests.

Number of events per test pattern:	64K events or less
Number of test patterns:	20 test patterns or less
Total number of test pattern events:	256K events or less

These event and test pattern constraints include the test patterns for test patterns for leakage testing, test patterns for test circuits, and the test patterns for RAM/ROM and megacell testing (prepared by EPSON). Direct inquiries regarding the number of test patterns and number of events per test pattern for the RAM/ROM and megacell testing to EPSON.

When designing, please structure circuits in such a way as to increase the testability of the circuit (and to allow the compression of the test patterns), using methods such as including test pins which allow the input of clocks between the counter stages and adding test pins by which to monitor internal signals.

6.3 RAM Test Circuit

When a RAM is used it is necessary to test all bits before shipping the product. RAM terminals must be accessible via primary I/O pins. RAM test circuitry can be implemented, which multiplexes existing pin functionality with direct RAM access functionality so as to avoid increasing the designs pin count.

Also, when multiple RAMs are used, we recommend that each RAM's pins be accessible via unique I/O pins. However, when the number of external I/O pins is inadequate, each RAM's pins may share common external I/O pins. Please insure that while in RAM test mode, all RAM CS pins can be held "L" simultaneously to facilitate quiescent current meas urement.

Figure 6-1 is an example of a test circuit for two word x 2 bit RAMs. When the test pin "TEST" is "L", then normal functioning is performed. However, when the test pin "TEST" is "H", then the external pins ICS, IRW, ID0, ID1, and IA0 can write data directly to the RAM, and at the same time the RAM outputs can be read from the external pins AY0 and AY1.

Although it is possible to share the RAM pins with bi-directional pins or 3-state output pins, it is necessary to tie the bi-directional pins to either an input or an output state during RAM test. However, please do not share a bi-directional cell with a pull-up resistor with the RAM output, and do not share a input cell with a pull-up with the RAM CS pin, because doing so would make it impossible to measure the quiescent current.

When multiple RAMs are used, all RAM CS pins can be held "L" simultaneously to facilitate quiecent current measurement.

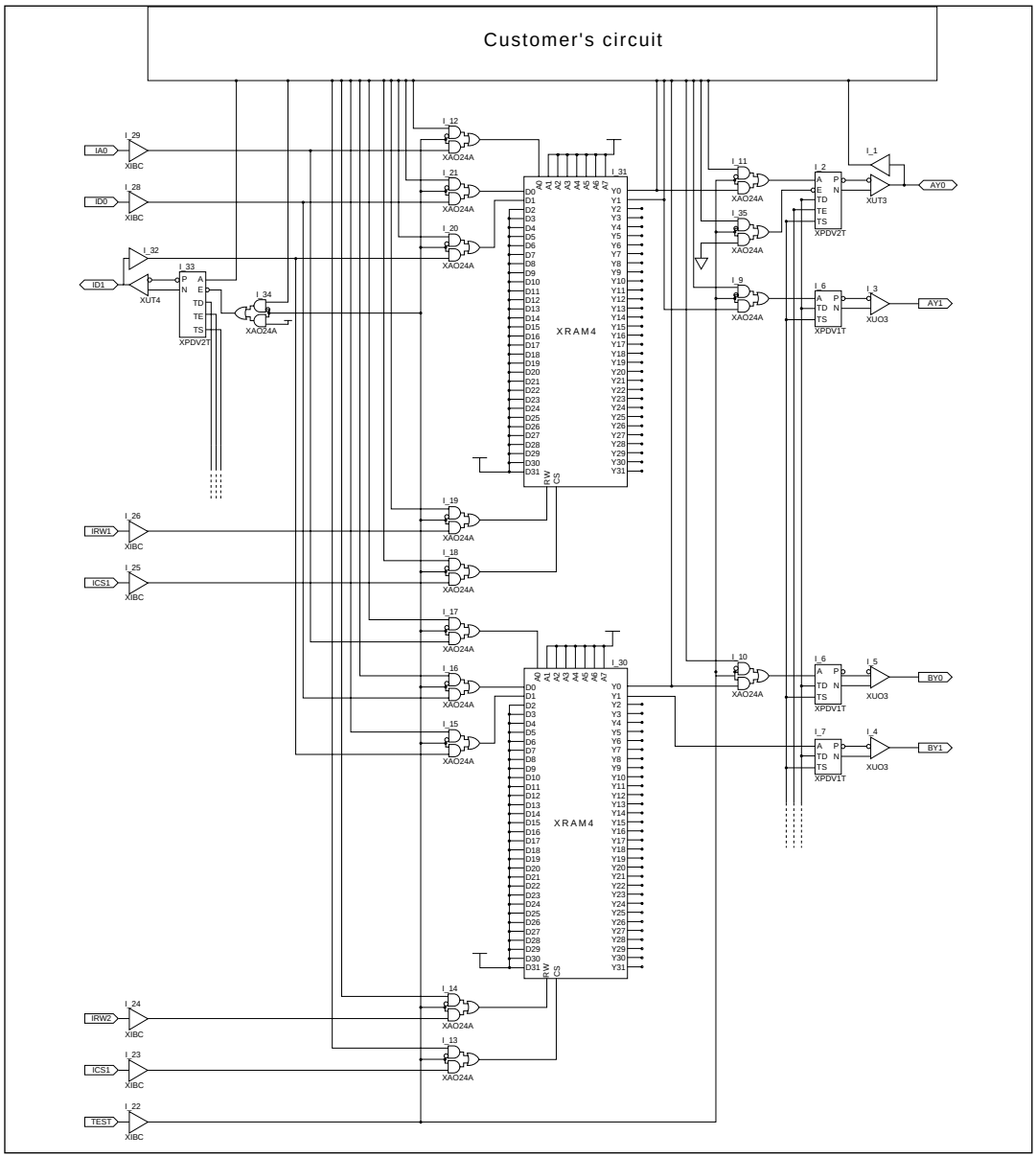


Figure 6-1 Example of a RAM Test Circuit

6.3.1 RAM Test Pattterns

After incorporating RAM test circuitry, it is necessary to make test patterns for both the normal operating state and the test state of the chip. Checks are performed in the normal state to verify the connection with the user circuits, and are performed to insure that the test circuit is correct in the test state. Also, we request a test pattern to serve as a template when EPSON generates the RAM test pattern. See Figure 6-2 and 6.3 for an outline of how to generate this test pattern.

This pattern serves as a template for 1-port RAM tests

```
$CLO INPH 500000
*RAM     AAADDDDRC     YYYY
* Signals0120123WS     0123
*

         0000000000.. 0000..
         0000000001.. 1111..
         1234567890.. 1234..
         IIIIIIIIIT.. 0000..
         NNNNNNNNNE.. UUUU..
         PPPPPPPPPS.. TTTT..
         ABCDEFGHIT.. ABCD..
                  E..
                  N..

1000000  IIIIIIIIII.. 0000..
                 2  ..
                 0  ..
                 0  ..
                 0  ..
         0000000000..

       0 0001010101.. XXXX..
       1 0001010N11.. XXXX..
       2 0001010111.. HLHL..
       3 1011111101.. XXXX..
       4 1011111N11.. XXXX..
       5 1011111111.. HHHH..
       6 1110101101.. XXXX..
       7 1110101N11.. XXXX..
       8 1110101111.. LHLH..
```

It is useful to place comments here.

Please provide all I/O pins used in performing simulation.

Reference the timing chart below to set timing.

When a sequence is necessary to set the test mode, input the pattern here.

[1] Access the lowest address, a middle address and the highest address.

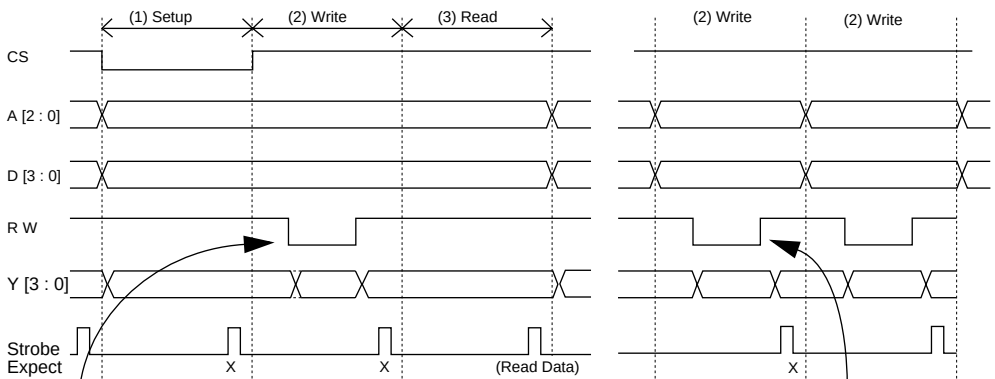
[2] Structure a single access from 3 events (test cycles). In the first event, set the data and the address. In the next event, perform a write. In the third event, perform a read.

[3] Use an RZ waveform to describe the RW signal so that the write operation can be completed in a single event.

[4] Change the data to be written for each address tested.

[5] Verify that the results are the same as expected from the results of the simulations.

Timing Chart



The tester may perform repetitive write operations with the timing shown in the timing chart on the right. The timing of the RW signal should take this into account.

Figure 6-3 Generating the RAM Test Pattern

• Example of test pattern for 2-port RAM (APF format)

```
$RATE   200000
$STROBE 185000
$RESOLUTION 0.001ns

$NODE
INPA    I  0
INPB    I  0
INPC    I  0
INPD    I  0
INPE    I  0
INPF    I  0
INPG    I  0
INPH    I  0
INPI    P  20000  520000
INPJ    I  0
TESTEN  I  0
  .
OUTA    0
OUTB    0
OUTC    0
OUTD    0
  .
  .
$ENDNODE

$PATTERN
          0   00010100001.XXXX..
          1   00010100P11.XXXX..
          2   00010101011.HLHL..
          3   10111110001.XXXX..
          4   10111110P11.XXXX..
          5   10111111011.HHHH..
          6   11101010001.XXXX..
          7   11101010P11.XXXX..
          8   11101011011.LHLH..
```

This pattern serves as a template for 2-port RAM tests

```
$CLO INPI 500000
*RAM      AAADDDDRWC     YYYY
* Signals 0120123DRS     0123
*
          00000000000  .0000 ..
          00000000011  .1111 ..
          12345678901  .2345 ..
          IIIIIIIIIIT  .0000 ..
          NNNNNNNNNNE  .UUUU ..
          PPPPPPPPPPS  .TTTT ..
          ABCDEFGHIJT  .ABCD ..
                     E  .
                     N  .

1000000   IIIIIIIIIII  .0000 ..
          00000000200  .
          00000000000  .
          00000000000  .
          00000000000  .
          00000000000  .

      0   00010100001  .XXXX..
      1   00010100P11  .XXXX..
      2   00010101011  .HLHL..
      3   10111110001  .XXXX..
      4   10111110P11  .XXXX..
      5   10111111011  .HHHH..
      6   11101010001  .XXXX..
      7   11101010P11  .XXXX..
      8   11101011011  .LHLH..
```

It is useful to place comments here.

Please provide all I/O pins used in performing simulation.

Reference the timing chart below to set timing.

When a sequence is necessary to set the test mode, input the pattern here.

[1] Access the lowest address, a middle address and the highest address.

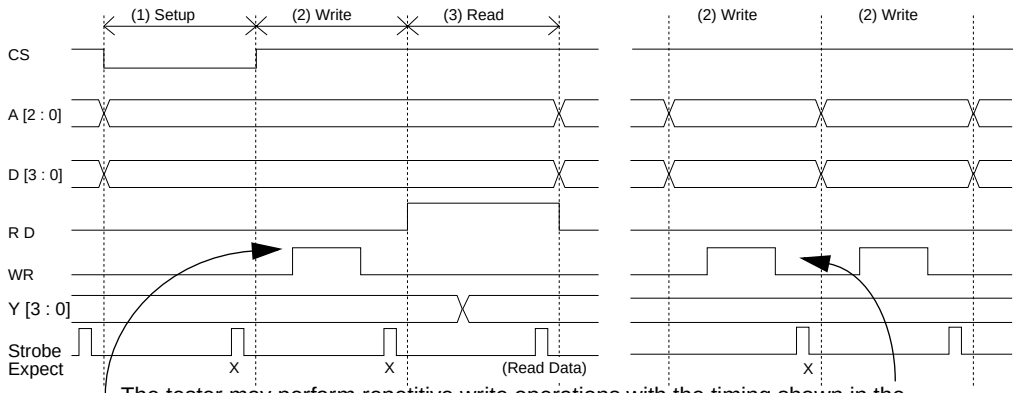
[2] Structure a single access from 3 events (test cycles). In the first event, set the data and the address. In the next event, perform a write. In the third event, perform a read.

[3] Use an WRwaveform to describe the WRsignal so that the write operation can be completed in a single event.

[4] Change the data to be written for each address tested.

[5] Verify that the results are the same as expected from the results of the simulations.

Timing Chart



The tester may perform repetitive write operations with the timing shown in the timing chart on the right. The timing of the WR signal should take this into account.

Figure 6-3 Generating the RAM Test Pattern

• Example of test pattern for 2-port RAM (APF format)

```
$RATE   200000
$STROBE 185000
$RESOLUTION 0.001ns

$NODE
INPA    I  0
INPB    I  0
INPC    I  0
INPD    I  0
INPE    I  0
INPF    I  0
INPG    I  0
INPH    I  0
INPI    P  20000  520000
INPJ    I  0
TESTEN  I  0
  .
OUTA    0
OUTB    0
OUTC    0
OUTD    0
  .
  .
$ENDNODE

$PATTERN
          0   00010100001.XXXX..
          1   00010100P11.XXXX..
          2   00010101011.HLHL..
          3   10111110001.XXXX..
          4   10111110P11.XXXX..
          5   10111111011.HHHH..
          6   11101010001.XXXX..
          7   11101010P11.XXXX..
          8   11101011011.LHLH..
```

6.4 Function Cell Test Circuits

When function cells are used, then testing the operation of all circuits (including the user circuits) requires a vast number of test patterns and a great amount of time. It is because of this that it is necessary to design test circuits able to verify the operation of each independent functional cell and user circuit, as was done with the RAM blocks. When designing the test circuits, please keep the following cautions and considerations in mind. For more details, contact EPSON.

6.4.1 Test Circuit Structures

(1) Provide test circuitry which facilitates direct access to all pins of each functional cell via I/O pins. Add a test circuit (connected to a terminal) which isolates each functional cell from the surrounding circuits.
(2) Even when functional cell input pins are fixed to logic 0 or logic 1, design test circuitry which insures access to all functional cell pins.
(3) Even when functional cell output pins are not used, design test circuitry which insures access to all functional cell pins.
(4) Each functional cell pin must be connected to a unique I/O pin.
(5) Do not use sequential elements in the test circuitry for functional cells.
(6) Do not invert the input signal from the test input terminal and input it into the functional cell. Similarly, do not invert the functional cell output signal and output it to the test output terminal.
(7) There is no need to design a test circuit when the functional cell input pins and output pins are directly connected to the I/O pins.
(8) Do not use an input cell with pull-up or a bi-directional cell with pull-up as the test mode switch pin (although a bi-directional cell with pull-down may be used).

6.4.2 Test Patterns

The test patterns can be categorized into the following two types:

1) Test patterns to test only the user's circuit.
2) Test patterns to test all circuits.
3) Test patterns to test the functional cells only.

Test patterns that the customers generateare of type 1 and 2. Customers are not required to generate test patterns of type 3. EPSON maintains test patterns to be used for type 3. Please be advised that EPSON will not disclose information pertaining to the functional cell test patterns.

6.4.3 Test Circuit Data

Please provide the following information regarding functional test circuitry. This information is required for functional cell testing during simulation and IC device testing.

(1) Please clearly define the I/O pin to functional cell pin connectivity while in test mode.
(2) When the test circuits are structured in such a way that a single test terminal is able to test multiple functional cells, please clearly define the names of the functional cells which can be selected and the type of the test modes, and their relationships.
(3) Please clearly define pass numbers on the names of the functional cells on the drawings, and clearly define the test terminals and their association with functional cells, especially when identical functional cells are used more than once.
(4) Please clearly define the method of switching into test mode.

6.5 Test Circuit Which Simplifies AC and DC Testing

Test Circuit Structure

The S1L35000 Series requires the construction of test circuits so that DC testing and AC testing can be done efficiently.

If the customer experiences difficulties while implementing test circuitry, then the customer should contact EPSON.

Figure 6-4 shows specific examples of test circuits. This figure should be referenced when designing test circuits. Recommended test circuit control and monitor pin configurations are shown below.

(1) Test Circuit Control and Monitor Pins

Please add or select the following 4 types of test pins.

- Dedicated input pin for testing: 1 pin
- Test mode select input pin: 3 pins (can be functionally shared with input pins of application)
- Monitor output pin for AC testing: 1 pin (can be functionally shared with output pin of application)

Table 6-1 Table of Test Terminal Constraints

Test Pin Type	Number of Pins	Name of Pins (See Fig. 6.4)	Constraints, Notes, Etc.
Test Enable Pin	1 pin	TSTEN	Dedicated input pin Use XITST1. H: Test mode L: Normal mode
Test Mode Pins	3 terminals	INP0 INP1 INP2	May be shared with existing input pin. Do not share with an input pin associated with a critical path.
Monitor output pin for AC testing	1pin	OUT3	May be shared with existing output pin. Do not share with a bidirectional, 3-state terminal or with an N-channel open-drain cell.
All output and bi-directional pins	--	--	Uses pre-drivers with test mode select (When comparing usual pre-drives, three or four gates for a pin are added.)

(2) Measurements are performed to insure that all input and output pins adhere to DCcharacteristic specifications. When test circuitry is not implemented, it is necessary for the customer to generate test patterns by which the DC characteristics can be measured. The amount of work in generating the test patterns may increase dramatically when there are no test circuits.
The task of generating test patterns and measuring the DC chracteristics is simplifiedby using test circuits.

(3)AC Testing

AC testing is a pin-to-pin (i.e. input pin to output pin) delay measurement. If device testing is not performed at actual operating frequency, device performance is assured through delay measurements along specific paths.

Also, the AC test monitor output pin is used to evaluate the variance between lots in the manufacturing process by measuring a defined AC path (cell name: XACP1). (When test circuits are used, be sure to insert cell XACP1 when designing the AC path test circuit.)

(4) Adding the Test Mode Control Circuit

The following items (a through j) pertain to test circuit implementation. Please refer to the test circuit examples of Figure 6-4.

a. Select 4 test input pins and 1 output pin
   - Dedicated input pin for testing: 1 pin (test enable signal:two pins if it is possible.)
   - Test mode select input pin: 3 pins (can be functionally shared with input pins of application)
   - Monitor output pin for AC testing: 1 pin (can be functionally shared with output pin of application)

b. The dedicated input pin for test enable/disable (TSTEN) must use cell XITST1.

c. The dedicated or shared input pins for test mode selection (INP0, INP1 and INP2) can use any input buffer cell type. Avoid sharing these test inputs with critical path input pins of the application.

d. The dedicated or shared output pins for AC monitoring (OUT3) can use any uni-directional output buffer type (except 3-state type). Avoid sharing these test outputs with critical path output pins of the application.

e. All pre-drivers for output and bi-directional pin configurations must have test mode functionality.

f. Please utilize the test mode control circuit (TCIR).

g. The primary test enable/disable signal (output pin 'IN' of cell XITST1) should be connected to the 'TST' input pin of functional block TCIR. When this signal is enabled (set to logic "H"), the test mode control circuitry (block TCIR) becomes functional and facilitates AC and quiescent current testing.

h. Three dedicated shared input signals (output pins of uni-directional input buffer cells) should be connected to the 'IP0', 'IP1' and 'IP2' input pins of functional block TCIR.

A first dedicated/shared input signal (INP0 in Figure 6-4) should be connected to input pin 'IP0' of functional block TCIR. This signal will control the mode of all bi-directional I/O cells which utilize pre-drivers with test functionality. When 'IP0' is state 'H' and 'IP2' is state 'H' , all bi-directional I/O will be placed in input mode, and all 3-state outputs will be in high-impedance state. When 'IP0' is state 'L', all bi-directional and 3-state I/O will be in output mode.

A second dedicated/shared input signal (INP1 in Figure 6-4) should be connected to input pin 'IP1' of functional block TCIR. This signal controls output data while in test mode. The data which appears at pin 'IP1' will be passed to all output and bi-directional I/O cells when 'IP2' is state 'L' .

A third dedicated/shared input signal (INP2 in Figure 6-4) should be connected to input signal pin 'IP2' of functional block TCIR. This signal controls all output and bi-directional

signals excluding the AC monitor output pin during AC testing. When input signal 'IP2' is state 'H' and all outputs remain in stable state 'H' so as to minimize switching noise during AC testing.

i. The following describes the recommended connections for the output pins of the test circuit functional block TCIR.

The TCIR output pin 'ACO' is used for AC characterization testing. This output of TCIR must be connected to one and only one 'TD' input pin of a user selected pre-driver (OUT3), which is connected to a uni-directional output driver (not 3-state).

The TCIR output pin 'TS' is the test mode control signal. This output is used to put all pre-drivers connected to output and bi-directional I/O's into test mode. When 'TS' is state 'H', all pre-drivers are in test mode.

The TCIR output pin 'TE' is used for test mode bi-directional enable (or control). This output is connected to all 3-state and bi-directional pre-driver's 'TE' input pin. when 'TE' is state 'L', all 3-state (OUT2) and bi-directional drivers (BID1) are placed in output mode.

j. Fan-out violations which may occur on TCIR output pins 'TS', 'TD' and 'TE' can be ignored.

(5) Setting the Test Mode (Please refer to Figure 6-4)

• Output Characteristics (V_{OH}/V_{OL}) Measurement Mode

TSTEN	. . . High
INP0	. . . High
INP1	. . . High for V_{OH} test and Low for V_{OL} test
INP2	. . . This controls the bi-directional and 3-state pin mode
High	. . . Hi-Z (input) mode*
Low	. . . Output mode

* Can be used as 3-state and bi-directional off-state leakage current measurement mode.

•Dedicated AC Path Measurement Mode

TSTEN	. . . High
INP0	. . . Low
INP1	. . . Change from High to Low, then change from Low to High
OUT3	. . . Is used to monitor delay from INP1
INP2	. . . High

Generating the Test Pattern

It is necessary for the customer to design test patterns at the same time that the customer designs the test circuits so that the DC testing and the AC testing can be performed in an efficient manner.

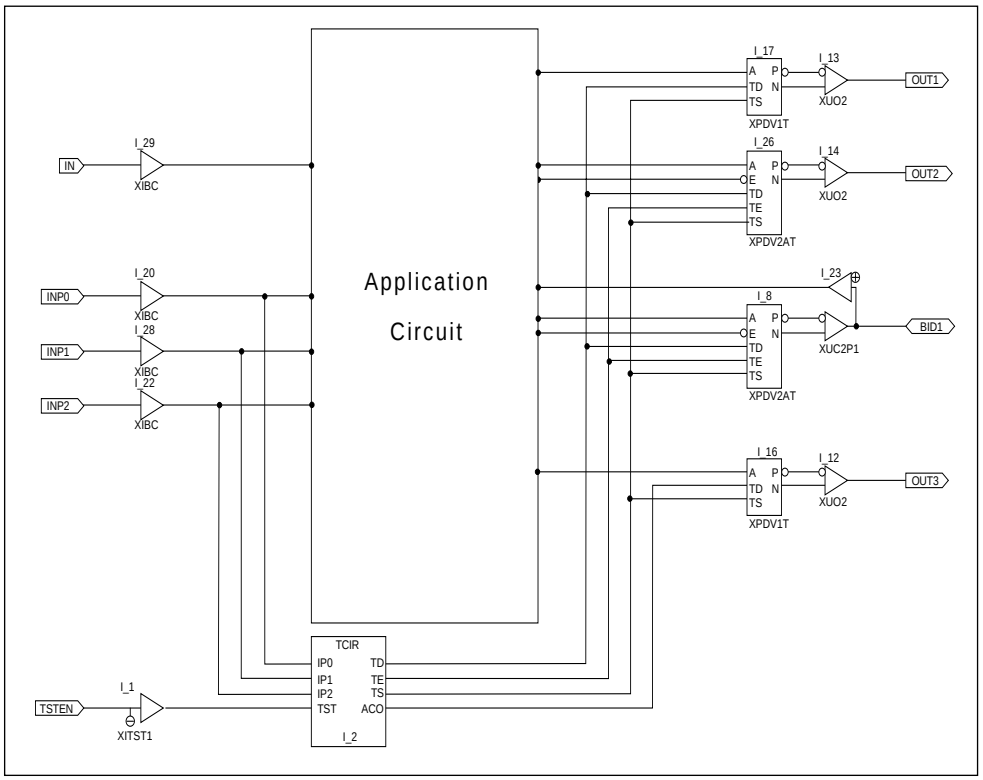
Figure 6-5 shows a specific example of the test pattern related to the test circuits in Figure 6-4. The following should be kept in mind when generating the test patterns:

a. Please generate a test pattern to exercise test circuitry separate from standard application functional test patterns.

b. Test circuit test patterns must specify all input, output and bi-directional I/O signals.

c. Please insure that the dedicated test enable pin (i.e. TESTEN in Figure 6-4) is present and set to state ‘L’ in the standard application functional test patterns.

d. When the input level (TSTEN) of test terminal is set to “1” all pull-up resistance are non-active (off).



<Test mode control circuit “TCIR”>

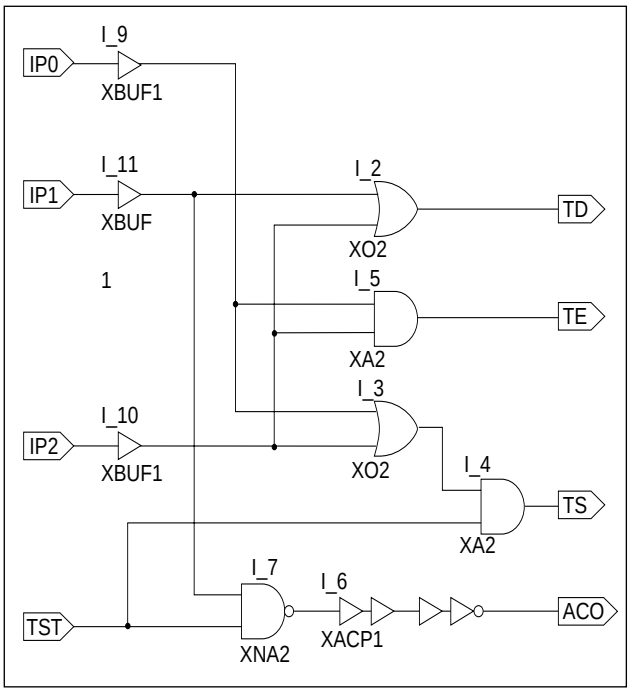


Figure 6-4 : Example of Test Cicuit

• Example of test pattern for AC & DC test (press format)

```
          0000000000
          0000000001
          1234567890
          TIIIIBBOOO
          SNNNNIIUUU
          TPPP DDTTT
          E012 11123
          N    X
               I


 1000000   IIIIII0000

          000000

      0   0.....XXXX
      1   10.0..XXXX ;pull-up/down off
      2   1001..HHHL ;AC path (L), other output all High
      3   1011..HHHH ;AC path (H), other output all High
      4   1001..HHHL ;AC path (L), other output all High
      5   1101.0ZHZL ;Off state except normal output (Low input)
      6   1111.1ZHZH ;Off state except normal output (High input)
      7   1100..LLLL ;Output all Low
      8   1110..HHHH ;Output all High


    note)

    "." is 1 or 0 input.
```

Figure 6-5 Example of the generation of a test pattern when there is a test option

- Example of test pattern for AC & DC test (APF format)

```
$DESIGN  testckt

$RATE   200000
$STROBE 185000
$RESOLUTION 0.001ns

$IOCONT
AA08.E  E0  BID1
$ENDIOCONT

$NODE
TESTEN  I  0
INP0    I  0
INP1    I  0
INP2    I  0
IN      I  0
BID1    BU 0
OUT1    0
OUT2    0
OUT3    0
$ENDNODE

$PATTERN
#             TIIIIBOOO
#             SNNNNIUUU
#             TPPP DTTT
#             E012 1123
#             N
#
#             IIIIIBOOO
#                  U
#

            0 0....XXXX
            1 10.0.XXXX  #pull-up/down off
            2 1001.HHHL  #AC path (L), other output all High
            3 1011.HHHH  #AC path (H), other output all High
            4 1001.HHHL  #AC path (L), other output all High
            5 1101.0HZL  #Off state except normal output (Low input)
            6 1111.1HZH  #Off state except normal output (High input)
            7 1100.LLLL  #Output all Low
            8 1110.HHHH  #Output all High

$ ENDPATTERN

#
# EOF

note)

"."is 1 or 0 input.
```

Figure 6-6 Example of the generation of a test pattern when there is a test option

Chapter 7 Propagation Delay and Timing

Propagation delay time is determined by the intrinsic cell delay and by the per-load delay, which is a function of the wire interconnect and fan-in capacitances.

Delay times vary depending upon power supply voltage, ambient temperature, and process conditions. They also vary depending on factors involved in the structure of the circuit, input waveform, input logic level, and the mirror effect.
Post Simulation uses more acculate environment.

7.1 Simple Delay Models

Simple propagation delay time t_{pd} can be calculated using the following formula:

$$t_{pd} = t_0 + K \times (\cdot\text{Load A} + \text{Load B})$$

where,	t_0:	Intrinsic cell delay [ps]
	K:	Load delay coefficient [ps/Lu]
	Load A:	The input load capacitance due to fan-in [Lu]
	Load B:	The interconnect load capacitance [Lu]

Note: The values for t_0 and K differ depending upon the operating voltage, the ambient temperature, and the process conditions. Use the values provided in the “Gate Array S1L35000 Series MSI Cell Library.” The unit “Lu” stands for loading unit, which is equivalent to one “XIN1” input fan-in.

Typ. values for t_0 and K (V_{DD} = nominal value, Ta = 25°C, and process = nominal value) are found in the “Gate Array S1L35000 Series MSI Cell Library.” Select Typ. values for T_0 and K according to the target power supply voltage.The Min. value for T_0 and K (where V_{DD} is the Max. value, Ta = Min. value and process = fast) and the Max. value for t_0 and K (where V_{DD} = Min. value, Ta = Max. value, and process = slow) are calculated by multiplying the Typ. value, described above, by the delay coefficient M. (These Min. and Max. values are required to verify ASIC operation over commercial and industrial variances in supply voltage, ambient temperature and process.)

The delay coefficient M can be calculated using the following formula:

$$M = M_V \times M_T \times M_P$$

where,	M_V:	Delay Multiplier due to voltage variation
	M_T:	Delay Multiplier due to temperature variation
	M_P:	Delay Multiplier due to process variation

Although values for M_V and M_T can be obtained by reading them off of the characteristic graphs in the “Gate Array S1L35000 Series MSI Cell Library,” please use the duration delay coefficient vaues M, given in Table 7-1. Also, please direct inquiries to the EPSON regarding ASIC operation outside of the limits shown in Table 7-1.

Note 1: The Typ. value for V_{DD} = 3.0 V is not listed in the "Gate Array S1L35000 Series MSI Cell Library." As is shown in Table 7-1, it is calculated by multiplying the Typ. value for V_{DD} = 3.3 V by 1.11.

Table 7-1 Delay Coefficient M (Used For All Cells Excluding Pre-Driver With Level Shifter)

Conditions	M Value			Usage
	$M_{Min.}$	$M_{Typ.}$	$M_{Max.}$	
Power supply voltage: 5.0 V ± 5%; Ta: 0 to 70 °C	0.59	1.00	1.62	Use after multiplying the Typ. values of t_0 and K for V_{DD} = 5.0 V
Power supply voltage: 5.0 V ± 10%; Ta: -40 to 85 °C	0.53	1.00	1.72	
Power supply voltage: 3.3 V ± 10%; Ta: 0 to 70 °C	0.51	1.00	1.82	Use after multiplying the Typ. values of t_0 and K for V_{DD} = 3.3 V
Power supply voltage: 3.3 V ± 10%; Ta: -40 to 85°C	0.47	1.00	1.87	
Power supply voltage: 3.0 V ± 10%; Ta: 0 to 70°C	0.56	1.11	2.05	
Power supply voltage: 3.0 V ± 10%; Ta: -40 to 85°C	0.51	1.11	2.10	

7.2 Load Due to Input Capacitance (Load A)

Cell propagation delay is dependent upon the sum of input pin capacitances (Load A) attached to the cell's output terminal (i.e. the sum of the fan-ins). The input capacitances (fan-ins) of each gate and the output terminal load constraints (fan-outs) are listed in the "Gate Array S1L35000 Series MSI Cell Library. Cell output terminal fan-out must not exceed the listed Max. value. A Load A calculation example is shown in Figure 7-1 and Table 7-2.

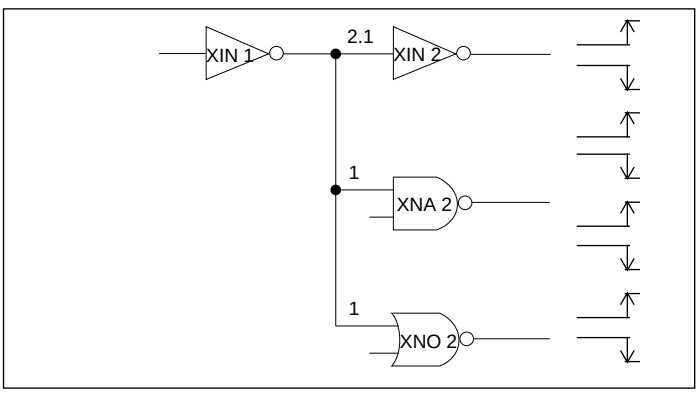


Figure 7-1 Example Calculating Load A

Table 7-2 Data Used in the Example of Calculating Load A

Cell	Input		Output	
	Pin	Fan-in	Pin	Fan-out
XIN1	A	1.0	X	23.4
XIN2	A	2.1	X	49.3
XNA2	A1 A2	1.0 1.0	X	22.7
XNO2	A1 A2	1.0 1.0	X	12.3

The fan-in values for XIN2, XNA2, and XNO2 can be obtained from Table 7-2. Their sum is the Load A value, as seen by the XIN1 output terminal in load units (Lu).

$$\Sigma\text{Load A (XIN1)} = (\text{Fan-in of XIN2}) + (\text{Fan-in of XNA2}) + (\text{Fan-in of XNO2})$$
$$= 2.1\text{Lu} + 1\text{Lu} + 1\text{Lu} = 4.1\text{Lu}$$

7.3 Load Due to Interconnect Capacitance (Load B)

The load resulting from the capacitance of the interconnect between cells (Load B) cannot be accurately calculated until the ASIC layout has been performed. However, Load B is correlated with the number of branches (number of nodes) connected to the wire, so it is possible to statistically estimate the Load B value. The estimated interconnect capacitance for each master is listed in the “Gate Array S1L35000 Series MSI Library.”

7.4 Propagation Delay Calculations

Below we present a sample propagation delay time calculation using the circuit shown in Figure 7-2 (assume an operating voltage of 5.0 V) and the data of Table 7-3.

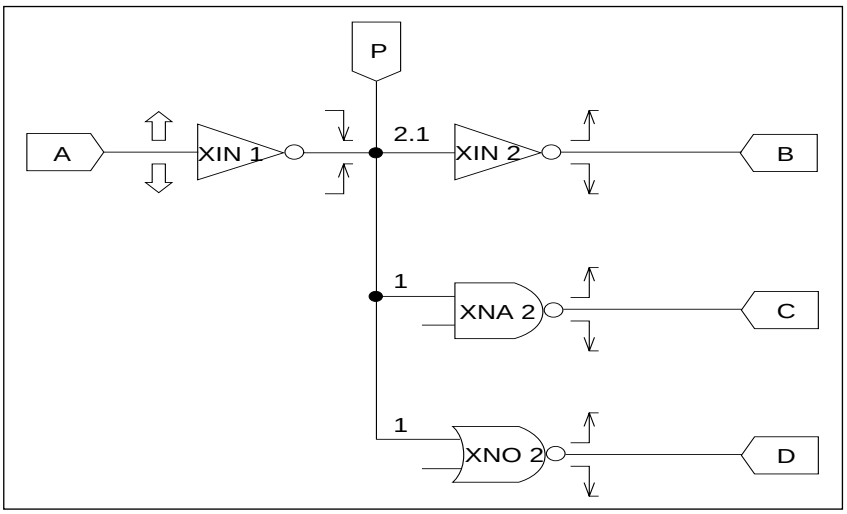


Figure 7-2 Circuit for the Sample Calculation of the Propagation Delay Time

Table 7-3 Table of Characteristics (Power Supply Voltage = 5.0 V)

Cell	Input		Output		t_{pd} (Typ.)				
	Pin	Fan-in	Pin	Fan-out	From	To	Edge	T_0 (ps)	K (ps/Lu)
XIN1	A	1.0	X	23.4	A	X	↑	76	40.8
							↓	70	20.8
XIN2	A	2.1	X	49.3	A	X	↑	56	19.4
							↓	64	10.4
XNA2	A1	1.0	X	22.7	A	X	↑	115	40.6
							↓	97	30.8
XNO 2	A1	1.0	X	12.3	A	X	↑	129	72.2
							↓	97	20.7

For this example, assume that Load B of NODE P = 2 (Lu), and assume that Load B of Nodes B, C and D = 0 (Lu). Also, note that propagation delay varies depending on the output terminal state transition (rising or falling edge). Below please find examples calculating the propagation delays for paths A to P, A to B, A to C and A to D for both rising and falling cases under Typ. operating conditions at 5V.

1. PATH A toP: $t_{pd} = t_{pd}$ (XIN1)

t_{pd} (A_{rising} to $P_{falling}$) = t_0 + K x (Load A + Load B)
= 70 + 20.8 x (4.1 + 2)
= 196.9 (ps)

t_{pd} (A_{rising} to $P_{falling}$)= t_0 + K x (Load A + Load B)
= 76 + 40.8 x (4.1 + 2)
= 324.9 (ps)

2. PATH A to B: $t_{pd}= t_{pd}$ (XIN1) + t_{pd} (XIN2)

t_{pd} (A_{rising} to B_{rising})= t_{pd} (A_{rising} to $P_{falling}$) + t_{pd} ($P_{falling}$ to B_{rising})
= 196.9 + t_0
= 196.9 + 56
= 252.9 (ps)

t_{pd} ($A_{falling}$ to $B_{falling}$)= t_{pd} ($A_{falling}$ to P_{rising}) + t_{pd} (P_{rising} to $B_{falling}$)
= 324.9 + t_0
= 324.9 + 68
= 388.9 (ps)

3. PATH A to C: $t_{pd} = t_{pd}$ (XIN1) + t_{pd} (XNA2)

t_{pd} (A_{rising} to C_{rising})= t_{pd} (A_{rising} to $P_{falling}$) + t_{pd} ($P_{falling}$ to C_{rising})
= 196.9 + t_0
= 196.9 + 115
= 311.9 (ps)

t_{pd} ($A_{falling}$ to $C_{falling}$)= t_{pd} ($A_{falling}$ to P_{rising}) + t_{pd} (P_{rising} to $C_{falling}$)
= 324.9 + t_0
= 324.9 + 97
= 421.9 (ps)

4. PATH A to D: $t_{pd}= t_{pd}$ (XIN1) + t_{pd} (XNO2)

t_{pd} (A_{rising} to D_{rising})= t_{pd} (A_{rising} to $P_{falling}$) + t_{pd} ($P_{falling}$ to D_{rising})
= 196.9 + t_0
= 196.9 + 129
= 325.9 (ps)

t_{pd} ($A_{falling}$ to $D_{falling}$)= t_{pd} ($A_{falling}$ to P_{rising}) + t_{pd} (P_{rising} to $D_{falling}$)
= 324.9 + t_0
= 324.9 + 97
= 421.9 (ps)

7.5 Calculating Output Buffer Delay

As was discussed in Chapter 4, all of the output buffers are isolated from the pre-drivers in the S1L35000 Series. Because of this, the output buffer delay times are the sum of the output cell delay times and the pre-driver delay times. Assuming that the load capacitance connected to the output buffer is C_L, the delay time t_{pd} is calculated as follows:

$$t_{pd} = t_0 \text{ (Output cell)} + K \text{ (Output cell)} \times C_L/10 + t_0 \text{ (pre-driver)} + K \text{ (pre-driver)} \times \text{Output Cell Input Capacitance}$$

t_0 (Output cell):	The intrinsic delay of the output cell	[ps]
t_0 (Pre-driver):	The intrinsic delay of the pre-driver	[ps]
K (Output cell):	The output cell load delay coefficient	[ps/10 pF]
K (Pre-driver):	The pre-driver load delay coefficient	[ps/Lu]
C_L:	The attached load capacitance	[pF]

Please reference the “Gate Array S1L35000 Series MSI Cell Library” regarding the intrinsic delays and load delay coefficients of the output cells and pre-drivers.

7.6 Sequential Cell Setup/Hold Time

A critical factor to analyze when designing an ASIC is sequential cell usage and operation. Data which is to be stored by sequential logic must arrive before the gating or clock signal to insure sufficient data setup and proper operation. That same data must remain unchanged or held subsequent to the gating or clock signal. These timing rules and others (see below) must be taken into consideration when designing sequential logic. Sequential cell specific timing values can be found in the “Gate Array S1L35000 Series MSI Cell Library.”

(1) Min. Pulse Width: TPWC, TPWS or TPWR

The Min. pulse width refers to the Min. value of the time between a leading edge and a trailing edge of an input pulse waveform, as seen at the clock, set, preset or reset terminal of a sequential cell. Circuit malfunction may occur when a narrow pulse is applied which volates this constraint.

The Min. pulse widths may be of the following three types:

- t_{PWC}: Clock signal Min. pulse width violation.
- t_{PWS}: Set signal Min. pulse width violation.
- t_{PWR}: Reset signal Min. pulse width violation.

(2) Setup Time: TEROR/SETUP
"Setup time" refers to the required time interval in which the data state must be set before the active edge transition of the gate or clock signal in order to correctly store the data in a sequential cell or an MSI function which is made up of sequential cells.

(3) Hold Time: TEROR/HOLD
"Hold time" refers to the required time interval in which the data state must be held after the active edge of the gate or clock signal in order to correctly store the data in a sequential cell or an MSI function which is made up of sequential cells.

(4) Release Time (Setup): CSERO, CRERO/SETUP
"Release time" (setup) refers to the required time interval between a set/reset signal transition to inactive and the active edge of the gate or clock signal in a sequential cell of an MSI function which is made up of sequential cells.

(5) Release Time (Hold): CSERO, CRERO/HOLD
"Release time" (Hold) refers to the required time interval between a set/reset signal transition to active and the active edge of the gate or clock signal in a sequential cell or an MSI function which is made up of sequential cells.

(6) Set/Reset (Setup): RSERO/SETUP
"Set/Reset" (Setup) refers to the required time interval after a set input state is released until it is possible to have a rising edge on a reset input in a sequential cell or MSI function which is made up of sequential cells.

(7) Set/Reset (Hold): RSERO/HOLD
The "Set/Reset" (Hold) refers to the required time interval after a reset input state is released until it is possible to have a rising edge on a set input in a sequential cell or MSI function which is made up of sequential cells.Figure 7-3 XDFSR (Example)

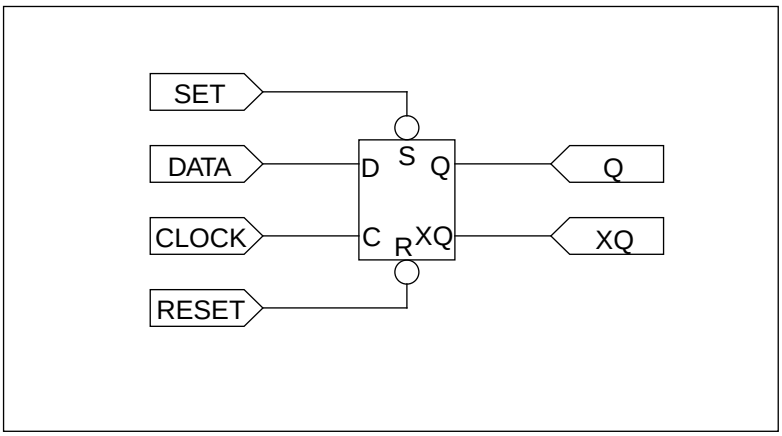


Figure 7-3 XDFSR (Example)

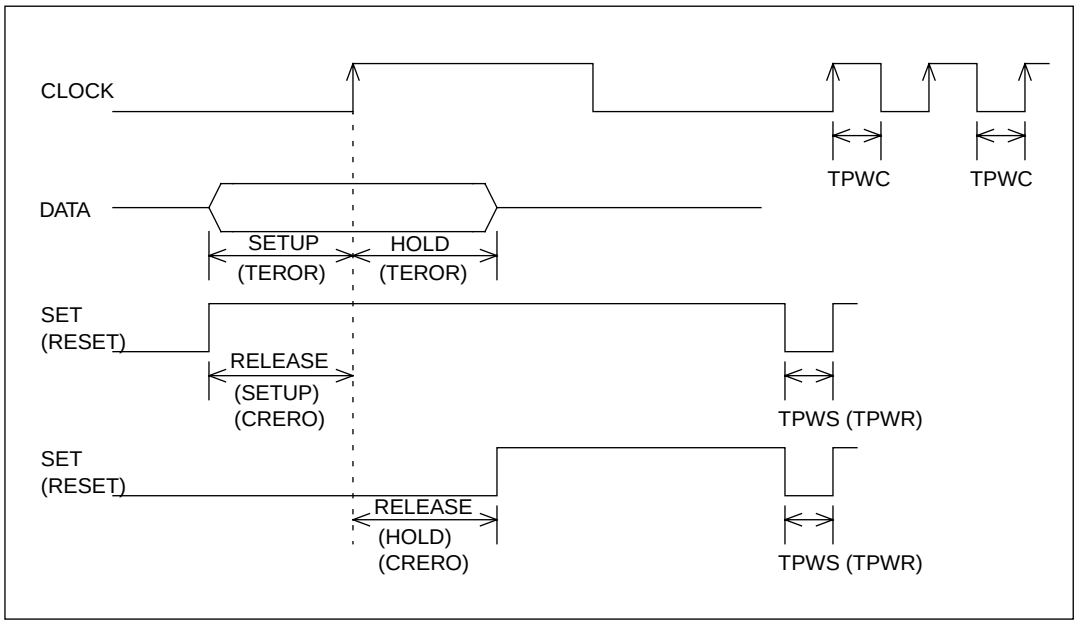


Figure 7-4 Timing Wave Form (Explanatory Diagram for Numbers 1-5)

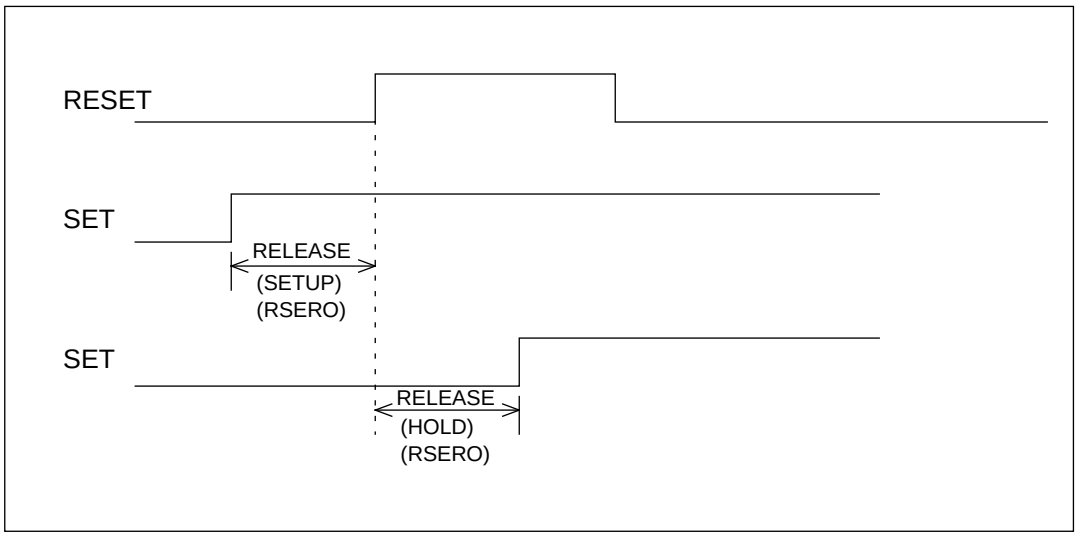


Figure 7-5 Timing Wave Form (Explanatory Diagram for Numbers 6-7)

Table 7-4 DFSR Timing Characteristics (Example)

Pin	Setup time1 t_{su} (ps)	Hold time,t_h (ps)	Pulsewidth, t_w (ps)	Setup time, t_{su} (ps)	Hold time, t_h (ps)	Pulsewidth, t_w (ps)
	Typ.(V_{DD}=5.0V)	Typ.(V_{DD}=5.0V)	Typ.(V_{DD}=5.0V)	Typ.(V_{DD}=3.3V)	Typ.(V_{DD}=3.3V)	Typ.(V_{DD}=3.3V)
C(P) to D	952	360	-	1388	516	-
C(P) to S	609	710	-	871	1028	-
C(P) to R	740	681	-	1058	989	-
R(P) to S(P)	877	668	-	1222	949	-
C(P)	-	-	1249	-	-	1813
C(N)	-	-	1286	-	-	1823
S(N)	-	-	1356	-	-	1903
R(N)	-	-	1224	-	-	1736

Note : P = transition from 0 to 1 level or Positive pulse
N = transition from 1 to 0 level or Negative pulse

7.7 Chip Internal Skew

Because of transistor characteristic variance within an ASIC, the tpd of similar gates within an ASIC may vary. Skew is a term used to describe this variance. Skew must be taken into account so as to provide margin in timing critical portions of logic to insure proper operation.

Table 7-5 Skew Within the Chip

Cell	Layout Area	Skew
Internal cells	All regions	5%
I/O cell	All regions	5%

Chapter 8 Test Pattern Generation

Test patterns must be generated once the logical design has been completed. Test patterns are used to simulate and verify circuit functionality. Test patterns are also used for product inspection prior to shipment. Please keep the following guidelines in mind when generating test patterns, thereby improving manufacturability and insuring product quality.

8.1 Testability Considerations

Because the test pattern is used in the final inspection of the product before it is shipped, it must be able to test all circuits within the LSI. If there are areas within the circuits of the LSI which are untested, it will not be possible to test those areas before the product is shipped, and thus there will be the danger of shipping defective product.

It is difficult to test all of the circuits within the LSI, so it is important to consider testability during the process of designing the circuit.

8.2 Waveform Types

Although the test pattern is normally a series of “0” and “1” when a simulation is performed or the LSI tests are run, the input wave forms can be delayed, and the wave forms can be changed. The wave forms which can be used when the test pattern is generated include the following two types:

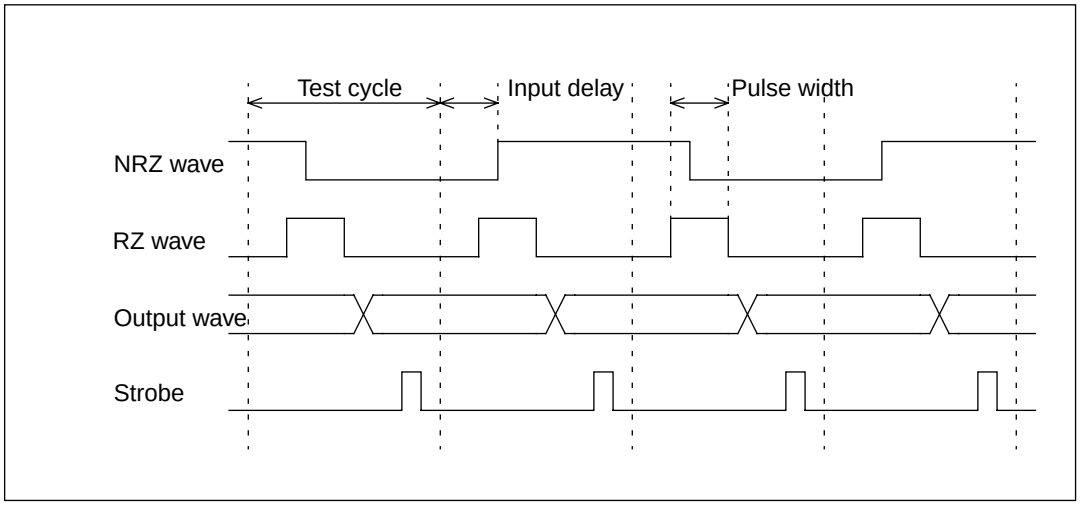


Figure 8-1 Constraints on Timing Settings

NRZ (Non Return to Zero)

A signal whose state changes no more than once per test pattern cycle is defined as being an NRZ type waveform. This waveform type can be delayed by a constant offset from the beginning of the test pattern cycle boundary.

RZ (Return to Zero)

A signal whose state may change twice per test pattern cycle is defined as being an RZ type waveform. This waveform type can be delayed by a constant offset from the beginning of the test pattern cycle boundary. This waveform type is useful for defining clock signals using positive or negative pulse definitions.

8.3 Constraints on the Types of Test Patterns

During design verification, test patterns can be set to accurately reflect actual operating frequency, yet in order to be used in final device inspection, the test patterns must adhere to constraints of the LSI tester. These constraints are explained below and should be kept in mind during test pattern development.

8.3.1 Test Period

The test period must be 100 nsec or longer in duration and is defined in 1 nsec intervals. (Recommended test period: 200 nsec.)

8.3.2 Input Delay

(a) Range of Input Delays
0 nsec ≤ input delay value < strobe point.
The input delay is defined in 1 nsec intervals within the range above. See Section 8.3.5 below regarding constraints on the strobe point.

(b) Input delay values must have a Min. of 5 nsec resolution from one another.

(c) Types of input delays
No more than 8 types of input delays can be used in a single test pattern. A 0 nS delay is also counted as 1 type. When there are identical delays on an RZ wave form as on an NRZ wave form, these are counted as different delay types. When 2 RZ wave forms have identical delay values or 2 NRZ wave forms have identical delay values, these are counted as identical delay types.

(d) Constrains on the LDI tester
The test patterns are constrained by the LSI tester. Refer to the qchapter 6.2 about the constrains.

8.3.3 Pulse Width

Pulse widths for RZ wave forms must be 15 nsec or more.

8.3.4 Input Waveform Format

The input wave form must assume a value of “0”, “1”, “P”, or “N”. “P” and “N” indicate RZ positive pulse and negative pulse type. Use state “0” to disable positive pulse RZ waveform, and state “1” to disable negative pulse RZ waveform (i.e. RZ type state combinations of (0,P) and (1,N) are valid, while state combinations of (0,N) and (1,P) are invalid).
Do not use a bi-directional pin as the clock.

8.3.5 Strobe

The constraints on the strobe are as follows.

(a) Only a single strobe may be used within a single test pattern event.
(b) The smallest value for a strobe should be at least 30 nsec after the completion of all output signal changes, where the change results from input signals state change applied during that event.
(c) The Max. value for the strobe should be the test period minus 15 nsec.
(d) The strobe is defined in 1nsec intervals.

8.4 Notes Regarding DC Testing

The test pattern is used for functional testing and DC testing of the LSI. Please generate the test patterns so that the following DC tests can be performed.

DC tests are performed to verify the DC parameters of the LSI. Because the DC tests perform measurements on the trailing edge of the measurement events, those terminals which are measured must not have state changes after the strobe during the measurement events.

The DC parameters measured are as described below:

(a) Output Driver Test (V_{OH}, V_{OL})
The output buffer current driving capabilities are tested. The terminals which are to be tested are caused to enter the output level through the operation of the device, the specified current load is applied, and the level of the voltage drop is measured.

In order to perform the output driver tests, it is necessary for the test pattern to cause all of the terminals to enter all of the states which are obtained when the device is operating. Also, the states must be such that they do not change even if the measurement event extends the test period indefinitely.

(b) Quiescent Current Test (I_{DDS})
The quiescent current is the leakage current which flows to the LSI power supply when the input is in an fixed state. While generally this current is extremely small, this measurement must be done in a state where there are no other currents flowing aside from the leakage current. To do this, all of the following conditions must be fulfilled, and there must be two or more places wherein there are events which can measure the quiescent current.

(1) The input terminals are all in a fixed state.
(2) The bi-directional terminals are given “H” level or “L” level inputs or are in an output state.
(3) There are no oscillators or operating functions within the circuit.
(4) None of the internal 3-state buffers (internal bus) are in a floating or a contention state.
(5) The RAM, the ROM, and the megacells are not in states wherein current is flowing.
(6) An “H” level input is applied to input terminals which have pull-up resistors.
(7) Bi-directional terminals with pull-up resistors attached are either given “H” level inputs or are producing “H” level outputs.
(8) Bi-directional terminals with pull-down resistors are either in an input state or are producing “L” level outputs.

(c) The Input Current Test

The input current test measures the inputs to the input buffer. The test items include measurements of input leakage current and of pull-up/pull-down currents. The tests for these measurement items are performed by applying a V_{DD} level or V_{SS} level voltage to the terminal being measured, and measuring the current which flows. In other words, the test is performed by applying either an “H” level or a “L” level voltage to the terminal being measured. For example, when a V_{DD} (“H” level) signal is applied during the test to a terminal being measured and which is in a state having an “L” level, then there is the potential for this to cause the state to change from “L” to “H” in the terminal being measured, and the potential that this will cause the LSI to function incorrectly.

In order to measure the input current tests, a test where a V_{DD} level is applied at an event where there is an “H” input to the terminal being measured in the test pattern, and a test is performed where a V_{SS} level is applied in the event where a “L” is applied. Because of this, it is not possible to perform these tests when the terminals being measured are not in these states in the test pattern.

The input current tests are further broken down into the following classifications.

(1) Input Leakage Current Test (I_{LH}. I_{LL})
Measurements are performed regarding the input current of the input buffers which have no pull-up/pull-down resistors.

The current which flows when an “H” level voltage is applied to the input buffer is called I_{LH}, and its Max. current value is guaranteed. In order to perform this test there must be an event in the test pattern which causes the input terminal to be measured to have an “H” level input. Bi-directional terminals must have “H” level inputs in the input state.

The current which flows when a “L” level voltage is applied to the input buffer is called I_{LL}, and its Max. value is guaranteed. In order to perform this test there must be an event in the test pattern which causes the input terminal to be measured to have a “L” level input. Bi-directional terminals must have “L” level inputs in the input state.

(2) Pull-up Current Tests (I_{PU})

This test measures the current which flows when an “L” level voltage is applied to an input buffer having a pull-up resistance. In order to perform this test there must be an event in the test pattern which causes the input terminal to be measured to have an “L” level input. Bi-directional terminals must have “L” level inputs in the input state.

(3) Pull-down Current Tests (I_{PD})

This test measures the current which flows when an “H” level voltage is applied to an input buffer having a pull-down resistance. In order to perform this test there must be an event in the test pattern which causes the input terminal to be measured to have an “H” level input. Bi-directional terminals must have “H” level inputs in the input state.

(4) Off State Leakage Current (I_{OZH}, I_{OZL})

This measures the leakage current which flows when the output is a high-impedance state in output buffers which have open drains or which are 3-state output buffers. The actual measurement is the measurement of the currents when a V_{DD} level voltage is applied, and when a V_{SS} level voltage is applied to the terminal being measured when the terminal is in a high-impedance state. Because of this, the terminal being measured must enter into a high impedance state in the test pattern.

8.5 Notes Regarding the Use of Oscillation Circuits

An example of an oscillation circuit (oscillator, interval oscillator) is shown below.

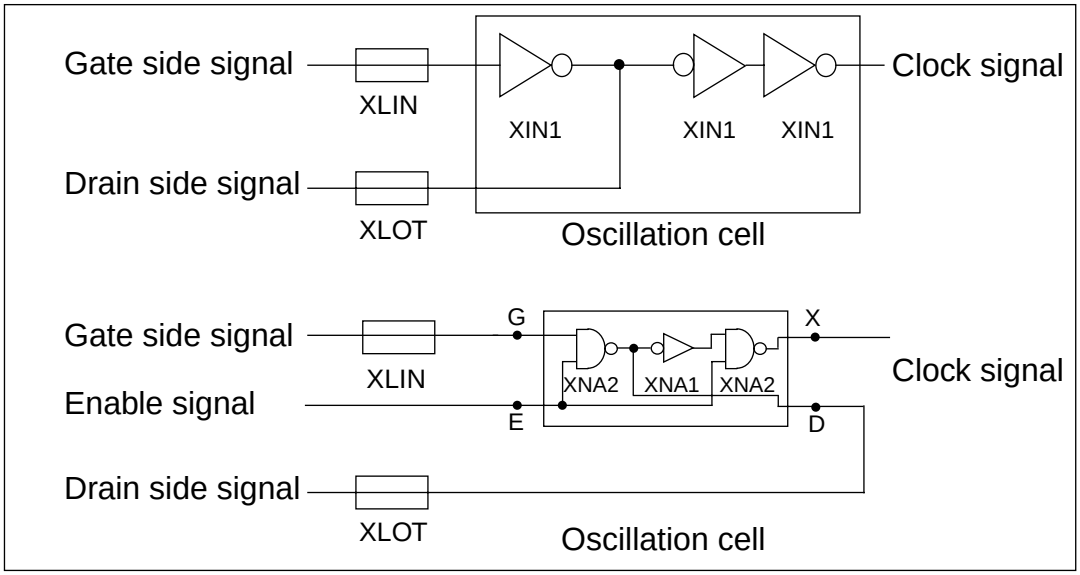


Figure 8-2 Example of Oscillator Circuits

Generally when oscillator circuits are used, the driving power of the oscillator inverter is small and the output wave form of the oscillator circuit is influenced by the load of the measurement environment. Thus the oscillator circuit is unable to transmit precise wave forms to the next-stage gates.

Because of this, in order to reproduce the conditions of the simulation in the tests, a procedure known as “reverse drive” (i.e. a procedure wherein a signal having the same wave form as the output from the drain is input to the drain terminal) is used.

When the oscillator inverter is structured as an inverter, it is possible to generate a reverse drive signal if the signal input from the drain is simply a reverse-phase input of the signal applied to the gate; however, in the case of NAND gate structures (known as interval oscillators or gated-OSC), then decisions cannot be made simply based on the gate signal alone, but rather the reverse drive wave form must be determined by looking at the expected values of the drain terminal.

In this method, if the input wave form is the NRZ wave form and the strobe is at the end of the test period, then the input wave form is put to the drain terminal expected value directly and a reverse drive wave form can be generated. However, in the case of the RZ wave form, then the expected value of the drain terminal is fixed to either an “H” or an “L” whether or oscillator is in a oscillating state or an oscillation stop state, so it is not possible to determine a reverse drive wave form by examining the expected state of the drain terminal.

Because of this, please keep the following cautions and notes in mind when a circuit having a interval oscillator is used:

(1) An RZ wave form cannot be used as the input signal.
(2) Do not cause transitions in the clock signal by transitions in the enable signal.

8.6 Regarding AC Testing

AC testing measures the time it takes for a signal to propagate to the output terminal when there has been a transition at the input terminal during a single event. The AC testing can be performed on a measurement path selected by the customer.

8.6.1 Constraints Regarding Measurement Events

Because this test is done using a testing method known as the “normal binary search method,” the terminal being measured (i.e. the output terminal wherein there is a transition) must have only a single transition point within a measurement event. (Measurements cannot be performed on terminals having an RZ wave form output, nor can they be performed in situations where a hazard is output during the measurement event.) Also, the state transitions of the signal being measure must be either “H” to “L” or “L” to “H”. (Transitions involving a high-impedance state cannot be measured.)

Other cautions and notes include the necessity for selecting events so that there are no signal contentions between the bi-directional terminals and the LSI tester, and that there are no situations where many output terminals have simultaneous transitions at the measurement event. This is because the LSI power source is overwhelmed when there are simultaneous transitions or signal contentions, affecting the output wave form of the terminals being measured and making it impossible to get an accurate measurement.

8.6.2 Constraints on the Measurement Locations for AC Testing

Please use only 4 or less measurement locations in the AC testing.

8.6.3 Constraints Regarding the Path Delay Which is Tested

The longer the delay in the AC measurement, the more accurate the measurement. The measurement path delay time should be recorded using Max. delay simulation conditions targeting a path delay value of 30 nsec or more, and less than the strobe point.

8.6.4 Other Constraints

(1) Do not designate a path from the oscillator circuit.
(2) Designate a path which does not pass through a circuit having an internal 3-state unit (i.e. the internal bus).
(3) Do not designate a path passing through other bi-directional cells between the input cell and the output cell of the measurement path.
(4) When there are two or more voltage ranges used, reconcile these to a single AC test measurement voltages.

8.7 Test Pattern Constraints for Bi-directional Terminals

By the constraints of testing, the bi-directional terminals cannot switch between input mode and output mode more than once within a single event. Because of this, the test pattern generated should not use an RZ wave form for controlling the bi-directional cell input/output mode switching.

Also, an RZ wave form cannot be used as an input to the bi-directional terminal.

Chapter 9 Estimating the Power Consumption

CMOS LSIs consume very little current when they are not operating. However, when they are operating, the power they consume depends on the operating frequency. When the power consumed is large, then the temperature of the LSI chip increases, and the quality of the LSI can be negatively affected if the temperature of the chip gets too high.

Because of this, it is necessary to calculate the power consumption and to check whether or not the power consumption is within allowable tolerances.

9.1 Calculating the Power Consumption

The power consumption of a CMOS circuit is generally dependent on the operating frequency, the capacitance, and the power supply voltage. (This excludes those special situations where there is a normal current through RAM/ROM, etc.) Here the CMOS gate array power consumption can be calculated easily if the operating frequencies and load captaincies of the various cells used within the circuit are known. However, because it is difficult to calculate the load captaincies for each internal cell, use the rough calculations described below.

After the power consumption for the input cells, the output cells and the internal cells are calculated, and these values are summed to produce the total power consumption.

(1) The Input Cell Power Consumption (P_i)

The input cell power consumption is the sum of the products of the signal frequencies (MHz) input into each cell, and the input buffer power coefficient K_{pi} (µW/MHz) for each cell.

.

$$P_i = \sum_{i=1}^{K} (K_{pi} \times f_i) \quad (W)$$

K_{pi}: Input Buffer Power Coefficient (Reference Table 9-1 below)
f_i: The operating frequency of the ith input cell (MHz)

Table 9-1 K_{pi} of input cells in the S1L35000 Series.

V_{DD} (Typ.)	K_{pi}
5.0 V	25µ W/MHz
3.3 V	9.7µ W/MHz
3.0 V	7.7µ W/MHz

(2) Output Cell Power Consumption (Po)

The output cell power consumption differs depending on whether the load is a direct

current load (such as resistive loads, TTL device connections, etc.) or whether the loads are alternating current loads (such as capacitance loads, CMOS device connections, etc.).

In the case of alternating current loads, the output cell power consumption is calculated from the load capacitance C_L as follows:

• Alternating current power consumption

$P_{AC} = f \times C_L \times (V_{DD})^2$ (W)

f: Output cell operating frequency (Hz)
C_L: Load capacitance (F)
V_{DD}: Power supply voltage (V)

In the case of the direct current load, the power consumed in the direct current load is added to the power consumed in the alternating current load.

• Direct current power consumption

$P_{DC} = P_{DCH} + P_{DCL}$

Where,

$P_{DCH} = |I_{OH}| \times (V_{DD} - V_{OH})$ (W)

$P_{DCL} = I_{OL} \times V_{OL}$ (W)

The ratio of P_{DCH} and P_{DCL} is determined by the output signal duty cycle.

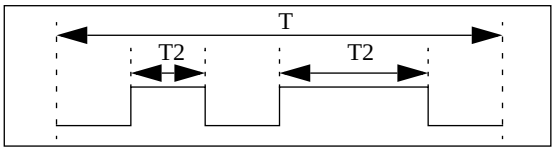


Figure 9-1 Example of the Duty Cycle

Duty H = $(T_1 + T_2) / T$
Duty L = $(T - T_1 - T_2) / T$

Because of this,

$P_{DC} = P_{DCH} + P_{DC}$

$$= \sum_{i=1}^{K} \{(V_{DD}-V_{OHi}) \times I_{OHi} \times \text{Duty H}\} + \sum_{i=1}^{K} \{V_{OLi} \times I_{OLi} \times \text{Duty L}\}$$

Consequently, the power consumption P_0 of the output cell is calculated by:

$$Po = \Sigma (P_{AC} + P_{DC})$$
$$= \sum_{i=1}^{K} \{fi \times C_{Li} \times (V_{DD})^2\} + \sum_{i=1}^{K} \{(V_{DD} - V_{OHi}) \times I_{OHi} \times \text{Duty H}\}$$
$$+ \sum_{i=1}^{K} \{V_{OLi} \times I_{OLi} \times \text{Duty L}\}$$

(3) Internal Cell Power Consumption (P_{int})

The internal cell power consumption depends on the type of device used, the cell use efficiency, the operating frequency, and the ratio of cells operating at the operating frequency. It is calculated as follows:

$$P_{int} = \sum_{i=1}^{K} \{ (Nb \times U) \times fi \times S_{pi} \times (k_{pint}) \} \ (W)$$

Nb: Total number of BCs in the device type used.
U: Cell use ratio (Use 50% to 60%)
fi: Operating frequency of the ith group (MHz)
S_{pi}: Percentage of cells operating at frequency fi.
(Use 20% to 30%, though it depends on system.)
k_{pint}: Internal cell power coefficient (Please reference Table 9-2 below.)

Table 9-2 Kpint of Internal Cells in the S1L35000 Series

V_{DD} (Typ.)	K_{pi}
5.0 V	2.4µ W/MHz
3.3 V	0.91µ W/MHz
3.0 V	0.77µ W/MHz

Because of this, the total power consumption P_{total} is calculated as follows:

$$P_{total} = P_i + P_O + P_{int}$$

9.2 Constraints on Power Consumption

The LSI chip heats up according to the power consumption within the LSI. The temperature of the LSI chip when it is mounted in a package can be calculated from the ambient temperature Ta, the thermal resistance(θ_{j-a}) of the of the package, and the power consumption P_D.

The chip temperature (T_j) = Ta + (P_D x θ_{j-a}) (^oC)

In normal use, the chip temperature (T_j) should be less than about 85^{o}C.

Please reference Table 9-3 for the thermal resistances of each of the various packages. Because the thermal resistances listed in Table 9-3 are thermal resistances in a situation where there is no air circulation, these values will change substantially depending on the mounting of the packages on the circuit board and depending on whether or not there is forced air cooling.

Table 9-3 Thermal Resistances of Various Packages (Without Air Circulation)

ALLOY42

PKG	PIN	0 m/sec	1 m/sec	2 m/sec	3 m/sec
		θj-a	θj-a	θj-a	θj-a
QFP5	100	110(°C/W)	75	60	55
QFP5	128	110	75	60	55
QFP8	128	65	—	—	—
QFP8	208	45	—	—	—
QFP12	48	230	—	—	—
QFP13	64	170	—	—	—
QFP14	80	110	—	—	—
QFP15	100	115	50	45	35
QFP20	144	85	70	50	40
TQFP14	80	100	—	—	—
TQFP14	100	100	—	—	—
TQFP15	100	110	—	—	—

CFLGA (Board installation under the windless condition)

Package type	Customer's board size	Chip Size		
		3.82 mm × 3.82 mm	5.73 mm × 5.73 mm	9.55 mm × 9.55 mm
CFLGA424	75mm	44.0(°C/W)	32.9	24.6
	50mm	46.9	36.4	27.8
	30mm	61.1	50.1	42.1
CFLGA307	75mm	44.0	33.1	24.9
	50mm	47.1	37.4	28.5
	30mm	61.7	51.5	43.1
CFLGA239	75mm	44.0	33.1	25.1
	50mm	47.3	38.3	29.2
	30mm	62.2	52.9	43.9
CFLGA152	75mm	44.8	34.4	—
	50mm	48.8	39.7	—
	30mm	63.3	53.9	—
CFLGA104	75mm	45.5	35.6	—
	50mm	50.3	41.1	—
	30mm	64.3	54.9	—

Cu-L/F

PKG	PIN	0 m/sec	1 m/sec	2 m/sec	3 m/sec
		θj-a	θj-a	θj-a	θj-a
QFP5	80	85(°C/W)	55	45	40
QFP5	100	80	55	35	30
QFP5	128	80	55	35	30
QFP8	160	45	32	25	23
QFP8	256	50	—	—	—
QFP10	304	35	20	16	—
QFP12	48	175	120	90	80
QFP13	64	130	80	55	50
QFP14	80	110	—	—	—
QFP15	100	90	—	—	—
QFP20	184	65	—	—	—
QFP21	176	55	—	—	—
QFP21	216	55	—	—	—
QFP22	208	45	35	25	23
QFP22	256	45	35	25	23
QFP23	184	40	—	—	—
QFP23	240	40	—	—	—
TQFP12	48	165	—	—	—
TQFP13	64	140	—	—	—
TQFP15	128	105	—	—	—
TQFP24	144	80	—	—	—
HQFP5	128	60	—	—	—
HQFP8	160	32	19	12	10
H2QFP8	208	34	—	—	—
H2QFP23	240	30	—	—	—
H3QFP15	128	85	—	—	—

PBGA

PKG	PIN	0 m/sec	1 m/sec	2 m/sec	3 m/sec
		θj-a	θj-a	θj-a	θj-a
PBGA	225	72(°C/W)	46	37	—
PBGA	256	53	33	25	—
PBGA	388	45	—	—	—

Chapter 10 Pin Layout Considerations

10.1 Estimating the Number of Power Supply Terminals

It is necessary to estimate the number of power supply terminals required based on the power consumed by the LSI and on the number of output buffers. The output buffers use a large current when switching.

The number of power supply terminals required by the LSI can be estimated by its relationship with the current consumed as shown below.

If the current consumed is I_{DD} (mA), then the number of power supply terminals required (N_{IDD}) to supply the consumption current I_{DD} is as follows:

$N_{IDD} \geq I_{DD}/50$ (pairs)

NOTE: Insert at least two pair of power terminal N_{IDD}.
I_{DD}: Calculate I_{DD} by dividing the power consumption calculated in Chapter 9 by the operating voltage.

10.2 Number of Simultaneous Operations and Adding Power Supplies

In the S1L35000 Series, the output drive capability is extremely large at a Max. of 12 mA, and thus the noise generated by the output buffers when they are operating is also extremely large.

V_{SS} power supplies need to be added, as shown in Table 10-1 to prevent malfunction from the noise when multiple output buffers operate at the same time.

Moreover, add V_{DD} terminals at 1-to-1 ratio with additional V_{SS} terminals. (See Table 10-2.)

Table 10-1 Number of V_{SS} Power Supplies to Add Depending on the Simultaneous Operation of Output Buffers (V_{DD}=5V)

Output Drive Ability (I_{OL})	Number of Output Buffers Operating Simultaneously	Number of Additional Power Supplies		
		$C_L \leqq 50pF$	$C_L \leqq 100pF$	$C_L \leqq 200pF$
8mA	$\leqq 8$	0	1	2
	$\leqq 16$	1	2	4
	$\leqq 24$	1	3	6
	$\leqq 32$	2	4	8
12mA	$\leqq 8$	1	2	3
	$\leqq 16$	2	3	5
	$\leqq 24$	2	5	7
	$\leqq 32$	3	6	12

NOTE: When using power of 3.0V_{DD} or 3.3V_{DD}(Typ.), the number of output buffers should be about 60% of the number metioned above list.

Table 10-2 Number of V_{DD} Power Supplies to Add Depending on the Simultaneous Operation of Output Buffers (V_{DD}=5V)

Output Drive Ability (I_{OH})	Number of Output Buffers Operating Simultaneously	Number of Additional Power Supplies		
		$C_L \leqq 50pF$	$C_L \leqq 100pF$	$C_L \leqq 200pF$
8mA	$\leqq 8$	0	1	1
	$\leqq 16$	1	1	3
	$\leqq 24$	1	2	4
	$\leqq 32$	1	3	5
12mA	$\leqq 8$	1	2	3
	$\leqq 16$	2	3	4
	$\leqq 24$	2	4	5
	$\leqq 32$	3	5	9

NOTE: When using power of 3.0V_{DD} or 3.3V_{DD}(Typ.), the number of output buffers should be about 60% of the number metioned above list.

10.3 Cautions and Notes Regarding the Layout of Terminals

Once the package to be used has been selected, then it is time to layout the pins. Please see the specific “Pin Layout Table” regarding the number of power supply pins and useable input/output terminals in the various S1L35000 Series Packages.

Once the pin layout has been established, submit to EPSON a pin assignment specification which has been filled out with the pin layout. EPSON will layout the interconnections according to the specification submitted by the customer, so we request that the customer carefully check this specification.

The pin layout is one of the critical specifications which controls the quality of the LSI. It is especially important in avoiding malfunctions due to noise. Moreover, problems with noise are difficult to check for in simulations. So that there will be are no malfunctions with non-traceable causes in the customer’s LSI, we urge the customer to carefully study the guidelines detailed in this chapter before generating the pin layout.

10.3.1 Fixed Power Supply Pins

There are some pins which can only be used for power supply, depending on the combination of each device and package in this series. Because there are some pins which must be set to V_{DD} pins and some pins which must be set to V_{SS} pins please consult with EPSON when selecting a package.

10.3.2 Cautions and Notes Regarding the Pin Layout

The pin layout influences the logical functioning and electrical characteristics of the LSI. Moreover, the pin layout may be constrained by the construction of the LSI, the structuring of the cells and the bulk, etc. Because of this, we will explain factors which must be researched when creating the pin layout, factors such as the power supply current, the input pin/output pin isolation, the critical signals, the pull-up/pull-down resistor inputs, simultaneous output, current drivers, etc.

(1) Power Supply Current (I_{DD}, I_{SS})

When it comes to the power supply current (I_{DD}, I_{SS}) there are limitations on the tolerable levels for current from the power supply through the power supply pins when in an operating state. When the tolerable levels are exceeded, the current density within the power supply interconnects within the LSI becomes too high, and the voltage generated by the current and the resistance within the interconnects increases or decreases. This may lead to malfunctioning and may have an impact on DC or AC characteristics

In order to avoid these types of problems, it is necessary to reduce the current density and the power supply interconnect line impedance. To do this, it is necessary to estimate the power consumption during the design of the gate array, and to make sure that there are enough power supply pins so that the current through each of the power supply pins does not exceed tolerances. Moreover, the layout should be such that the power supply pins are not concentrated all in one location, but rather are spread out.

However, the final power supply pin count may require the addition of power supply pins according to the above, and the power supply pin count must include additional power supply pins for the purpose of reducing noise, etc. See Section 10.1, “Number of Simultaneous Operations and Adding Power Supplies,” regarding additional the number of additional power supply pins.

(2) Noise Resulting from the Operation of Output Cells

The noise resulting from the operation of the output cells can be broadly divided into two categories. To reduce this noise as many power supplies should be added as possible as the countermeasure.

a) Noise Generated in the Power Supply Lines

When many outputs switch simultaneously, there will be problems with noise generated in the power supply line. This can change the LSI input threshold levels, causing malfunctions. This power supply line noise is a result of the large current which is caused to flow in the power supply lines when output cells switch simultaneously. The power supply noise exerts an especially large impact on the interface components. Because of this, the LSI equivalent circuits can be represented as shown in Figure 10-1. The output of this circuit diagram shows that when there is an “H” to “L” transition, the current from the output pin flows through the components within the LSI, and flows through the equivalent inductance L_2 of the LSI package, etc. At this time, the voltage in the V_{SS} power supply line within the LSI is distorted by the equivalent inductance L_2. This voltage distortion in the V_{SS} power supply line is the noise that is generated within the power supply line. The noise which is generated within the power supply lines is primarily a result of the equivalent inductance L_2, so a large amount of noise is generated when power supply currents change rapidly.

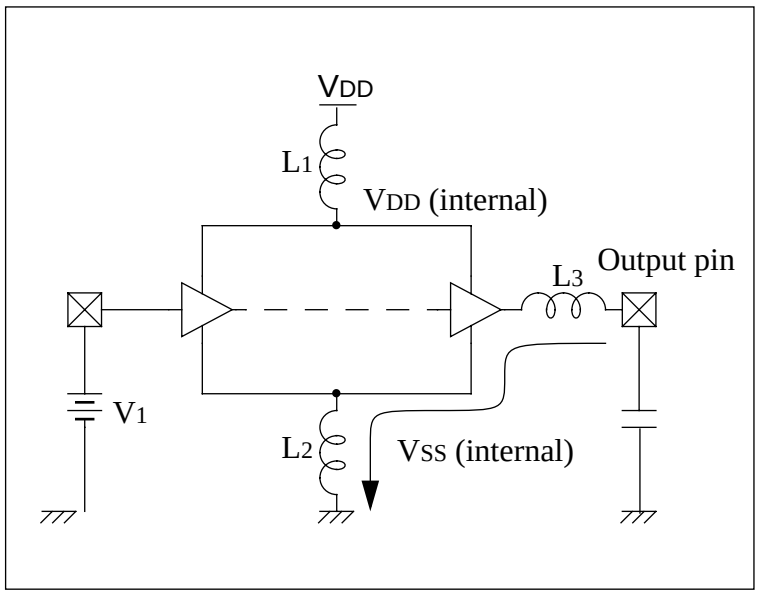


Figure 10-1 An LSI Equivalent Circuit

b) Overshoot, Undershoot, Ringing

The equivalent inductance in the output pins causes noises known as “overshoot,” “undershoot” and “ringing.” This equivalent inductance is marked by L_3 in Figure 10-1. Because inductance has the property of storing energy, this overshoot, undershoot or ringing is the result of the output becoming either low or high. When there is a transition, the overshoot and undershoot is proportional to the size of the current to the rate of change of the current.

The most effective way to reduce overshoot and undershoot is to use output cells with relatively small drive current, and there is a tendency for the overshoot and undershoot to be reduced when there is a relatively large load capacitance. Because of this, there is a need for caution when using cells with especially large current driving capabilities.

(3) Isolating Input Pins and Output Pins

Separating the input pin group from the output pin group in the pin layout is an important technique for reducing the impact of noise.

Because input pins and bi-directional pins in the input state are especially susceptible to noise, one should avoid mixing these pins with output pins whenever possible, and the input pin group, the output pin group, and the bi-directional pin group should be separated from each other by the power supply pins (V_{DD}, V_{SS}).

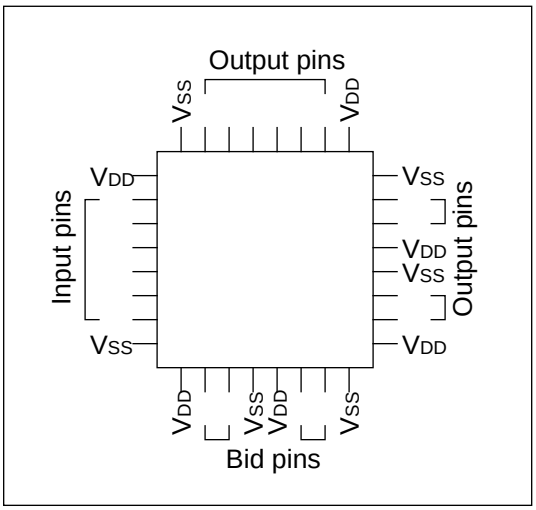


Figure 10-2 Example of Separating Input Pins and Output Pins

(4) Critical Signals

The following cautions and notes should be kept in mind when laying out the pins for critical signals such as clock input pins and high-speed output pins.

a) Pins for which it is necessary to reduce the noise, such as clock and reset pins, should be placed near the power supply pins and far from the output pins. (See Figure 10-3)

b) Oscillator circuit pins (OSCIN, OSCOUT) should be placed near one another, sandwiched between power supply pins (V_{DD}, V_{SS}). Moreover, they should not be placed near output pins. (See Figure 10-4.)

c) High-speed input and output pins should be placed near the center of the edge of the chip (of the package). (See Figure 10-3.)

d) When there is little margin in the customer specifications for delays between the input pins and the output pins, these input and output pins should be placed near to one another. (See Figure 10-3.)

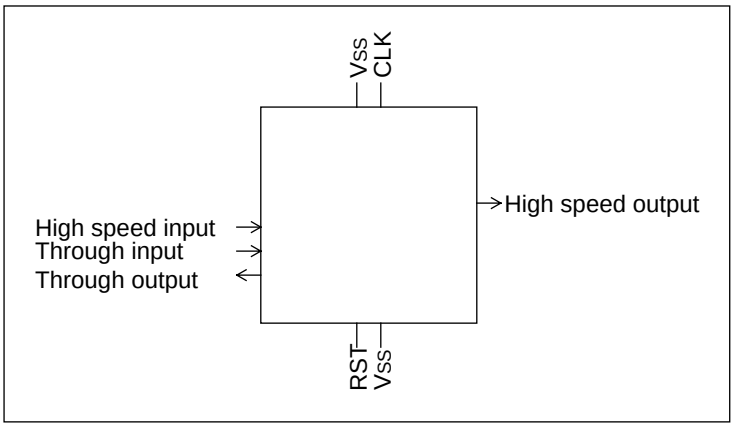


Figure 10-3 Example 1 of a Layout for Critical Signals

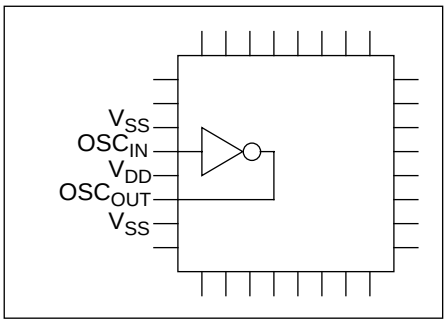


Figure 10-4 Example 2 of a Layout for Critical Signals

(5) Pull-up/Pull-down Resistor Inputs

The pull-up and pull-down resistance values are relatively large, ranging from a few dozen to a few hundred kohms. The structure of the resistors depends on the power supply voltage. Because of this, the pins are especially vulnerable to noise coming from the power supply. The following cautions should be carefully considered when creating the pin layout in order to prevent this noise from causing malfunctions.

a) Locate as far as possible from high-speed inputs (such as clock pins). (See Figure 10-5.)
b) Locate away from output pins (especially large-current output pins). (See Figure 10-6.)

Please consider the following points prior to pin layout.
• Perform pull-up and pull-down processes on the PCB itself whenever possible.
• Select resistors with low resistances whenever possible.

\

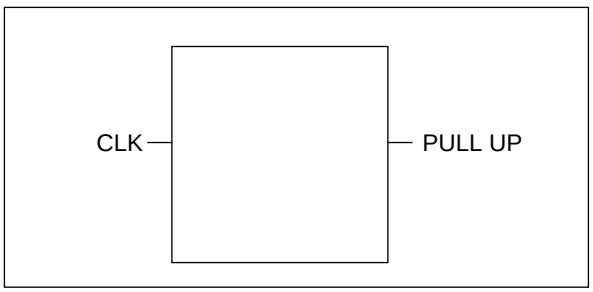


Figure 10-5 Example 1 of Placement of Pull-up and Pull-down Resistors

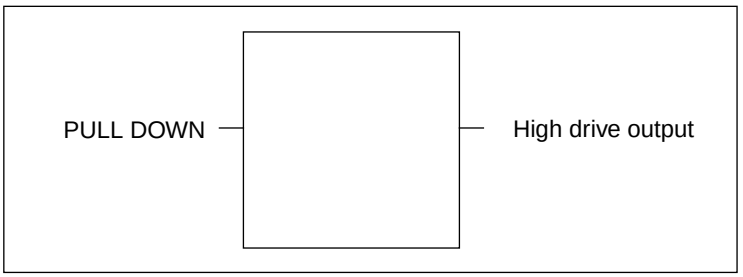


Figure 10-6 Example 2 of Placement of Pull-up and Pull-down Resistors

(6) Simultaneous Switching of Outputs

Noise is generated when multiple output pins change at the same time, which may cause malfunctioning of the LSI. In order to reduce the risk of malfunction due to noise when multiple output pins change at the same time, a power supply pin should be added to the group of output pins which are changing simultaneously. See section 10.2 regarding the number of power supply pins which must be added and the method for laying out these power supply pins. In order to reduce this noise, one may alternatively add a cell to delay the previous stage of these output cell groups, thereby reducing the amount of simultaneous changes of the output cells, thereby reducing noise as well. (See Figure 10-8.)

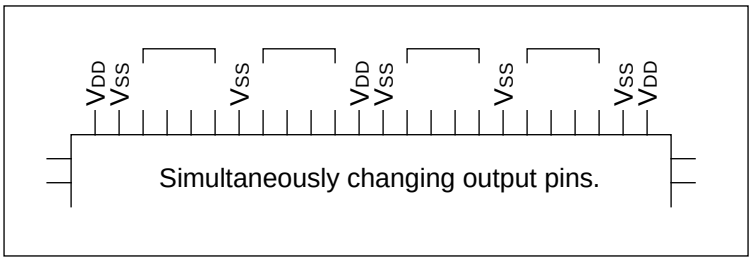


Figure 10-7 Example of Adding Power Supply Pins

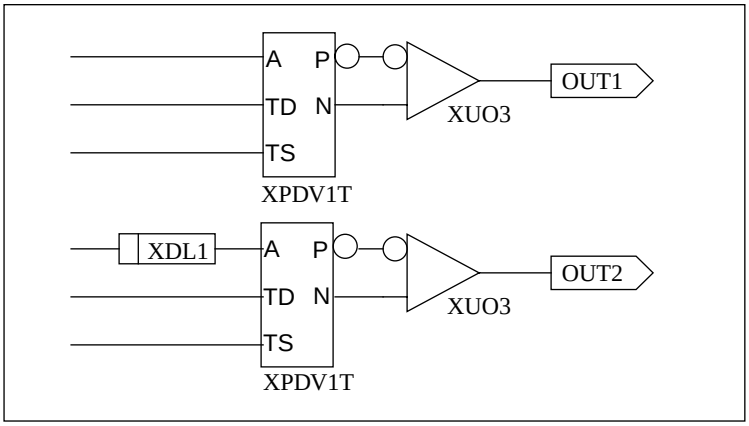


Figure 10-8 Example of Adding Delay Cells

(7) Large Current Drivers

When outputs are used which drive large currents (I_{OL} = 12 mA), pin layout should be performed following the constraints below:

a) Constraints on Strengthening the Power Supplies

Power supply pins should be located near the large-current driver pins to minimize switching niose. (See Figure 10-9.)

b) Low-Noise Pre-drivers

Low-noise output cells and low-noise pre-drivers have been prepared in order to reduce the noise generated by the operation of output cells with large current drivers. See Chapter 4 regarding recommended combinations of pre-drivers and output cells.

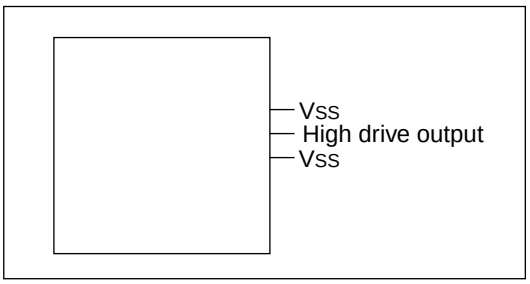


Figure 10-9 Example of Strengthening Power Supplies

(8) Other Cautions and Notes

The relationship between the package pins and the LSI pads is already established by the combination of each series device type and package type. Because of this, there may be constraints on the use of pins because of the package, and constraints on the pin layout due to the I/O cell types.

Notes and cautions regarding these restraints are described below; these should be kept in mind when determining the pin layouts.

a) NC Pins (non-connection)

A pin might be unavailable for use when the number of pads on the LSI is less than the number of pins on the package, or when the LSI pad cannot be connected to one of the package pins.

Mark these with a double asterisk (**) on the pin layout table.

10.3.3 Examples of Recommended Pin Connections

The pin layout is a critical point in ensuring that the LSI operates correctly. Determine pin layouts after referencing the example pin layout (Figure 10-10) which takes into consideration the entire content explained in this chapter.

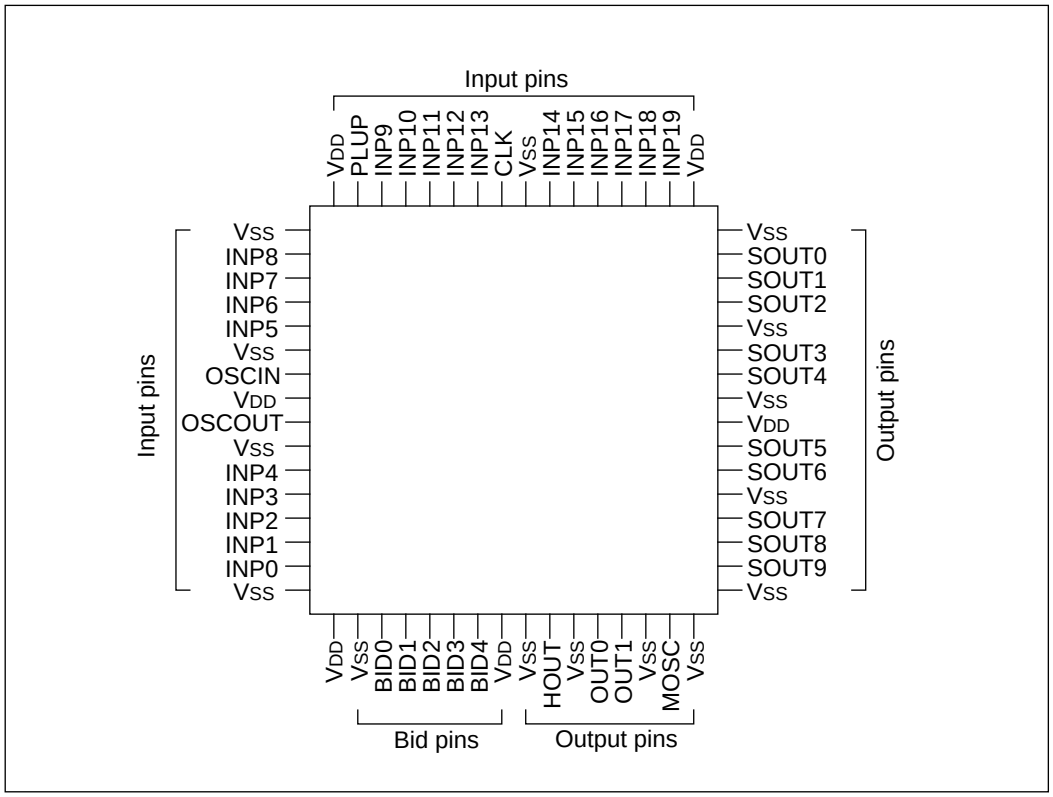


Figure 10-10 Example of Recommended Pin Layout

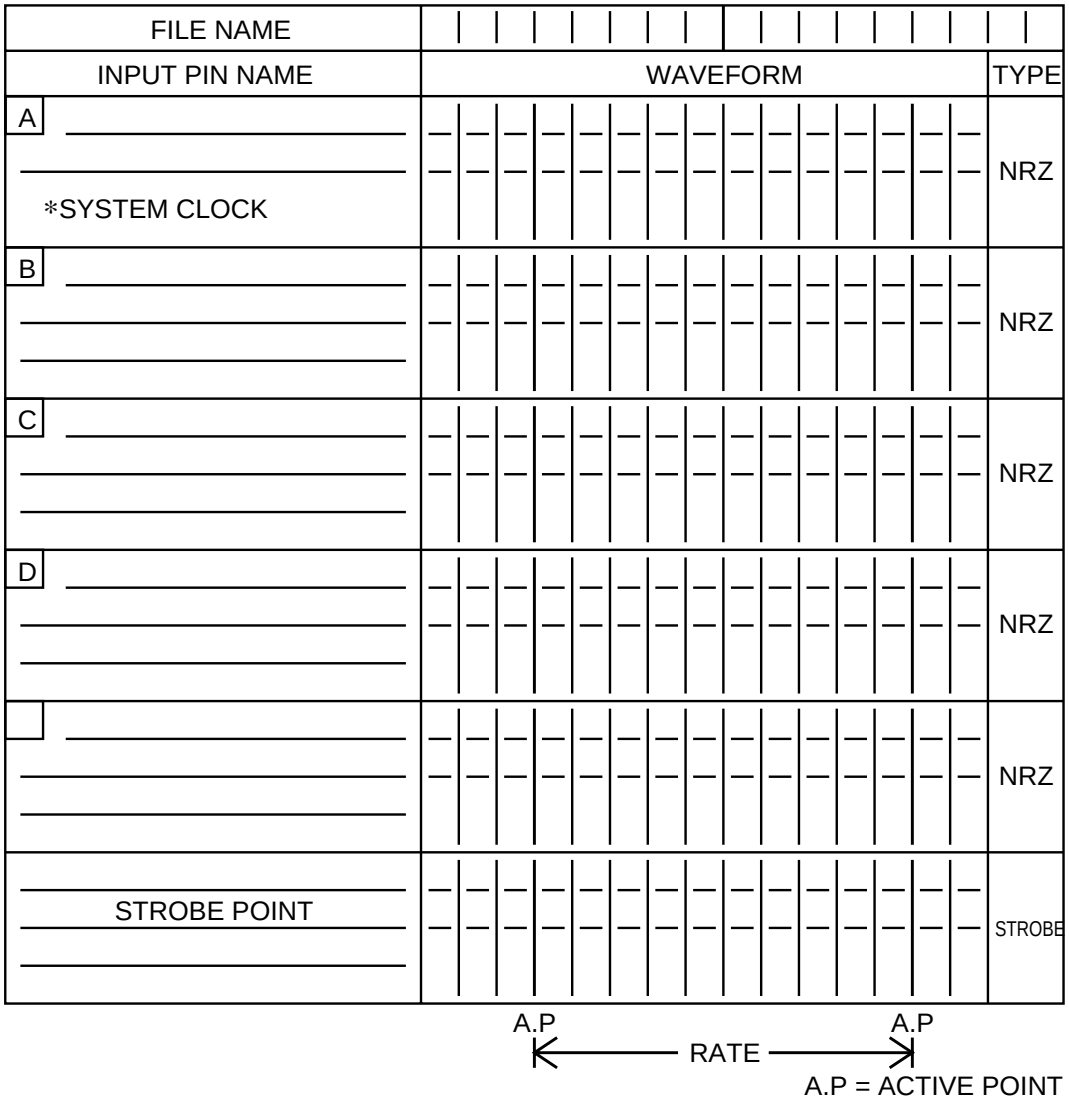
Input pins are located on the upper and left hand edges of the package, output pins which change simultaneously are located on the right hand side of the package, and bi-directional pins and other output pins are located on the bottom edge of the package.

Table 10-2 Pin Layout Example

Location	Pin Name	Explanation of Pin Name	Detailed Explanation of the Position of Each Pin
Upper Edge	PULP CLK	Input pins with pull-ups Input pins for the clock	Located where the impact of noise is the least. Located near the center of the package, and near power supply pins.
Left Edge	OSCIN, OSCOUT INP0 to19	Oscillator pins Input pins	Located near the center of the package, and near power supply pins. Located with power supply pins, away from other pins.
Right-hand Edge	SOUT0 to 9	Simultaneously changing output pins	Located near power supply pins and separated from other pins with additional power supply pins.
Bottom Edge	BID0-4 MOSC HOUT OUT01	Bi-directional pins Oscillator monitor output pins High-drive output pins Output pins	Located near power supply pins and separated from other pins. Located separated from oscillator pins and near power supply pins. Located near power supply pins. Located near power supply pins and separated from other pins.
All Edges	V_{DD} V_{SS}	V_{DD} power supply pins V_{SS} (GND) power supply pins	

Simulation Input Timing Waveforms

*The about timing might change with the limitation of the measuring system including a tester.



RATE (ns)	•	(SYSTEM CLOCK)

	DELAY (ns)	COMMENT
A	•	Duty
B	•	
C	•	
D	•	
E	•	

EPSON International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.

- HEADQUARTERS -
150 River Oaks Parkway
San Jose, CA 95134, U.S.A.
Phone: +1-408-922-0200 Fax: +1-408-922-0238

- SALES OFFICES -

West
1960 E. Grand Avenue
El Segundo, CA 90245, U.S.A.
Phone: +1-310-955-5300 Fax: +1-310-955-5400

Central
101 Virginia Street, Suite 290
Crystal Lake, IL 60014, U.S.A.
Phone: +1-815-455-7630 Fax: +1-815-455-7633

Northeast
301 Edgewater Place, Suite 120
Wakefield, MA 01880, U.S.A.
Phone: +1-781-246-3600 Fax: +1-781-246-5443

Southeast
3010 Royal Blvd. South, Suite 170
Alpharetta, GA 30005, U.S.A.
Phone: +1-877-EEA-0020 Fax: +1-770-777-2637

- DESIGN SUPPORT CENTERS -
Boston Asic Design Center
301 Edgewater Place, Suite 120
Wakefield, MA 01880, U.S.A.
Phone: +1-781-246-3600 Fax: +1-781-246-5443

San Jose Asic Design Center
150 River Oaks Parkway
San Jose, CA 95134, U.S.A.
Phone: +1-408-922-0200 Fax: +1-408-922-0238

EUROPE

EPSON EUROPE ELECTRONICS GmbH

- HEADQUARTERS -
Riesstrasse 15
80992 Munich, GERMANY
Phone: +49-(0)89-14005-0 Fax: +49-(0)89-14005-110

SALES OFFICE
Altstadtstrasse 176
51379 Leverkusen, GERMANY
Phone: +49-(0)2171-5045-0 Fax: +49-(0)2171-5045-10

UK BRANCH OFFICE
Unit 2.4, Doncastle House, Doncastle Road
Bracknell, Berkshire RG12 8PE, ENGLAND
Phone: +44-(0)1344-381700 Fax: +44-(0)1344-381701

FRENCH BRANCH OFFICE
1 Avenue de l' Atlantique, LP 915 Les Conquerants
Z.A. de Courtaboeuf 2, F-91976 Les Ulis Cedex, FRANCE
Phone: +33-(0)1-64862350 Fax: +33-(0)1-64862355

BARCELONA BRANCH OFFICE
Barcelona Design Center
Edificio Prima Sant Cugat
Adva. Alcalde Barrils num. 64-68
E-08190 Sant Cugat del Vallès, SPAIN
Phone: +34-93-544-2490 Fax: +34-93-544-2491

ASIA

EPSON (CHINA) CO., LTD.
28F, Beijing Silver Tower 2# North RD DongSanHuan ChaoYang District, Beijing, CHINA
Phone: 64106655 Fax: 64107319

SHANGHAI BRANCH
4F, Bldg., 27, No. 69, Gui Jing Road
Caohejing, Shanghai, CHINA
Phone: 21-6485-5552 Fax: 21-6485-0775

EPSON HONG KONG LTD.
20/F., Harbour Centre, 25 Harbour Road
Wanchai, Hong Kong
Phone: +852-2585-4600 Fax: +852-2827-4346
Telex: 65542 EPSCO HX

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
10F, No. 287, Nanking East Road, Sec. 3
Taipei
Phone: 02-2717-7360 Fax: 02-2712-9164
Telex: 24444 EPSONTB

HSINCHU OFFICE
13F-3, No. 295, Kuang-Fu Road, Sec. 2
HsinChu 300
Phone: 03-573-9900 Fax: 03-573-9169

EPSON SINGAPORE PTE., LTD.
No. 1 Temasek Avenue, #36-00
Millenia Tower, SINGAPORE 039192
Phone: +65-337-7911 Fax: +65-334-2716

SEIKO EPSON CORPORATION

KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-dong
Youngdeungpo-Ku, Seoul, 150-763, KOREA
Phone: 02-784-6027 Fax: 02-767-3677

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

Electronic Device Marketing Department

IC Marketing & Engineering Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5816 Fax: +81-(0)42-587-5624

ED International Marketing Department
Europe & U.S.A.
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5812 Fax: +81-(0)42-587-5564

ED International Marketing Department

Asia
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5814 Fax: +81-(0)42-587-5110

In pursuit of "Saving" Technology, Epson electronic devices.
Our lineup of semiconductors, liquid crystal displays and quartz devices
assists in creating the products of our customers' dreams.
Epson IS energy savings.

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

■ **EPSON Electronic Devices Website**

http://www.epson.co.jp/device/

First issue March,2000 Ⓓ
Printed May, 2001 in Japan ⒸA