MF1391-01

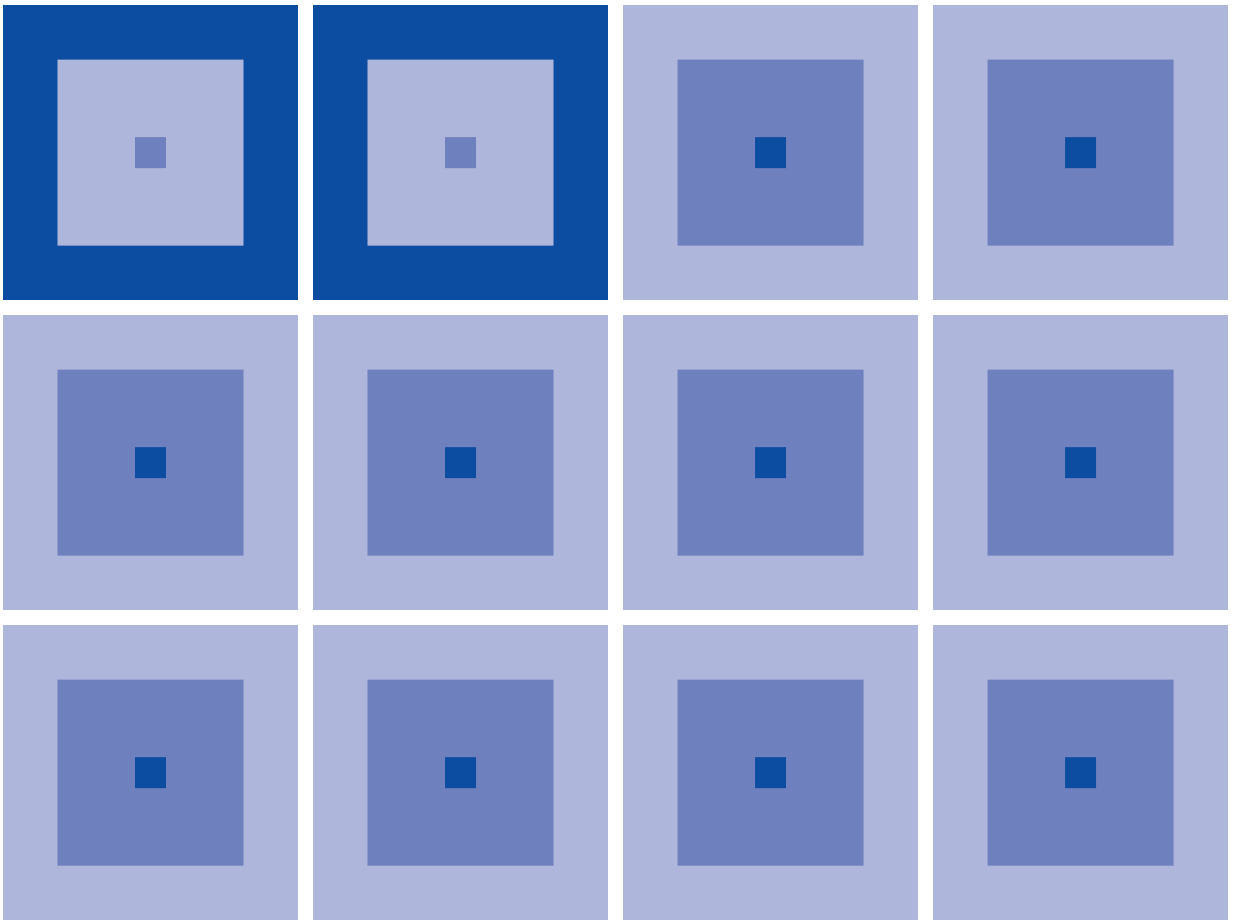
EPSON

CMOS 8-BIT SINGLE CHIP MICROCOMPUTER

S1C88349

Technical Manual

S1C88349 Technical Hardware



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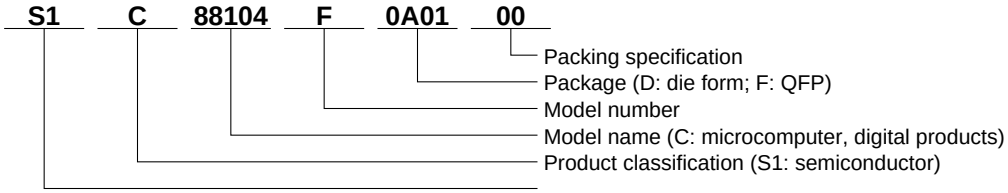
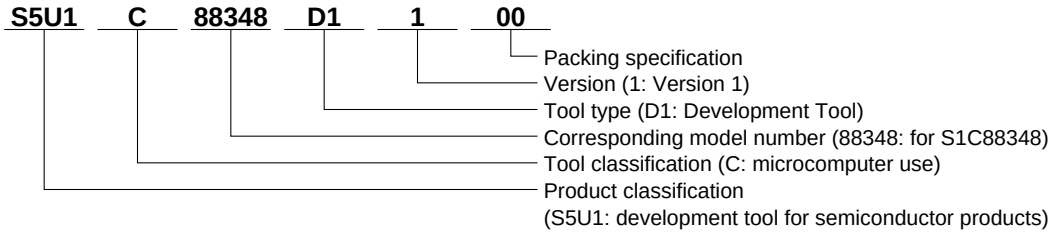
New configuration of product number

Starting April 1, 2001, the configuration of product number descriptions will be changed as listed below. To order from April 1, 2001 please use these product numbers. For further information, please contact Epson sales representative.

Devices



Development tools



Contents

1 INTRODUCTION

The S1C88349 microcomputer features the S1C88 (Model 3) CMOS 8-bit core CPU along with 48K bytes of ROM, 2K bytes of RAM, three different timers, a serial interface with optional asynchronization or clock synchronization, and an A / D converter.
The S1C88349 is fully operable over a wide range of voltages, and can perform high speed operations even at low voltage. Like all the equipment in the S1C Family, these microcomputers have low power consumption.
A 19-bit external address bus and 4 bits chip enable signals make it possible for this microcomputer to control up to 512K × 4 bytes of memory, making them ideal for high performance data bank systems.

1.1 Features

Table 1.1.1 lists the features of the S1C88349.

Table 1.1.1 Main features

Core CPU	S1C88 (MODEL3) CMOS 8-bit core CPU
OSC1 oscillation circuit	Crystal oscillation circuit/CR oscillation circuit/external clock input 32.768 kHz (Typ.)
OSC3 oscillation circuit	Crystal oscillation circuit/ceramic oscillation circuit/CR oscillation circuit/external clock input 8.2 MHz (Max.)
Instruction set	608 types (usable for multiplication and division instructions)
Min. instruction execution time	0.244 µsec/8.2 MHz (2 clock)
Internal ROM capacity	48K bytes
Internal RAM capacity	2K bytes/RAM 3,216 bits/display memory
Bus line	Address bus: 19 bits (also usable as a general output port when not used as a bus) Data bus: 8 bits (also usable as a general I/O port when not used as a bus) $\overline{CE}$ signal: 4 bits $\overline{WR}$ signal: 1 bit (also usable as a general output port when not used as a bus) $\overline{RD}$ signal: 1 bit
Input port	10 bits (2 bits can be set for event counter external clock input and bus request signal input terminal)
Output port	9 bits (6 bits can be set for buzzer output, LCD control, FOUT, TOUT and bus acknowledge signal output terminal)
I/O port	8 bits (4 bits each can be set for serial interface input/output and analog comparator/AD input)
Serial interface	1ch (optional clock synchronous system or asynchronous system)
Timer	Programmable timer (8 bits): 2ch(1ch can be set as a an event counter or 2ch as a 16 bits programmable timer for 1ch) Clock timer (8 bits): 1ch Stopwatch timer (8 bits): 1ch
LCD driver	Dot matrix type (supports5 × 8 or 5 × 5 fonts) 51 segments × 32 commons (1/5 bias) 67 segments × 16 or 8 commons (1/5 bias) Built-in LCD power supply circuit (booster type, 5 potentials)
Sound generator	Envelope function, equipped with volume control
Watchdog timer	Built-in
Analog comparator	2ch built-in (not available if A/D converter is used)
A/D converter	Resolution: 10 bits, input: 4ch, Maximum error: ±5 LSB (not available if analog comparator is used)
Supply voltage detection (SVD) circuit	Can detect up to 16 different voltage levels
Interrupt	External interrupt: Input interrupt 2 systems (3 types) Internal interrupt: Timer interrupt 3 systems (9 types) Serial interface interrupt 1 system (3 types) A/D converter interrupt 1 system (1 type)
Supply voltage	Normal mode: 2.4 V–5.5 V (Max. 4.2 MHz) V_{D1} = 2.2 V Low power mode: 1.8 V–3.5 V (Max. 80 kHz) V_{D1} = 1.2 V High speed mode: 3.5 V–5.5 V (Max. 8.2 MHz) V_{D1} = 3.3 V
Current consumption	SLEEP mode: 0.3 µA HALT mode: 1.5 µA (Typ./normal mode) Run (32 kHz): 9 µA (Typ./normal mode) Run (4 MHz): 1.1 mA (Typ./normal mode)
Supply form	QFP18-176pin, QFP21-176pin or chip

* The number of bits cited for output ports and I / O ports does not include those shared with the bus.

1.2 Block Diagram

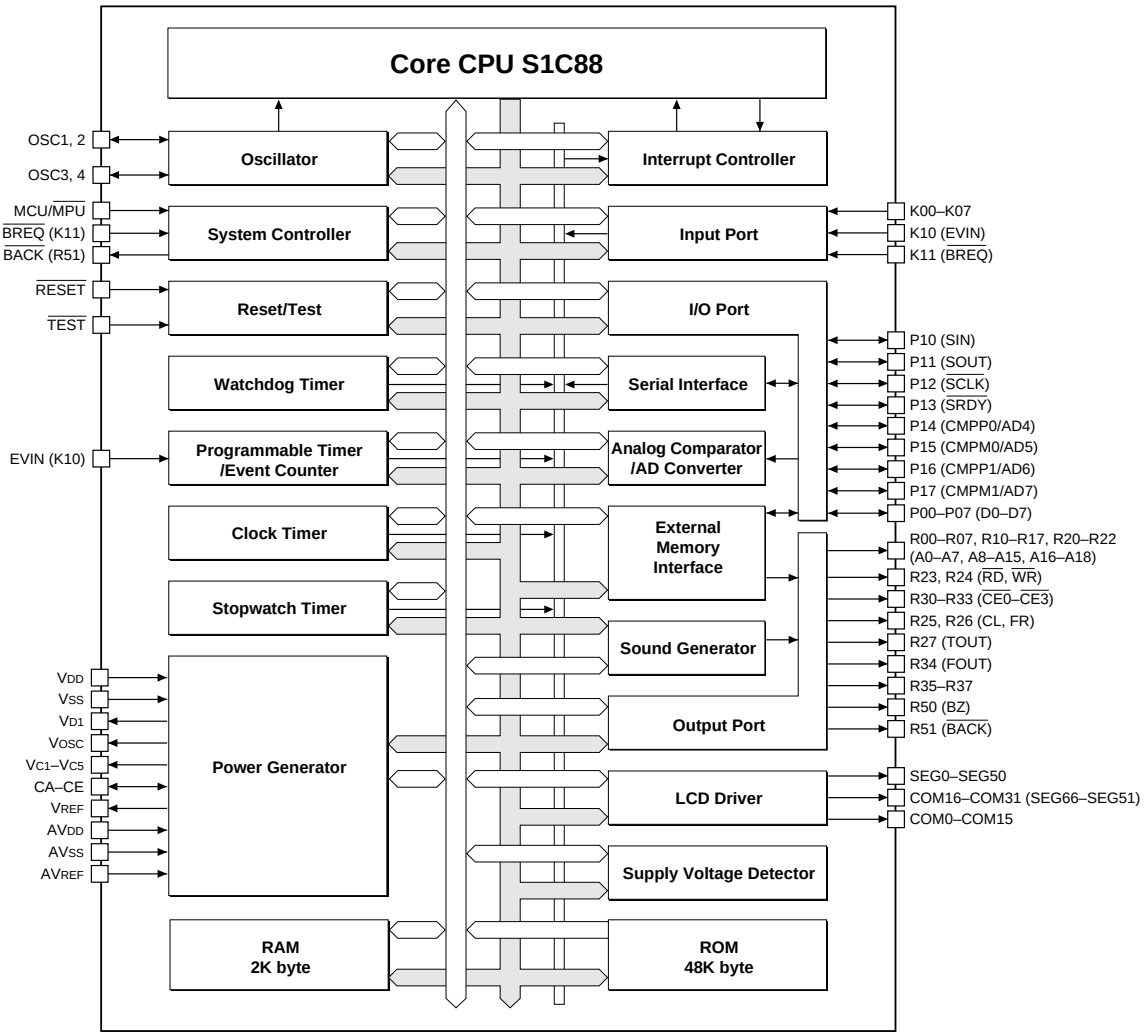
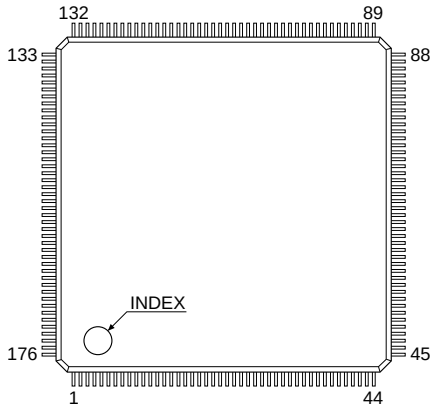


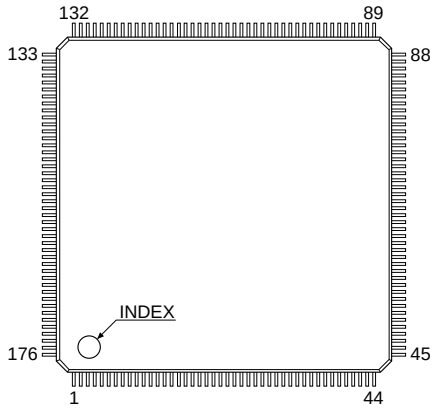
Fig. 1.2.1 S1C88349 block diagram

1.3 Pin Layout Diagram

QFP18-176pin



QFP21-176pin



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	SEG2	45	SEG46	89	OSC1	133	R11/A9
2	SEG3	46	SEG47	90	OSC2	134	R12/A10
3	SEG4	47	SEG48	91	$\overline{\text{TEST}}$	135	R13/A11
4	SEG5	48	SEG49	92	$\overline{\text{RESET}}$	136	R14/A12
5	SEG6	49	SEG50	93	MCU/$\overline{\text{MPU}}$	137	R15/A13
6	SEG7	50	COM31/SEG51	94	K11/$\overline{\text{BREQ}}$	138	R16/A14
7	SEG8	51	COM30/SEG52	95	K10/EVIN	139	R17/A15
8	SEG9	52	COM29/SEG53	96	K07	140	R20/A16
9	SEG10	53	COM28/SEG54	97	K06	141	R21/A17
10	SEG11	54	COM27/SEG55	98	K05	142	R22/A18
11	SEG12	55	COM26/SEG56	99	K04	143	R23/$\overline{\text{RD}}$
12	SEG13	56	COM25/SEG57	100	K03	144	R24/$\overline{\text{WR}}$
13	SEG14	57	COM24/SEG58	101	K02	145	R25/CL
14	SEG15	58	COM23/SEG59	102	K01	146	R26/FR
15	SEG16	59	COM22/SEG60	103	K00	147	R27/TOUT
16	SEG17	60	COM21/SEG61	104	P17/CMPM1/AD7	148	R30/$\overline{\text{CE0}}$
17	SEG18	61	COM20/SEG62	105	P16/CMPP1/AD6	149	R31/$\overline{\text{CE1}}$
18	SEG19	62	COM19/SEG63	106	P15/CMPM0/AD5	150	R32/$\overline{\text{CE2}}$
19	SEG20	63	COM18/SEG64	107	P14/CMPP0/AD4	151	R33/$\overline{\text{CE3}}$
20	SEG21	64	COM17/SEG65	108	P13/$\overline{\text{SRDY}}$	152	R34/FOUT
21	SEG22	65	COM16/SEG66	109	P12/$\overline{\text{SCLK}}$	153	R35
22	SEG23	66	N.C.	110	P11/SOUT	154	R36
23	SEG24	67	N.C.	111	P10/SIN	155	R37
24	SEG25	68	N.C.	112	AV_{DD}	156	V_{SS}
25	SEG26	69	N.C.	113	AV_{SS}	157	R50/$\overline{\text{BZ}}$
26	SEG27	70	N.C.	114	AV_{REF}	158	R51/$\overline{\text{BACK}}$
27	SEG28	71	N.C.	115	V_{DD}	159	COM0
28	SEG29	72	V_{REF}	116	P07/D7	160	COM1
29	SEG30	73	CE	117	P06/D6	161	COM2
30	SEG31	74	CD	118	P05/D5	162	COM3
31	SEG32	75	CC	119	P04/D4	163	COM4
32	SEG33	76	CB	120	P03/D3	164	COM5
33	SEG34	77	CA	121	P02/D2	165	COM6
34	SEG35	78	V_{C5}	122	P01/D1	166	COM7
35	SEG36	79	V_{C4}	123	P00/D0	167	COM8
36	SEG37	80	V_{C3}	124	R00/A0	168	COM9
37	SEG38	81	V_{C2}	125	R01/A1	169	COM10
38	SEG39	82	V_{C1}	126	R02/A2	170	COM11
39	SEG40	83	OSC3	127	R03/A3	171	COM12
40	SEG41	84	OSC4	128	R04/A4	172	COM13
41	SEG42	85	V_{D1}	129	R05/A5	173	COM14
42	SEG43	86	V_{DD}	130	R06/A6	174	COM15
43	SEG44	87	V_{SS}	131	R07/A7	175	SEG0
44	SEG45	88	V_{OSC}	132	R10/A8	176	SEG1

Fig. 1.3.1 S1C88349 pin layout

1.4 Pin Description

Table 1.4.1 S1C88349 pin description

Pin name	Pin No.	In/Out	Function
V_{DD}	86, 115	–	Power supply (+) terminal
V_{SS}	87, 156	–	Power supply (GND) terminal
V_{D1}	85	–	Internal logic system voltage regulator output terminal
V_{OSC}	88	–	Oscillation system voltage regulator output terminal
V_{C1}–V_{C5}	82–78	–	LCD drive voltage output terminals
CA–CE	77–73	–	Booster capacitor connection terminals for LCD
V_{REF}	72	–	LCD system power testing terminal
OSC1	89	I	OSC1 oscillation input terminal (select crystal oscillation/CR oscillation/external clock input by mask option)
OSC2	90	O	OSC1 oscillation output terminal
OSC3	83	I	OSC3 oscillation input terminal (select crystal/ceramic/CR oscillation/external clock input by mask option)
OSC4	84	O	OSC3 oscillation output terminal
MCU/$\overline{\text{MPU}}$	93	I	Terminal for setting MCU or MPU modes
K00–K07	103–96	I	Input terminals (K00–K07)
K10/EVIN	95	I	Input terminal (K10) or event counter external clock input terminal (EVIN)
K11/$\overline{\text{BREQ}}$	94	I	Input terminal (K11) or bus request signal input terminal ($\overline{\text{BREQ}}$)
R00–R07/A0–A7	124–131	O	Output terminals (R00–R07) or address bus (A0–A7)
R10–R17/A8–A15	132–139	O	Output terminals (R10–R17) or address bus (A8–A15)
R20–R22/A16–A18	140–142	O	Output terminals (R20–R22) or address bus (A16–A18)
R23/$\overline{\text{RD}}$	143	O	Output terminal (R23) or read signal output terminal ($\overline{\text{RD}}$)
R24/$\overline{\text{WR}}$	144	O	Output terminal (R24) or write signal output terminal ($\overline{\text{WR}}$)
R25/CL	145	O	Output terminal (R25) or LCD synchronous signal output terminal (CL)
R26/FR	146	O	Output terminal (R26) or LCD frame signal output terminal (FR)
R27/TOUT	147	O	Output terminal (R27) or programmable timer underflow signal output terminal (TOUT)
R30–R33/$\overline{\text{CE0}}$–$\overline{\text{CE3}}$	148–151	O	Output terminals (R30–R33) or chip enable output terminals ($\overline{\text{CE0}}$–$\overline{\text{CE3}}$)
R34/FOUT	152	O	Output terminal (R34) or clock output terminal (FOUT)
R35–R37	153–155	O	Output terminals (R35–R37)
R50/BZ	157	O	Output terminal (R50) or buzzer output terminal (BZ)
R51/$\overline{\text{BACK}}$	158	O	Output terminal (R51) or bus acknowledge signal output terminal ($\overline{\text{BACK}}$)
P00–P07/D0–D7	123–116	I/O	I/O terminals (P00–P07) or data bus (D0–D7)
P10/SIN	111	I/O	I/O terminal (P10) or serial I/F data input terminal (SIN)
P11/SOUT	110	I/O	I/O terminal (P11) or serial I/F data output terminal (SOUT)
P12/$\overline{\text{SCLK}}$	109	I/O	I/O terminal (P12) or serial I/F clock I/O terminal ($\overline{\text{SCLK}}$)
P13/$\overline{\text{SRDY}}$	108	I/O	I/O terminal (P13) or serial I/F ready signal output terminal ($\overline{\text{SRDY}}$)
P14/CMPP0/AD4	107	I/O	I/O terminal (P14), analog comparator 0 non-inverted input terminal or A/D converter input terminal
P15/CMPM0/AD5	106	I/O	I/O terminal (P15), analog comparator 0 inverted input terminal or A/D converter input terminal
P16/CMPP1/AD6	105	I/O	I/O terminal (P16), analog comparator 1 non-inverted input terminal or A/D converter input terminal
P17/CMPM1/AD7	104	I/O	I/O terminal (P17), analog comparator 1 inverted input terminal or A/D converter input terminal
COM0–COM15	159–174	O	LCD common output terminals
COM16–COM31 /SEG66–SEG51	65–50	O	LCD common output terminals (when 1/32 duty is selected) or LCD segment output terminal (when 1/16 duty is selected)
SEG0–SEG50	175–176, 1–49	O	LCD segment output terminals
$\overline{\text{RESET}}$	92	I	Initial reset input terminal
$\overline{\text{TEST}}$	91	I	Test input terminal
AV_{DD}	112	–	Analog system power supply (+) terminal
AV_{SS}	113	–	Analog system power supply (–) terminal
AV_{REF}	114	–	Analog system reference voltage terminal

1.5 Mask Option

Mask options shown below are provided for the S1C88349. Several hardware specifications are prepared in each mask option, and one of them can be selected according to the application. The function option generator winfog, that has been prepared as the development software tool of the S1C88349, is used for this selection. Mask pattern of the IC is finally generated based on the data created by the winfog. Refer to the "S1C88 Family Development Tool Manual" for details on the winfog.

Option list

The following options can be set for the S1C88349 and ICE (S5U1C88000H5). Multiple specifications are available in each option item as indicated in the Option List. Select the specifications that meet the target system and check the appropriate box.
The option selection is done interactively on the screen during winfog execution, using this option list as reference.

PERIPHERAL CIRCUIT BOARD option list

A OSC1 SYSTEM CLOCK

☐ 1. Internal Clock (32.768 kHz)
☐ 2. User Clock

B OSC3 SYSTEM CLOCK

☐ 1. Internal Clock (4.9152 MHz)
☐ 2. User Clock

S1C88349 mask option list

1 OSC1 SYSTEM CLOCK

☐ 1. Crystal
☐ 2. External Clock
☐ 3. CR
☐ 4. Crystal (with Gate Capacity)

2 OSC3 SYSTEM CLOCK

☐ 1. Crystal
☐ 2. Ceramic
☐ 3. CR
☐ 4. External Clock

3 MULTIPLE KEY ENTRY RESET

• Combination ... ☐ 1. Not Use
☐ 2. Use K00, K01
☐ 3. Use K00, K01, K02
☐ 4. Use K00, K01, K02, K03

4 MPU MODE INITIAL SET

☐ 1. 512K (MAX)
☐ 2. 512K (MIN)
☐ 3. 64K

5 SVD RESET

☐ 1. Not Use
☐ 2. Use

6 INPUT PORT PULL UP RESISTOR

• K00	☐ 1. With Resistor	☐ 2. Gate Direct
• K01	☐ 1. With Resistor	☐ 2. Gate Direct
• K02	☐ 1. With Resistor	☐ 2. Gate Direct
• K03	☐ 1. With Resistor	☐ 2. Gate Direct
• K04	☐ 1. With Resistor	☐ 2. Gate Direct
• K05	☐ 1. With Resistor	☐ 2. Gate Direct
• K06	☐ 1. With Resistor	☐ 2. Gate Direct
• K07	☐ 1. With Resistor	☐ 2. Gate Direct
• K10	☐ 1. With Resistor	☐ 2. Gate Direct
• K11	☐ 1. With Resistor	☐ 2. Gate Direct
• $\overline{\text{MCU}}$ / $\overline{\text{MPU}}$	☐ 1. With Resistor	☐ 2. Gate Direct
• $\overline{\text{RESET}}$	☐ 1. With Resistor	☐ 2. Gate Direct

7 I/O PORT PULL UP RESISTOR

• P00	☐ 1. With Resistor	☐ 2. Gate Direct
• P01	☐ 1. With Resistor	☐ 2. Gate Direct
• P02	☐ 1. With Resistor	☐ 2. Gate Direct
• P03	☐ 1. With Resistor	☐ 2. Gate Direct
• P04	☐ 1. With Resistor	☐ 2. Gate Direct
• P05	☐ 1. With Resistor	☐ 2. Gate Direct
• P06	☐ 1. With Resistor	☐ 2. Gate Direct
• P07	☐ 1. With Resistor	☐ 2. Gate Direct
• P10	☐ 1. With Resistor	☐ 2. Gate Direct
• P11	☐ 1. With Resistor	☐ 2. Gate Direct
• P12	☐ 1. With Resistor	☐ 2. Gate Direct
• P13	☐ 1. With Resistor	☐ 2. Gate Direct
• P14	☐ 1. With Resistor	☐ 2. Gate Direct
• P15	☐ 1. With Resistor	☐ 2. Gate Direct
• P16	☐ 1. With Resistor	☐ 2. Gate Direct
• P17	☐ 1. With Resistor	☐ 2. Gate Direct

8 OUTPUT PORT SPECIFICATION

• R00	☐ 1. Complementary	☐ 2. Nch Open Drain
• R01	☐ 1. Complementary	☐ 2. Nch Open Drain
• R02	☐ 1. Complementary	☐ 2. Nch Open Drain
• R03	☐ 1. Complementary	☐ 2. Nch Open Drain
• R04	☐ 1. Complementary	☐ 2. Nch Open Drain
• R05	☐ 1. Complementary	☐ 2. Nch Open Drain
• R06	☐ 1. Complementary	☐ 2. Nch Open Drain
• R07	☐ 1. Complementary	☐ 2. Nch Open Drain
• R10	☐ 1. Complementary	☐ 2. Nch Open Drain
• R11	☐ 1. Complementary	☐ 2. Nch Open Drain
• R12	☐ 1. Complementary	☐ 2. Nch Open Drain
• R13	☐ 1. Complementary	☐ 2. Nch Open Drain
• R14	☐ 1. Complementary	☐ 2. Nch Open Drain
• R15	☐ 1. Complementary	☐ 2. Nch Open Drain
• R16	☐ 1. Complementary	☐ 2. Nch Open Drain
• R17	☐ 1. Complementary	☐ 2. Nch Open Drain

9 LCD POWER SUPPLY

☐ 1. Internal
☐ 2. External

Outline of mask options

(1) OSC1 oscillation circuit

The specification of the OSC1 oscillation circuit can be selected from among four types: "Crystal oscillation", "CR oscillation", "Crystal oscillation (gate capacitor built-in)" and "External clock input". Refer to Section 5.4.3, "OSC1 oscillation circuit", for details.

(2) OSC3 oscillation circuit

The specification of the OSC3 oscillation circuit can be selected from among four types: "Crystal oscillation", "Ceramic oscillation", "CR oscillation" and "External clock input". Refer to Section 5.4.4, "OSC3 oscillation circuit", for details.

(3) Multiple key entry reset (K00–K03)

This function resets the IC when several keys are pressed simultaneously. The mask option is used to select whether this function is used or not. Further when the function is used, a combination of the input ports (K00–K03), which are connected to the keys to be pressed simultaneously, can be selected. Refer to Section 4.1.2, "Simultaneous LOW level input at input port terminals K00–K03", for details.

(4) Initial bus mode for MPU mode

The bus mode that is initially set in MPU mode can be selected from expanded 512K maximum mode, expanded 512K minimum mode and expanded 64K mode. Refer to Section 5.2, "System controller and Bus Control", for details.

(5) Initial reset by SVD circuit

The SVD circuit has a function that generates an initial reset signal when the supply voltage drops to level 0 or less. The mask option is used to select whether this function is used or not. Refer to Section 5.16, "Supply Voltage Detection (SVD) Circuit", for details.

(6) Input port, MCU/$\overline{\text{MPU}}$ and $\overline{\text{RESET}}$ terminal pull-up resistors

This mask option can select whether the pull-up resistor for the input (K) port terminal is used or not. It is possible to select for each bit of the input ports. Refer to Section 5.5, "Input Ports (K ports)", for details.
Furthermore, a pull-up option is also provided for the MCU/$\overline{\text{MPU}}$ and $\overline{\text{RESET}}$ terminals.

(7) I/O port pull-up resistors

This mask option can select whether the pull-up resistor for the I/O port terminal (it works during input mode) is used or not. It is possible to select for each bit of the I/O ports. Refer to Section 5.7, "I/O Ports (P ports)", for details.

Since P10 to P13 are shared with the serial interface I/O terminals, the selected P10 and P12 terminal configuration is applied to the serial input (SIN) terminal and serial clock input terminal ($\overline{\text{SCLK}}$ in clock synchronous mode) when the serial interface is used. Refer to Section 5.8, "Serial Interface", for details.

(8) Output port specifications

Either complementary output or Nch open drain output can be selected as the output specification for the output ports R00–R07 and R10–R17 in 1 bit units. Refer to Section 5.6.2, "Mask option", for details.

(9) LCD power supply

Either the internal power supply (internal LCD system voltage regulator and voltage booster that generate V_{C1} to V_{C5}) or an external power supply can be selected as the LCD system power source. Refer to Section 5.12.2, "Mask option", for details.

2 POWER SUPPLY

In this section, we will explain the operating voltage and the configuration of the internal power supply circuit of the S1C88349.

2.1 Operating Voltage

The S1C88349 operating power voltage is as follows:

Normal mode:	2.4 V to 5.5 V
Low power mode:	1.8 V to 3.5 V
High speed mode:	3.5 V to 5.5 V

2.2 Internal Power Supply Circuit

The S1C88349 incorporates the power supply circuit shown in Figure 2.2.1. When voltage within the range described above is supplied to V_{DD} (+) and V_{SS} (GND), all the voltages needed for the internal circuit are generated internally in the IC.

Roughly speaking, the power supply circuit is divided into three sections.

The internal logic voltage regulator generates the operating voltage <V_{D1}> for driving the internal logic circuits and the OSC3 oscillation circuit. The V_{D1} voltage can be selected from the following three types: 1.2 V for low-power mode, 2.2 V for normal mode and 3.1 V for high-speed mode.
It should be selected by a program to switch according to the supply voltage and oscillation frequency.
See Section 5.4, "Oscillation Circuits and Operating Mode", for the switching of operating mode.

Note: Under no circumstances should V_{D1} terminal output be used to drive external circuit.

The oscillation system voltage regulator generates the operating voltage <V_{OSC}> for the OSC1 oscillation circuit.

The LCD system power supply circuit generates the drive voltage for the LCD. Drive voltage has five potentials V_{C1}–V_{C5} for 1/5 bias: V_{C1} and V_{C2} are generated by the LCD voltage regulator, and are boosted to generate V_{C3}–V_{C5}. These voltages are output from the terminals to drive an external LCD driver (S1D15210 or equivalent).
See Chapter 8, "ELECTRICAL CHARACTERISTICS" for the voltage values.

In the S1C88349, the LCD drive voltage is supplied to the built-in LCD driver which drives the LCD panel connected to the SEG and COM terminals.

Notes:
- *Do not use terminals V_{C1}–V_{C5} except to supply voltage to the expanded LCD driver.*
- *Refer to the "S1D15000 Series Technical Manual" for the S1D15210 externaly expanded LCD driver.*

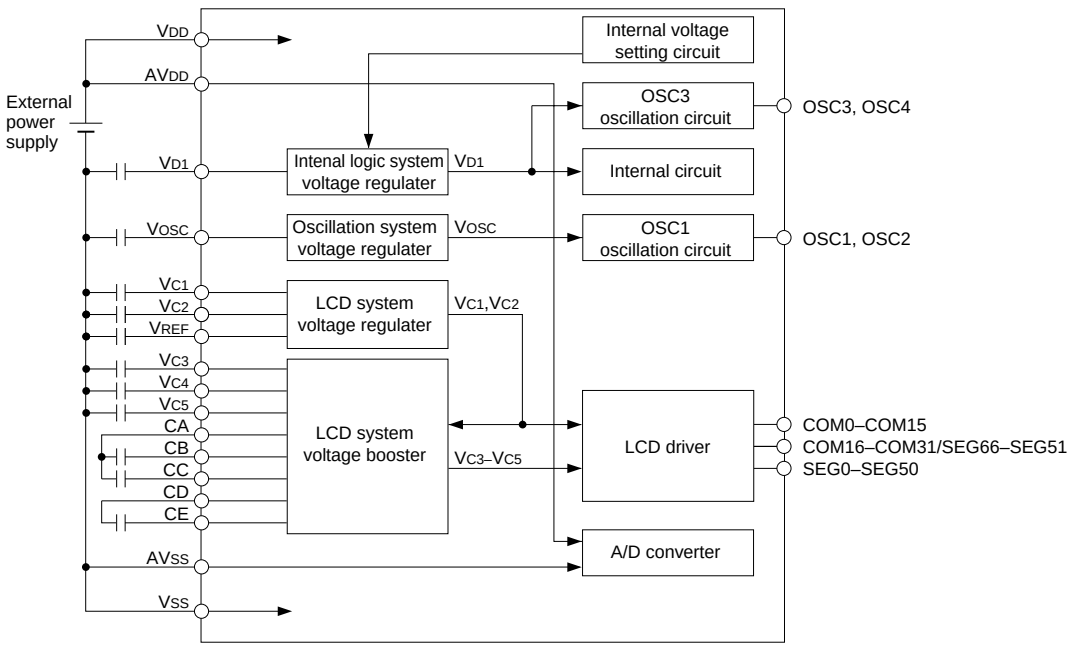


Fig. 2.2.1 Configuration of power supply circuit

3 CPU AND BUS CONFIGURATION

In this section, we will explain the CPU, operating mode and bus configuration.

3.1 CPU

The S1C88349 utilize the S1C88 8-bit core CPU whose resistor configuration, command set, etc. are virtually identical to other units in the family of processors incorporating the S1C88.

See the "S1C88 Core CPU Manual" for the S1C88.

Specifically, the S1C88349 employ the Model 3 S1C88 CPU which has a maximum address space of 512K bytes × 4.

3.2 Internal Memory

The S1C88349 is equipped with internal ROM and RAM as shown in Figure 3.2.1. Small scale applications can be handled by one chip. It is also possible to utilize internal memory in combination with external memory.
Furthermore, internal ROM can be disconnected from the bus and the resulting space released for external applications.

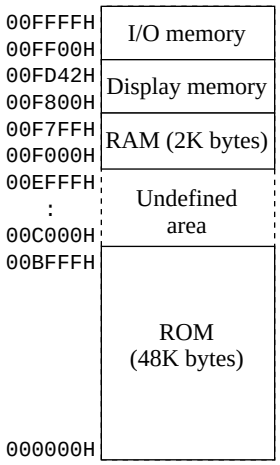


Fig. 3.2.1 Internal memory map

3.2.1 ROM

The S1C88349 has a built-in 48K-byte ROM. The ROM is allocated to 000000H–00BFFFH.
The ROM areas shown above can be released to external memory depending on the setting of the MCU/$\overline{\text{MPU}}$ terminal. (See "3.5 Chip Mode".)

3.2.2 RAM

The internal RAM capacity is 2K bytes and is allocated to 00F000H–00F7FFH.
Even when external memory which overlaps the internal RAM area is expanded, the RAM area is not released to external memory. Access to this area is via internal RAM.

3.2.3 I/O memory

A memory mapped I/O method is employed in the S1C88349 for interfacing with internal peripheral circuit. Peripheral circuit control bits and data register are arranged in data memory space. Control and data exchange are conducted via normal memory access. I/O memory is arranged in page 0: 00FF00H–00FFFFH area.
See Section 5.1, "I/O Memory Map", for details of the I/O memory.
Even when external memory which overlaps the I/O memory area is expanded, the I/O memory area is not released to external memory. Access to this area is via I/O memory.

3.2.4 Display memory

The S1C88349 is equipped with an internal display memory which stores a display data for LCD driver.
Display memory is arranged in page 0: 00Fx00H–00Fx42H (x = 8–DH) in the data memory area. See Section 5.12, "LCD Controller", for details of the display memory. Like the I/O memory, display memory cannot be released to external memory.

3.3 Exception Processing Vectors

000000H–000025H in the program area of the S1C88349 is assigned as exception processing vectors. Furthermore, from 000028H to 0000FFH, software interrupt vectors are assignable to any two bytes which begin with an even address.
Table 3.3.1 lists the vector addresses and the exception processing factors to which they correspond.

Table 3.3.1 Exception processing vector table

Vector address	Exception processing factor	Priority
000000H	Reset	High ↑
000002H	Zero division	
000004H	Watchdog timer ($\overline{NMI}$)	
000006H	Programmable timer 1 interrupt	
000008H	Programmable timer 0 interrupt	
00000AH	K10, K11 input interrupt	
00000CH	K04–K07 input interrupt	
00000EH	K00–K03 input interrupt	
000010H	Serial I/F error interrupt	
000012H	Serial I/F receiving complete interrupt	
000014H	Serial I/F transmitting complete interrupt	
000016H	Stopwatch timer 100 Hz interrupt	
000018H	Stopwatch timer 10 Hz interrupt	
00001AH	Stopwatch timer 1 Hz interrupt	
00001CH	Clock timer 32 Hz interrupt	
00001EH	Clock timer 8 Hz interrupt	
000020H	Clock timer 2 Hz interrupt	
000022H	Clock timer 1 Hz interrupt	↓
000024H	A/D converter interrupt	Low
000026H	System reserved (cannot be used)	No priority rating
000028H : 0000FEH	Software interrupt	

For each vector address and the address after it, the start address of the exception processing routine is written into the subordinate and super ordinate sequence. When an exception processing factor is generated, the exception processing routine is executed starting from the recorded address.
When multiple exception processing factors are generated at the same time, execution starts with the highest priority item.
The priority sequence shown in Table 3.3.1 assumes that the interrupt priority levels are all the same. The interrupt priority levels can be set by software in each system. (See Section 5.17 "Interrupt and Standby Status".)

Note: For exception processing other than reset, SC (system condition flag) and PC (program counter) are evacuated to the stack and branches to the exception processing routines. Consequently, when returning to the main routine from exception processing routines, please use the RETE instruction.

See the "S1C88 Core CPU Manual" for information on CPU operations when an exception processing factor is generated.

3.4 CC (Customized Condition Flag)

The S1C88349 does not use the customized condition flag (CC) in the core CPU. Accordingly, it cannot be used as a branching condition for the conditional branching instruction (JRS, CARS).

3.5 Chip Mode

3.5.1 MCU mode and MPU mode

The chip operating mode can be set to one of two settings using the MCU / $\overline{MPU}$ terminal.

■ **MCU mode...Set the MCU/$\overline{MPU}$ terminal to HIGH**
Switch to this setting when using internal ROM. With respect to areas other than internal memory, external memory can even be expanded. See Section 3.5.2, "Bus mode", for the memory map.

In the MCU mode, during initial reset, only systems in internal memory are activated. Internal ROM is normally fixed as the top portion of the program memory from the common area (logical space 0000H–7FFFH). Exception processing vectors are assigned in internal ROM. Furthermore, the application initialization routines that start with reset exception processing must likewise be written to internal ROM. Since bus and other settings which correlate with external expanded memory can be executed in software, this processing is executed in the initialization routine written to internal ROM. Once these bus mode settings are made, external memory can be accessed.

When accessing internal memory in this mode, the chip enable ($\overline{CE}$) and read ($\overline{RD}$) / write ($\overline{WR}$) signals are not output to external memory, and the data bus (D0–D7) goes into high impedance status (pull-up status when the "pull-up resistors for P00–P07 enabled" have been selected by the mask option).
Consequently, in cases where addresses overlap in external and internal memory, the areas in external memory will be unavailable.

■ **MPU mode...Set the MCU/$\overline{MPU}$ terminal to LOW**
Internal ROM area is released to an external device source. Internal ROM then becomes unusable and when this area is accessed, chip enable ($\overline{CE}$) and read ($\overline{RD}$) / write ($\overline{WR}$) signals are output to external memory and the data bus (D0–D7) become active. These signals are not output to an external source when other areas of internal memory are accessed.

In the MPU mode, the system is activated by external memory.
For this reason, in order to adjust bus settings to conform to the configuration of external memory during initial reset, the user can select the applicable system configuration using the mask option. (See "3.5.2 Bus mode".)

When employing this mode, the exception processing vectors and initialization routine must be assigned within the common area (000000H–007FFFH).
You can select whether to use the built-in pull-up resistor of the MCU/$\overline{\text{MPU}}$ terminal by the mask option.

Note: Setting of MCU/$\overline{\text{MPU}}$ terminal is latched at the rising edge of a reset signal input from the $\overline{\text{RESET}}$ terminal. Therefore, if the setting is to be changed, the $\overline{\text{RESET}}$ terminal must be set to LOW level once again.

3.5.2 Bus mode

In order to set bus specifications to match the configuration of external expanded memory, four different bus modes described below are selectable in software.

■ Single chip mode

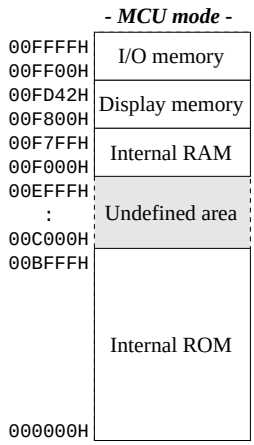


Fig. 3.5.2.1 Memory map for the single chip mode

The single chip mode setting applies when the S1C88349 is used as a single chip microcomputer without external expanded memory. Since this mode employs internal ROM, the system can only be operated in the MCU mode discussed in Section 3.5.1. In the MPU mode, the system cannot be set to the single chip mode. Since there is no need for an external bus line in this mode, terminals normally set for bus use can be used as general purpose output ports or I/O ports.
Accordingly, the output ports are in a 34-bit configuration in the S1C88349 and the I/O ports are in a 16-bit configuration.

CPU operation in this mode is equivalent to the S1C88 core CPU Model 3 minimum mode. Addresses assigned to internal memory within physical space 000000H to 00FFFFH are only effective as a target for accessing.

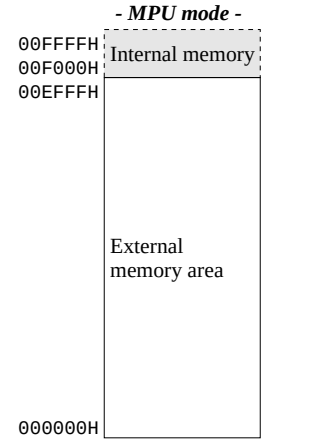
■ Expanded 64K mode (MPU mode)

The expanded 64K mode setting applies when the S1C88349 is used with 64K bytes or less of external expanded memory. This mode is only usable on the MPU mode setting.

Since the internal ROM area is released in the MPU mode, external memory in this model can be assigned to the area from 000000H to 00EFFFH. The area from 00F000H to 00FFFFH is assigned to internal memory (RAM, etc.) and cannot be used to access an external device.

This mode setting is suitable for small- to mid-scale systems. The address range of the chip enable ($\overline{\text{CE}}$) signal, adapted to memory chips with a capacity of from 8 to 64K bytes, can be selected in software to any one of four settings. See Section 3.6.4, "Chip enable ($\overline{\text{CE}}$) signal", for the $\overline{\text{CE}}$ signal.

CPU operation in this mode is equivalent to the S1C88 core CPU Model 3 minimum mode. The area within physical space 000000H to 00FFFFH is only effective as a target for accessing.



See Figure 3.2.1 for the internal memory

Fig. 3.5.2.2 Memory map for the expanded 64K mode (MPU mode)

■ Expanded 512K minimum mode

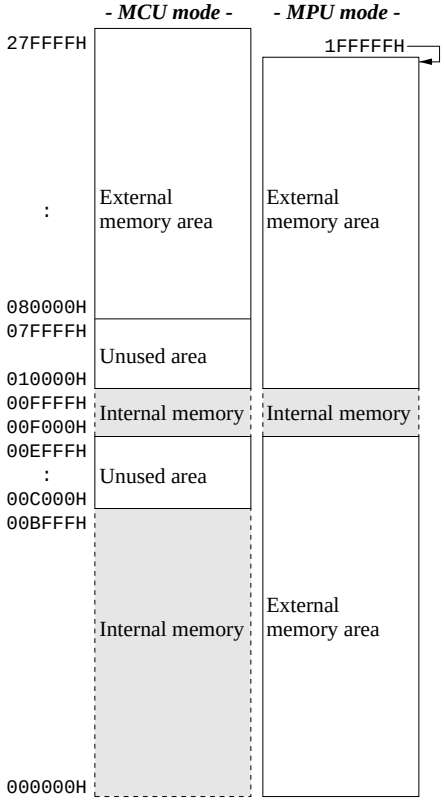
The expanded 512K minimum mode setting applies when the S1C88349 is used with over 64K bytes and less than 512K bytes × 4 of external expanded memory. This mode is usable regardless of the MCU/MPU mode setting.

Because internal ROM is being used in the MCU mode, external memory in this model can be assigned to the area from 080000H to 27FFFFH. Since the internal ROM area is released in the MPU mode, external memory in this model can be assigned to the area from 000000H to 1FFFFFH.

However, the area from 00F000H to 00FFFFH is assigned to internal memory and cannot be used to access an external device.

CPU operation in this mode is equivalent to the S1C88 core CPU Model3 minimum mode. The area within physical space 000000H to 1FFFFFH in the MPU mode or physical space 080000H to 27FFFFH + internal memory in the MCU mode is effective as a target for accessing. Furthermore, since program memory expansion is limited to less than 64K bytes configured with the common area (000000H to 007FFFH) and one optional bank area (internal ROM + 32K in the MCU mode), this mode is suitable for small- to mid-scale program memory and large-scale data memory systems.

The address range of chip enable ($\overline{CE}$) signals in this mode is fixed at 512K bytes.



See Figure 3.2.1 for the internal memory

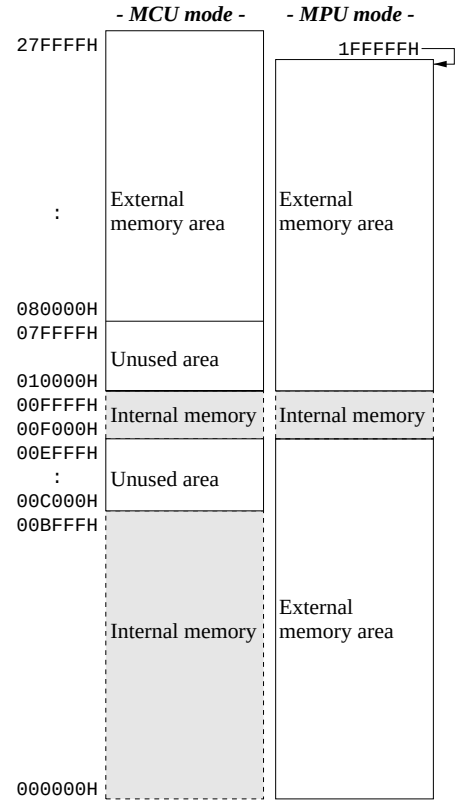
Fig. 3.5.2.3 Memory map for the expanded 512K minimum mode

■ Expanded 512K maximum mode

The expanded 512K maximum mode setting applies when the S1C88349 is used with over 64K bytes and less than 512K bytes × 4 of external expanded memory. This mode is usable regardless of the MCU / MPU mode setting.

Because internal ROM is being used in the MCU mode, external memory in this model can be assigned to the area from 080000H to 27FFFFH. Since the internal ROM area is released in the MPU mode, external memory in this model can be assigned to the area from 000000H to 1FFFFFH.
The area from 00F000H to 00FFFFH is assigned to internal memory and cannot be used to access an external device.
CPU operation in this mode is equivalent to the S1C88 core CPU Model 3 maximum mode, the area within physical space 000000H to 1FFFFFH in the MPU mode or physical space 080000H to 27FFFFH + internal memory in the MCU mode is effective as a target for accessing. In the above mentioned physical space, since program memory and data memory can be secured with an optional (maximum 512K bytes × 4 program + data) size, this mode is suitable for systems with large-scale program and data capacity.

The address range of chip enable ($\overline{CE}$) signals in this mode is fixed at 512K bytes.



See Figure 3.2.1 for the internal memory

Fig. 3.5.2.4 Memory map for the expanded 512K maximum mode

There is an explanation on how all these settings are actually made in "5.2 System Controller and Bus Control" of this Manual.

3.6 External Bus

The S1C88349 has bus terminals that can address a maximum of 512K × 4 bytes and memory (and other) devices can be externally expanded according to the range of each bus mode described in the previous section.

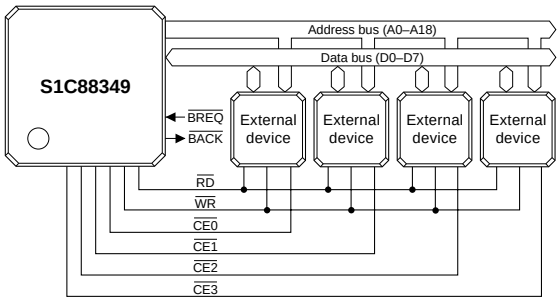


Fig. 3.6.1 External bus lines

Below is an explanation of external bus terminals. For information on control methods, see Section 5.2, "System Controller and Bus Control".

3.6.1 Data bus

The S1C88349 possesses an 8-bit external data bus (D0–D7). The terminals and I/O circuits of data bus D0–D7 are shared with I/O ports P00–P07, switching between these functions being determined by the bus mode setting.
In the single chip mode, the 8-bit terminals are all set as I/O ports P00–P07 and in the other expanded modes, they are set as data bus (D0–D7).
When set as data bus, the data register and I/O control register of each I/O port are detached from the I/O circuits and usable as a general purpose data register with read/write capabilities.
With regard to the pull-up resistors that go ON only in input mode, the mask option can be used to select whether or not to use the pull-up resistor for each data bus line. (The same holds true when the terminals are used as I/O ports.)

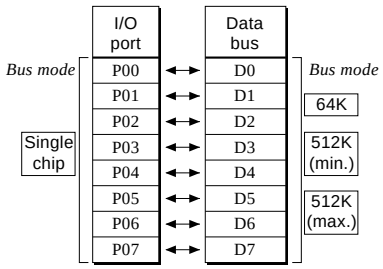


Fig. 3.6.1.1 Correspondence between data bus and I/O ports

3.6.2 Address bus

The S1C88349 possesses a 19-bit external address bus A0–A18. The terminals and output circuits of address bus A0–A18 are shared with output ports R00–R07 (=A0–A7), R10–R17 (=A8–A15) and R20–R22 (=A16–A18), switching between these functions being determined by the bus mode setting.
In the single chip mode, the 19-bit terminals are all set as output ports R00–R07, R10–R17 and R20–R22.
In the expanded 64K mode, 16 of the 19-bit terminals, A0–A15, are set as the address bus, while the remaining 3 bits, A16–A18, are set as output ports R20–R22.
In the expanded 512K minimum and maximum modes, all of the 19-bit terminals are set as the address bus (A0–A18).
When set as an address bus, the data register and high impedance control register of each output port are detached from the output circuit and used as a general purpose data register with read/write capabilities.

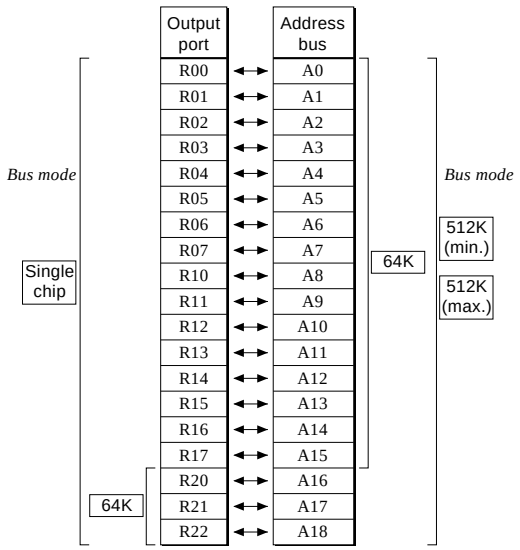


Fig. 3.6.2.1 Correspondence between address bus and output ports

3.6.3 Read ($\overline{RD}$)/write ($\overline{WR}$) signals

The output terminals and output circuits for the read ($\overline{RD}$)/write ($\overline{WR}$) signals directed to external devices are shared respectively with output ports R23 and R24, switching between these functions being determined by the bus mode setting.
In the single chip mode, both of these terminals are set as output port terminals and in the other expanded modes, they are set as read ($\overline{RD}$)/write ($\overline{WR}$) signal output terminals. When set as read ($\overline{RD}$)/write ($\overline{WR}$) signal output terminal, the data register and high impedance control register for each output port (R23, R24) are detached from the output circuit and is usable as a general purpose data register with read/write capabilities.

These two signals are only output when the memory area of the external device is being accessed. They are not output when internal memory is accessed.
See Section 3.6.5, "WAIT control", for the output timing of the signal.

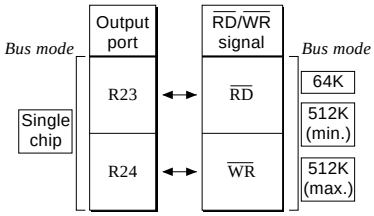


Fig. 3.6.3.1 Correspondence between read (RD)/write (WR) signal and output ports

3.6.4 Chip enable (CE) signal

The S1C88349 is equipped with address decoders which can output four different chip enable (CE) signals.
Consequently, four devices equipped with a chip enable (CE) or chip select (CS) terminal can be directly connected without setting the address decoder to an external device.

The four chip enable (CE0–CE3) signal output terminals and output circuits are shared with output ports R30–R33 and in modes other than the single chip mode, the selection of chip enable (CE) or output port can be set in software for each of the four bits. When set for chip enable (CE) output, the data register and high impedance control register for each output port are detached from the output circuit and is usable as general purpose data register with read / write capabilities.

In the single chip mode, these terminals are set as output ports R30–R33.

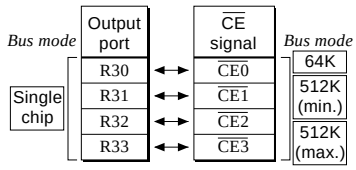


Fig. 3.6.4.1 Correspondence between CE signals and output ports

The address range assigned to the four chip enable (CE) signals is determined by the bus mode setting. In the expanded 64K mode, the four different address ranges which match the amount of memory in use can be selected in software.
Table 3.6.4.1 shows the address ranges which are assigned to the chip enable (CE) signal in each mode. When accessing the internal memory area, the CE signal is not output. Care should be taken here because the address range for these portions of memory involves irregular settings.
The arrangement of memory space for external devices does not necessarily have to be continuous from a subordinate address and any of the chip enable signals can be used to assign areas in memory.

Each of these signals is only output when the memory area of the external device is being accessed. They are not output when internal memory is accessed.

Note: The CE signals will be inactive status when the chip enters the standby mode (HALT mode or SLEEP mode).

See Section 3.6.5, "WAIT control", for the output timing of signal.

Table 3.6.4.1 CE0–CE3 address settings

(1) Expanded 64K mode (MPU mode only)

CE signal	Address range (selected in software)			
	8K bytes	16K bytes	32K bytes	64K bytes
CE0	000000H–001FFFH	000000H–003FFFH	000000H–007FFFH	000000H–00EFFFH
CE1	002000H–003FFFH	004000H–007FFFH	008000H–00EFFFH	–
CE2	004000H–005FFFH	008000H–00BFFFH	–	–
CE3	006000H–007FFFH	00C000H–00EFFFH	–	–

(2) Expanded 512K minimum/maximum modes

CE signal	Address range	
	MCU mode	MPU mode
CE0	200000H–27FFFFH	000000H–00EFFFH, 010000H–07FFFFH
CE1	080000H–0FFFFFH	080000H–0FFFFFH
CE2	100000H–17FFFFH	100000H–17FFFFH
CE3	180000H–1FFFFFH	180000H–1FFFFFH

3.6.5 WAIT control

In order to insure accessing of external low speed devices during high speed operations, the S1C88349 is equipped with a WAIT function which prolongs access time. (See the "S1C88 Core CPU Manual" for details of the WAIT function.)

The WAIT state numbers to be inserted can be selected in software from a series of 8 as shown in Table 3.6.5.1.

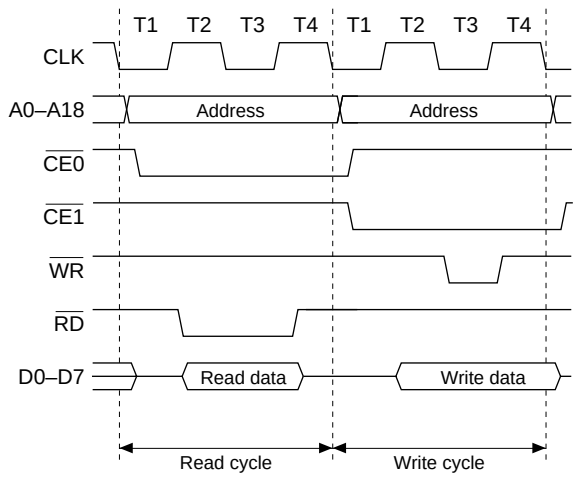
Table 3.6.5.1 Selectable WAIT state numbers

Selection No.	1	2	3	4	5	6	7	8
Insert states	0	2	4	6	8	10	12	14

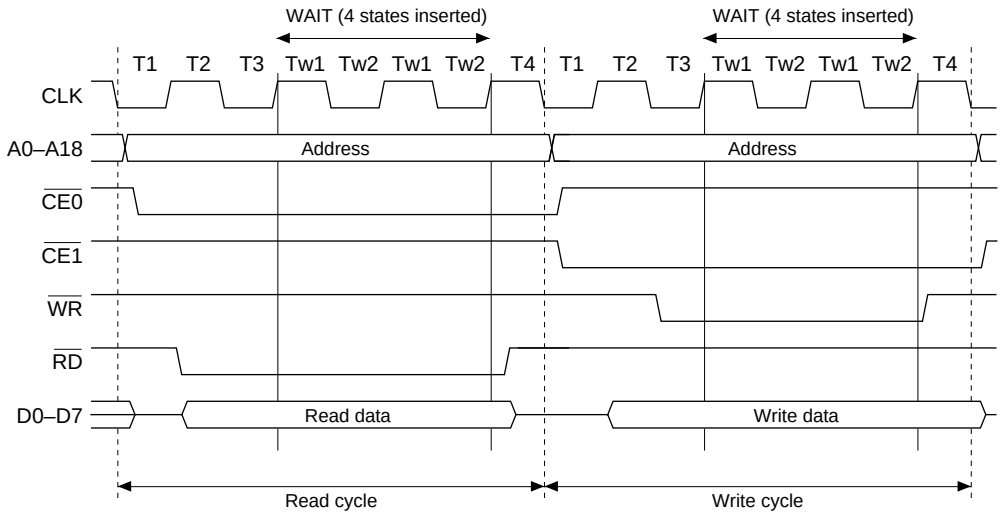
* One state is a 1/2 cycle of the clock in length.

The WAIT states set in software are inserted between bus cycle states T3–T4.
Note, however, that WAIT states cannot be inserted when an internal register and internal memory are being accessed and when operating with the OSC1 oscillation circuit (see "5.4 Oscillation Circuits and Operating Mode").
Consequently, WAIT state settings are meaningless in the single chip mode.

Figure 3.6.5.1 shows the memory read / write timing charts.



(1) No WAIT



(2) WAIT state insertion

Fig. 3.6.5.1 Memory read/write cycle

3.6.6 Bus authority release state

The S1C88349 is equipped with a bus authority release function on request from an external device so that DMA (Direct Memory Access) transfer can be conducted between external devices. The internal memory cannot be accessed by this function.

There are two terminals used for this function: the bus authority release request signal ($\overline{BREQ}$) input terminal and the bus authority release acknowledge signal ($\overline{BACK}$) output terminal.
The $\overline{BREQ}$ input terminal is shared with input port terminal K11 and the $\overline{BACK}$ output terminal with output port terminal R51, use with setting to $\overline{BREQ}$ / $\overline{BACK}$ terminals done in software. In the single chip mode, or when using a system which does not require bus authority release, set respective terminals as input and output ports.

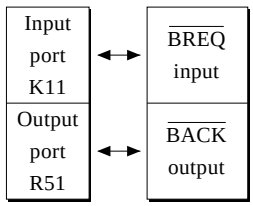


Fig. 3.6.6.1 $\overline{BREQ}$/$\overline{BACK}$ terminals

When the bus authority release request ($\overline{BREQ}$ = LOW) is received from an external device, the S1C88349 switches the address bus, data bus, $\overline{RD}$ / $\overline{WR}$ signal, and $\overline{CE}$ signal lines to a high impedance state, outputs a LOW level from the $\overline{BACK}$ terminal and releases bus authority.
As soon as a LOW level is output from the $\overline{BACK}$ terminal, the external device can use the external bus. When DMA is completed, the external device returns the $\overline{BREQ}$ terminal to HIGH and releases bus authority.
Figure 3.6.6.2 shows the bus authority release sequence.

During bus authority release state, internal memory cannot be accessed from the external device. In cases where external memory has areas which overlap areas in internal memory, the external memory areas can be accessed accordance with the $\overline{CE}$ signal output by the external device.

Note: Be careful with the system, such that an external device does not become the bus master, other than during the bus release status.
After setting the $\overline{BREQ}$ terminal to LOW level, hold the $\overline{BREQ}$ terminal at LOW level until the $\overline{BACK}$ terminal becomes LOW level. If the $\overline{BREQ}$ terminal is returned to HIGH level, before the $\overline{BACK}$ terminal becomes LOW level, the shift to the bus authorization release status will become indefinite.

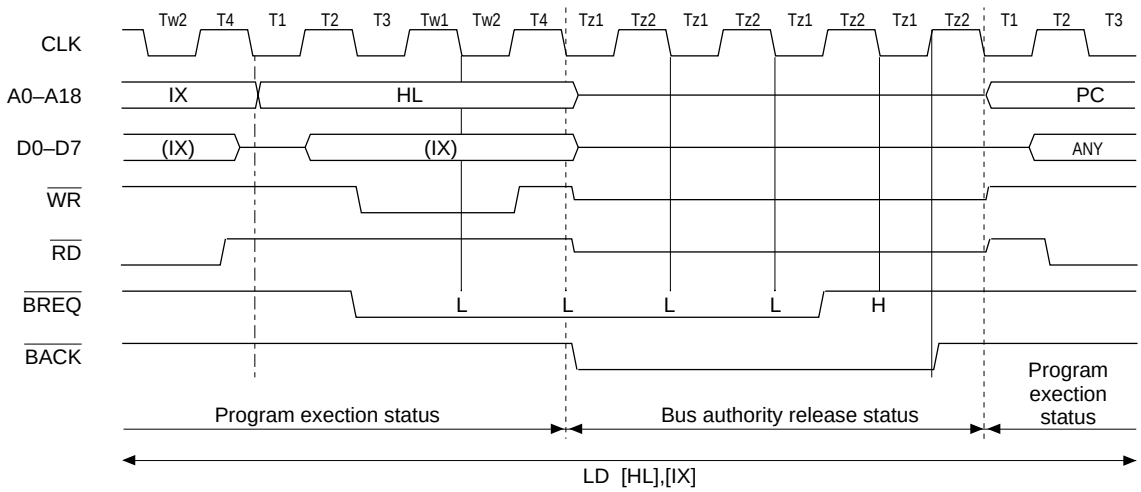


Fig. 3.6.6.2 Bus authority release sequence

4 INITIAL RESET

Initial reset in the S1C88349 is required in order to initialize circuits. This section of the Manual contains a description of initial reset factors and the initial settings for internal registers, etc.

4.1 Initial Reset Factors

There are three initial reset factors for the S1C88349 as shown below.

(1) $\overline{\text{RESET}}$ terminal
(2) Simultaneous LOW level input at input port terminals K00–K03
(3) Supply voltage detection (SVD) circuit

Figure 4.1.1 shows the configuration of the initial reset circuit.

The CPU and peripheral circuits are initialized by means of initial reset factors. When the factor is canceled, the CPU commences reset exception processing. (See "S1C88 Core CPU Manual".)

When this occurs, reset exception processing vectors, Bank 0, 000000H–000001H from program memory are read out and the program (initialization routine) which begins at the readout address is executed.

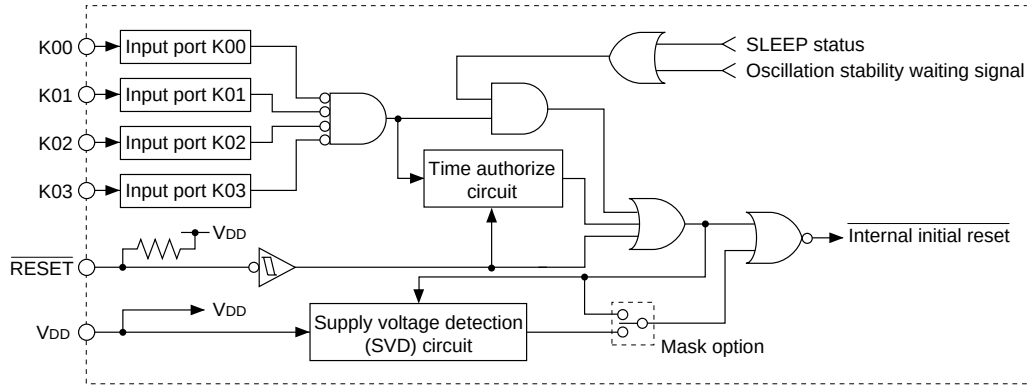


Fig. 4.1.1 Configuration of initial reset circuit

4.1.1 $\overline{\text{RESET}}$ terminal

Initial reset can be done by executed externally inputting a LOW level to the $\overline{\text{RESET}}$ terminal.
Be sure to maintain the $\overline{\text{RESET}}$ terminal at LOW level for the regulation time after the power on to assure the initial reset.
In addition, be sure to use the $\overline{\text{RESET}}$ terminal for the first initial reset after the power is turned on.
The $\overline{\text{RESET}}$ terminal is equipped with a pull-up resistor. You can select whether or not to use by mask option.

4.1.2 Simultaneous LOW level input at input port terminals K00–K03

Another way of executing initial reset externally is to input a LOW level simultaneously to the input ports (K00–K03) selected by mask option.
Since there is a built-in time authorize circuit, be sure to maintain the designated input port terminal at LOW level for two seconds (when the oscillation frequency is f_{OSC1} = 32.768 kHz) or more to perform the initial reset by means of this function.

However, the time authorize circuit is bypassed during the SLEEP (standby) status and oscillation stabilization waiting period, and initial reset is executed immediately after the simultaneous LOW level input to the designated input ports.
The combination of input ports (K00–K03) that can be selected by mask option are as follows:

Multiple key entry reset
- ☐ Not use
- ☐ K00 & K01
- ☐ K00 & K01 & K02
- ☐ K00 & K01 & K02 & K03

For instance, let's say that mask option "K00 & K01 & K02 & K03" is selected.
When the input level at input ports K00–K03 is simultaneously LOW, initial reset will take place.

When using this function, make sure that the designated input ports do not simultaneously switch to LOW level while the system is in normal operation.

4.1.3 Supply voltage detection (SVD) circuit

When the SVD circuit detects that supply voltage has dropped below level 0 four successive times (see Chapter 8, "ELECTRICAL CHARACTERISTICS"), it outputs an initial reset signal until the supply voltage has been restored to level 2.
You can select whether or not to use this SVD initial reset function by mask option.
For more information, see "5.16 Supply Voltage Detection (SVD) Circuit" in this Manual.

Note: The supply voltage must be at least level 2 for the first sampling of the SVD circuit after an initial reset regardless of the mask option selected. At this time, if the power voltage level is less than level 2, the SVD circuit will continue sampling until the supply voltage reaches level 2 or more.

4.1.4 Initial reset sequence

After cancellation of the LOW level input to the $\overline{\text{RESET}}$ terminal, when the power is turned on, the start-up of the CPU is held back until the oscillation stabilization waiting time (8,192 / f_{OSC1} sec.) and the SVD initial sampling time (248 / f_{OSC1} sec.) have elapsed.
Figure 4.1.4.1 shows the operating sequence following initial reset release.

Also, when using the initial reset by simultaneous LOW level input into the input port, you should be careful of the following points.

(1) During SLEEP status, since the time authorization circuit is bypassed, an initial reset is triggered immediately after a LOW level simultaneous input value. In this case, the CPU starts after waiting the oscillation stabilization time and the SVD circuit initial sampling time, following cancellation of the LOW level simultaneous input.

(2) Other than during SLEEP status, an initial reset will be triggered 1–2 seconds after a LOW level simultaneous input. In this case, since a reset differential pulse (64 / f_{OSC1} sec.) is generated within the S1C88349, the CPU will start even if the LOW level simultaneous input status is not canceled.

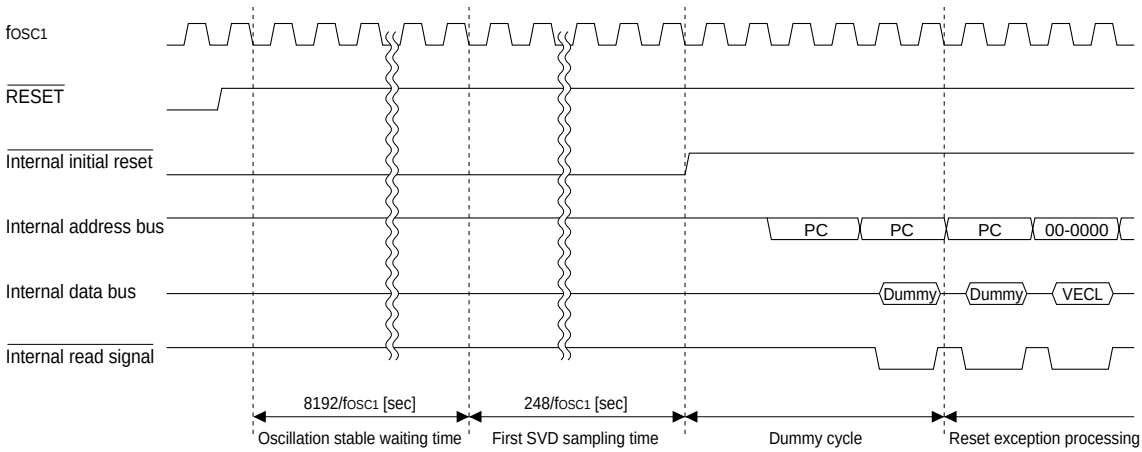


Fig. 4.1.4.1 Initial reset sequence

4.2 Initial Settings After Initial Reset

The CPU internal registers are initialized as follows during initial reset.

Table 4.2.1 Initial settings

Register name	Code	Bit length	Setting value
Data register A	A	8	Undefined
Data register B	B	8	Undefined
Index (data) register L	L	8	Undefined
Index (data) register H	H	8	Undefined
Index register IX	IX	16	Undefined
Index register IY	IY	16	Undefined
Program counter	PC	16	Undefined*
Stack pointer	SP	16	Undefined
Base register	BR	8	Undefined
Zero flag	Z	1	0
Carry flag	C	1	0
Overflow flag	V	1	0
Negative flag	N	1	0
Decimal flag	D	1	0
Unpack flag	U	1	0
Interrupt flag 0	I0	1	1
Interrupt flag 1	I1	1	1
New code bank register	NB	8	01H
Code bank register	CB	8	Undefined*
Expand page register	EP	8	00H
Expand page register for IX	XP	8	00H
Expand page register for IY	YP	8	00H

* Reset exception processing loads the preset values stored in 0 bank, 0000H–0001H into the PC. At the same time, 01H of the NB initial value is loaded into CB.

Initialize the registers which are not initialized at initial reset using software.

Since the internal RAM and display memory are not initialized at initial reset, be sure to initialize using software.

The respectively stipulated initializations are done for internal peripheral circuits. If necessary, the initialization should be done using software.
For initial value at initial reset, see the sections on the I/O memory map and peripheral circuit descriptions in the following chapter of this Manual.

5 PERIPHERAL CIRCUITS AND THEIR OPERATION

The peripheral circuits of the S1C88349 is interfaced with the CPU by means of the memory mapped I/O method. For this reason, just as with other memory access operations, peripheral circuits can be controlled by manipulating I/O memory. Below is a description of the operation and control method for each individual peripheral circuit.

5.1 I/O Memory Map

Table 5.1.1(a) I/O Memory map (00FF00H–00FF02H, MCU mode)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF00 (MCU)	D7	BSMD1	Bus mode (CPU mode) BSMD1 BSMD0 Mode 1 1 512K (Maximum) 1 0 512K (Minimum) 0 1 × 0 0 Single chip			0	R/W	Do not set BSMD1–0 to 01B.
	D6	BSMD0				0	R/W	
	D5	CEMD1	R/W register			1	R/W	
	D4	CEMD0	R/W register			1	R/W	
	D3	CE3	$\overline{CE3}$ (R33)	$\overline{CE3}$ enable	$\overline{CE3}$ disable	0	R/W	In the Single chip mode, these setting are fixed at DC output.
	D2	CE2	$\overline{CE2}$ (R32)	$\overline{CE2}$ enable	$\overline{CE2}$ disable	0	R/W	
	D1	CE1	$\overline{CE1}$ (R31)	$\overline{CE1}$ enable	$\overline{CE1}$ disable	0	R/W	
	D0	CE0	$\overline{CE0}$ (R30) $\overline{CE}$ signal output Enable/Disable Enable: $\overline{CE}$ signal output Disable: DC (R3x) output	$\overline{CE0}$ enable	$\overline{CE0}$ disable	0	R/W	
00FF01	D7	SPP7	Stack pointer page address (MSB)	1	0	0	R/W	
	D6	SPP6		1	0	0	R/W	
	D5	SPP5	< SP page allocatable address >	1	0	0	R/W	
	D4	SPP4	• Single chip mode: only 0 page	1	0	0	R/W	
	D3	SPP3	• 64K mode: only 0 page	1	0	0	R/W	
	D2	SPP2	• 512K (min) mode: 0–27H page	1	0	0	R/W	
	D1	SPP1	• 512K (max) mode: 0–27H page	1	0	0	R/W	
	D0	SPP0	(LSB)	1	0	0	R/W	
00FF02	D7	EBR	Bus release enable register (K11 and R51 terminal specification) K11 R51	$\overline{BREQ}$ $\overline{BACK}$	Input port Output port	0	R/W	
	D6	WT2	Wait control register WT2 WT1 WT0 Number of state 1 1 1 14 1 1 0 12 1 0 1 10 1 0 0 8 0 1 1 6 0 1 0 4 0 0 1 2 0 0 0 No wait			0	R/W	
	D5	WT1				0	R/W	
	D4	WT0				0	R/W	
	D3	CLKCHG	CPU operating clock switch	OSC3	OSC1	0	R/W	
	D2	OSCC	OSC3 oscillation On/Off control	On	Off	0	R/W	
	D1	VDC1	Operating mode selection VDC1 VDC0 Operating mode 1 × High speed (V_{D1}=3.3V) 0 1 Low power (V_{D1}=1.2V) 0 0 Normal (V_{D1}=2.2V)			0	R/W	
	D0	VDC0				0	R/W	

Note: All the interrupts including $\overline{NMI}$ are disabled, until you write the optional value into both the "00FF00H" and "00FF01H" addresses.

Table 5.1.1(b) I/O Memory map (00FF00H–00FF02H, MPU mode)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF00 (MPU)	D7	BSMD1	Bus mode (CPU mode) BSMD1 BSMD0 Mode 1 1 512K (Maximum) 1 0 512K (Minimum) 0 1 64K 0 0 * Option selection ◀			*	R/W	* Initial setting can be selected among 3 types (64K, 512K min and 512K max) by mask option setting.
	D6	BSMD0				*	R/W	
	D5	CEMD1	Chip enable mode CEMD1 CEMD0 Mode 1 1 64K ($\overline{CE0}$) 1 0 32K ($\overline{CE0}$, $\overline{CE1}$) 0 1 16K ($\overline{CE0}$–$\overline{CE3}$) 0 0 8K ($\overline{CE0}$–$\overline{CE3}$)			1	R/W	Only for 64K bus mode
	D4	CEMD0				1	R/W	
	D3	CE3	$\overline{CE3}$ (R33) $\overline{CE}$ signal output Enable/Disable Enable: $\overline{CE}$ signal output Disable: DC (R3x) output	$\overline{CE3}$ enable	$\overline{CE3}$ disable	0	R/W	
	D2	CE2	$\overline{CE2}$ (R32)	$\overline{CE2}$ enable	$\overline{CE2}$ disable	0	R/W	
	D1	CE1	$\overline{CE1}$ (R31)	$\overline{CE1}$ enable	$\overline{CE1}$ disable	0	R/W	
	D0	CE0	$\overline{CE0}$ (R30)	$\overline{CE0}$ enable	$\overline{CE0}$ disable	1	R/W	
00FF01	D7	SPP7	Stack pointer page address (MSB)	1	0	0	R/W	
	D6	SPP6		1	0	0	R/W	
	D5	SPP5	< SP page allocatable address >	1	0	0	R/W	
	D4	SPP4	• Single chip mode: only 0 page	1	0	0	R/W	
	D3	SPP3	• 64K mode: only 0 page	1	0	0	R/W	
	D2	SPP2	• 512K (min) mode: 0–27H page	1	0	0	R/W	
	D1	SPP1	• 512K (max) mode: 0–27H page	1	0	0	R/W	
	D0	SPP0	(LSB)	1	0	0	R/W	
00FF02	D7	EBR	Bus release enable register (K11 and R51 terminal specification) K11 R51	$\overline{BREQ}$ $\overline{BACK}$	Input port Output port	0	R/W	
	D6	WT2	Wait control register WT2 WT1 WT0 Number of state 1 1 1 14 1 1 0 12 1 0 1 10 1 0 0 8 0 1 1 6 0 1 0 4 0 0 1 2 0 0 0 No wait			0	R/W	
	D5	WT1				0	R/W	
	D4	WT0				0	R/W	
	D3	CLKCHG	CPU operating clock switch	OSC3	OSC1	0	R/W	
	D2	OSCC	OSC3 oscillation On/Off control	On	Off	0	R/W	
	D1	VDC1	Operating mode selection VDC1 VDC0 Operating mode 1 × High speed (V_{D1}=3.3V) 0 1 Low power (V_{D1}=1.2V) 0 0 Normal (V_{D1}=2.2V)			0	R/W	
	D0	VDC0				0	R/W	

Note: All the interrupts including $\overline{NMI}$ are disabled, until you write the optional value into both the "00FF00H" and "00FF01H" addresses.

Table 5.1.1(c) I/O Memory map (00FF09H–00FF13H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF09	D7	–	–	–	–	–		
	D6	–	–	–	–	–		Constantry "0" when
	D5	–	–	–	–	–		being read
	D4	–	–	–	–	–		
	D3	VCCHG	Reserved	1	0	0	R/W	
	D2	LCDB	Reserved	1	0	0	R/W	
	D1	LCDAJ	Power TYPE A (4.5V)/B (5.5V) switch	TYPE A	TYPE B	0	R/W	
	D0	DUTY8	LCD drive duty switch	1/8 duty	1/16, 1/32	0	R/W	*1
00FF10	D7	–	–	–	–	–		Constantry "0" when
	D6	–	–	–	–	–		being read
	D5	–	–	–	–	–		
	D4	LCCLK	CL output control for expanded LCD driver	On	Off	0	R/W	
	D3	LCFRM	FR output control for expanded LCD driver	On	Off	0	R/W	
	D2	DTFNT	LCD dot font selection	5 x 5 dots	5 x 8 dots	0	R/W	
	D1	LDUTY	LCD drive duty selection	1/16 duty	1/32 duty	0	R/W	*1
	D0	SGOUT	R/W register	1	0	0	R/W	Reserved register
00FF11	D7	–	–	–	–	–		"0" when being read
	D6	DSPAR	LCD display memory area selection	Display area 1	Display area 0	0	R/W	
	D5	LCDC1	LCD display control LCDC1 LCDC0 LCD display 1 1 All LCDs lit 1 0 All LCDs out 0 1 Normal display 0 0 Drive off			0	R/W	These bits are reset to (0, 0) when SLP instruction is executed.
	D4	LCDC0				0	R/W	
	D3	LC3	LCD contrast adjustment LC3 LC2 LC1 LC0 Contrast 1 1 1 1 Dark 1 1 1 0 : : : : : : 0 0 0 0 Light			0	R/W	
	D2	LC2				0	R/W	
	D1	LC1				0	R/W	
	D0	LC0				0	R/W	
00FF12	D7	–	–	–	–	–		Constantry "0" when
	D6	–	–	–	–	–		being read
	D5	SVDSP	SVD auto-sampling control	On	Off	0	R/W	These registers are reset to "0" when
	D4	SVDON	SVD continuous sampling control/status R	Busy	Ready	1→0*2	R/W	SLP instruction is executed.
			W	On	Off	0		
	D3	SVD3	SVD detection level SVD3 SVD2 SVD1 SVD0 Detection level 1 1 1 1 Level 15 1 1 1 0 Level 14 : : : : : 0 0 0 0 Level 0			X	R	*3
	D2	SVD2				X	R	
	D1	SVD1				X	R	
	D0	SVD0				X	R	
00FF13	D7	–	–	–	–	–		Constantly "0" when
	D6	–	–	–	–	–		being read
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	CMP1ON	Comparator 1 On/Off control	On	Off	0	R/W	
	D2	CMP0ON	Comparator 0 On/Off control	On	Off	0	R/W	
	D1	CMP1DT	Comparator 1 data	+ > -	+ < -	0	R	
	D0	CMP0DT	Comparator 0 data	+ > -	+ < -	0	R	

*1 Writing "1" to DUTY8 (FF09•D0) disables 1/16 and 1/32 duty selection using LDUTY (FF10•D1).
*2 After initial reset, this status is set "1" until conclusion of hardware first sampling.
*3 Initial value is set according to the supply voltage detected at first hardware sampling after an initial reset.
Until conclusion of first sampling, SVD0–SVD3 data are undefined.

Table 5.1.1(d) I/O Memory map (00FF20H–00FF25H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF20	D7	PK01	K00–K07 interrupt priority register	PK01 PK00 PSIF1 PSIF0 PSW1 PSW0 Priority PTM1 PTM0 level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PK00						
	D5	PSIF1	Serial interface interrupt priority register			0	R/W	
	D4	PSIF0						
	D3	PSW1	Stopwatch timer interrupt priority register			0	R/W	
	D2	PSW0						
	D1	PTM1	Clock timer interrupt priority register			0	R/W	
	D0	PTM0						
00FF21	D7	–	–	–	–	–		
	D6	–	–	–	–	–		Constantly "0" when being read
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	PPT1	Programmable timer interrupt priority register	PPT1 PPT0 Priority PK11 PK10 level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D2	PPT0						
	D1	PK11	K10 and K11 interrupt priority register			0	R/W	
	D0	PK10						
00FF22	D7	–	–	–	–	–		"0" when being read
	D6	ESW100	Stopwatch timer 100 Hz interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D5	ESW10	Stopwatch timer 10 Hz interrupt enable register					
	D4	ESW1	Stopwatch timer 1 Hz interrupt enable register					
	D3	ETM32	Clock timer 32 Hz interrupt enable register					
	D2	ETM8	Clock timer 8 Hz interrupt enable register					
	D1	ETM2	Clock timer 2 Hz interrupt enable register					
	D0	ETM1	Clock timer 1 Hz interrupt enable register					
00FF23	D7	EPT1	Programmable timer 1 interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D6	EPT0	Programmable timer 0 interrupt enable register					
	D5	EK1	K10 and K11 interrupt enable register					
	D4	EK0H	K04–K07 interrupt enable register					
	D3	EK0L	K00–K03 interrupt enable register					
	D2	ESERR	Serial I/F (error) interrupt enable register					
	D1	ESREC	Serial I/F (receiving) interrupt enable register					
	D0	ESTRA	Serial I/F (transmitting) interrupt enable register					
00FF24	D7	–	–	–	–	–		"0" when being read
	D6	FSW100	Stopwatch timer 100 Hz interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D5	FSW10	Stopwatch timer 10 Hz interrupt factor flag					
	D4	FSW1	Stopwatch timer 1 Hz interrupt factor flag					
	D3	FTM32	Clock timer 32 Hz interrupt factor flag					
	D2	FTM8	Clock timer 8 Hz interrupt factor flag					
	D1	FTM2	Clock timer 2 Hz interrupt factor flag					
	D0	FTM1	Clock timer 1 Hz interrupt factor flag					
00FF25	D7	FPT1	Programmable timer 1 interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D6	FPT0	Programmable timer 0 interrupt factor flag					
	D5	FK1	K10 and K11 interrupt factor flag					
	D4	FK0H	K04–K07 interrupt factor flag					
	D3	FK0L	K00–K03 interrupt factor flag					
	D2	FSERR	Serial I/F (error) interrupt factor flag					
	D1	FSREC	Serial I/F (receiving) interrupt factor flag					
	D0	FSTRA	Serial I/F (transmitting) interrupt factor flag					

Table 5.1.1(e) I/O Memory map (00FF28H–00FF31H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF28	D7	PADC1	A/D converter interrupt priority register	PADC1 PADC0 Priority 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PADC0				0	R/W	
	D5	–	Reserved	Prohibited	–	0		Do not write "1".
	D4	–	Reserved	Prohibited	–	0		
	D3	–	–	–	–	–		Constantly "0" when being read
	D2	–	–	–	–	–		
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		
00FF2A	D7	EAD	A/D converter interrupt enable register	Enable	Disable	0	R/W	
	D6	–	Reserved	–	–	0	R/W	
	D5	–	–	–	–	–		Constantly "0" when being read
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		
00FF2C	D7	FAD	A/D converter interrupt factor flag R) W)	Generated Reset	Not generated No operation	0	R/W	
	D6	–	Reserved	–	–	0	R/W	
	D5	–	–	–	–	–		Constantly "0" when being read
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		
00FF30	D7	–	–	–	–	–		Constantry "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	MODE16	8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D3	CHSEL	TOUT output channel selection	Timer 1	Timer 0	0	R/W	
	D2	PTOUT	TOUT output control	On	Off	0	R/W	
	D1	CKSEL1	Prescaler 1 source clock selection	f_{OSC3}	f_{OSC1}	0	R/W	
	D0	CKSEL0	Prescaler 0 source clock selection	f_{OSC3}	f_{OSC1}	0	R/W	
00FF31	D7	EVCNT	Timer 0 counter mode selection	Event counter	Timer	0	R/W	
	D6	FCSEL	Timer 0 function selection: In timer mode	Pulse width measurement	Normal mode	0	R/W	
			Timer 0 function selection: In event counter mode	With noise rejector	Without noise rejector			
	D5	PLPOL	Timer 0 pulse polarity selection: Down count timing in event counter mode	Rising edge of K10 input	Falling edge of K10 input	0	R/W	
			Timer 0 pulse polarity selection: In pulse width measurement mode	High level measurement for K10 input	Low level measurement for K10 input			
	D4	PSC01	Timer 0 prescaler dividing ratio selection PSC01 PSC00 Prescaler dividing ratio 1 1 Source clock / 64			0	R/W	
	D3	PSC00	1 0 Source clock / 16 0 1 Source clock / 4 0 0 Source clock / 1			0	R/W	
	D2	CONT0	Timer 0 continuous/one-shot mode selection	Continuous	One-shot	0	R/W	
	D1	PSET0	Timer 0 preset	Preset	No operation	–	W	"0" when being read
	D0	PRUN0	Timer 0 Run/Stop control	Run	Stop	0	R/W	

Table 5.1.1(f) I/O Memory map (00FF32H–00FF36H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF32	D7	–	–	–	–	–		Constantry "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	PSC11	Timer 1 prescaler dividing ratio selection PSC11 PSC10 Prescaler dividing ratio 1 1 Source clock / 64 1 0 Source clock / 16 0 1 Source clock / 4 0 0 Source clock / 1			0	R/W	
	D3	PSC10				0	R/W	
	D2	CONT1	Timer 1 continuous/one-shot mode selection	Continuous	One-shot	0	R/W	
	D1	PSET1	Timer 1 preset	Preset	No operation	–	W	"0" when being read
	D0	PRUN1	Timer 1 Run/Stop control	Run	Stop	0	R/W	
00FF33	D7	RLD07	Timer 0 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RLD06	Timer 0 reload data D6					
	D5	RLD05	Timer 0 reload data D5					
	D4	RLD04	Timer 0 reload data D4					
	D3	RLD03	Timer 0 reload data D3					
	D2	RLD02	Timer 0 reload data D2					
	D1	RLD01	Timer 0 reload data D1					
	D0	RLD00	Timer 0 reload data D0 (LSB)					
00FF34	D7	RLD17	Timer 1 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RLD16	Timer 1 reload data D6					
	D5	RLD15	Timer 1 reload data D5					
	D4	RLD14	Timer 1 reload data D4					
	D3	RLD13	Timer 1 reload data D3					
	D2	RLD12	Timer 1 reload data D2					
	D1	RLD11	Timer 1 reload data D1					
	D0	RLD10	Timer 1 reload data D0 (LSB)					
00FF35	D7	PTD07	Timer 0 counter data D7 (MSB)	High	Low	1	R	
	D6	PTD06	Timer 0 counter data D6					
	D5	PTD05	Timer 0 counter data D5					
	D4	PTD04	Timer 0 counter data D4					
	D3	PTD03	Timer 0 counter data D3					
	D2	PTD02	Timer 0 counter data D2					
	D1	PTD01	Timer 0 counter data D1					
	D0	PTD00	Timer 0 counter data D0 (LSB)					
00FF36	D7	PTD17	Timer 1 counter data D7 (MSB)	High	Low	1	R	
	D6	PTD16	Timer 1 counter data D6					
	D5	PTD15	Timer 1 counter data D5					
	D4	PTD14	Timer 1 counter data D4					
	D3	PTD13	Timer 1 counter data D3					
	D2	PTD12	Timer 1 counter data D2					
	D1	PTD11	Timer 1 counter data D1					
	D0	PTD10	Timer 1 counter data D0 (LSB)					

Table 5.1.1(g) I/O Memory map (00FF40H–00FF44H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF40	D7	–	–	–	–	–		"0" when being read
	D6	FOUT2	FOUT frequency selection FOUT2 FOUT1 FOUT0 Frequency 0 0 0 fOSC1 / 1 0 0 1 fOSC1 / 2 0 1 0 fOSC1 / 4 0 1 1 fOSC1 / 8 1 0 0 fOSC3 / 1 1 0 1 fOSC3 / 2 1 1 0 fOSC3 / 4 1 1 1 fOSC3 / 8			0	R/W	
	D5	FOUT1				0	R/W	
	D4	FOUT0				0	R/W	
	D3	FOUTON	FOUT output control	On	Off	0	R/W	
	D2	WDRST	Watchdog timer reset	Reset	No operation	–	W	Constantly "0" when
	D1	TMRST	Clock timer reset	Reset	No operation	–	W	being read
	D0	TMRUN	Clock timer Run/Stop control	Run	Stop	0	R/W	
00FF41	D7	TMD7	Clock timer data 1 Hz	High	Low	0	R	
	D6	TMD6	Clock timer data 2 Hz					
	D5	TMD5	Clock timer data 4 Hz					
	D4	TMD4	Clock timer data 8 Hz					
	D3	TMD3	Clock timer data 16 Hz					
	D2	TMD2	Clock timer data 32 Hz					
	D1	TMD1	Clock timer data 64 Hz					
	D0	TMD0	Clock timer data 128 Hz					
00FF42	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	SWRST	Stopwatch timer reset	Reset	No operation	–	W	
	D0	SWRUN	Stopwatch timer Run/Stop control	Run	Stop	0	R/W	
00FF43	D7	SWD7	Stopwatch timer data			0	R	
	D6	SWD6						
	D5	SWD5	BCD (1/10 sec)					
	D4	SWD4						
	D3	SWD3	Stopwatch timer data					
	D2	SWD2						
	D1	SWD1	BCD (1/100 sec)					
	D0	SWD0						
00FF44	D7	–	–	–	–	–		Constantry "0" when
	D6	BZSTP	One-shot buzzer forcibly stop	Forcibly stop	No operation	–	W	being read
	D5	BZSHT	One-shot buzzer trigger/status R	Busy	Ready	0	R/W	
			W	Trigger	No operation			
	D4	SHTPW	One-shot buzzer duration width selection	125 msec	31.25 msec	0	R/W	
	D3	ENRTM	Envelope attenuation time	1 sec	0.5 sec	0	R/W	
	D2	ENRST	Envelope reset	Reset	No operation	–	W	"0" when being read
	D1	ENON	Envelope On/Off control	On	Off	0	R/W	*1
	D0	BZON	Buzzer output control	On	Off	0	R/W	

*1 Reset to "0" during one-shot output.

Table 5.1.1(h) I/O Memory map (00FF45H–00FF49H)

Address	Bit	Name	Function		1	0	SR	R/W	Comment
00FF45	D7	–	–		–	–	–		"0" when being read
	D6	DUTY2	Buzzer signal duty ratio selection				0	R/W	
	D5	DUTY1	DUTY2–1 (2 1 0) / Buzzer frequency (Hz): 4096.0 2048.0 / 3276.8 1638.4 / 2730.7 1365.3 / 2340.6 1170.3				0	R/W	
	D4	DUTY0	0 0 0: 8/16 8/20 12/24 12/28 0 0 1: 7/16 7/20 11/24 11/28 0 1 0: 6/16 6/20 10/24 10/28 0 1 1: 5/16 5/20 9/24 9/28 1 0 0: 4/16 4/20 8/24 8/28 1 0 1: 3/16 3/20 7/24 7/28 1 1 0: 2/16 2/20 6/24 6/28 1 1 1: 1/16 1/20 5/24 5/28				0	R/W	
	D3	–	–		–	–	–		"0" when being read
	D2	BZFQ2	Buzzer frequency selection				0	R/W	
	D1	BZFQ1	BZFQ2 BZFQ1 BZFQ0 Frequency (Hz): 0 0 0 4096.0 0 0 1 3276.8 0 1 0 2730.7 0 1 1 2340.6 1 0 0 2048.0 1 0 1 1638.4 1 1 0 1365.3 1 1 1 1170.3				0	R/W	
	D0	BZFQ0					0	R/W	
00FF48	D7	–	–		–	–	–		"0" when being read
	D6	EPR	Parity enable register		With parity	Non parity	0	R/W	Only for
	D5	PMD	Parity mode selection		Odd	Even	0	R/W	asynchronous mode
	D4	SCS1	Clock source selection				0	R/W	
	D3	SCS0	SCS1 SCS0 Clock source: 1 1 Programmable timer 1 0 f_{OSC3} / 4 0 1 f_{OSC3} / 8 0 0 f_{OSC3} / 16				0	R/W	In the clock synchronous slave mode, external clock is selected.
	D2	SMD1	Serial I/F mode selection				0	R/W	
	D1	SMD0	SMD1 SMD0 Mode: 1 1 Asynchronous 8-bit 1 0 Asynchronous 7-bit 0 1 Clock synchronous slave 0 0 Clock synchronous master				0	R/W	
	D0	ESIF	Serial I/F enable register		Serial I/F	I/O port	0	R/W	
00FF49	D7	–	–		–	–	–		"0" when being read
	D6	FER	Framing error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D5	PER	Parity error flag	R	Error	No error	0	R/W	Only for
				W	Reset (0)	No operation			asynchronous mode
	D4	OER	Overrun error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D3	RXTRG	Receive trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D2	RXEN	Receive enable		Enable	Disable	0	R/W	
	D1	TXTRG	Transmit trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D0	TXEN	Transmit enable		Enable	Disable	0	R/W	

Table 5.1.1(i) I/O Memory map (00FF4AH–00FF54H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF4A	D7	TRXD7	Transmit/Receive data D7 (MSB)	High	Low	X	R/W	
	D6	TRXD6	Transmit/Receive data D6					
	D5	TRXD5	Transmit/Receive data D5					
	D4	TRXD4	Transmit/Receive data D4					
	D3	TRXD3	Transmit/Receive data D3					
	D2	TRXD2	Transmit/Receive data D2					
	D1	TRXD1	Transmit/Receive data D1					
	D0	TRXD0	Transmit/Receive data D0 (LSB)					
00FF50	D7	SIK07	K07 interrupt selection register	Interrupt enable	Interrupt disable	0	R/W	
	D6	SIK06	K06 interrupt selection register					
	D5	SIK05	K05 interrupt selection register					
	D4	SIK04	K04 interrupt selection register					
	D3	SIK03	K03 interrupt selection register					
	D2	SIK02	K02 interrupt selection register					
	D1	SIK01	K01 interrupt selection register					
	D0	SIK00	K00 interrupt selection register					
00FF51	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	SIK11	K11 interrupt selection register	Interrupt enable	Interrupt disable	0	R/W	
	D0	SIK10	K10 interrupt selection register					
00FF52	D7	KCP07	K07 interrupt comparison register	Interrupt generated at falling edge	Interrupt generated at rising edge	1	R/W	
	D6	KCP06	K06 interrupt comparison register					
	D5	KCP05	K05 interrupt comparison register					
	D4	KCP04	K04 interrupt comparison register					
	D3	KCP03	K03 interrupt comparison register					
	D2	KCP02	K02 interrupt comparison register					
	D1	KCP01	K01 interrupt comparison register					
	D0	KCP00	K00 interrupt comparison register					
00FF53	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	KCP11	K11 interrupt comparison register	Falling edge	Rising edge	1	R/W	
	D0	KCP10	K10 interrupt comparison register					
00FF54	D7	K07D	K07 input port data	High level input	Low level input	–	R	
	D6	K06D	K06 input port data					
	D5	K05D	K05 input port data					
	D4	K04D	K04 input port data					
	D3	K03D	K03 input port data					
	D2	K02D	K02 input port data					
	D1	K01D	K01 input port data					
	D0	K00D	K00 input port data					

Table 5.1.1(j) I/O Memory map (00FF55H–00FF70H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF55	D7	–	–	–	–	–		
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		Constantly "0" when
	D4	–	–	–	–	–		being read
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	K11D	K11 input port data	High level	Low level	–	R	
	D0	K10D	K10 input port data	input	input			
00FF60	D7	IOC07	P07 I/O control register					
	D6	IOC06	P06 I/O control register					
	D5	IOC05	P05 I/O control register					
	D4	IOC04	P04 I/O control register					
	D3	IOC03	P03 I/O control register	Output	Input	0	R/W	
	D2	IOC02	P02 I/O control register					
	D1	IOC01	P01 I/O control register					
	D0	IOC00	P00 I/O control register					
00FF61	D7	IOC17	P17 I/O control register					
	D6	IOC16	P16 I/O control register					
	D5	IOC15	P15 I/O control register					
	D4	IOC14	P14 I/O control register					
	D3	IOC13	P13 I/O control register	Output	Input	0	R/W	
	D2	IOC12	P12 I/O control register					
	D1	IOC11	P11 I/O control register					
	D0	IOC10	P10 I/O control register					
00FF62	D7	P07D	P07 I/O port data					
	D6	P06D	P06 I/O port data					
	D5	P05D	P05 I/O port data					
	D4	P04D	P04 I/O port data					
	D3	P03D	P03 I/O port data	High	Low	1	R/W	
	D2	P02D	P02 I/O port data					
	D1	P01D	P01 I/O port data					
	D0	P00D	P00 I/O port data					
00FF63	D7	P17D	P17 I/O port data					
	D6	P16D	P16 I/O port data					
	D5	P15D	P15 I/O port data					
	D4	P14D	P14 I/O port data					
	D3	P13D	P13 I/O port data	High	Low	1	R/W	
	D2	P12D	P12 I/O port data					
	D1	P11D	P11 I/O port data					
	D0	P10D	P10 I/O port data					
00FF70	D7	HZR51	R51 high impedance control	High	Comple-	0	R/W	
	D6	HZR50	R50 high impedance control	impedance	mentary			
	D5	HZR4H	R/W register	1	0	0	R/W	Reserved register
	D4	HZR4L	R/W register					
	D3	HZR1H	R14–R17 high impedance control					
	D2	HZR1L	R10–R13 high impedance control	High	Comple-	0	R/W	
	D1	HZR0H	R04–R07 high impedance control	impedance	mentary			
	D0	HZR0L	R00–R03 high impedance control					

Table 5.1.1(k) I/O Memory map (00FF71H–00FF76H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF71	D7	HZR27	R27 high impedance control	High impedance	Complementary	0	R/W	
	D6	HZR26	R26 high impedance control					
	D5	HZR25	R25 high impedance control					
	D4	HZR24	R24 high impedance control					
	D3	HZR23	R23 high impedance control					
	D2	HZR22	R22 high impedance control					
	D1	HZR21	R21 high impedance control					
	D0	HZR20	R20 high impedance control					
00FF72	D7	HZR37	R37 high impedance control	High impedance	Complementary	0	R/W	
	D6	HZR36	R36 high impedance control					
	D5	HZR35	R35 high impedance control					
	D4	HZR34	R34 high impedance control					
	D3	HZR33	R33 high impedance control					
	D2	HZR32	R32 high impedance control					
	D1	HZR31	R31 high impedance control					
	D0	HZR30	R30 high impedance control					
00FF73	D7	R07D	R07 output port data	High	Low	1	R/W	
	D6	R06D	R06 output port data					
	D5	R05D	R05 output port data					
	D4	R04D	R04 output port data					
	D3	R03D	R03 output port data					
	D2	R02D	R02 output port data					
	D1	R01D	R01 output port data					
	D0	R00D	R00 output port data					
00FF74	D7	R17D	R17 output port data	High	Low	1	R/W	
	D6	R16D	R16 output port data					
	D5	R15D	R15 output port data					
	D4	R14D	R14 output port data					
	D3	R13D	R13 output port data					
	D2	R12D	R12 output port data					
	D1	R11D	R11 output port data					
	D0	R10D	R10 output port data					
00FF75	D7	R27D	R27 output port data	High	Low	1	R/W	
	D6	R26D	R26 output port data					
	D5	R25D	R25 output port data					
	D4	R24D	R24 output port data					
	D3	R23D	R23 output port data					
	D2	R22D	R22 output port data					
	D1	R21D	R21 output port data					
	D0	R20D	R20 output port data					
00FF76	D7	R37D	R37 output port data	High	Low	1	R/W	
	D6	R36D	R36 output port data					
	D5	R35D	R35 output port data					
	D4	R34D	R34 output port data					
	D3	R33D	R33 output port data					
	D2	R32D	R32 output port data					
	D1	R31D	R31 output port data					
	D0	R30D	R30 output port data					

Table 5.1.1(l) I/O Memory map (00FF77H–00FF82H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF77	D7	R47D	R/W register	1	0	1	R/W	Reserved register
	D6	R46D	R/W register					
	D5	R45D	R/W register					
	D4	R44D	R/W register					
	D3	R43D	R/W register					
	D2	R42D	R/W register					
	D1	R41D	R/W register					
	D0	R40D	R/W register					
00FF78	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	R51D	R51 output port data	High	Low	1	R/W	
	D0	R50D	R50 output port data	High	Low	0	R/W	
00FF80	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	PRAD	A/D converter clock control	On	Off	0	R/W	
	D2	PSAD2	A/D converter division ratio PSAD2 PSAD1 PSAD0 Division ratio 1 1 1 fOSC1 / 1 1 1 0 fOSC3 / 64 1 0 1 fOSC3 / 32 1 0 0 fOSC3 / 16 0 1 1 fOSC3 / 8 0 1 0 fOSC3 / 4 0 0 1 fOSC3 / 2 0 0 0 fOSC3 / 1			0	R/W	
	D1	PSAD1				0	R/W	
	D0	PSAD0				0	R/W	
00FF81	D7	PAD7	P17 A/D converter input control	A/D converter input	I/O port	0	R/W	
	D6	PAD6	P16 A/D converter input control			0	R/W	
	D5	PAD5	P15 A/D converter input control			0	R/W	
	D4	PAD4	P14 A/D converter input control			0	R/W	
	D3	–	–	–	–	–		Constantly "0" when being read
	D2	–	–	–	–	–		
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		
00FF82	D7	ADRUN	A/D conversion start control register	Start	Invalid	0	W	Constantry "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	CHS1	Analog input channel selection CHS1 CHS0 Input channel 1 1 AD7 1 0 AD6 0 1 AD5 0 0 AD4			0	R/W	
	D0	CHS0				0	R/W	

Table 5.1.1(m) I/O Memory map (00FF83H–00FF84H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF83	D7	ADDR9	A/D conversion result D9 (MSB)			–	R	
	D6	ADDR8	A/D conversion result D8					
	D5	ADDR7	A/D conversion result D7					
	D4	ADDR6	A/D conversion result D6					
	D3	ADDR5	A/D conversion result D5					
	D2	ADDR4	A/D conversion result D4					
	D1	ADDR3	A/D conversion result D3					
	D0	ADDR2	A/D conversion result D2					
00FF84	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	ADDR1	A/D conversion result D1			–	R	
	D0	ADDR0	A/D conversion result D0 (LSB)					

5.2 System Controller and Bus Control

The system controller is a management unit which sets such items as the bus mode in accordance with memory system configuration factors.
For the purposes of controlling the system, the following settings can be performed in software:

(1) Bus mode (CPU mode) settings
(2) Chip enable ($\overline{CE}$) signal output settings
(3) WAIT state settings for external memory
(4) Bus authority release request / acknowledge signal ($\overline{BREQ}$/$\overline{BACK}$) settings
(5) Page address setting of the stack pointer

Below is a description of the how these settings are to be made.

5.2.1 Bus mode settings

As explained in "3.5.2 Bus mode", the S1C88349 has four bus modes. Settings for bus modes must be made in software and must match the capacity of the external memory.

As shown in Table 5.2.1.1, bus mode settings are performed on the basis of the preset values for each mode written to the registers BSMD0 and BSMD1.

Table 5.2.1.1 Bus mode settings

Setting value		Bus mode	Configuration of external memory
BSMD1	BSMD0		
1	1	Expanded 512K maximum mode	ROM+RAM>64K bytes (Program>64K bytes)
1	0	Expanded 512K minimum mode	ROM+RAM>64K bytes (Program≤64K bytes)
0	1	Expanded 64K mode	ROM+RAM≤64K bytes
0	0	Single chip mode (MCU)	None
		Optional setting of one of the expanded modes (MPU)	See above

* The single chip mode setting is only possible when this IC is used in the MCU mode. The single chip mode setting is incompatible with the MPU mode, since this mode does not utilize internal ROM.
When using in the MPU mode, it is necessary to select the bus mode at the time of the initial resetting and at the time of the <BSMD1 = "0" and BSMD0 = "0"> setting from among the three types of expanded modes (expanded 64K mode, expanded 512K minimum mode and expanded 512K maximum mode) by mask option.
Select the expanded 512K maximum mode for this option, when the MPU mode is not used at all.

The function of I/O terminals is set as shown in Table 5.2.1.2 in accordance with mode selection.

Table 5.2.1.2 I/O terminal settings

Terminal	Bus mode		
	Single chip	Expanded 64K mode	Expanded 512K mode
R00	Output port R00	Address bus A0	
R01	Output port R01	Address bus A1	
R02	Output port R02	Address bus A2	
R03	Output port R03	Address bus A3	
R04	Output port R04	Address bus A4	
R05	Output port R05	Address bus A5	
R06	Output port R06	Address bus A6	
R07	Output port R07	Address bus A7	
R10	Output port R10	Address bus A8	
R11	Output port R11	Address bus A9	
R12	Output port R12	Address bus A10	
R13	Output port R13	Address bus A11	
R14	Output port R14	Address bus A12	
R15	Output port R15	Address bus A13	
R16	Output port R16	Address bus A14	
R17	Output port R17	Address bus A15	
R20	Output port R20		Address bus A16
R21	Output port R21		Address bus A17
R22	Output port R22		Address bus A18
R23	Output port R23	$\overline{RD}$ signal	
R24	Output port R24	$\overline{WR}$ signal	
P00	I/O port P00	Data bus D0	
P01	I/O port P01	Data bus D1	
P02	I/O port P02	Data bus D2	
P03	I/O port P03	Data bus D3	
P04	I/O port P04	Data bus D4	
P05	I/O port P05	Data bus D5	
P06	I/O port P06	Data bus D6	
P07	I/O port P07	Data bus D7	

At initial reset, the bus mode is set as explained below.

- **In MCU mode:**
  At initial reset, the S1C88349 is set in single chip mode.
  Accordingly, in MCU mode, even if a memory has been externally expanded, the system is activated by the program written to internal ROM.
  In the system with externally expanded memory, perform the applicable bus mode settings during the initialization routine originating in internal ROM.

- **In MPU mode:**
  When the MPU mode is used, the expanded mode (expanded 64K mode, expanded 512K minimum mode or expanded 512K maximum mode) set during initial reset must be pre-selected by mask option.
  You should set it to conform properly to system configuration.

5.2.2 Address decoder ($\overline{CE}$ output) settings

As explained in Section 3.6.4, the S1C88349 is equipped with address decoders that can output a maximum of four chip enable signals ($\overline{CE0}$–$\overline{CE3}$) to external devices.
The output terminals and output circuits for $\overline{CE0}$–$\overline{CE3}$ are shared with output ports R30–R33. At initial reset, they are set as output port terminals. For this reason, when operating in a mode other than single chip mode, the ports to be used as $\overline{CE}$ signal output terminals must be set as such.
This setting is performed through software which writes "1" to registers CE0–CE3 corresponding the $\overline{CE}$ signals to be used.
Table 5.2.2.1 shows the address range assigned to the four chip enable ($\overline{CE}$) signals.

The arrangement of memory space for external devices does not necessarily have to be continuous from a subordinate address and any of the chip enable signals can be used to assign areas in memory. However, in the MPU mode, program memory must be assigned to $\overline{CE0}$.
In the expanded 512K mode, the address range of each of the $\overline{CE}$ signals is fixed. In the expanded 64K mode, the four address ranges, which match the amount of memory in use, are selected with registers CEMD0 and CEMD1.

These signals are only output when the appointed external memory area is accessed and are not output when internal memory is accessed.

Table 5.2.2.1 Address settings of $\overline{CE0}$–$\overline{CE3}$

(1) Expanded 64K mode (MPU mode only)

CEMD1	CEMD0	Chip size	$\overline{CE0}$	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$
1	1	64K bytes	000000H–00EFFFH	–	–	–
1	0	32K bytes	000000H–007FFFH	008000H–00EFFFH	–	–
0	1	16K bytes	000000H–003FFFH	004000H–007FFFH	008000H–00BFFFH	00C000H–00EFFFH
0	0	8K bytes	000000H–001FFFH	002000H–003FFFH	004000H–005FFFH	006000H–007FFFH

(2) Expanded 512K minimum/maximum modes

$\overline{CE}$ signal	Address range	
	MCU mode	MPU mode
$\overline{CE0}$	200000H–27FFFFH	000000H–00EFFFH, 010000H–07FFFFH
$\overline{CE1}$	080000H–0FFFFFH	080000H–0FFFFFH
$\overline{CE2}$	100000H–17FFFFH	100000H–17FFFFH
$\overline{CE3}$	180000H–1FFFFFH	180000H–1FFFFFH

5.2.3 WAIT state settings

In order to insure accessing of external low speed devices during high speed operations, the S1C88349 is equipped with a WAIT function which prolongs access time.
The number of wait states inserted can be selected from a choice of eight as shown in Table 5.2.3.1 by means of registers WT0–WT2.

Table 5.2.3.1 Setting the number of WAIT states

WT2	WT1	WT0	Number of inserted states
1	1	1	14
1	1	0	12
1	0	1	10
1	0	0	8
0	1	1	6
0	1	0	4
0	0	1	2
0	0	0	No wait

* A state is 1/2 cycles of the clock in length.

WAIT states set in software are inserted between bus cycle states T3–T4.
Note, however, that WAIT states cannot be inserted when an internal register and internal memory are being accessed and when operating with the OSC1 oscillation circuit (see "5.4 Oscillation Circuits and Operating Mode").
Consequently, WAIT state settings in single chip mode are meaningless.
With regard to WAIT insertion timing, see Section 3.6.5, "WAIT control".

5.2.4 Setting the bus authority release request signal

With systems performing DMA transfer, the bus authority release request signal ($\overline{BREQ}$) input terminal and acknowledge signal ($\overline{BACK}$) output terminal have to be set.
The $\overline{BREQ}$ input terminal is shared with input port terminal K11 and the $\overline{BACK}$ output terminal with output port terminal R51. At initial reset, these terminal facilities are set as input port terminal and output port terminal, respectively. The terminals can be altered to function as $\overline{BREQ}$/$\overline{BACK}$ terminals by writing a "1" to register EBR.

For details on bus authority release, see "3.6.6 Bus authority release state" and "S1C88 Core CPU Manual".

5.2.5 Stack page setting

Although the stack area used to evacuate registers during subroutine calls can be arbitrarily moved to any area in data RAM using the stack pointer SP, its page address is set in registers SPP0–SPP7 in I/O memory.
At initial reset, SPP0–SPP7 are set to "00H" (page 0).

Since the internal RAM is arranged on page 0 (00F000H–00F7FFH), the stack area in single chip mode is inevitably located in page 0.
In expanded 64K mode where RAM is externally expanded, stack page is likewise limited to page 0.
In order to place the stack area at the final address in internal RAM, the stack pointer SP is placed at an initial setting of "F800H". (SP is pre-decremented.)

In the expanded 512K mode, to place the stack in external expanded RAM, set a corresponding page to SPP0–SPP7. The page addresses to which SPP0–SPP7 can be set are 00H–27H and must be within a RAM area.

* A page is each recurrent 64K division of data memory beginning at address zero.

5.2.6 Control of system controller

Table 5.2.6.1 shows the control bits for the system controller.

Table 5.2.6.1(a) System controller control bits (MCU mode)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF00 (MCU)	D7	BSMD1	Bus mode (CPU mode) BSMD1 BSMD0 Mode 1 1 512K (Maximum) 1 0 512K (Minimum) 0 1 × 0 0 Single chip			0	R/W	Do not set BSMD1–0 to 01B.
	D6	BSMD0				0	R/W	
	D5	CEMD1	R/W register			1	R/W	
	D4	CEMD0	R/W register			1	R/W	
	D3	CE3	$\overline{CE3}$ (R33)	$\overline{CE3}$ enable	$\overline{CE3}$ disable	0	R/W	In the Single chip mode, these setting are fixed at DC output.
	D2	CE2	$\overline{CE2}$ (R32)	$\overline{CE2}$ enable	$\overline{CE2}$ disable	0	R/W	
	D1	CE1	$\overline{CE1}$ (R31)	$\overline{CE1}$ enable	$\overline{CE1}$ disable	0	R/W	
	D0	CE0	$\overline{CE0}$ (R30) $\overline{CE}$ signal output Enable/Disable Enable: $\overline{CE}$ signal output Disable: DC (R3x) output	$\overline{CE0}$ enable	$\overline{CE0}$ disable	0	R/W	
00FF01	D7	SPP7	Stack pointer page address (MSB)	1	0	0	R/W	
	D6	SPP6		1	0	0	R/W	
	D5	SPP5	< SP page allocatable address >	1	0	0	R/W	
	D4	SPP4	• Single chip mode: only 0 page	1	0	0	R/W	
	D3	SPP3	• 64K mode: only 0 page	1	0	0	R/W	
	D2	SPP2	• 512K (min) mode: 0–27H page	1	0	0	R/W	
	D1	SPP1	• 512K (max) mode: 0–27H page	1	0	0	R/W	
	D0	SPP0	(LSB)	1	0	0	R/W	
00FF02	D7	EBR	Bus release enable register (K11 and R51 terminal specification) K11 R51	$\overline{BREQ}$ $\overline{BACK}$	Input port Output port	0	R/W	
	D6	WT2	Wait control register WT2 WT1 WT0 Number of state 1 1 1 14 1 1 0 12 1 0 1 10 1 0 0 8 0 1 1 6 0 1 0 4 0 0 1 2 0 0 0 No wait			0	R/W	
	D5	WT1				0	R/W	
	D4	WT0				0	R/W	
	D3	CLKCHG	CPU operating clock switch	OSC3	OSC1	0	R/W	
	D2	OSCC	OSC3 oscillation On/Off control	On	Off	0	R/W	
	D1	VDC1	Operating mode selection VDC1 VDC0 Operating mode 1 × High speed (V_{D1}=3.3V) 0 1 Low power (V_{D1}=1.2V) 0 0 Normal (V_{D1}=2.2V)			0	R/W	
	D0	VDC0				0	R/W	

Note: All the interrupts including $\overline{NMI}$ are disabled, until you write the optional value into both the "00FF00H" and "00FF01H" addresses.

Table 5.2.6.1(b) System controller control bits (MPU mode)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF00 (MPU)	D7	BSMD1	Bus mode (CPU mode) BSMD1 BSMD0 Mode 1 1 512K (Maximum) 1 0 512K (Minimum) 0 1 64K 0 0 * Option selection			*	R/W	* Initial setting can be selected among 3 types (64K, 512K min and 512K max) by mask option setting.
	D6	BSMD0				*	R/W	
	D5	CEMD1	Chip enable mode CEMD1 CEMD0 Mode 1 1 64K ($\overline{CE0}$) 1 0 32K ($\overline{CE0}$, $\overline{CE1}$) 0 1 16K ($\overline{CE0}$–$\overline{CE3}$) 0 0 8K ($\overline{CE0}$–$\overline{CE3}$)			1	R/W	Only for 64K bus mode
	D4	CEMD0				1	R/W	
	D3	CE3	$\overline{CE3}$ (R33) $\overline{CE}$ signal output Enable/Disable Enable: $\overline{CE}$ signal output Disable: DC (R3x) output	$\overline{CE3}$ enable	$\overline{CE3}$ disable	0	R/W	
	D2	CE2	$\overline{CE2}$ (R32)	$\overline{CE2}$ enable	$\overline{CE2}$ disable	0	R/W	
	D1	CE1	$\overline{CE1}$ (R31)	$\overline{CE1}$ enable	$\overline{CE1}$ disable	0	R/W	
	D0	CE0	$\overline{CE0}$ (R30)	$\overline{CE0}$ enable	$\overline{CE0}$ disable	1	R/W	
00FF01	D7	SPP7	Stack pointer page address (MSB)	1	0	0	R/W	
	D6	SPP6		1	0	0	R/W	
	D5	SPP5	< SP page allocatable address >	1	0	0	R/W	
	D4	SPP4	• Single chip mode: only 0 page	1	0	0	R/W	
	D3	SPP3	• 64K mode: only 0 page	1	0	0	R/W	
	D2	SPP2	• 512K (min) mode: 0–27H page	1	0	0	R/W	
	D1	SPP1	• 512K (max) mode: 0–27H page	1	0	0	R/W	
	D0	SPP0	(LSB)	1	0	0	R/W	
00FF02	D7	EBR	Bus release enable register (K11 and R51 terminal specification) K11 R51	$\overline{BREQ}$ $\overline{BACK}$	Input port Output port	0	R/W	
	D6	WT2	Wait control register WT2 WT1 WT0 Number of state 1 1 1 14 1 1 0 12 1 0 1 10 1 0 0 8 0 1 1 6 0 1 0 4 0 0 1 2 0 0 0 No wait			0	R/W	
	D5	WT1				0	R/W	
	D4	WT0				0	R/W	
	D3	CLKCHG	CPU operating clock switch	OSC3	OSC1	0	R/W	
	D2	OSCC	OSC3 oscillation On/Off control	On	Off	0	R/W	
	D1	VDC1	Operating mode selection VDC1 VDC0 Operating mode 1 × High speed (V_{D1}=3.3V) 0 1 Low power (V_{D1}=1.2V) 0 0 Normal (V_{D1}=2.2V)			0	R/W	
	D0	VDC0				0	R/W	

Note: All the interrupts including $\overline{NMI}$ are disabled, until you write the optional value into both the "00FF00H" and "00FF01H" addresses.

BSMD0, BSMD1: 00FF00H•D6, D7

Bus modes are set as shown in Table 5.2.6.2.

Table 5.2.6.2 Bus mode settings

Setting values		Bus mode
BSMD1	BSMD0	
1	1	Expanded 512K maximum mode
1	0	Expanded 512K minimum mode
0	1	Expanded 64K mode
0	0	Single chip mode (MCU)
		Optional setting of one of the expanded modes (MPU)

The single chip mode setting is only possible when this IC is used in the MCU mode. The single chip mode setting is incompatible with the MPU mode, since this mode does not utilize internal ROM.
When using in the MPU mode, it is necessary to select the bus mode at the time of the initial resetting and at the time of the <BSMD1 = "0" and BSMD0 = "0"> setting from among the three types of expanded modes (expanded 64K mode, expanded 512K minimum mode and expanded 512K maximum mode) by mask option.
Select the expanded 512K maximum mode for this option, when the MPU mode is not used at all.
At initial reset, in the MCU mode the unit is set to single chip mode and in the MPU mode the mask option is used to select the applicable mode.

CEMD0, CEMD1: 00FF00H•D4, D5

Sets the $\overline{CE}$ signal address range (valid only in the expanded 64K mode∗).
Settings are made according to external memory chip size as shown in Table 5.2.6.3.

Table 5.2.6.3 $\overline{CE}$ signal settings

CEMD1	CEMD0	Address range	Usable terminals
1	1	64K bytes	$\overline{CE0}$
1	0	32K bytes	$\overline{CE0}$, $\overline{CE1}$
0	1	16K bytes	$\overline{CE0}$–$\overline{CE3}$
0	0	8K bytes	$\overline{CE0}$–$\overline{CE3}$

These settings are invalid for any mode other than expanded 64K mode.
At initial reset, each register is set to "1" (64K bytes).

∗ Settings of these registers are valid only in the MPU mode. CEMD0 and CEMD1 can be used as general purpose registers with read / write capabilities in the MCU mode.

CE0–CE3: 00FF00H•D0–D3

Sets the $\overline{CE}$ output terminals being used.

When "1" is written: $\overline{CE}$ output enable
When "0" is written: $\overline{CE}$ output disable
Reading: Valid

$\overline{CE}$ output is enabled when a "1" is written to registers CE0–CE3 which correspond to the $\overline{CE}$ output being used. A "0" written to any of the registers disables $\overline{CE}$ signal output from that terminal and it reverts to its alternate function as an output port terminal (R30–R33).
At initial reset, register CE0 is set to "0" in the MCU mode and in the MPU mode, "1" is set in the register. Registers CE1–CE3 are always set to "0" regardless of the MCU / MPU mode setting.

Note: To avoid a malfunction from an interrupt generated before the bus configuration is initialized, all interrupts including $\overline{NMI}$ are masked until you write an optional value into address "00FF00H".

SPP0–SPP7: 00FF01H

Sets the page address of stack area. In single chip mode and expanded 64K mode, set page address to "00H".
In expanded 512K mode, it can be set to any value within the range "00H"–"27H".
Since a carry and borrow from / to the stack pointer SP is not reflected in register SPP, the upper limit on continuous use of the stack area is 64K bytes.
At initial reset, this register is set to "00H" (page 0).

Note: To avoid a malfunction from an interrupt generated before the bus configuration is initialized, all interrupts including $\overline{NMI}$ are disabled, until you write an optional value into "00FF01H" address. Furthermore, to avoid generating an interrupt while the stack area is being set, all interrupts including $\overline{NMI}$ are disabled in one instruction execution period after writing to address "00FF01H".

WT0–WT2: 00FF02H•D4–D6

How WAIT state settings are performed.
The number of WAIT states to be inserted based on register settings is as shown in Table 5.2.6.4.

Table 5.2.6.4 Setting WAIT states

WT2	WT1	WT0	No. of inserted states
1	1	1	14
1	1	0	12
1	0	1	10
1	0	0	8
0	1	1	6
0	1	0	4
0	0	1	2
0	0	0	No wait

* A state is 1/2 cycles of the clock in length.

At initial reset, this register is set to "0" (no wait).

EBR: 00FF02H•D7

Sets the $\overline{\text{BREQ}}$/$\overline{\text{BACK}}$ terminals function.

When "1" is written: $\overline{\text{BREQ}}$/$\overline{\text{BACK}}$ enabled
When "0" is written: $\overline{\text{BREQ}}$/$\overline{\text{BACK}}$ disabled
Reading: Valid

How $\overline{\text{BREQ}}$ and $\overline{\text{BACK}}$ terminal functions are set. Writing "1" to EBR enables $\overline{\text{BREQ}}$/$\overline{\text{BACK}}$ input/output. Writing "0" sets the $\overline{\text{BREQ}}$ terminal as input port terminal K11 and the $\overline{\text{BACK}}$ terminal as output port terminal R51.
At initial reset, EBR is set to "0" ($\overline{\text{BREQ}}$/$\overline{\text{BACK}}$ disabled).

5.2.7 Programming notes

(1) All the interrupts including $\overline{\text{NMI}}$ are masked, until you write the optional value into both the "00FF00H" and "00FF01H" addresses. Consequently, even if you do not change the content of this address (You use the initial value, as is.), you should still be sure to perform the writing operation using the initialization routine.

(2) When setting stack fields, including page addresses as well, you should write them in the order of the register SPP ("00FF01H") and the stack pointer SP.

Example: When setting the "178000H" address

```
LD   EP, #00H
LD   HL, #0FF01H
LD   [HL], #17H   ┐ During this period the
LD   SP, #8000H   ┘ interrupts (including NMI) are masked.
```

5.3 Watchdog Timer

5.3.1 Configuration of watchdog timer

The S1C88349 is equipped with a watchdog timer driven by OSC1 as source oscillation. The watchdog timer must be reset periodically in software, and if reset of more than 3–4 seconds (when fOSC1 = 32.768 kHz) does not take place, a non-maskable interrupt signal is generated and output to the CPU.

Figure 5.3.1.1 is a block diagram of the watchdog timer.

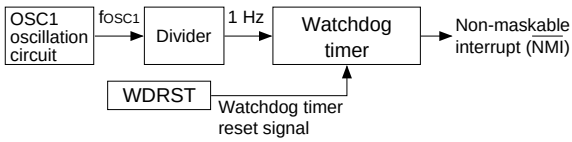


Fig. 5.3.1.1 Block diagram of watchdog timer

By running watchdog timer reset during the main routine of the program, it is possible to detect program runaway as if watchdog timer processing had not been applied. Normally, this routine is integrated at points that are regularly being processed.

The watchdog timer continues to operate during HALT and when a HALT state is continuous for longer than 3–4 seconds, the CPU shifts to exception processing.
During SLEEP, the watchdog timer is stopped.

5.3.2 Interrupt function

In cases where the watchdog timer is not periodically reset in software, the watchdog timer outputs an interrupt signal to the CPU's $\overline{\text{NMI}}$ (level 4) input. Unmaskable and taking priority over other interrupts, this interrupt triggers the generation of exception processing. See the "S1C88 Core CPU Manual" for more details on $\overline{\text{NMI}}$ exception processing.
This exception processing vector is set at 000004H.

5.3.3 Control of watchdog timer

Table 5.3.3.1 shows the control bits for the watchdog timer.

WDRST: 00FF40H•D2

Resets the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Constantly "0"

By writing "1" to WDRST, the watchdog timer is reset, after which it is immediately restarted. Writing "0" will mean no operation.
Since WDRST is for writing only, it is constantly set to "0" during readout.

5.3.4 Programming notes

(1) The watchdog timer must reset within 3-second cycles by software.

(2) Do not execute the SLP instruction for 2 msec after a $\overline{\text{NMI}}$ interrupt has occurred (when fOSC1 is 32.768 kHz).

Table 5.3.3.1 Watchdog timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF40	D7	–	–	–	–	–		"0" when being read
	D6	FOUT2	FOUT frequency selection			0	R/W	
	D5	FOUT1	FOUT2 FOUT1 FOUT0 Frequency 0 0 0 fOSC1 / 1 0 0 1 fOSC1 / 2 0 1 0 fOSC1 / 4 0 1 1 fOSC1 / 8 1 0 0 fOSC3 / 1 1 0 1 fOSC3 / 2 1 1 0 fOSC3 / 4 1 1 1 fOSC3 / 8			0	R/W	
	D4	FOUT0				0	R/W	
	D3	FOUTON	FOUT output control	On	Off	0	R/W	
	D2	WDRST	Watchdog timer reset	Reset	No operation	–	W	Constantly "0" when
	D1	TMRST	Clock timer reset	Reset	No operation	–	W	being read
	D0	TMRUN	Clock timer Run/Stop control	Run	Stop	0	R/W	

5.4 Oscillation Circuits and Operating Mode

5.4.1 Configuration of oscillation circuits

The S1C88349 is twin clock system with two internal oscillation circuits (OSC1 and OSC3). OSC1 oscillation circuit generates the 32.768 kHz (Typ.) main clock and OSC3 oscillation circuit the sub-clock when the CPU and some peripheral circuits (output port, serial interface and programmable timer) are in high speed operation.
Figure 5.4.1.1 shows the configuration of the oscillation circuit.

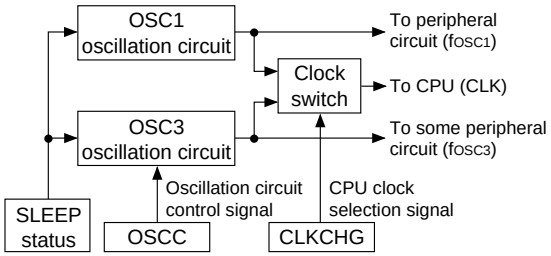


Fig. 5.4.1.1 Configuration of oscillation circuits

At initial reset, OSC1 oscillation circuit is selected for the CPU operating clock and OSC3 oscillation circuit is in a stopped state. ON / OFF switching of the OSC3 oscillation circuit and switching of the system clock between OSC1 and OSC3 are controlled in software. OSC3 circuit is utilized when high speed operation of the CPU and some peripheral circuits become necessary. Otherwise, OSC1 should be used to generate the operating clock and OSC3 circuit placed in a stopped state in order to reduce current consumption.

5.4.2 Mask option

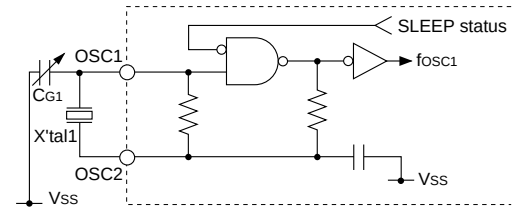
OSC1 oscillation circuit
- ☐ Crystal oscillation circuit
- ☐ External clock input
- ☐ CR oscillation circuit
- ☐ Crystal oscillation circuit (gate capacitor built-in)

OSC3 oscillation circuit
- ☐ Crystal oscillation circuit
- ☐ Ceramic oscillation circuit
- ☐ CR oscillation circuit
- ☐ External clock input

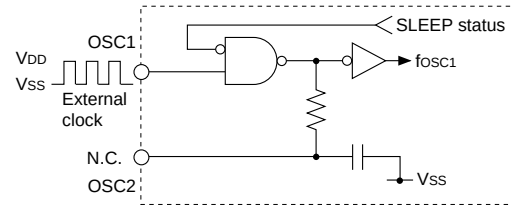
In terms of the oscillation circuit types for OSC1, either crystal oscillation, CR oscillation, crystal oscillation (gate capacitor built-in) or external clock input can be selected with the mask option.
In terms of oscillation circuit types for OSC3, either crystal oscillation, ceramic oscillation, CR oscillation or external clock input can be selected with the mask option, in the same way as OSC1.

5.4.3 OSC1 oscillation circuit

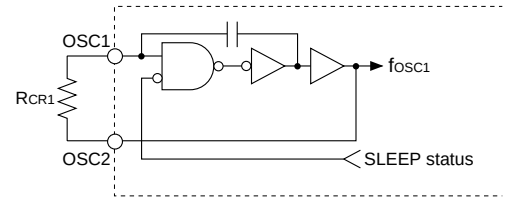
The OSC1 oscillation circuit generates the 32.768 kHz (Typ.) system clock which is utilized during low speed operation (low power mode) of the CPU and peripheral circuits. Furthermore, even when OSC3 is utilized as the system clock, OSC1 continues to generate the source clock for the clock timer and stopwatch timer.
This oscillation circuit stops when the SLP instruction is executed. However, in case the SVD circuit is executing an SLP instruction, oscillation is stopped in synchronization with the completion of sampling.
In terms of the oscillation circuit types, either crystal oscillation, CR oscillation, crystal oscillation (gate capacitor built-in) or external clock input can be selected with the mask option.
Figure 5.4.3.1 shows the configuration of the OSC1 oscillation circuit.



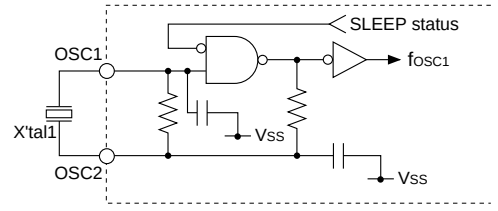
(1) Crystal oscillation circuit



(2) External clock input



(3) CR oscillation circuit



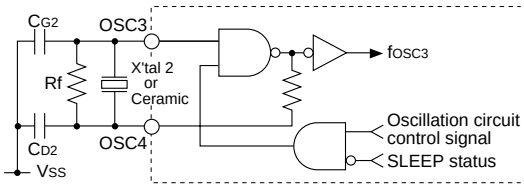
(4) Crystal oscillation circuit (gate capacitor built-in)

Fig. 5.4.3.1 OSC1 oscillation circuit

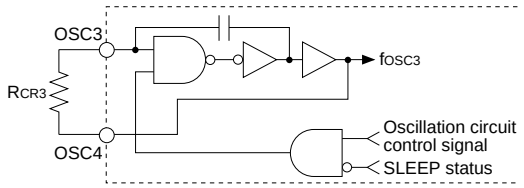
When crystal oscillation is selected, a crystal oscillation circuit can be easily formed by connecting a crystal oscillator X'tal1 (Typ. 32.768 kHz) between the OSC1 and OSC2 terminals along with a trimmer capacitor CG1 (5–25 pF) between the OSC1 terminal and VSS.
In addition, the gate capacitor CG1 (5 pF) can be built into the circuit by the mask option.
When CR oscillation is selected, connect a resistor (RCR1) between the OSC1 and OSC2 terminals.
When external input is selected, release the OSC2 terminal and input the rectangular wave clock into the OSC1 terminal.

5.4.4 OSC3 oscillation circuit

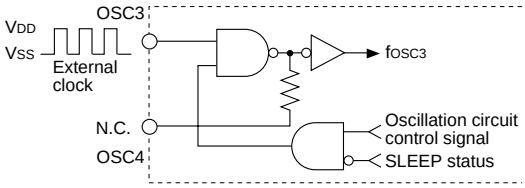
The OSC3 oscillation circuit generates the system clock when the CPU and some peripheral circuits (output port, serial interface and programmable timer) are in high speed operation.
This oscillation circuit stops when the SLP instruction is executed, or the OSCC register is set to "0".
In terms of oscillation circuit types, any one of crystal oscillation, ceramic oscillation, CR oscillation or external clock input can be selected with the mask option.
Figure 5.4.4.1 shows the configuration of the OSC3 oscillation circuit.



(1) Crystal/Ceramic oscillation circuit



(2) CR oscillation circuit



(3) External clock input

Fig. 5.4.4.1 OSC3 oscillation circuit

When crystal or ceramic oscillation circuit is selected, the crystal or ceramic oscillation circuit are formed by connecting either a crystal oscillator (X'tal2) or a combination of ceramic oscillator (Ceramic) and feedback resistor (Rf) between OSC3 and OSC4 terminals and connecting two capacitors (CG2, CD2) between the OSC3 terminal and VSS, and between the OSC4 terminal and VSS, respectively.
When CR oscillation is selected, the CR oscillation circuit is formed merely by connecting a resistor (RCR3) between OSC3 and OSC4 terminals.
When external input is selected, release the OSC4 terminal and input the rectangular wave clock into the OSC3 terminal.

5.4.5 Operating mode

You can select three types of operating modes using software, to obtain a stable operation and good characteristics (operating frequency and current consumption) over a broad operation voltage. Here below are indicated the features of the respective modes.

- **Normal mode (VDD = 2.4 V–5.5 V)**
  This mode is set following the initial reset. It permits the OSC3 oscillation circuit (Max. 4.2 MHz) to be used and also permits relative low power operation.

- **Low power mode (VDD = 1.8 V–3.5 V)**
  This is a lower power mode than the normal mode. It makes ultra-low power consumption possible by operation on the OSC1 oscillation circuit, although the OSC3 circuit cannot be used.

- **High speed mode (VDD = 3.5 V–5.5 V)**
  This mode permits higher speed operation than the normal mode. Since the OSC3 oscillation circuit (Max. 8.2 MHz) can be used, you should use this mode, when you require operation at 4.2 MHz or more. However, the current consumption will increase relative to the normal mode.

Using software to switch over among the above three modes to meet your actual usage circumstances will make possible a low power system. For example, you will be able to reduce current consumption by switching over to the normal mode when using the OSC3 as the CPU clock and, conversely, changing over to the low power mode when using the OSC1 as the CPU clock (OSC3 oscillation circuit is OFF).

Note: Do not turn the OSC3 oscillation circuit ON in the low power mode.
Do not switch over the operating mode (normal mode ↔ high speed mode) in the OSC3 oscillation circuit ON status, as this will cause faulty operation.
You can not use two modes, the low power mode and the high speed mode on one application, with respect to the operating voltages.

5.4.6 Switching the CPU clocks

You can use either OSC1 or OSC3 as the system clock for the CPU and you can switch over by means of software.
You can save power by turning the OSC3 oscillation circuit off while the CPU is operating in OSC1. When you must operate on OSC3, you can change to high speed operation by turning the OSC3 oscillation circuit ON and switching over the system clock.

In this case, since several msec to several tens of msec are necessary for the oscillation to stabilize after turning the OSC3 oscillation circuit ON, you should switch over the clock after stabilization time has elapsed. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 8, "ELECTRICAL CHARACTERISTICS".)

When switching over from the OSC3 to the OSC1, turn the OSC3 oscillation circuit OFF immediately following the clock changeover. The basic clock switching procedure is as described above, however, you must also combine it with the changeover of the operating mode to permit low current consumption and high speed operation.
Figure 5.4.6.1 indicates the status transition diagram for the operation mode and clock changeover.

Note: When turning ON the OSC3 oscillation circuit after switching the operating mode, you should allow a minimum waiting time of 5 msec.

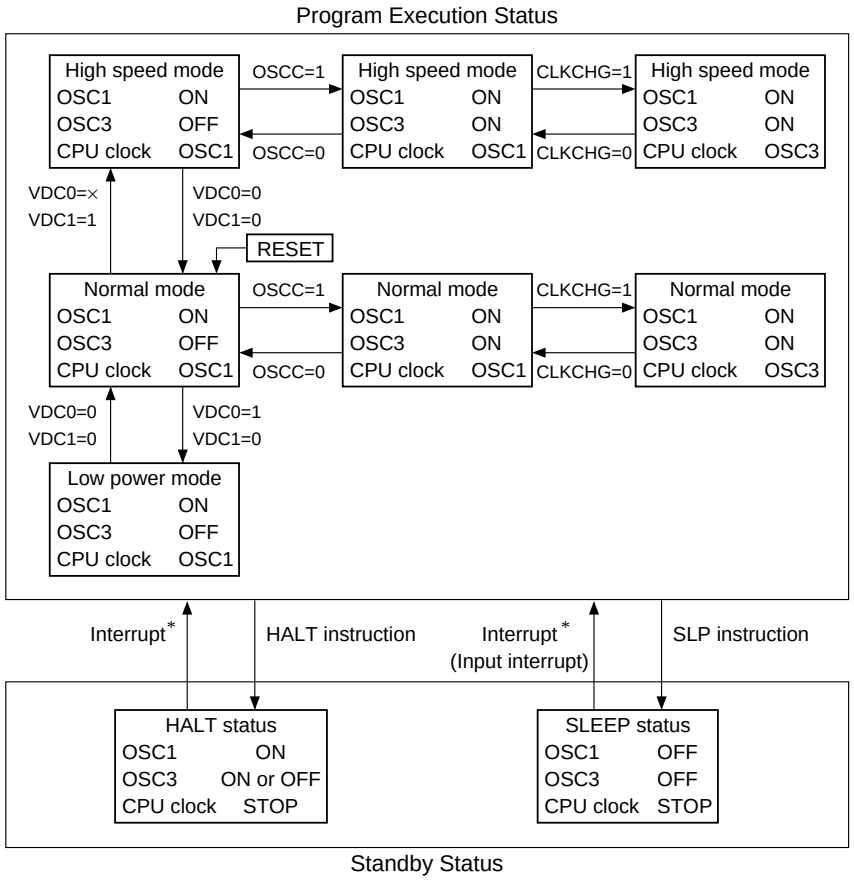


Fig. 5.4.6.1
Status transition diagram for the operation mode and clock changeover

* The return destination from the standby status becomes the program execution status prior to shifting to the standby status

5.4.7 Control of oscillation circuit and operating mode

Table 5.4.7.1 shows the control bits for the oscillation circuits and operating modes.

Table 5.4.7.1 Oscillation circuit and operating mode control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF02	D7	EBR	Bus release enable register (K11 and R51 terminal specification) K11 / R51	$\overline{BREQ}$ / $\overline{BACK}$	Input port / Output port	0	R/W	
	D6	WT2	Wait control register — WT2 WT1 WT0 → Number of state: 1 1 1 → 14; 1 1 0 → 12; 1 0 1 → 10; 1 0 0 → 8; 0 1 1 → 6; 0 1 0 → 4; 0 0 1 → 2; 0 0 0 → No wait			0	R/W	
	D5	WT1				0	R/W	
	D4	WT0				0	R/W	
	D3	CLKCHG	CPU operating clock switch	OSC3	OSC1	0	R/W	
	D2	OSCC	OSC3 oscillation On/Off control	On	Off	0	R/W	
	D1	VDC1	Operating mode selection — VDC1 VDC0 → Operating mode: 1 × → High speed (V_{D1}=3.3V); 0 1 → Low power (V_{D1}=1.2V); 0 0 → Normal (V_{D1}=2.2V)			0	R/W	
	D0	VDC0				0	R/W	

VDC1, VDC0: 00FF02H•D1, D0

Selects the operating mode according to supply voltage and operating frequency.
Table 5.4.7.2 shows the correspondence between register preset values and operating modes.

Table 5.4.7.2 Correspondence between register preset values and operating modes

Operating mode	VDC1	VDC0	V_{D1}	Power voltage	Operating frequency
Normal mode	0	0	2.2 V	2.4–5.5 V	4.2 MHz (Max.)
Low power mode	0	1	1.2 V	1.8–3.5 V	50 kHz (Max.)
High speed mode	1	×	3.3 V	3.5–5.5 V	8.2 MHz (Max.)

* The V_{D1} voltage is the value where V_{SS} has been made the standard (GND).

At initial reset, this register is set to "0" (normal mode).

OSCC: 00FF02H•D2

Controls the ON and OFF settings of the OSC3 oscillation circuit.

When "1" is written: OSC3 oscillation ON
When "0" is written: OSC3 oscillation OFF
Reading: Valid

When the CPU and some peripheral circuits (output port, serial interface and programmable timer) are to be operated at high speed, OSCC is to be set to "1". At all other times, it should be set to "0" in order to reduce current consumption.
At initial reset, OSCC is set to "0" (OSC3 oscillation OFF).

CLKCHG: 00FF02H•D3

Selects the operating clock for the CPU.

When "1" is written: OSC3 clock
When "0" is written: OSC1 clock
Reading: Valid

When the operating clock for the CPU is switched to OSC3, CLKCHG should be set to "1" and when the clock is switched to OSC1, CLKCHG should be set to "0".
At initial reset, CLKCHG is set to "0" (OSC1 clock).

5.4.8 Programming notes

(1) When the high speed CPU operation is not necessary, you should operate the peripheral circuits according to the setting outline indicate below.

- CPU operating clock
  OSC1
- OSC3 oscillation circuit
  OFF (When the OSC3 clock is not necessary for some peripheral circuits.)
- Operating mode
  Low power mode (When V_{DD}–V_{SS} is 3.5 V or less)
  or Normal mode (When V_{DD}–V_{SS} is 3.5 V or more)

(2) Do not turn the OSC3 oscillation circuit ON in the low power mode.
Do not switch over the operating mode (normal mode ↔ high speed mode) in the OSC3 oscillation circuit ON status, as this will cause faulty operation.

(3) When turning ON the OSC3 oscillation circuit after switching the operating mode, you should allow a minimum waiting time of 5 msec.

(4) Since several msec to several tens of msec are necessary for the oscillation to stabilize after turning the OSC3 oscillation circuit ON. Consequently, you should switch the CPU operating clock (OSC1 → OSC3) after allowing for a sufficient waiting time once the OSC3 oscillation goes ON. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 8, "ELECTRICAL CHARACTERISTICS".)

(5) When switching the clock from OSC3 to OSC1, be sure to switch OSC3 oscillation OFF with separate instructions. Using a single instruction to process simultaneously can cause a malfunction of the CPU.

5.5 Input Ports (K ports)

5.5.1 Configuration of input ports

The S1C88349 is equipped with 10 input port bits (K00–K07, K10 and K11) all of which are usable as general purpose input port terminals with interrupt function.

K10 terminal doubles as the external clock (EVIN) input terminal of the programmable timer (event counter) with input port functions sharing the input signal as is. (See "5.11 Programmable Timer")

Furthermore, it should be noted, however, that K11 terminal is shared with the bus authority release request signal ($\overline{BREQ}$) input terminal. Function assignment of this terminal can be selected in software. When this terminal is selected for $\overline{BREQ}$ signal, K11 cannot be used as an input port. (See "5.2 System Controller and Bus Control")
In the explanation below, it is assumed that K11 is set as an input port.

Each input port is equipped with a pull-up resistor. The mask option can be used to select either "With resistor" or "Gate direct" for each input port.
Figure 5.5.1.1 shows the structure of the input port.

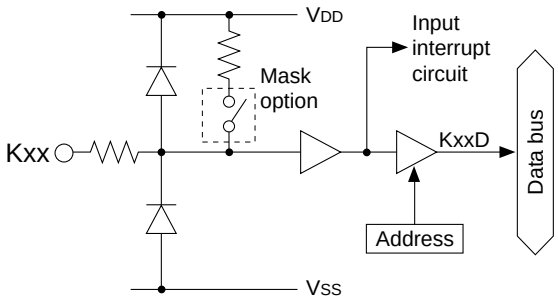


Fig. 5.5.1.1 Structure of input port

Each input port terminal is directly connected via a three-state buffer to the data bus. Furthermore, the input signal state at the instant of input port readout is read in that form as data.

5.5.2 Mask option

Input port pull-up resistors

K00	☐ With resistor	☐ Gate direct
K01	☐ With resistor	☐ Gate direct
K02	☐ With resistor	☐ Gate direct
K03	☐ With resistor	☐ Gate direct
K04	☐ With resistor	☐ Gate direct
K05	☐ With resistor	☐ Gate direct
K06	☐ With resistor	☐ Gate direct
K07	☐ With resistor	☐ Gate direct
K10	☐ With resistor	☐ Gate direct
K11	☐ With resistor	☐ Gate direct

Input ports K00–K07, K10 and K11 are all equipped with pull-up resistors. The mask option can be used to select 'With resistor' or 'Gate direct' for each port (bit).

The 'With resistor' option is rendered suitable for purposes such as push switch or key matrix input. When changing the input terminal from LOW level to HIGH with the built-in pull-up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull-up resistor and the load capacitance of the terminal. It is necessary to set an appropriate wait time for introduction of an input port. In particular, special attention should be paid to key scan for key matrix formation. Make this wait time the amount of time or more calculated by the following expression.

Wait time = R_{IN} x (C_{IN} + load capacitance on the board) x 1.6 [sec]

R_{IN}: Pull up resistance Max. value
C_{IN}: Terminal capacitance Max. value

When 'Gate direct' is selected, the pull-up resistor is detached and the port is rendered suitable for purposes such as slide switch input and interfacing with other LSIs.
In this case, take care that a floating state does not occur in input.

For unused input ports, select the default setting of "With resistor".

5.5.3 Interrupt function and input comparison register

Input port K00–K07, K10 and K11 are all equipped with an interrupt function. These input ports are divided into three groupings: K00–K03 (K0L), K04–K07 (K0H) and K10–K11 (K1). Furthermore, the interrupt generation condition for each series of terminals can be set by software.
When the interrupt generation condition set for each series of terminals is met, the interrupt factor flag FK0L, FK0H or FK1 corresponding to the applicable series is set at "1" and an interrupt is generated.
Interrupt can be prohibited by setting the interrupt enable registers EK0L, EK0H and EK1 for the corresponding interrupt factor flags.
Furthermore, the priority level for input interrupt can be set at the desired level (0–3) using the interrupt priority registers PK00–PK01 and PK10–PK11 corresponding to each of two groups K0x (K00–K07) and K1x (K10–K11).
For details on the interrupt control registers for the above and on operations subsequent to interrupt generation, see "5.17 Interrupt and Standby Status".

The exception processing vectors for each interrupt factor are set as follows:

K10 and K11 input interrupt:	00000AH
K04–K07 input interrupt:	00000CH
K00–K03 input interrupt:	00000EH

Figure 5.5.3.1 shows the configuration of the input interrupt circuit.

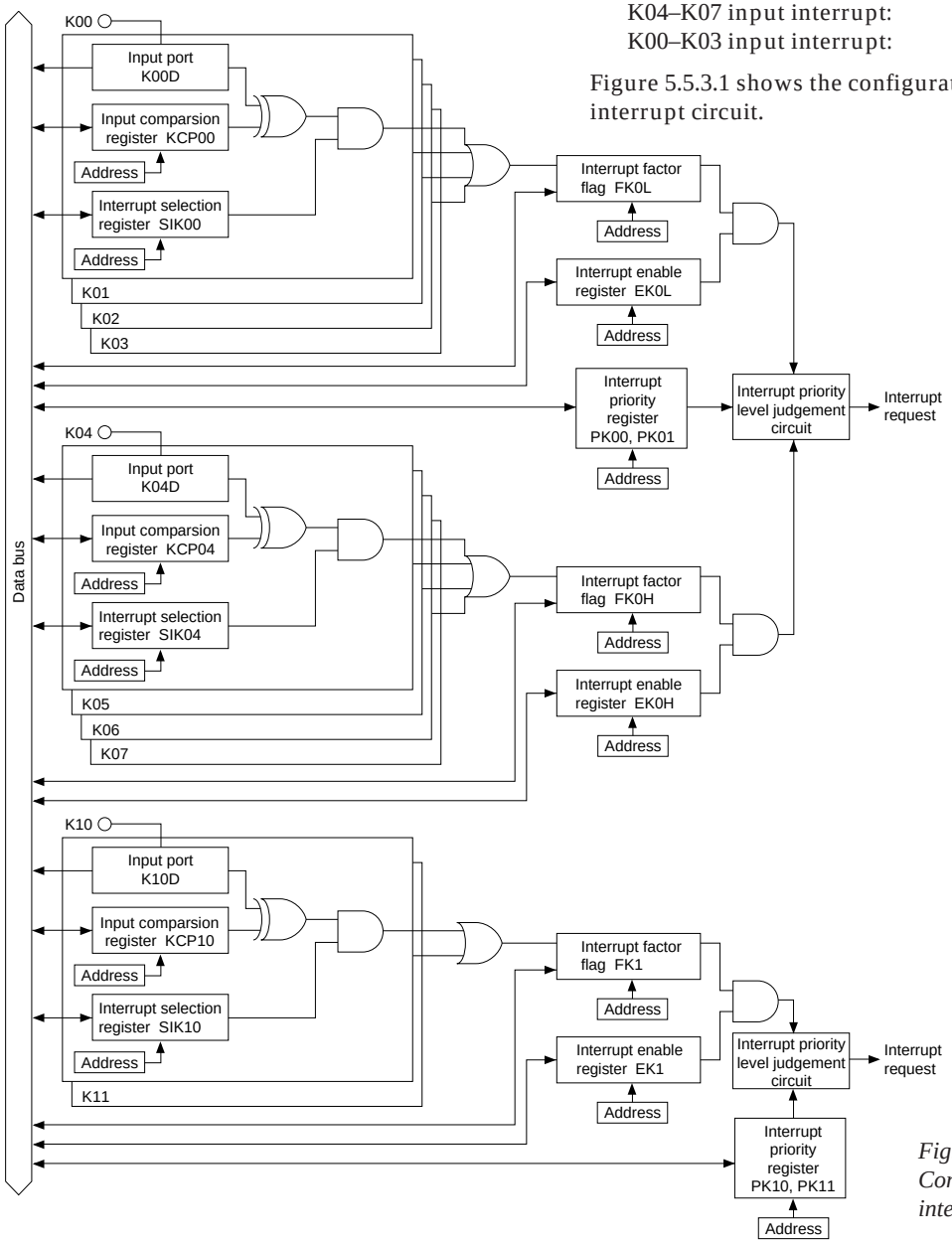


Fig. 5.5.3.1 Configuration of input interrupt circuit

The interrupt selection registers SIK00–SIK03, SIK04–SIK07 and SIK10–SIK11 and input comparison registers KCP00–KCP03, KCP04–KCP07 and KCP10–KCP11 for each port are used to set the interrupt generation condition described above.

Input port interrupt can be permitted or prohibited by the setting of the interrupt selection register SIK. In contrast to the interrupt enable register EK which masks the interrupt factor for each series of terminals, the interrupt selection register SIK is masks the bit units.

The input comparison register KCP selects whether the interrupt for each input port will be generated on the rising edge or the falling edge of input.

When the data content of the input terminals in which interrupt has been permitted by the interrupt selection register SIK and the data content of the input comparison register KCP change from a conformity state to a non-conformity state, the interrupt factor flag FK should be set to "1" and an interrupt is generated.

Figure 5.5.3.2 shows an example of interrupt generation in the series of terminals K0L (K00–K03).

Because interrupt has been prohibited for K00 by the interrupt selection register SIK00, with the settings as shown in (2), an interrupt will not be generated.
Since K03 is "0" in the next settings (3) in the figure, the non-conformity between the input terminal data K01–K03 where interrupt is permitted and the data from the input comparison registers KCP01–KCP03 generates an interrupt.
In line with the explanation above, since the change in the contents of input data and input comparison registers KCP from a conformity state to a non-conformity state introduces an interrupt generation condition, switching from one non-conformity state to another, as is the case in (4) in the figure, will not generate an interrupt. Consequently, in order to be able to generate a second interrupt, either the input terminal must be returned to a state where its content is once again in conformity with that of the input comparison register KCP, or the input comparison register KCP must be reset.
Input terminals for which interrupt is prohibited will not influence an interrupt generation condition.

Interrupt is generated in exactly the same way in the other two series of terminals K0H (K04–K07) and K1 (K10 and K11).

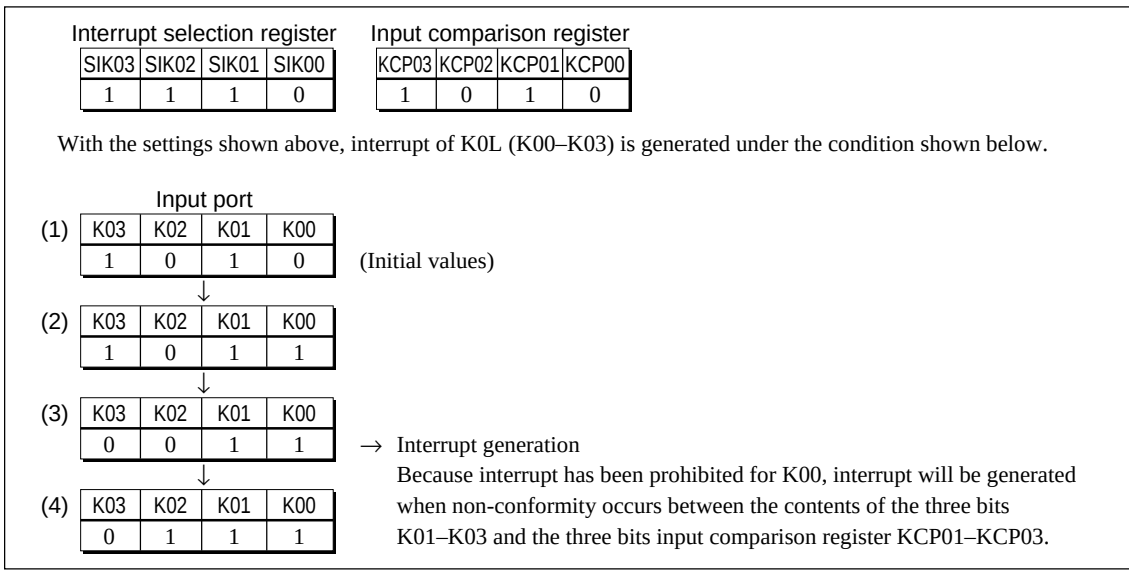


Fig. 5.5.3.2 Interrupt generation example in K0L (K00–K03)

5.5.4 Control of input ports

Table 5.5.4.1 shows the input port control bits.

Table 5.5.4.1(a) Input port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF50	D7	SIK07	K07 interrupt selection register	Interrupt enable	Interrupt disable	0	R/W	
	D6	SIK06	K06 interrupt selection register					
	D5	SIK05	K05 interrupt selection register					
	D4	SIK04	K04 interrupt selection register					
	D3	SIK03	K03 interrupt selection register					
	D2	SIK02	K02 interrupt selection register					
	D1	SIK01	K01 interrupt selection register					
	D0	SIK00	K00 interrupt selection register					
00FF51	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	SIK11	K11 interrupt selection register	Interrupt enable	Interrupt disable	0	R/W	
	D0	SIK10	K10 interrupt selection register					
00FF52	D7	KCP07	K07 interrupt comparison register	Interrupt generated at falling edge	Interrupt generated at rising edge	1	R/W	
	D6	KCP06	K06 interrupt comparison register					
	D5	KCP05	K05 interrupt comparison register					
	D4	KCP04	K04 interrupt comparison register					
	D3	KCP03	K03 interrupt comparison register					
	D2	KCP02	K02 interrupt comparison register					
	D1	KCP01	K01 interrupt comparison register					
	D0	KCP00	K00 interrupt comparison register					
00FF53	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	KCP11	K11 interrupt comparison register	Falling edge	Rising edge	1	R/W	
	D0	KCP10	K10 interrupt comparison register					
00FF54	D7	K07D	K07 input port data	High level input	Low level input	–	R	
	D6	K06D	K06 input port data					
	D5	K05D	K05 input port data					
	D4	K04D	K04 input port data					
	D3	K03D	K03 input port data					
	D2	K02D	K02 input port data					
	D1	K01D	K01 input port data					
	D0	K00D	K00 input port data					
00FF55	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	K11D	K11 input port data	High level input	Low level input	–	R	
	D0	K10D	K10 input port data					

Table 5.5.4.1(b) Input port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF20	D7	PK01	K00–K07 interrupt priority register	PK01 PK00 Priority level: 1 1 Level 3; 1 0 Level 2; 0 1 Level 1; 0 0 Level 0		0	R/W	
	D6	PK00						
	D5	PSIF1	Serial interface interrupt priority register	PSIF1 PSIF0 Priority level: 1 1 Level 3; 1 0 Level 2; 0 1 Level 1; 0 0 Level 0		0	R/W	
	D4	PSIF0						
	D3	PSW1	Stopwatch timer interrupt priority register	PSW1 PSW0 Priority level: 1 1 Level 3; 1 0 Level 2; 0 1 Level 1; 0 0 Level 0		0	R/W	
	D2	PSW0						
	D1	PTM1	Clock timer interrupt priority register	PTM1 PTM0 Priority level: 1 1 Level 3; 1 0 Level 2; 0 1 Level 1; 0 0 Level 0		0	R/W	
	D0	PTM0						
00FF21	D7	–	–	–	–	–		
	D6	–	–	–	–	–		Constantly "0" when being read
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	PPT1	Programmable timer interrupt priority register	PPT1 PPT0 Priority level: 1 1 Level 3; 1 0 Level 2; 0 1 Level 1; 0 0 Level 0		0	R/W	
	D2	PPT0						
	D1	PK11	K10 and K11 interrupt priority register	PK11 PK10 Priority level: 1 1 Level 3; 1 0 Level 2; 0 1 Level 1; 0 0 Level 0		0	R/W	
	D0	PK10						
00FF23	D7	EPT1	Programmable timer 1 interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D6	EPT0	Programmable timer 0 interrupt enable register					
	D5	EK1	K10 and K11 interrupt enable register					
	D4	EK0H	K04–K07 interrupt enable register					
	D3	EK0L	K00–K03 interrupt enable register					
	D2	ESERR	Serial I/F (error) interrupt enable register					
	D1	ESREC	Serial I/F (receiving) interrupt enable register					
	D0	ESTRA	Serial I/F (transmitting) interrupt enable register					
00FF25	D7	FPT1	Programmable timer 1 interrupt factor flag	(R) Interrupt factor is generated	(R) No interrupt factor is generated	0	R/W	
	D6	FPT0	Programmable timer 0 interrupt factor flag					
	D5	FK1	K10 and K11 interrupt factor flag					
	D4	FK0H	K04–K07 interrupt factor flag					
	D3	FK0L	K00–K03 interrupt factor flag					
	D2	FSERR	Serial I/F (error) interrupt factor flag	(W) Reset	(W) No operation			
	D1	FSREC	Serial I/F (receiving) interrupt factor flag					
	D0	FSTRA	Serial I/F (transmitting) interrupt factor flag					

K00D–K07D: 00FF54H
K10D, K11D: 00FF55H•D0, D1

Input data of input port terminal Kxx can be read out.

When "1" is read: HIGH level
When "0" is read: LOW level
Writing: Invalid

The terminal voltage of each of the input port K00–K07, K10 and K11 can be directly read out as either a "1" for HIGH (V_{DD}) level or a "0" for LOW (V_{SS}) level.
This bit is exclusively for readout and are not usable for write operations.

SIK00–SIK07: 00FF50H
SIK10, SIK11: 00FF51H•D0, D1

Sets the interrupt generation condition (interrupt permission / prohibition) for input port terminals K00–K07, K10 and K11.

When "1" is written: Interrupt permitted
When "0" is written: Interrupt prohibited
Reading: Valid

SIKxx is the interrupt selection register which correspond to the input port Kxx. A "1" setting permits interrupt in that input port and a "0" prohibits it. Changes of state in an input terminal in which interrupt is prohibited, will not influence interrupt generation.
At initial reset, this register is set to "0" (interrupt prohibited).

KCP00–KCP07: 00FF52H
KCP10, KCP11: 00FF53H•D0, D1

Sets the interrupt generation condition (interrupt generation timing) for input port terminals K00–K07, K10 and K11.

When "1" is written: Falling edge
When "0" is written: Rising edge
Reading: Valid

KCPxx is the input comparison register which correspond to the input port Kxx. Interrupt in those ports which have been set to "1" is generated on the falling edge of the input and in those set to "0" on the rising edge.
At initial reset, this register is set to "1" (falling edge).

PK00, PK01: 00FF20H•D6, D7
PK10, PK11: 00FF21H•D0, D1

Sets the input interrupt priority level. The two bits PK00 and PK01 are the interrupt priority registers corresponding to the interrupts for K00–K07 (K0L and K0H). Corresponding to K10–K11 (K1), the two bits PK10 and PK11 perform the same function.
Table 5.5.4.2 shows the interrupt priority level which can be set by this register.

Table 5.5.4.2 Interrupt priority level settings

PK11 PK01	PK10 PK00	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

EK0L, EK0H, EK1: 00FF23H•D3, D4, D5

How interrupt generation to the CPU is permitted or prohibited.

When "1" is written: Interrupt permitted
When "0" is written: Interrupt prohibited
Reading: Valid

The interrupt enable register EK0L corresponds to K00–K03, EK0H to K04–K07, and EK1 to K10–K11. Interrupt is permitted in those series of terminals set to "1" and prohibited in those set to "0".
At initial reset, this register is set to "0" (interrupt prohibited).

FK0L, FK0H, FK1: 00FF25H•D3, D4, D5

Indicates the generation state for an input interrupt.

When "1" is read: Interrupt factor present
When "0" is read: Interrupt factor not present

When "1" is written: Reset factor flag
When "0" is written: Invalid

The interrupt factor flag FK0L corresponds to K00–K03, FK0H to K04–K07, and FK1 to K10–K11 and they are set to "1" by the occurrence of an interrupt generation condition.
When set in this manner, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU. Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.
To accept the subsequent interrupt after interrupt generation, re-setting of the interrupt flags (set interrupt flag to lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and interrupt factor flag reset are necessary. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, this flag is all reset to "0".

5.5.5 Programming note

When changing the input terminal from LOW level to HIGH with the built-in pull-up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull-up resistor and the load capacitance of the terminal. It is necessary to set an appropriate wait time for introduction of an input port. In particular, special attention should be paid to key scan for key matrix formation. Make this wait time the amount of time or more calculated by the following expression.

Wait time = R_{IN} x (C_{IN} + load capacitance on the board) x 1.6 [sec]

R_{IN}: Pull up resistance Max. value
C_{IN}: Terminal capacitance Max. value

5.6 Output Ports (R ports)

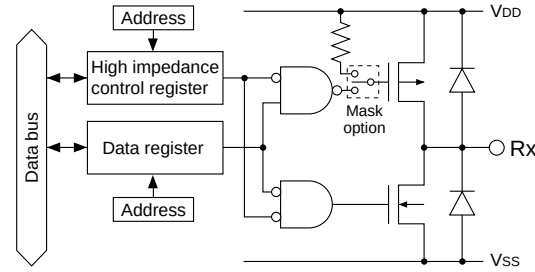
5.6.1 Configuration of output ports

The S1C88349 is equipped with 34 bits of output ports (R00–R07, R10–R17, R20–R27, R30–R37, R50, R51).
Depending on the bus mode setting, the configuration of the output ports may vary as shown in the table below.

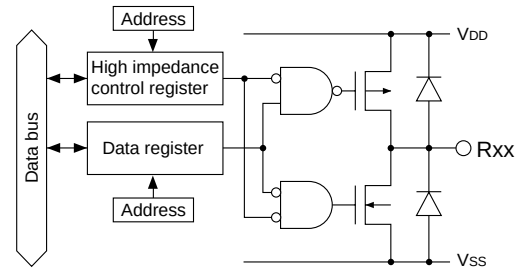
Table 5.6.1.1 Configuration of output ports

Terminal	Bus mode		
	Single chip	Expanded 64K	Expanded 512K
R00	Output port R00	Address A0	
R01	Output port R01	Address A1	
R02	Output port R02	Address A2	
R03	Output port R03	Address A3	
R04	Output port R04	Address A4	
R05	Output port R05	Address A5	
R06	Output port R06	Address A6	
R07	Output port R07	Address A7	
R10	Output port R10	Address A8	
R11	Output port R11	Address A9	
R12	Output port R12	Address A10	
R13	Output port R13	Address A11	
R14	Output port R14	Address A12	
R15	Output port R15	Address A13	
R16	Output port R16	Address A14	
R17	Output port R17	Address A15	
R20	Output port R20		Address A16
R21	Output port R21		Address A17
R22	Output port R22		Address A18
R23	Output port R23	$\overline{RD}$ signal	
R24	Output port R24	$\overline{WR}$ signal	
R25	Output port R25		
R26	Output port R26		
R27	Output port R27		
R30	Output port R30	Output port R30/$\overline{CE0}$ signal	
R31	Output port R31	Output port R31/$\overline{CE1}$ signal	
R32	Output port R32	Output port R32/$\overline{CE2}$ signal	
R33	Output port R33	Output port R33/$\overline{CE3}$ signal	
R34	Output port R34		
R35	Output port R35		
R36	Output port R36		
R37	Output port R37		
R50	Output port R50		
R51	Output port R51	Output port R51/$\overline{BACK}$ signal	

Only the configuration of the output ports in single chip mode will be discussed here. With respect to bus control, see "5.2 System Controller and Bus Control".
Figure 5.6.1.1 shows the basic structure (excluding special output circuits) of the output ports.



Nch open drain can be set for R00–R07 and R10–R17 by the mask option.



R20–R27, R30–R37, R50, R51

Fig. 5.6.1.1 Structure of output ports

In modes other than single chip mode, the data registers and high impedance control registers of the output ports used for bus function can be used as general purpose registers with read / write capabilities. This will not in any way affect bus signal output.
The output specification of each output port is as complementary output with high impedance control in software possible.
Besides normal DC output, output ports R25–R27, R34, and R50 have a special output function, which can be selected by software.

5.6.2 Mask option

Output ports R00–R07 and R10–R17 output specifications

R00 ..... ☐ Complementary ☐ Nch open drain
R01 ..... ☐ Complementary ☐ Nch open drain
R02 ..... ☐ Complementary ☐ Nch open drain
R03 ..... ☐ Complementary ☐ Nch open drain
R04 ..... ☐ Complementary ☐ Nch open drain
R05 ..... ☐ Complementary ☐ Nch open drain
R06 ..... ☐ Complementary ☐ Nch open drain
R07 ..... ☐ Complementary ☐ Nch open drain

R10 ..... ☐ Complementary ☐ Nch open drain
R11 ..... ☐ Complementary ☐ Nch open drain
R12 ..... ☐ Complementary ☐ Nch open drain
R13 ..... ☐ Complementary ☐ Nch open drain
R14 ..... ☐ Complementary ☐ Nch open drain
R15 ..... ☐ Complementary ☐ Nch open drain
R16 ..... ☐ Complementary ☐ Nch open drain
R17 ..... ☐ Complementary ☐ Nch open drain

Output ports R00–R07 and R10–R17 can be used to select output specification for each port (1 bit) by mask option.

The output specification can be selected for either complementary output or Nch open drain output.

Nch open drain output is rendered suitable for purposes as key matrix common output.

For unused input ports, select the default setting of "Complementary".

Note: When Nch open drain has been selected, voltage in excess of the supply voltage range must not applied to the output port terminal.

5.6.3 High impedance control

The output port can be high impedance controlled in software.
This makes it possible to share output signal lines with an other external device.

A high impedance control register is set for each series of output port terminals as shown below. Either complementary output and high impedance state can be selected with this register.

Table 5.6.3.1 Correspondence between output ports and high impedance control registers

Register	Output port terminal
HZR0L	R00–R03
HZR0H	R04–R07
HZR1L	R10–R13
HZR1H	R14–R17
HZR20	R20
HZR21	R21
HZR22	R22
HZR23	R23
HZR24	R24
HZR25	R25
HZR26	R26
HZR27	R27
HZR30	R30
HZR31	R31
HZR32	R32
HZR33	R33
HZR34	R34
HZR35	R35
HZR36	R36
HZR37	R37
HZR4L *	–
HZR4H *	–
HZR50	R50
HZR51	R51

* This is a 2-bit reserved register, it can be used as a general purpose register with read / write capabilities.

When a high impedance control register HZRxx is set to "1", the corresponding output port terminal becomes high impedance state and when set to "0", it becomes complementary output.

5.6.4 DC output

As Figure 5.6.1.1 shows, when "1" is written to the output port data register, the output terminal switches to HIGH (V_{DD}) level and when "0" is written it switches to LOW (V_{SS}) level. When output is in a high impedance state, the data written to the data register is output from the terminal at the instant when output is switched to complementary.

5.6.5 Special output

Besides normal DC output, output ports R25–R27, R34 and R50 can also be assigned special output functions in software as shown in Table 5.6.5.1.

Table 5.6.5.1 Special output ports

Output port	Special output
R25	CL output
R26	FR output
R27	TOUT output
R34	FOUT output
R50	BZ output

■ CL and FR output (R25 and R26)

In order for the S1C88349 to handle connection to an externally expanded LCD driver, output ports R25 and R26 can be used to output a CL signal (LCD synchronous signal) and FR signal (LCD frame signal), respectively.
The configuration of output ports R25 and R26 are shown in Figure 5.6.5.1.

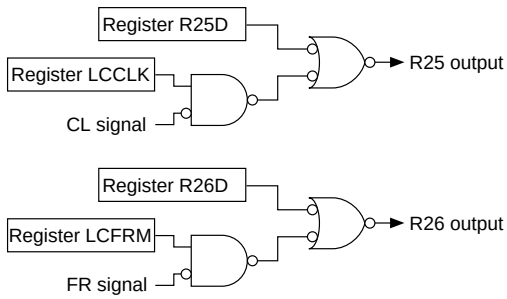


Fig. 5.6.5.1 Configuration of R25 and R26

The output control for the CL signal is done by the register LCCLK. When you set "1" for the LCCLK, the CL signal is output from the output port terminal R25, when "0" is set, the HIGH (V_{DD}) level is output. At this time, "1" must always be set for the data register R25D.
The output control for the FR signal is done by the register LCFRM. When you set "1" for the LCFRM, the FR signal is output from the output port terminal R26, when "0" is set, the HIGH (V_{DD}) level is output. At this time, "1" must always be set for the data register R26D.

The frequencies of each signal are changed as shown in Table 5.6.5.2 according to the drive duty selection.

Table 5.6.5.2 Frequencies of CL and FR signals

Drive duty	CL signal (Hz)	FR signal (Hz)
1/32	2,048	32
1/16	1,024	32
1/8	1,024	64

Since the signals are generated asynchronously from the registers LCCLK and LCFRM, when the signals are turned ON or OFF by the register settings, a hazard of a 1/2 cycle or less is generated. Figure 5.6.5.2 shows the output waveforms of the CL and FR signals.

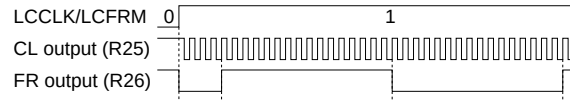


Fig. 5.6.5.2 Output waveforms of CL and FR signals

■ TOUT output (R27)

In order for the S1C88349 to provide clock signal to an external device, the output port terminal R27 can be used to output a TOUT signal (clock output by the programmable timer). The configuration of output port R27 is shown in Figure 5.6.5.3.

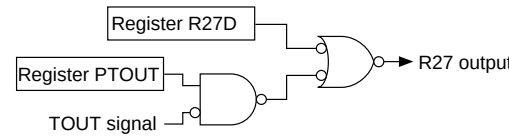


Fig. 5.6.5.3 Configuration of R27

The output control for the TOUT signal is done by the register PTOUT. When you set "1" for the PTOUT, the TOUT signal is output from the output port terminal R27, when "0" is set, the HIGH (V_{DD}) level is output. At this time, "1" must always be set for the data register R27D.
The TOUT signal is the programmable timer underflow divided by 1/2.
With respect to frequency control, see "5.11 Programmable Timer".
Since the TOUT signal is generated asynchronously from the register PTOUT, when the signal is turned ON or OFF by the register settings, a hazard of a 1/2 cycle or less is generated.
Figure 5.6.5.4 shows the output waveform of the TOUT signal.

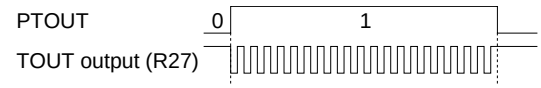


Fig. 5.6.5.4 Output waveform of TOUT signal

■ FOUT output (R34)

In order for the S1C88349 to provide clock signal to an external device, a FOUT signal (oscillation clock fOSC1 or fOSC3 dividing clock) can be output from the output port terminal R34.
Figure 5.6.5.5 shows the configuration of output port R34.

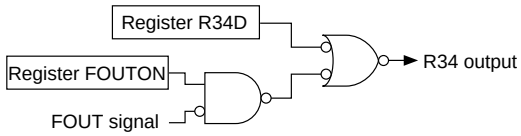


Fig. 5.6.5.5 Configuration of R34

The output control for the FOUT signal is done by the register FOUTON. When you set "1" for the FOUTON, the FOUT signal is output from the output port terminal R34, when "0" is set, the HIGH (VDD) level is output. At this time, "1" must always be set for the data register R34D.
The frequency of the FOUT signal can be selected in software by setting the registers FOUT0–FOUT2. The frequency is selected any one from among eight settings as shown in Table 5.6.5.3.

Table 5.6.5.3 FOUT frequency setting

FOUT2	FOUT1	FOUT0	FOUT frequency
0	0	0	fOSC1 / 1
0	0	1	fOSC1 / 2
0	1	0	fOSC1 / 4
0	1	1	fOSC1 / 8
1	0	0	fOSC3 / 1
1	0	1	fOSC3 / 2
1	1	0	fOSC3 / 4
1	1	1	fOSC3 / 8

fOSC1: OSC1 oscillation frequency
fOSC3: OSC3 oscillation frequency

When the FOUT frequency is made "fOSC3 / n", you must turn on the OSC3 oscillation circuit before outputting FOUT. A time interval of several msec to several 10 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, if an abnormality occurs as the result of an unstable FOUT signal being output externally, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before turning outputting FOUT. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 8, "ELECTRICAL CHARACTERISTICS".)
At initial reset, OSC3 oscillation circuit is set to OFF state.

Since the FOUT signal is generated asynchronously from the register FOUTON, when the signal is turned ON or OFF by the register settings, a hazard of a 1/2 cycle or less is generated.
Figure 5.6.5.6 shows the output waveform of the FOUT signal.

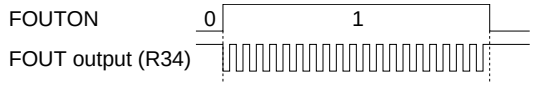


Fig. 5.6.5.6 Output waveform of FOUT signal

■ BZ output (R50)

In order for the S1C88349 to drive an external buzzer, a BZ signal (sound generator output) can be output from the output port terminal R50.
The configuration of the output port R50 is shown in Figure 5.6.5.7.

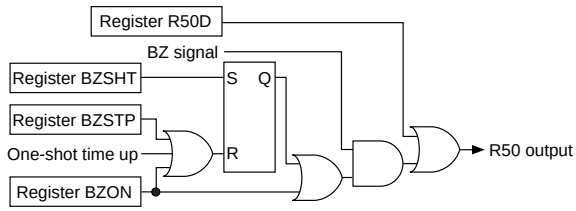


Fig. 5.6.5.7 Configuration of R50

The output control for the BZ signal is done by the registers BZON, BZSHT and BZSTP. When you set "1" for the BZON or BZSHT, the BZ signal is output from the output port terminal R50, when "0" is set for the BZON or "1" is set for the BZSTP, the LOW (VSS) level is output. At this time, "0" must always be set for the data register R50D.

The BZ signal which is output makes use of the output of the sound generator. With respect to control of frequency and envelope, see "5.13 Sound Generator".
Since the BZ signal is generated asynchronously from the registers BZON, BZSHT and BZSTP, when the signal is turned ON or OFF by the register settings, a hazard of a 1/2 cycle or less is generated.
Figure 5.6.5.8 shows the output waveform of the BZ signal.

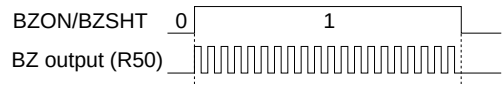


Fig. 5.6.5.8 Output waveform of BZ signal

5.6.6 Control of output ports

Table 5.6.6.1 shows the output port control bits.

Table 5.6.6.1(a) Output port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF70	D7	HZR51	R51 high impedance control	High impedance	Complementary	0	R/W	
	D6	HZR50	R50 high impedance control					
	D5	HZR4H	R/W register	1	0	0	R/W	Reserved register
	D4	HZR4L	R/W register					
	D3	HZR1H	R14–R17 high impedance control	High impedance	Complementary	0	R/W	
	D2	HZR1L	R10–R13 high impedance control					
	D1	HZR0H	R04–R07 high impedance control					
	D0	HZR0L	R00–R03 high impedance control					
00FF71	D7	HZR27	R27 high impedance control	High impedance	Complementary	0	R/W	
	D6	HZR26	R26 high impedance control					
	D5	HZR25	R25 high impedance control					
	D4	HZR24	R24 high impedance control					
	D3	HZR23	R23 high impedance control					
	D2	HZR22	R22 high impedance control					
	D1	HZR21	R21 high impedance control					
	D0	HZR20	R20 high impedance control					
00FF72	D7	HZR37	R37 high impedance control	High impedance	Complementary	0	R/W	
	D6	HZR36	R36 high impedance control					
	D5	HZR35	R35 high impedance control					
	D4	HZR34	R34 high impedance control					
	D3	HZR33	R33 high impedance control					
	D2	HZR32	R32 high impedance control					
	D1	HZR31	R31 high impedance control					
	D0	HZR30	R30 high impedance control					
00FF73	D7	R07D	R07 output port data	High	Low	1	R/W	
	D6	R06D	R06 output port data					
	D5	R05D	R05 output port data					
	D4	R04D	R04 output port data					
	D3	R03D	R03 output port data					
	D2	R02D	R02 output port data					
	D1	R01D	R01 output port data					
	D0	R00D	R00 output port data					
00FF74	D7	R17D	R17 output port data	High	Low	1	R/W	
	D6	R16D	R16 output port data					
	D5	R15D	R15 output port data					
	D4	R14D	R14 output port data					
	D3	R13D	R13 output port data					
	D2	R12D	R12 output port data					
	D1	R11D	R11 output port data					
	D0	R10D	R10 output port data					
00FF75	D7	R27D	R27 output port data	High	Low	1	R/W	
	D6	R26D	R26 output port data					
	D5	R25D	R25 output port data					
	D4	R24D	R24 output port data					
	D3	R23D	R23 output port data					
	D2	R22D	R22 output port data					
	D1	R21D	R21 output port data					
	D0	R20D	R20 output port data					

Table 5.6.6.1(b) Output port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF76	D7	R37D	R37 output port data	High	Low	1	R/W	
	D6	R36D	R36 output port data					
	D5	R35D	R35 output port data					
	D4	R34D	R34 output port data					
	D3	R33D	R33 output port data					
	D2	R32D	R32 output port data					
	D1	R31D	R31 output port data					
	D0	R30D	R30 output port data					
00FF77	D7	R47D	R/W register	1	0	1	R/W	Reserved register
	D6	R46D	R/W register					
	D5	R45D	R/W register					
	D4	R44D	R/W register					
	D3	R43D	R/W register					
	D2	R42D	R/W register					
	D1	R41D	R/W register					
	D0	R40D	R/W register					
00FF78	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	R51D	R51 output port data	High	Low	1	R/W	
	D0	R50D	R50 output port data	High	Low	0	R/W	
00FF10	D7	–	–	–	–	–		Constantry "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	LCCLK	CL output control for expanded LCD driver	On	Off	0	R/W	
	D3	LCFRM	FR output control for expanded LCD driver	On	Off	0	R/W	
	D2	DTFNT	LCD dot font selection	5 x 5 dots	5 x 8 dots	0	R/W	
	D1	LDUTY	LCD drive duty selection	1/16 duty	1/32 duty	0	R/W	*1
	D0	SGOUT	R/W register	1	0	0	R/W	Reserved register
00FF30	D7	–	–	–	–	–		Constantry "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	MODE16	8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D3	CHSEL	TOUT output channel selection	Timer 1	Timer 0	0	R/W	
	D2	PTOUT	TOUT output control	On	Off	0	R/W	
	D1	CKSEL1	Prescaler 1 source clock selection	f_{OSC3}	f_{OSC1}	0	R/W	
	D0	CKSEL0	Prescaler 0 source clock selection	f_{OSC3}	f_{OSC1}	0	R/W	
00FF44	D7	–	–	–	–	–		Constantry "0" when being read
	D6	BZSTP	One-shot buzzer forcibly stop	Forcibly stop	No operation	–	W	
	D5	BZSHT	One-shot buzzer trigger/status R	Busy	Ready	0	R/W	
			W	Trigger	No operation			
	D4	SHTPW	One-shot buzzer duration width selection	125 msec	31.25 msec	0	R/W	
	D3	ENRTM	Envelope attenuation time	1 sec	0.5 sec	0	R/W	
	D2	ENRST	Envelope reset	Reset	No operation	–	W	"0" when being read
	D1	ENON	Envelope On/Off control	On	Off	0	R/W	*2
	D0	BZON	Buzzer output control	On	Off	0	R/W	

*1 Writing "1" to DUTY8 (FF09•D0) disables 1/16 and 1/32 duty selection using LDUTY (FF10•D1).
*2 Reset to "0" during one-shot output.

Table 5.6.6.1(c) Output port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF40	D7	–	–	–	–	–		"0" when being read
	D6	FOUT2	FOUT frequency selection			0	R/W	
	D5	FOUT1	FOUT2 FOUT1 FOUT0 Frequency 0 0 0 fOSC1 / 1 0 0 1 fOSC1 / 2 0 1 0 fOSC1 / 4 0 1 1 fOSC1 / 8 1 0 0 fOSC3 / 1 1 0 1 fOSC3 / 2 1 1 0 fOSC3 / 4 1 1 1 fOSC3 / 8			0	R/W	
	D4	FOUT0				0	R/W	
	D3	FOUTON	FOUT output control	On	Off	0	R/W	
	D2	WDRST	Watchdog timer reset	Reset	No operation	–	W	Constantly "0" when
	D1	TMRST	Clock timer reset	Reset	No operation	–	W	being read
	D0	TMRUN	Clock timer Run/Stop control	Run	Stop	0	R/W	

■ High impedance control

HZR0L, HZR0H: 00FF70H•D0, D1
HZR1L, HZR1H: 00FF70H•D2, D3
HZR20–HZR27: 00FF71H
HZR30–HZR37: 00FF72H
HZR4L, HZR4H: 00FF70H•D4, D5 *1
HZR50, HZR51: 00FF70H•D6, D7

Sets the output terminals to a high impedance state.

When "1" is written: High impedance
When "0" is written: Complementary
Reading: Valid

HZRxx is the high impedance control register which correspond as shown in Table 5.6.3.1 to the various output port terminals.
When "1" is set to the HZRxx register, the corresponding output port terminal becomes high impedance state and when "0" is set, it becomes complementary output.
At initial reset, this register is set to "0" (complimentary).

*1 HZR4L and HZR4H is 2-bit reserved register, it can be used as a general purpose register with read / write capabilities.

■ DC output control

R00D–R07D: 00FF73H
R10D–R17D: 00FF74H
R20D–R27D: 00FF75H
R30D–R37D: 00FF76H
R40D–R47D: 00FF77H *1
R50D, R51D: 00FF78H•D0, D1

Sets the data output from the output port terminal Rxx.

When "1" is written: HIGH level output
When "0" is written: LOW level output
Reading: Valid

RxxD is the data register for each output port.
When "1" is set, the corresponding output port terminal switches to HIGH (V_{DD}) level, and when "0" is set, it switches to LOW (V_{SS}) level.
At initial reset, R50D is set to "0" (LOW level output), all other registers are set to "1" (HIGH level output).
The output data registers set for bus signal output can be used as general purpose registers with read / write capabilities which do not affect the output terminals.

*1 R40D–R47D is 8-bit reserved register, it can be used as a general purpose register with read / write capabilities.

■ Special output control

LCCLK: 00FF10H•D4

Controls the CL (LCD synchronous) signal output.

When "1" is written: CL signal output
When "0" is written: HIGH level (DC) output
Reading: Valid

LCCLK is the output control register for CL signal. When "1" is set, the CL signal is output from the output port terminal R25 and when "0" is set, HIGH (V_{DD}) level is output. At this time, "1" must always be set for the data register R25D.
At initial reset, LCCLK is set to "0" (HIGH level output).

LCFRM: 00FF10H•D3

Controls the FR (LCD frame) signal output.

When "1" is written: FR signal output
When "0" is written: HIGH level (DC) output
Reading: Valid

LCFRM is the output control register for FR signal. When "1" is set, the FR signal is output from the output port terminal R26 and when "0" is set, HIGH (V_{DD}) level is output. At this time, "1" must always be set for the data register R26D.
At initial reset, LCFRM is set to "0" (HIGH level output).

PTOUT: 00FF30H•D2

Controls the TOUT (programmable timer output clock) signal output.

When "1" is written: TOUT signal output
When "0" is written: HIGH level (DC) output
Reading: Valid

PTOUT is the output control register for TOUT signal. When "1" is set, the TOUT signal is output from the output port terminal R27 and when "0" is set, HIGH (V_{DD}) level is output. At this time, "1" must always be set for the data register R27D.
At initial reset, PTOUT is set to "0" (HIGH level output).

FOUTON: 00FF40H•D3

Controls the FOUT (f_{OSC1} / f_{OSC3} dividing clock) signal output.

When "1" is written: FOUT signal output
When "0" is written: HIGH level (DC) output
Reading: Valid

FOUTON is the output control register for FOUT signal. When "1" is set, the FOUT signal is output from the output port terminal R34 and when "0" is set, HIGH (V_{DD}) level is output. At this time, "1" must always be set for the data register R34D.
At initial reset, FOUTON is set to "0" (HIGH level output).

FOUT0, FOUT1, FOUT2: 00FF40H•D4, D5, D6

FOUT signal frequency is set as shown in Table 5.6.6.2.

Table 5.6.6.2 FOUT frequency settings

FOUT2	FOUT1	FOUT0	FOUT frequency
0	0	0	f_{OSC1} / 1
0	0	1	f_{OSC1} / 2
0	1	0	f_{OSC1} / 4
0	1	1	f_{OSC1} / 8
1	0	0	f_{OSC3} / 1
1	0	1	f_{OSC3} / 2
1	1	0	f_{OSC3} / 4
1	1	1	f_{OSC3} / 8

f_{OSC1}: OSC1 oscillation frequency
f_{OSC3}: OSC3 oscillation frequency

At initial reset, this register is set to "0" (f_{OSC1} / 1).

BZON: 00FF44H•D0

Controls the BZ (buzzer) signal output.

When "1" is written: BZ signal output
When "0" is written: LOW level (DC) output
Reading: Valid

BZON is the output control register for BZ signal. When "1" is set, the BZ signal is output from the output port terminal R50 and when "0" is set, LOW (V_{SS}) level is output. At this time, "0" must always be set for the data register R50D.
At initial reset, BZON is set to "0" (LOW level output).

BZSHT: 00FF45H•D5

Controls the one-shot buzzer output.

When "1" is written: Trigger
When "0" is written: No operation

When "1" is read: Busy
When "0" is read: Ready

Writing "1" into BZSHT causes the one-shot output circuit to operate and the BZ signal to be output. The buzzer output is automatically turned OFF after the time set by SHTPW has elapsed. At this time, "0" must always be set for the data register R50D.
The one-shot output is only valid when the normal buzzer output is OFF (BZON = "0") state. The trigger is invalid during ON (BZON = "1") state. When a re-trigger is assigned during a one-shot output, the one-shot output time set with SHTPW is measured again from that point. (time extension)
The operation status of the one-shot output circuit can be confirmed by reading BZSHT, when the one-shot output is ON, BZSHT reads "1" and when the output is OFF, it reads "0".
At initial reset, BZSHT is set to "0" (ready).

BZSTP: 00FF45H•D6

Forcibly stops the one-shot buzzer output.

When "1" is written: Forcibly stop
When "0" is written: No operation
Reading: Constantly "0"

By writing "1" into BZSTP, the one-shot buzzer output can be stopped prior to the elapsing of the time set with SHTPW.
Writing "0" is invalid and writing "1" except during one-shot output is also invalid.
When "1" is written to BZSHT and BZSTP simultaneously, BZSTP takes precedence and one-shot output becomes stop status.
Since BZSTP is for writing only, during readout it is constantly set to "0".

5.6.7 Programming notes

(1) Since the special output signals (CL, FR, TOUT, FOUT and BZ) are generated asynchronously from the output control registers (LCCLK, LCFRM, PTOUT, FOUTON, BZON, BZSHT and BZSTP), when the signals is turned ON or OFF by the output control register settings, a hazard of a 1/2 cycle or less is generated.

(2) When the FOUT frequency is made "f_{OSC3}/n", you must turn on the OSC3 oscillation circuit before outputting FOUT. A time interval of several msec to several 10 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, if an abnormality occurs as the result of an unstable FOUT signal being output externally, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before turning outputting FOUT. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 8, "ELECTRICAL CHARACTERISTICS".)
At initial reset, OSC3 oscillation circuit is set to OFF state.

(3) The SLP instruction has executed when the special output signals (TOUT, FOUT and BZ) are in the enable status, an unstable clock is output for the special output at the time of return from the SLEEP state. Consequently, when shifting to the SLEEP state, you should set the special output signal to the disable status prior to executing the SLP instruction.

5.7 I/O Ports (P ports)

5.7.1 Configuration of I/O ports

The S1C88349 is equipped with 16 bits of I/O ports (P00–P07, P10–P17). The configuration of these I/O ports will vary according to the bus mode as shown below.

Table 5.7.1.1 Configuration of I/O ports

Terminal	Bus mode		
	Single chip	Expanded 64K	Expanded 512K
P00	I/O port P00	Data bus D0	
P01	I/O port P01	Data bus D1	
P02	I/O port P02	Data bus D2	
P03	I/O port P03	Data bus D3	
P04	I/O port P04	Data bus D4	
P05	I/O port P05	Data bus D5	
P06	I/O port P06	Data bus D6	
P07	I/O port P07	Data bus D7	
P10	I/O port P10 (SIN)		
P11	I/O port P11 (SOUT)		
P12	I/O port P12 ($\overline{\text{SCLK}}$)		
P13	I/O port P13 ($\overline{\text{SRDY}}$)		
P14	I/O port P14 (CMPP0/AD4)		
P15	I/O port P15 (CMPM0/AD5)		
P16	I/O port P16 (CMPP1/AD6)		
P17	I/O port P17 (CMPM1/AD7)		

With respect to the data bus, see "5.2 System Controller and Bus Control".
Figure 5.7.1.1 shows the structure of an I/O port.

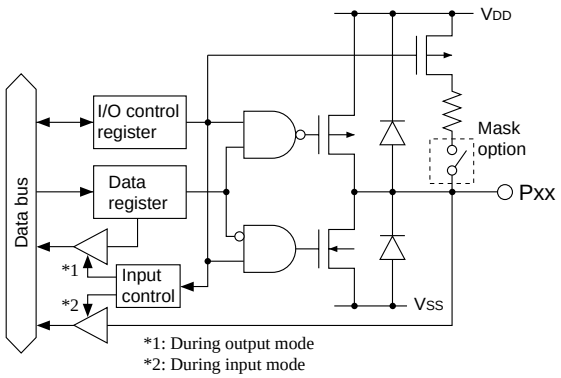


Fig. 5.7.1.1 Structure of I/O port

I/O port can be set for input or output mode in one bit unit. These settings are performed by writing data to the I/O control registers.
I/O port terminals P10–P13 are shared with serial interface input/output terminal and P14–P17 are shared with analog comparator and A/D converter input terminals. The function of each terminals is switchable in software.

With respect to serial interface, analog comparator and A/D converter, see "5.8 Serial Interface", "5.14 Analog Comparator" and "5.15 A/D converter", respectively.

The data registers and I/O control registers of I/O ports set for data bus and serial interface output terminals use are usable as general purpose registers with read/write capabilities which do not affect I/O activities of the terminal.
The same as above, the I/O control register of I/O port set for serial interface input terminal use is usable as general purpose register.

5.7.2 Mask option

I/O port pull-up resistors

P00	☐ With resistor	☐ Gate direct
P01	☐ With resistor	☐ Gate direct
P02	☐ With resistor	☐ Gate direct
P03	☐ With resistor	☐ Gate direct
P04	☐ With resistor	☐ Gate direct
P05	☐ With resistor	☐ Gate direct
P06	☐ With resistor	☐ Gate direct
P07	☐ With resistor	☐ Gate direct
P10	☐ With resistor	☐ Gate direct
P11	☐ With resistor	☐ Gate direct
P12	☐ With resistor	☐ Gate direct
P13	☐ With resistor	☐ Gate direct
P14	☐ With resistor	☐ Gate direct
P15	☐ With resistor	☐ Gate direct
P16	☐ With resistor	☐ Gate direct
P17	☐ With resistor	☐ Gate direct

I/O ports P00–P07 and P10–P17 are equipped with a pull-up resistor which goes ON in the input mode. Whether this resistor is used or not can be selected for each port (one bit unit).
In cases where the 'With resistor' option is selected, the pull-up resistor goes ON when the port is in input mode.
When changing the port terminal from LOW level to HIGH with the built-in pull-up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull-up resistor and the load capacitance of the terminal. It is necessary to set an appropriate wait time for introduction of an I/O port. Make this wait time the amount of time or more calculated by the following expression.

Wait time = R_{IN} x (C_{IN} + load capacitance on the board) x 1.6 [sec]

R_{IN}: Pull up resistance Max. value
C_{IN}: Terminal capacitance Max. value

When the analog comparator or A/D converter is used, select "Gate direct" for I/O ports (P14–P17) which then become input terminals.
For unused I/O ports, select the default setting of "With resistor".

5.7.3 I/O control registers and I/O mode

I/O ports P00–P07 and P10–P17 are set either to input or output modes by writing data to the I/O control registers IOC00–IOC07 and IOC10–IOC17 which correspond to each bit.
To set an I/O port to input mode, write "0" to the I/O control register.
An I/O port which is set to input mode will shift to a high impedance state and functions as an input port. Readout in input mode consists simply of a direct readout of the input terminal state: the data being "1" when the input terminal is at HIGH (V_{DD}) level and "0" when it is at LOW (V_{SS}) level.
When the "With resistor" option is selected using the mask option, the resistor is pulled up onto the port terminal in input mode.
Even in input mode, data can be written to the data registers without affecting the terminal state.
To set an I/O port to output mode, write "1" to the I/O control register. An I/O port which is set to output mode functions as an output port.
When port output data is "1", a HIGH (V_{DD}) level is output and when it is "0", a LOW (V_{SS}) level is output. Readout in output mode consists of the contents of the data register.
At initial reset, I/O control registers are set to "0" (I/O ports are set to input mode).

5.7.4 Control of I/O ports

Table 5.7.4.1 shows the I/O port control bits.

Table 5.7.4.1 I/O port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF60	D7	IOC07	P07 I/O control register	Output	Input	0	R/W	
	D6	IOC06	P06 I/O control register					
	D5	IOC05	P05 I/O control register					
	D4	IOC04	P04 I/O control register					
	D3	IOC03	P03 I/O control register					
	D2	IOC02	P02 I/O control register					
	D1	IOC01	P01 I/O control register					
	D0	IOC00	P00 I/O control register					
00FF61	D7	IOC17	P17 I/O control register	Output	Input	0	R/W	
	D6	IOC16	P16 I/O control register					
	D5	IOC15	P15 I/O control register					
	D4	IOC14	P14 I/O control register					
	D3	IOC13	P13 I/O control register					
	D2	IOC12	P12 I/O control register					
	D1	IOC11	P11 I/O control register					
	D0	IOC10	P10 I/O control register					
00FF62	D7	P07D	P07 I/O port data	High	Low	1	R/W	
	D6	P06D	P06 I/O port data					
	D5	P05D	P05 I/O port data					
	D4	P04D	P04 I/O port data					
	D3	P03D	P03 I/O port data					
	D2	P02D	P02 I/O port data					
	D1	P01D	P01 I/O port data					
	D0	P00D	P00 I/O port data					
00FF63	D7	P17D	P17 I/O port data	High	Low	1	R/W	
	D6	P16D	P16 I/O port data					
	D5	P15D	P15 I/O port data					
	D4	P14D	P14 I/O port data					
	D3	P13D	P13 I/O port data					
	D2	P12D	P12 I/O port data					
	D1	P11D	P11 I/O port data					
	D0	P10D	P10 I/O port data					

P00D–P07D: 00FF62H
P10D–P17D: 00FF63H

How I/O port terminal Pxx data readout and output data settings are performed.

When writing data:

When "1" is written: HIGH level
When "0" is written: LOW level

When the I/O port is set to output mode, the data written is output as is to the I/O port terminal. In terms of port data, when "1" is written, the port terminal goes to HIGH (V_{DD}) level and when "0" is written to a LOW (V_{SS}) level.
Even when the port is in input mode, data can still be written in.

When reading out data:

When "1" is read: HIGH level ("1")
When "0" is read: LOW level ("0")

When an I/O port is in input mode, the voltage level being input to the port terminal is read out. When terminal voltage is HIGH (V_{DD}), it is read as a "1", and when it is LOW (V_{SS}), it is read as a "0". Furthermore, in output mode, the contents of the data register are read out.
At initial reset, this register is set to "1" (HIGH level).

Note: The data registers of I/O ports set for the data bus and output terminal of serial interface can be used as general purpose registers with read/write capabilities which do not affect I/O activities of the terminals.

IOC00–IOC07: 00FF60H
IOC10–IOC17: 00FF61H

Sets the I/O ports to input or output mode.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

IOCxx is the I/O control register which correspond to each I/O port in a bit unit.
Writing "1" to the IOCxx register will switch the corresponding I/O port Pxx to output mode, and writing "0" will switch it to input mode.
When the analog comparator or A/D converter is used, "0" must always be set for the I/O control registers (IOC14–IOC17) of I/O ports which will become input terminals.
At initial reset, this register is set to "0" (input mode).

Note: The data registers of I/O ports set for the data bus and input terminal of serial interface can be used as general purpose registers with read/write capabilities which do not affect I/O activities of the terminals.

5.7.5 Programming notes

(1) When changing the port terminal from LOW level to HIGH with the built-in pull-up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull-up resistor and the load capacitance of the terminal. It is necessary to set an appropriate wait time for introduction of an I/O port. Make this wait time the amount of time or more calculated by the following expression.

Wait time = R_{IN} x (C_{IN} + load capacitance on the board) x 1.6 [sec]

R_{IN}: Pull up resistance Max. value
C_{IN}: Terminal capacitance Max. value

(2) When the analog comparator or A/D converter is used, "0" must always be set for the I/O control registers (IOC14–IOC17) of I/O ports which will become input terminals.

5.8 Serial Interface

5.8.1 Configuration of serial interface

The S1C88349 incorporates a full duplex serial interface (when asynchronous system is selected) that allows the user to select either clock synchronous system or asynchronous system.
The data transfer method can be selected in software.
When the clock synchronous system is selected, 8-bit data transfer is possible.
When the asynchronous system is selected, either 7-bit or 8-bit data transfer is possible, and a parity check of received data and the addition of a parity bit for transmitting data can automatically be done by selecting in software.
Figure 5.8.1.1 shows the configuration of the serial interface.

Serial interface input/output terminals, SIN, SOUT, $\overline{\text{SCLK}}$ and $\overline{\text{SRDY}}$ are shared with I/O ports P10–P13. In order to utilize these terminals for the serial interface input/output terminals, proper settings have to be made with registers ESIF, SMD0 and SMD1. (At initial reset, these terminals are set as I/O port terminals.)
The direction of I/O port terminals set for serial interface input/output terminals are determined by the signal and transfer mode for each terminal. Furthermore, the settings for the corresponding I/O control registers for the I/O ports become invalid.

Table 5.8.1.1 Configuration of input/output terminals

Terminal	When serial interface is selected
P10	SIN
P11	SOUT
P12	$\overline{\text{SCLK}}$
P13	$\overline{\text{SRDY}}$

* The terminals used may vary depending on the transfer mode.

SIN and SOUT are serial data input and output terminals which function identically in clock synchronous system and asynchronous system. $\overline{\text{SCLK}}$ is exclusively for use with clock synchronous system and functions as a synchronous clock input/output terminal. $\overline{\text{SRDY}}$ is exclusively for use in clock synchronous slave mode and functions as a send-receive ready signal output terminal.
When asynchronous system is selected, since $\overline{\text{SCLK}}$ and $\overline{\text{SRDY}}$ are superfluous, the I/O port terminals P12 and P13 can be used as I/O ports.
In the same way, when clock synchronous master mode is selected, since $\overline{\text{SRDY}}$ is superfluous, the I/O port terminal P13 can be used as I/O port.

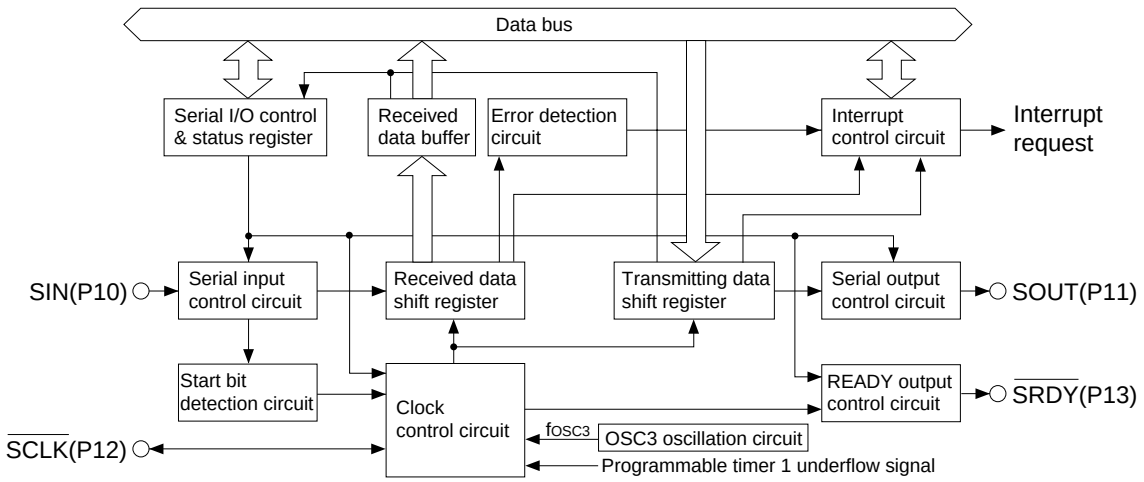


Fig. 5.8.1.1 Configuration of serial interface

5.8.2 Mask option

Since serial interface input/output terminals are shared with the I/O ports, serial interface terminal specifications have necessarily been selected with the mask option for I/O ports.

I/O port pull-up resistors
P10 (SIN) ..... ☐ With resistor ☐ Gate direct
P12 (SCLK) .... ☐ With resistor ☐ Gate direct

Each I/O port terminal is equipped with a pull-up resistor which goes ON in input mode. A selection can be made for each port (one bit unit) as to whether or not the resistor will be used.
Specifications (whether the pull-up will be used or not) of P10 (SIN) and P12 (SCLK) which will become input terminals when using the serial interface are decided by settings the options for the I/O port.

When "Gate direct" is selected in the serial I/F mode, be sure that the input terminals do not go into a floating state.

5.8.3 Transfer modes

There are four transfer modes for the serial interface and mode selection is made by setting the two bits of the mode selection registers SMD0 and SMD1 as shown in the table below.

Table 5.8.3.1 Transfer modes

SMD1	SMD0	Mode
1	1	Asynchronous 8-bit
1	0	Asynchronous 7-bit
0	1	Clock synchronous slave
0	0	Clock synchronous master

Table 5.8.3.2 Terminal settings corresponding to each transfer mode

Mode	SIN	SOUT	SCLK	SRDY
Asynchronous 8-bit	Input	Output	P12	P13
Asynchronous 7-bit	Input	Output	P12	P13
Clock synchronous slave	Input	Output	Input	Output
Clock synchronous master	Input	Output	Output	P13

At initial reset, transfer mode is set to clock synchronous master mode.

■ Clock synchronous master mode

In this mode, the internal clock is utilized as a synchronous clock for the built-in shift registers, and clock synchronous 8-bit serial transfers can be performed with this serial interface as the master.
The synchronous clock is also output from the SCLK terminal which enables control of the external (slave side) serial I/O device. Since the SRDY terminal is not utilized in this mode, it can be used as an I/O port.
Figure 5.8.3.1(a) shows the connection example of input/output terminals in the clock synchronous master mode.

■ Clock synchronous slave mode

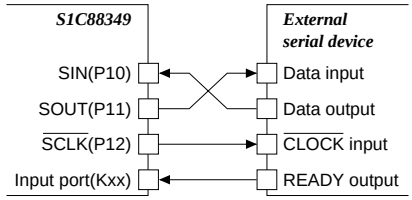
In this mode, a synchronous clock from the external (master side) serial input/output device is utilized and clock synchronous 8-bit serial transfers can be performed with this serial interface as the slave.
The synchronous clock is input to the SCLK terminal and is utilized by this interface as the synchronous clock.
Furthermore, the SRDY signal indicating the transmit-receive ready status is output from the SRDY terminal in accordance with the serial interface operating status.
In the slave mode, the settings for registers SCS0 and SCS1 used to select the clock source are invalid.
Figure 5.8.3.1(b) shows the connection example of input/output terminals in the clock synchronous slave mode.

■ Asynchronous 7-bit mode

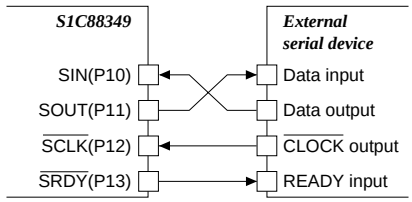
In this mode, asynchronous 7-bit transfer can be performed. Parity check during data reception and addition of parity bit (odd/even/none) during transmitting can be specified and data processed in 7 bits with or without parity. Since this mode employs the internal clock, the SCLK terminal is not used. Furthermore, since the SRDY terminal is not utilized either, both of these terminals can be used as I/O ports.
Figure 5.8.3.1(c) shows the connection example of input/output terminals in the asynchronous mode.

■ Asynchronous 8-bit mode

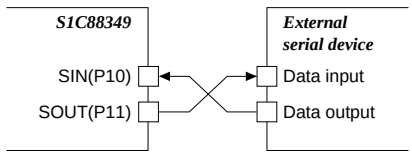
In this mode, asynchronous 8-bit transfer can be performed. Parity check during data reception and addition of parity bit (odd/even/none) during transmitting can be specified and data processed in 8 bits with or without parity. Since this mode employs the internal clock, the SCLK terminal is not used. Furthermore, since the SRDY terminal is not utilized either, both of these terminals can be used as I/O ports.
Figure 5.8.3.1(c) shows the connection example of input/output terminals in the asynchronous mode.



(a) Clock synchronous master mode



(b) Clock synchronous slave mode



(c) Asynchronous 7-bit/8-bit mode

Fig. 5.8.3.1 Connection examples of serial interface I/O terminals

5.8.4 Clock source

There are four clock sources and selection is made by setting the two bits of the clock source selection register SCS0 and SCS1 as shown in table below.

Table 5.8.4.1 Clock source

SCS1	SCS0	Clock source
1	1	Programmable timer
1	0	fOSC3 / 4
0	1	fOSC3 / 8
0	0	fOSC3 / 16

This register setting is invalid in clock synchronous slave mode and the external clock input from the SCLK terminal is used.
When the "programmable timer" is selected, the programmable timer 1 underflow signal is divided by 1/2 and this signal used as the clock source.
With respect to the transfer rate setting, see "5.11 Programmable Timer".
At initial reset, the synchronous clock is set to "fOSC3 / 16".
Whichever clock is selected, the signal is further divided by 1/16 and then used as the synchronous clock.
Furthermore, external clock input is used as is for SCLK in clock synchronous slave mode.
Table 5.8.4.2 shows an examples of transfer rates and OSC3 oscillation frequencies when the clock source is set to programmable timer.
When the demultiplied signal of the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
A time interval of several msec to several 10 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before starting transmitting / receiving of serial interface. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 8, "ELECTRICAL CHARACTERISTICS".)
At initial reset, the OSC3 oscillation circuit is set to OFF status.

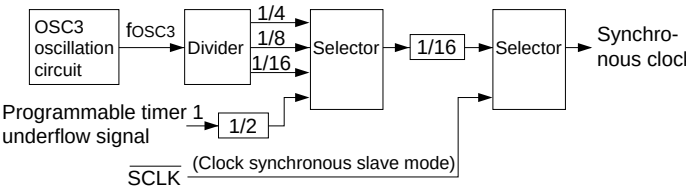


Fig. 5.8.4.1 Division of the synchronous clock

Table 5.8.4.2 OSC3 oscillation frequencies and transfer rates

Transfer rate (bps)	OSC3 oscillation frequency / Programmable timer settings					
	fOSC3 = 3.072 MHz		fOSC3 = 4.608 MHz		fOSC3 = 4.9152 MHz	
	PSC1X	RLD1X	PSC1X	RLD1X	PSC1X	RLD1X
9,600	0 (1/1)	09H	0 (1/1)	0EH	0 (1/1)	0FH
4,800	0 (1/1)	13H	0 (1/1)	1DH	0 (1/1)	1FH
2,400	0 (1/1)	27H	0 (1/1)	3BH	0 (1/1)	3FH
1,200	0 (1/1)	4FH	0 (1/1)	77H	0 (1/1)	7FH
600	0 (1/1)	9FH	0 (1/1)	EFH	0 (1/1)	FFH
300	1 (1/4)	4FH	1 (1/4)	77H	1 (1/4)	7FH
150	1 (1/4)	9FH	1 (1/4)	EFH	1 (1/4)	FFH

5.8.5 Transmit-receive control

Below is a description of the registers which handle transmit-receive control. With respect to transmit-receive control procedures and operations, please refer to the following sections in which these are discussed on a mode by mode basis.

■ Shift register and received data buffer

Exclusive shift registers for transmitting and receiving are installed in this serial interface. Consequently, duplex communication simultaneous transmit and receive is possible when the asynchronous system is selected.

Data being transmitted are written to TRXD0–TRXD7 and converted to serial through the shift register and is output from the SOUT terminal.

In the reception section, a received data buffer is installed separate from the shift register.
Data being received are input to the SIN terminal and is converted to parallel through the shift register and written to the received data buffer. Since the received data buffer can be read even during serial input operation, the continuous data is received efficiently.
However, since buffer functions are not used in clock synchronous mode, be sure to read out data before the next data reception begins.

■ Transmit enable register and transmit control bit

For transmitting control, use the transmit enable register TXEN and transmit control bit TXTRG.

The transmit enable register TXEN is used to set the transmitting enable / disable status. When "1" is written to this register to set the transmitting enable status, clock input to the shift register is enabled and the system is ready to transmit data. In the clock synchronous mode, synchronous clock input / output from the $\overline{\text{SCLK}}$ terminal is also enabled.

The transmit control bit TXTRG is used as the trigger to start transmitting data.
Data to be transmitted is written to the transmit data shift register, and when transmitting preparations a recomplete, "1" is written to TXTRG whereupon data transmitting begins.
When interrupt has been enabled, an interrupt is generated when the transmission is completed. If there is subsequent data to be transmitted it can be sent using this interrupt.

In addition, TXTRG can be read as the status. When set to "1", it indicates transmitting operation, and "0" indicates transmitting stop.
For details on timing, see the timing chart which gives the timing for each mode.

When not transmitting, set TXEN to "0" to disable transmitting status.

■ Receive enable register, receive control bit

For receiving control, use the receive enable register RXEN and receive control bit RXTRG.
Receive enable register RXEN is used to set receiving enable / disable status. When "1" is written into this register to set the receiving enable status, clock input to the shift register is enabled and the system is ready to receive data. In the clock synchronous mode, synchronous clock input / output from the $\overline{\text{SCLK}}$ terminal is also enabled.
With the above setting, receiving begins and serial data input from the SIN terminal goes to the shift register.
The operation of the receive control bit RXTRG is slightly different depending on whether a clock synchronous system or an asynchronous system is being used.
In the clock synchronous system, the receive control bit TXTRG is used as the trigger to start receiving data.
When received data has been read and the preparation for next data receiving is completed, write "1" into RXTRG to start receiving. (When "1" is written to RXTRG in slave mode, $\overline{\text{SRDY}}$ switches to "0".)
In an asynchronous system, RXTRG is used to prepare for next data receiving. After reading the received data from the received data buffer, write "1" into RXTRG to signify that the received data buffer is empty. If "1" is not written into RXTRG, the overrun error flag OER will be set to "1" when the next receiving operation is completed. (An overrun error will be generated when receiving is completed between reading the received data and the writing of "1" to RXTRG.)
In addition, RXTRG can be read as the status. In either clock synchronous mode or asynchronous mode, when RXTRG is set to "1", it indicates receiving operation and when set to "0", it indicates that receiving has stopped.
For details on timing, see the timing chart which gives the timing for each mode.

When you do not receive, set RXEN to "0" to disable receiving status.

5.8.6 Operation of clock synchronous transfer

Clock synchronous transfer involves the transfer of 8-bit data by synchronizing it to eight clocks. The same synchronous clock is used by both the transmitting and receiving sides.
When the serial interface is used in the master mode, the clock signal selected using SCS0 and SCS1 is further divided by 1/16 and employed as the synchronous clock. This signal is then sent via the $\overline{\text{SCLK}}$ terminal to the slave side (external serial I/O device).
When used in the slave mode, the clock input to the $\overline{\text{SCLK}}$ terminal from the master side (external serial input/output device) is used as the synchronous clock.

In the clock synchronous mode, since one clock line ($\overline{\text{SCLK}}$) is shared for both transmitting and receiving, transmitting and receiving cannot be performed simultaneously. (Half duplex only is possible in clock synchronous mode.)

Transfer data is fixed at 8 bits and both transmitting and receiving are conducted with the LSB (bit 0) coming first.

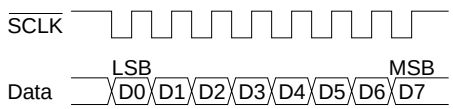


Fig. 5.8.6.1 Transfer data configuration using clock synchronous mode

Below is a description of initialization when performing clock synchronous transfer, transmit-receive control procedures and operations.
With respect to serial interface interrupt, see "5.8.8 Interrupt function".

■ Initialization of serial interface

When performing clock synchronous transfer, the following initial settings must be made.

(1) Setting of transmitting/receiving disable
To set the serial interface into a status in which both transmitting and receiving are disabled, "0" must be written to both the transmit enable register TXEN and the receive enable register RXEN. Fix these two registers to a disable status until data transfer actually begins.

(2) Port selection
Because serial interface input/output ports SIN, SOUT, $\overline{\text{SCLK}}$ and $\overline{\text{SRDY}}$ are set as I/O port terminals P10–P13 at initial reset, "1" must be written to the serial interface enable register ESIF in order to set these terminals for serial interface use.

(3) Setting of transfer mode
Select the clock synchronous mode by writing the data as indicated below to the two bits of the mode selection registers SMD0 and SMD1.

Master mode: SMD0 = "0", SMD1 = "0"
Slave mode: SMD0 = "1", SMD1 = "0"

(4) Clock source selection
In the master mode, select the synchronous clock source by writing data to the two bits of the clock source selection registers SCS0 and SCS1. (See Table 5.8.4.1.)
This selection is not necessary in the slave mode.

Since all the registers mentioned in (2)–(4) are assigned to the same address, it's possible to set them all with one instruction. The parity enable register EPR is also assigned to this address, however, since parity is not necessary in the clock synchronous mode, parity check will not take place regardless of how they are set.

(5) Clock source control
When the master mode is selected and programmable timer for the clock source is selected, set transfer rate on the programmable timer side. (See "5.11 Programmable Timer".)
When the divided signal of OSC3 oscillation circuit is selected for the clock source, be sure that the OSC3 oscillation circuit is turned ON prior to commencing data transfer. (See "5.4 Oscillation Circuits and Operating Mode".)

■ Data transmit procedure

The control procedure and operation during transmitting is as follows.

(1) Write "0" in the transmit enable register TXEN and the receive enable register RXEN to reset the serial interface.

(2) Write "1" in the transmit enable register TXEN to set into the transmitting enable status.

(3) Write the transmitting data into TRXD0–TRXD7.

(4) In case of the master mode, confirm the receive ready status on the slave side (external serial input / output device), if necessary. Wait until it reaches the receive ready status.

(5) Write "1" in the transmit control bit TXTRG and start transmitting.

In the master mode, this control causes the synchronous clock to change to enable and to be provided to the shift register for transmitting and output from the $\overline{SCLK}$ terminal.
In the slave mode, it waits for the synchronous clock to be input from the $\overline{SCLK}$ terminal.
The transmitting data of the shift register shifts one bit at a time at each falling edge of the synchronous clock and is output from the SOUT terminal. When the final bit (MSB) is output, the SOUT terminal is maintained at that level, until the next transmitting begins.

The transmitting complete interrupt factor flag FSTRA is set to "1" at the point where the data transmitting of the shift register is completed. When interrupt has been enabled, a transmitting complete interrupt is generated at this point.
Set the following transmitting data using this interrupt.

(6) Repeat steps (3) to (5) for the number of bytes of transmitting data, and then set the transmit disable status by writing "0" to the transmit enable register TXEN, when the transmitting is completed.

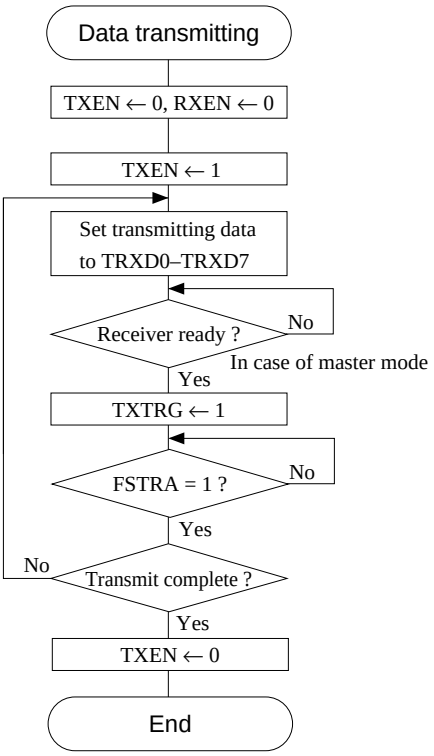


Fig. 5.8.6.2 Transmit procedure in clock synchronous mode

■ Data receive procedure

The control procedure and operation during receiving is as follows.

(1) Write "0" in the receive enable register RXEN and transmit enable register TXEN to reset the serial interface.

(2) Write "1" in the receive enable register RXEN to set into the receiving enable status.

(3) In case of the master mode, confirm the transmit ready status on the slave side (external serial input / output device), if necessary. Wait until it reaches the transmit ready status.

(4) Write "1" in the receive control bit RXTRG and start receiving.

In the master mode, this control causes the synchronous clock to change to enable and is provided to the shift register for receiving and output from the $\overline{SCLK}$ terminal.
In the slave mode, it waits for the synchronous clock to be input from the $\overline{SCLK}$ terminal. The received data input from the SIN terminal is successively incorporated into the shift register in synchronization with the rising edge of the synchronous clock.
At the point where the data of the 8th bit has been incorporated at the final (8th) rising edge of the synchronous clock, the content of the shift register is sent to the received data buffer and the receiving complete interrupt factor flag FSREC is set to "1". When interrupt has been enabled, a receiving complete interrupt is generated at this point.

(5) Read the received data from TRXD0–TRXD7 using receiving complete interrupt.

(6) Repeat steps (3) to (5) for the number of bytes of receiving data, and then set the receive disable status by writing "0" to the receive enable register RXEN, when the receiving is completed.

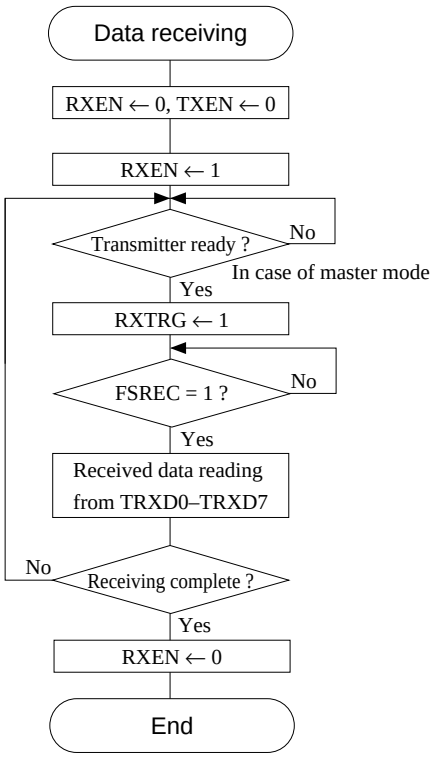


Fig. 5.8.6.3 Receiving procedure in clock synchronous mode

■ Transmit/receive ready ($\overline{\text{SRDY}}$) signal

When this serial interface is used in the clock synchronous slave mode (external clock input), an $\overline{\text{SRDY}}$ signal is output to indicate whether or not this serial interface can transmit / receive to the master side (external serial input / output device). This signal is output from the $\overline{\text{SRDY}}$ terminal and when this interface enters the transmit or receive enable (READY) status, it becomes "0" (LOW level) and becomes "1" (HIGH level) when there is a BUSY status, such as during transmit / receive operation.

The $\overline{\text{SRDY}}$ signal changes the "1" to "0," immediately after writing "1" into the transmit control bit TXTRG or the receive control bit RXTRG and returns from "0" to "1", at the point where the first synchronous clock has been input (falling edge). When you have set in the master mode, control the transfer by inputting the same signal from the slave side using the input port or I / O port. At this time, since the $\overline{\text{SRDY}}$ terminal is not set and instead P13 functions as the I / O port, you can apply this port for said control.

■ Timing chart

The timing chart for the clock synchronous system transmission is shown in Figure 5.8.6.4.

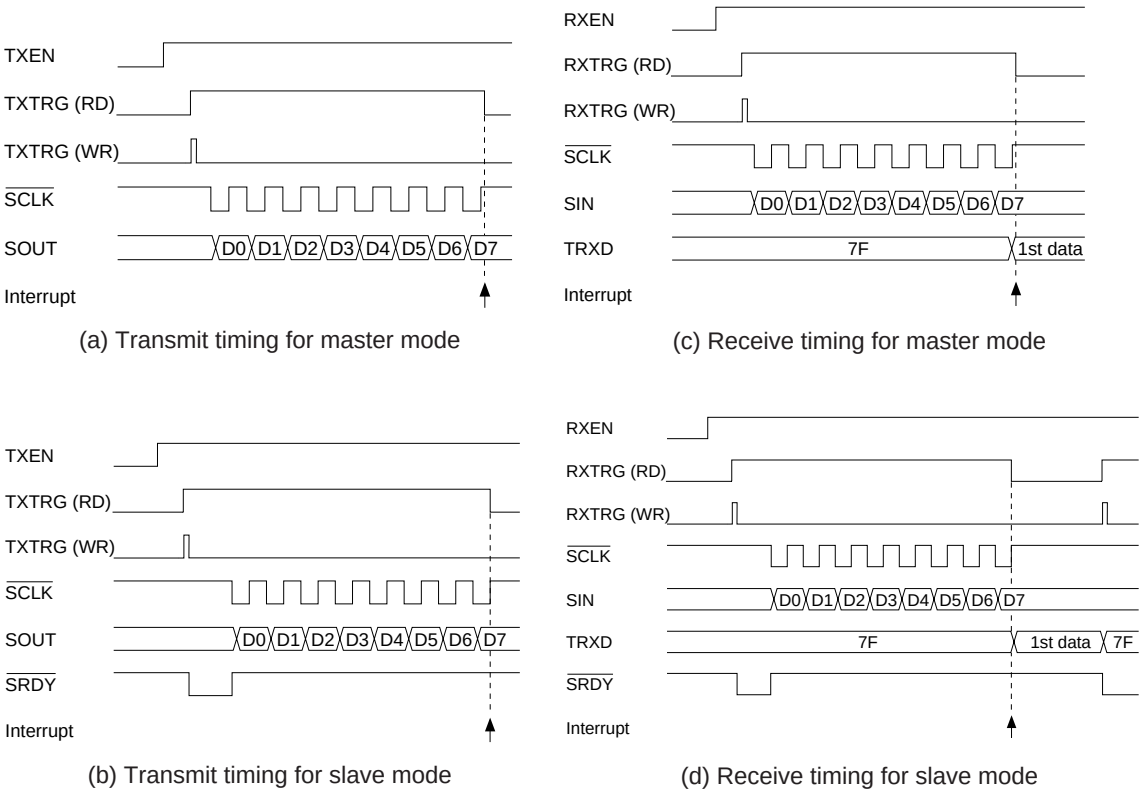
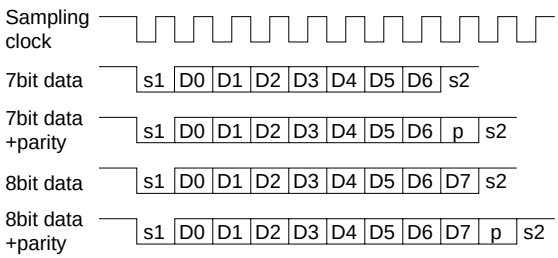


Fig. 5.8.6.4 Timing chart (clock synchronous system transmission)

5.8.7 Operation of asynchronous transfer

Asynchronous transfer is a mode that transfers by adding a start bit and a stop bit to the front and the back of each piece of serial converted data. In this mode, there is no need to use a clock that is fully synchronized clock on the transmit side and the receive side, but rather transmission is done while adopting the synchronization at the start / stop bits that have attached before and after each piece of data. The RS-232C interface functions can be easily realized by selecting this transfer mode.
This interface has separate transmit and receive shift registers and is designed to permit full duplex transmission to be done simultaneously for transmitting and receiving.

For transfer data in the asynchronous 7-bit mode, either 7 bits data (no parity) or 7 bits data + parity bit can be selected. In the asynchronous 8-bit mode, either 8 bits data (no parity) or 8 bits data + parity bit can be selected.
Parity can be even or odd, and parity checking of received data and adding a party bit to transmitting data will be done automatically. Thereafter, it is not necessary to be conscious of parity itself in the program.
The start bit and stop bit are respectively fixed at one bit and data is transmitted and received by placing the LSB (bit 0) at the front.



s1 : Start bit (Low level, 1 bit)
s2 : Stop bit (High level, 1 bit)
p : Parity bit

Fig. 5.8.7.1 Transfer data configuration for asynchronous system

Here following, we will explain the control sequence and operation for initialization and transmitting / receiving in case of asynchronous data transfer. See "5.8.8 Interrupt function" for the serial interface interrupts.

■ Initialization of serial interface

The below initialization must be done in cases of asynchronous system transfer.

(1) Setting of transmitting/receiving disable
To set the serial interface into a status in which both transmitting and receiving are disabled, "0" must be written to both the transmit enable register TXEN and the receive enable register RXEN. Fix these two registers to a disable status until data transfer actually begins.

(2) Port selection
Because serial interface input / output terminals SIN and SOUT are set as I / O port terminals P10 and P11 at initial reset, "1" must be written to the serial interface enable register ESIF in order to set these terminals for serial interface use. $\overline{SCLK}$ and $\overline{SRDY}$ terminals set in the clock synchronous mode are not used in the asynchronous mode. These terminals function as I / O port terminals P12 and P13.

(3) Setting of transfer mode
Select the asynchronous mode by writing the data as indicated below to the two bits of the mode selection registers SMD0 and SMD1.

7-bit mode: SMD0 = "0", SMD1 = "1"
8-bit mode: SMD0 = "1", SMD1 = "1"

(4) Parity bit selection
When checking and adding parity bits, write "1" into the parity enable register EPR to set to "with parity check". As a result of this setting, in the asynchronous 7-bit mode, it has a 7 bits data + parity bit configuration and in the asynchronous 8-bit mode it has an 8 bits data + parity bit configuration.In this case, parity checking for receiving and adding a party bit for transmitting is done automatically in hardware. Moreover, when "with parity check" has been selected, "odd" or "even" parity must be further selected in the parity mode selection register PMD.
When "0" is written to the PMD register to select "without parity check" in the asynchronous 7-bit mode, data configuration is set to 7 bits data (no parity) and in the asynchronous 8-bit mode (no parity) it is set to 8 bits data (no parity) and parity checking and parity bit adding will not be done.

(5) Clock source selection
Select the clock source by writing data to the two bits of the clock source selection registers SCS0 and SCS1. (See Table 5.8.4.1.)

Since all the registers mentioned in (2)–(5) are assigned to the same address, it's possible to set them all with one instruction.

(6) Clock source control
When the programmable timer is selected for the clock source, set transfer rate on the programmable timer side. (See "5.11 Programmable Timer".)
When the divided signal of OSC3 oscillation circuit is selected for the clock source, be sure that the OSC3 oscillation circuit is turned ON prior to commencing data transfer. (See "5.4 Oscillation Circuits and Operating Mode".)

■ Data transmit procedure

The control procedure and operation during transmitting is as follows.

(1) Write "0" in the transmit enable register TXEN to reset the serial interface.

(2) Write "1" in the transmit enable register TXEN to set into the transmitting enable status.

(3) Write the transmitting data into TRXD0–TRXD7. Also, when 7-bit data is selected, the TRXD7 data becomes invalid.

(4) Write "1" in the transmit control bit TXTRG and start transmitting.
This control causes the shift clock to change to enable and a start bit (LOW) is output to the SOUT terminal in synchronize to its rising edge. The transmitting data set to the shift register is shifted one bit at a time at each rising edge of the clock thereafter and is output from the SOUT terminal. After the data output, it outputs a stop bit (HIGH) and HIGH level is maintained until the next start bit is output.

The transmitting complete interrupt factor flag FSTRA is set to "1" at the point where the data transmitting is completed. When interrupt has been enabled, a transmitting complete interrupt is generated at this point.
Set the following transmitting data using this interrupt.

(5) Repeat steps (3) to (4) for the number of bytes of transmitting data, and then set the transmit disable status by writing "0" to the transmit enable register TXEN, when the transmitting is completed.

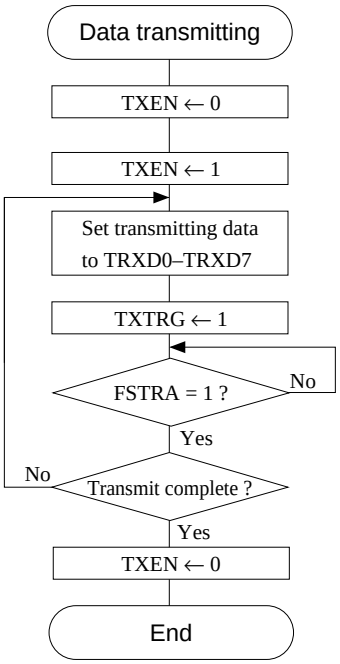


Fig. 5.8.7.2 Transmit procedure in asynchronous mode

■ Data receive procedure

The control procedure and operation during receiving is as follows.

(1) Write "0" in the receive enable register RXEN to set the receiving disable status and to reset the respective PER, OER, FER flags that indicate parity, overrun and framing errors.

(2) Write "1" in the receive enable register RXEN to set into the receiving enable status.

(3) The shift clock will change to enable from the point where the start bit (LOW) has been input from the SIN terminal and the receive data will be synchronized to the rising edge following the second clock, and will thus be successively incorporated into the shift register.
After data bits have been incorporated, the stop bit is checked and, if it is not HIGH, it becomes a framing error and the error interrupt factor flag FSERR is set to "1". When interrupt has been enabled, an error interrupt is generated at this point.
When receiving is completed, data in the shift register is transferred to the received data buffer and the receiving complete interrupt flag FSREC is set to "1". When interrupt has been enabled, a receiving complete interrupt is generated at this point. (When an overrun error is generated, the interrupt factor flag FSREC is not set to "1" and a receiving complete interrupt is not generated.)
If "with parity check" has been selected, a parity check is executed when data is transferred into the received data buffer from the shift register and if a parity error is detected, the error interrupt factor flag is set to "1". When the interrupt has been enabled, an error interrupt is generated at this point just as in the framing error mentioned above.

(4) Read the received data from TRXD0–TRXD7 using receiving complete interrupt.

(5) Write "1" to the receive control bit RXTRG to inform that the receive data has been read out. When the following data is received prior to writing "1" to RXTRG, it is recognized as an overrun error and the error interrupt factor flag is set to "1". When the interrupt has been enabled, an error interrupt is generated at this point just as in the framing error and parity error mentioned above.

(6) Repeat steps (3) to (5) for the number of bytes of receiving data, and then set the receive disable status by writing "0" to the receive enable register RXEN, when the receiving is completed.

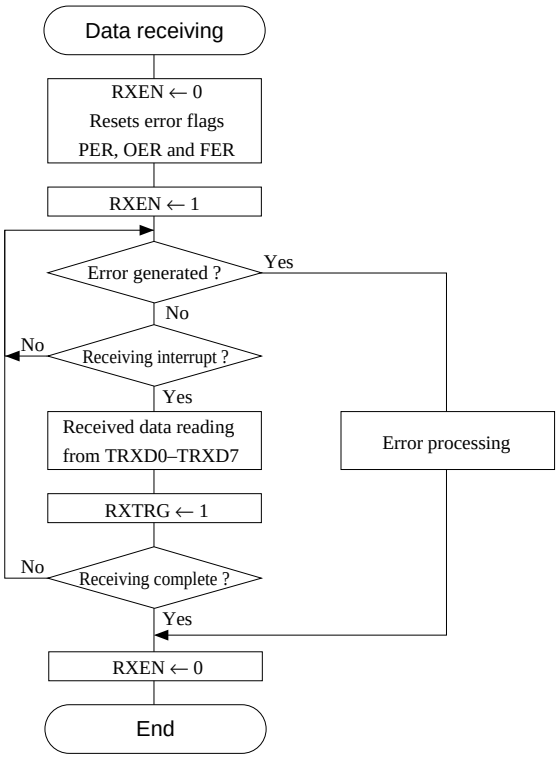


Fig. 5.8.7.3 Receiving procedure in asynchronous mode

■ Receive error

During receiving the following three types of errors can be detected by an interrupt.

(1) Parity error

When writing "1" to the EPR register to select "with parity check", a parity check (vertical parity check) is executed during receiving. After each data bit is sent a parity check bit is sent. The parity check bit is a "0" or a "1". Even parity checking will cause the sum of the parity bit and the other bits to be even. Odd parity causes the sum to be odd. This is checked on the receiving side.

The parity check is performed when data received in the shift register is transferred to the received data buffer. It checks whether the parity check bit is a "1" or a "0" (the sum of the bits including the parity bit) and the parity set in the PMD register match. When it does not match, it is recognized as an parity error and the parity error flag PER and the error interrupt factor flag FSERR is set to "1".

When interrupt has been enabled, an error interrupt is generated at this point.

The PER flag is reset to "0" by writing "1".

Even when this error has been generated, the received data corresponding to the error is transferred in the received data buffer and the receive operation also continues.

The received data at this point cannot assured because of the parity error.

(2) Framing error

In asynchronous transfer, synchronization is adopted for each character at the start bit ("0") and the stop bit ("1"). When receiving has been done with the stop bit set at "0", the serial interface judges the synchronization to be off and a framing error is generated. When this error is generated, the framing error flag FER and the error interrupt factor flag FSERR are set to "1". When interrupt has been enabled, an error interrupt is generated at this point.

The FER flag is reset to "0" by writing "1".

Even when this error has been generated, the received data for it is loaded into the receive data buffer and the receive operation also continues. However, even when it does not become a framing error with the following data receipt, such data cannot be assured.

Even when this error has been generated, the received data corresponding to the error is transferred in the received data buffer and the receive operation also continues. However, even when it does not become a framing error with the following data receiving, such data cannot be assured.

(3) Overrun error

When the next data is received before "1" is written to RXTRG, an overrun error will be generated, because the previous receive data will be overwritten. When this error is generated, the overrun error flag OER and the error interrupt factor flag FSERR are set to "1". When interrupt has been enabled, an error interrupt is generated at this point. The OER flag is reset to "0" by writing "1" into it.

Even when this error has been generated, the received data corresponding to the error is transferred in the received data buffer and the receive operation also continues.

Furthermore, when the timing for writing "1" to RXTRG and the timing for the received data transfer to the received data buffer overlap, it will be recognized as an overrun error.

■ Timing chart

Figure 5.8.7.4 show the asynchronous transfer timing chart.

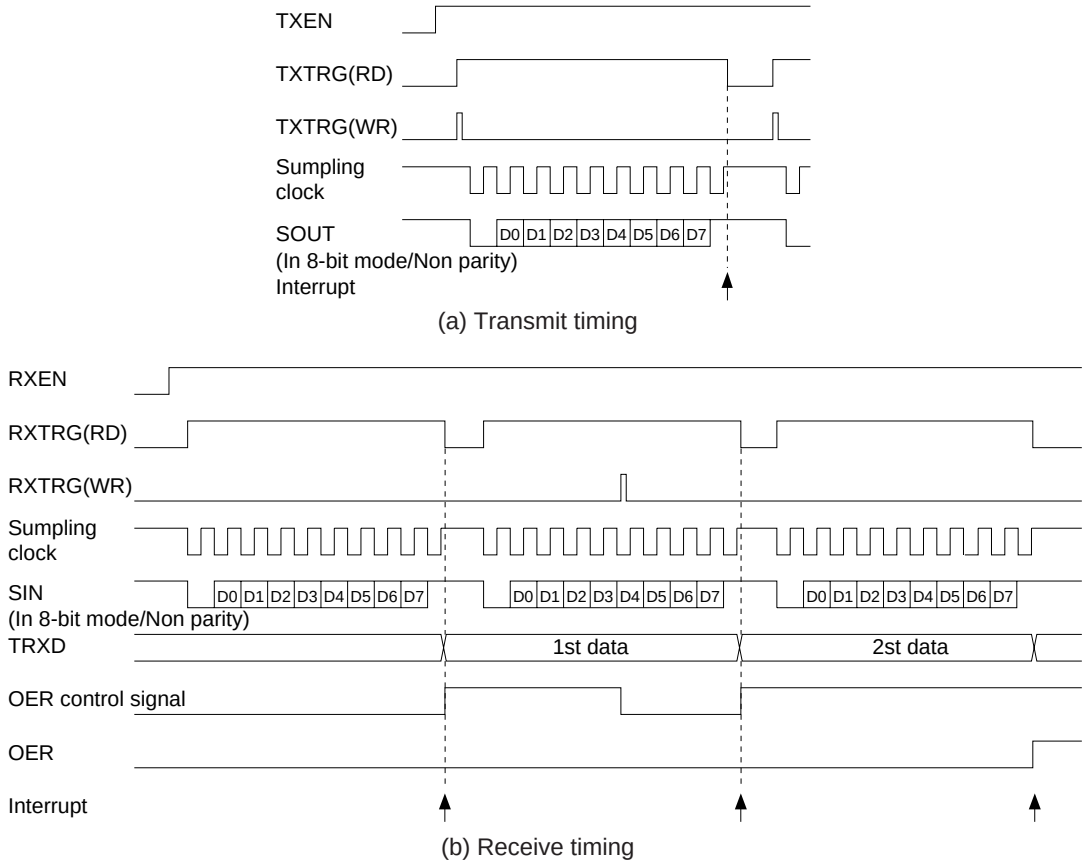


Fig. 5.8.7.4 Timing chart (asynchronous transfer)

5.8.8 Interrupt function

This serial interface includes a function that generates the below indicated three types of interrupts.

- **Transmitting complete interrupt**
- **Receiving complete interrupt**
- **Error interrupt**

The interrupt factor flag FSxxx and the interrupt enable register ESxxx for the respective interrupt factors are provided and then the interrupt enable / disable can be selected by the software. In addition, a priority level of the serial interface interrupt for the CPU can be optionally set at levels 0 to 3 by the interrupt priority registers PSIF0 and PSIF1.
For details on the above mentioned interrupt control register and the operation following generation of an interrupt, see "5.17 Interrupt and Standby Status".
Figure 5.8.8.1 shows the configuration of the serial interface interrupt circuit.

■ Transmitting complete interrupt

This interrupt factor is generated at the point where the sending of the data written into the shift register has been completed and sets the interrupt factor flag FSTRA to "1". When set in this manner, if the corresponding interrupt enable register ESTRA is set to "1" and the corresponding interrupt priority registers PSIF0 and PSIF1 are set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU.
When "0" has been written into the interrupt enable register ESTRA and interrupt has been disabled, an interrupt is not generated to the CPU. Even in this case, the interrupt factor flag FSTRA is set to "1".
The interrupt factor flag FSTRA is reset to "0" by writing "1".
The following transmitting data can be set and the transmitting start (writing "1" to TXTRG) can be controlled by generation of this interrupt factor.
The exception processing vector address for this interrupt factor is set at 000014H.

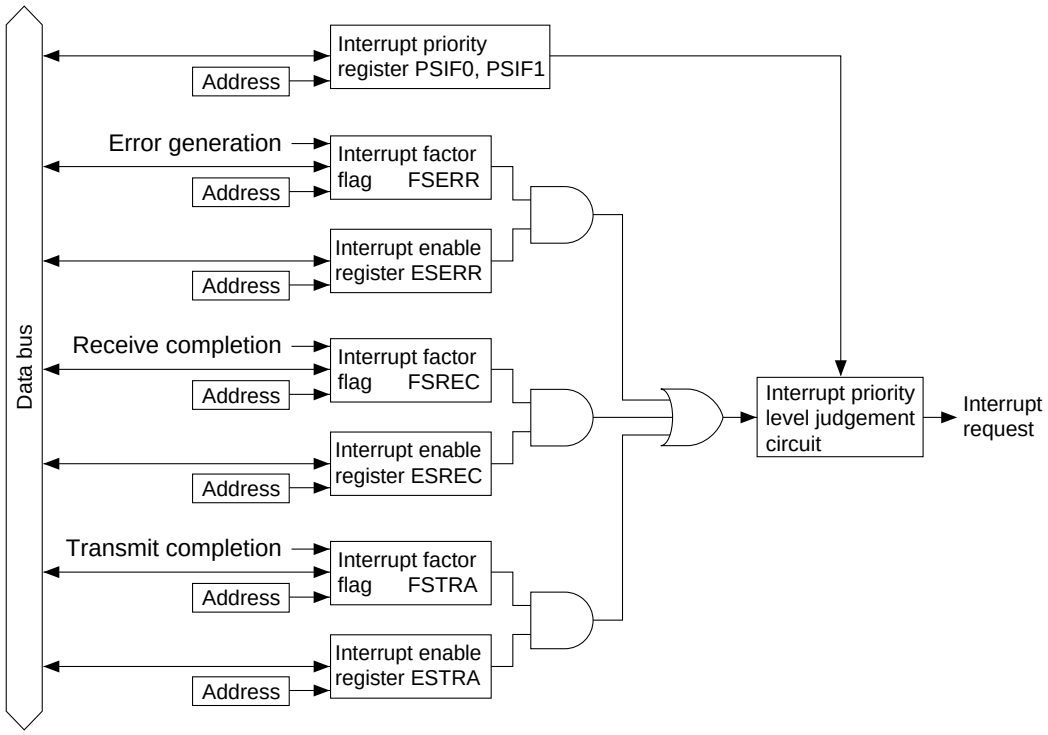


Fig. 5.8.8.1 Configuration of serial interface interrupt circuit

■ Receiving complete interrupt

This interrupt factor is generated at the point where receiving has been completed and the receive data incorporated into the shift register has been transferred into the received data buffer and it sets the interrupt factor flag FSREC to "1". When set in this manner, if the corresponding interrupt enable register ESREC is set to "1" and the corresponding interrupt priority registers PSIF0 and PSIF1 are set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU. When "0" has been written into the interrupt enable register ESREC and interrupt has been disabled, an interrupt is not generated to the CPU. Even in this case, the interrupt factor flag FSREC is set to "1". The interrupt factor flag FSREC is reset to "0" by writing "1".

The generation of this interrupt factor permits the received data to be read.

Also, the interrupt factor flag is set to "1" when a parity error or framing error is generated.

The exception processing vector address for this interrupt factor is set at 000012H.

■ Error interrupt

This interrupt factor is generated at the point where a parity error, framing error or overrun error is detected during receiving and it sets the interrupt factor flag FSERR to "1". When set in this manner, if the corresponding interrupt enable register ESERR is set to "1" and the corresponding interrupt priority registers PSIF0 and PSIF1 are set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU.
When "0" has been written in the interrupt enable register ESERR and interrupt has been disabled, an interrupt is not generated to the CPU. Even in this case, the interrupt factor flag FSERR is set to "1". The interrupt factor flag FSERR is reset to "0" by writing "1".

Since all three types of errors result in the same interrupt factor, you should identify the error that has been generated by the error flags PER (parity error), OER (overrun error) and FER (framing error).

The exception processing vector address for this interrupt factor is set at 000010H.

5.8.9 Control of serial interface

Table 5.8.9.1 show the serial interface control bits.

Table 5.8.9.1(a) Serial interface control

Address	Bit	Name	Function		1	0	SR	R/W	Comment
00FF48	D7	–	–		–	–	–		"0" when being read
	D6	EPR	Parity enable register		With parity	Non parity	0	R/W	Only for
	D5	PMD	Parity mode selection		Odd	Even	0	R/W	asynchronous mode
	D4	SCS1	Clock source selection				0	R/W	
			SCS1 SCS0 Clock source						In the clock synchro-
			1 1 Programmable timer						nous slave mode,
	D3	SCS0	1 0 f_{OSC3} / 4				0	R/W	external clock is
			0 1 f_{OSC3} / 8						selected.
			0 0 f_{OSC3} / 16						
	D2	SMD1	Serial I/F mode selection				0	R/W	
			SMD1 SMD0 Mode						
			1 1 Asynchronous 8-bit						
	D1	SMD0	1 0 Asynchronous 7-bit				0	R/W	
			0 1 Clock synchronous slave						
			0 0 Clock synchronous master						
	D0	ESIF	Serial I/F enable register		Serial I/F	I/O port	0	R/W	
00FF49	D7	–	–		–	–	–		"0" when being read
	D6	FER	Framing error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D5	PER	Parity error flag	R	Error	No error	0	R/W	Only for
				W	Reset (0)	No operation			asynchronous mode
	D4	OER	Overrun error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D3	RXTRG	Receive trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D2	RXEN	Receive enable		Enable	Disable	0	R/W	
	D1	TXTRG	Transmit trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D0	TXEN	Transmit enable		Enable	Disable	0	R/W	
00FF4A	D7	TRXD7	Transmit/Receive data D7 (MSB)		High	Low	X	R/W	
	D6	TRXD6	Transmit/Receive data D6						
	D5	TRXD5	Transmit/Receive data D5						
	D4	TRXD4	Transmit/Receive data D4						
	D3	TRXD3	Transmit/Receive data D3						
	D2	TRXD2	Transmit/Receive data D2						
	D1	TRXD1	Transmit/Receive data D1						
	D0	TRXD0	Transmit/Receive data D0 (LSB)						
00FF20	D7	PK01	K00–K07 interrupt priority register		PK01 PK00 Priority level		0	R/W	
	D6	PK00			1 1 Level 3				
	D5	PSIF1	Serial interface interrupt priority register		PSIF1 PSIF0		0	R/W	
	D4	PSIF0			1 0 Level 2				
	D3	PSW1	Stopwatch timer interrupt priority register		PSW1 PSW0		0	R/W	
	D2	PSW0			0 1 Level 1				
	D1	PTM1	Clock timer interrupt priority register		PTM1 PTM0		0	R/W	
	D0	PTM0			0 0 Level 0				

Table 5.8.9.1(b) Serial interface control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF23	D7	EPT1	Programmable timer 1 interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D6	EPT0	Programmable timer 0 interrupt enable register					
	D5	EK1	K10 and K11 interrupt enable register					
	D4	EK0H	K04–K07 interrupt enable register					
	D3	EK0L	K00–K03 interrupt enable register					
	D2	ESERR	Serial I/F (error) interrupt enable register					
	D1	ESREC	Serial I/F (receiving) interrupt enable register					
	D0	ESTRA	Serial I/F (transmitting) interrupt enable register					
00FF25	D7	FPT1	Programmable timer 1 interrupt factor flag	(R) Interrupt factor is generated	(R) No interrupt factor is generated	0	R/W	
	D6	FPT0	Programmable timer 0 interrupt factor flag					
	D5	FK1	K10 and K11 interrupt factor flag					
	D4	FK0H	K04–K07 interrupt factor flag					
	D3	FK0L	K00–K03 interrupt factor flag					
	D2	FSERR	Serial I/F (error) interrupt factor flag	(W) Reset	(W) No operation			
	D1	FSREC	Serial I/F (receiving) interrupt factor flag					
	D0	FSTRA	Serial I/F (transmitting) interrupt factor flag					

ESIF: 00FF48H•D0

Sets the serial interface terminals (P10–P13).

When "1" is written: Serial input/output terminal
When "0" is written: I/O port terminal
Reading: Valid

The ESIF is the serial interface enable register and P10–P13 terminals become serial input/output terminals (SIN, SOUT, $\overline{SCLK}$, $\overline{SRDY}$) when "1" is written, and they become I/O port terminals when "0" is written.
Also, see Table 5.8.3.2 for the terminal settings according to the transfer modes.
At initial reset, ESIF is set to "0" (I/O port).

SMD0, SMD1: 00FF48H•D1, D2

Set the transfer modes according to Table 5.8.9.2.

Table 5.8.9.2 Transfer mode settings

SMD1	SMD0	Mode
1	1	Asynchronous system 8-bit
1	0	Asynchronous system 7-bit
0	1	Clock synchronous system slave
0	0	Clock synchronous system master

SMD0 and SMD1 can also read out.
At initial reset, this register is set to "0" (clock synchronous master mode).

SCS0, SCS1: 00FF48H•D3, D4

Select the clock source according to Table 5.8.9.3.

Table 5.8.9.3 Clock source selection

SCS1	SCS0	Clock source
1	1	Programmable timer
1	0	f_{OSC3} / 4
0	1	f_{OSC3} / 8
0	0	f_{OSC3} / 16

SCS0 and SCS1 can also be read out.
In the clock synchronous slave mode, setting of this register is invalid.
At initial reset, this register is set to "0" (f_{OSC3} / 16).

EPR: 00FF48H•D6

Selects the parity function.

When "1" is written: With parity
When "0" is written: Non parity
Reading: Valid

Selects whether or not to check parity of the received data and to add a parity bit to the transmitting data. When "1" is written to EPR, the most significant bit of the received data is considered to be the parity bit and a parity check is executed. A parity bit is added to the transmitting data. When "0" is written, neither checking is done nor is a parity bit added.
Parity is valid only in asynchronous mode and the EPR setting becomes invalid in the clock synchronous mode.
At initial reset, EPR is set to "0" (non parity).

PMD: 00FF48H•D5

Selects odd parity / even parity.

When "1" is written:	Odd parity
When "0" is written:	Even parity
Reading:	Valid

When "1" is written to PMD, odd parity is selected and even parity is selected when "0" is written. The parity check and addition of a parity bit is only valid when "1" has been written to EPR. When "0" has been written to EPR, the parity setting by PMD becomes invalid.
At initial reset, PMD is set to "0" (even parity).

TXEN: 00FF49H•D0

Sets the serial interface to the transmitting enable status.

When "1" is written:	Transmitting enable
When "0" is written:	Transmitting disable
Reading:	Valid

When "1" is written to TXEN, the serial interface shifts to the transmitting enable status and shifts to the transmitting disable status when "0" is written.
Set TXEN to "0" when making the initial settings of the serial interface and similar operations.
At initial reset, TXEN is set to "0" (transmitting disable).

TXTRG: 00FF49H•D1

Functions as the transmitting start trigger and the operation status indicator (transmitting / stop status).

When "1" is read:	During transmitting
When "0" is read:	During stop
When "1" is written:	Transmitting start
When "0" is written:	Invalid

Starts the transmitting when "1" is written to TXTRG after writing the transmitting data.
TXTRG can be read as the status. When set to "1", it indicates transmitting operation, and "0" indicates transmitting stop.
At initial reset, TXTRG is set to "0" (during stop).

RXEN: 00FF49H•D2

Sets the serial interface to the receiving enable status.

When "1" is written:	Receiving enable
When "0" is written:	Receiving disable
Reading:	Valid

When "1" is written to RXEN, the serial interface shifts to the receiving enable status and shifts to the receiving disable status when "0" is written.
Set RXEN to "0" when making the initial settings of the serial interface and similar operations.
At initial reset, RXEN is set to "0" (receiving disable).

RXTRG: 00FF49H•D3

Functions as the receiving start trigger or preparation for the following data receiving and the operation status indicator (during receiving / during stop).

When "1" is read:	During receiving
When "0" is read:	During stop
When "1" is written:	Receiving start / following data receiving preparation
When "0" is written:	Invalid

RXTRG has a slightly different operation in the clock synchronous system and the asynchronous system.

The RXTRG in the clock synchronous system, is used as the trigger for the receiving start.
Writes "1" into RXTRG to start receiving at the point where the receive data has been read and the following receive preparation has been done. (In the slave mode, $\overline{\text{SRDY}}$ becomes "0" at the point where "1" has been written into into the RXTRG.)

RSTRG is used in the asynchronous system for preparation of the following data receiving. Reads the received data located in the received data buffer and writes "1" into RXTRG to inform that the received data buffer has shifted to empty. When "1" has not been written to RXTRG, the overrun error flag OER is set to "1" at the point where the following receiving has been completed. (When the receiving has been completed between the operation to read the received data and the operation to write "1" into RXTRG, an overrun error occurs.)

In addition, RXTRG can be read as the status. In either clock synchronous mode or asynchronous mode, when RXTRG is set to "1", it indicates receiving operation and when set to "0", it indicates that receiving has stopped.
At initial reset, RXTRG is set to "0" (during stop).

TRXD0–TRXD7: 00FF4AH

During transmitting

Write the transmitting data into the transmit shift register.

When "1" is written: HIGH level
When "0" is written: LOW level

Write the transmitting data prior to starting transmitting.
In the case of continuous transmitting, wait for the transmitting complete interrupt, then write the data.
The TRXD7 becomes invalid for the asynchronous 7-bit mode.
Converted serial data for which the bits set at "1" as HIGH (V_{DD}) level and for which the bits set at "0" as LOW (V_{SS}) level are output from the SOUT terminal.

During receiving

Read the received data.

When "1" is read: HIGH level
When "0" is read: LOW level

The data from the received data buffer can be read out. Since the sift register is provided separately from this buffer, reading can be done during the receive operation in the asynchronous mode. (The buffer function is not used in the clock synchronous mode.)
Read the data after waiting for the receiving complete interrupt.
When performing parity check in the asynchronous 7-bit mode, "0" is loaded into the 8th bit (TRXD7) that corresponds to the parity bit.
The serial data input from the SIN terminal is level converted, making the HIGH (V_{DD}) level bit "1" and the LOW (V_{SS}) level bit "0" and is then loaded into this buffer.
At initial reset, the buffer content is undefined.

OER: 00FF49H•D4

Indicates the generation of an overrun error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

OER is an error flag that indicates the generation of an overrun error and becomes "1" when an error has been generated.
An overrun error is generated when the receiving of data has been completed prior to the writing of "1" to RXTRG in the asynchronous mode.
OER is reset to "0" by writing "1".
At initial reset and when RXEN is "0", OER is set to "0" (no error).

PER: 00FF49H•D5

Indicates the generation of a parity error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

PER is an error flag that indicates the generation of a parity error and becomes "1" when an error has been generated.
When a parity check is performed in the asynchronous mode, if data that does not match the parity is received, a parity error is generated.
PER is reset to "0" by writing "1".
At initial reset and when RXEN is "0", PER is set to "0" (no error).

FER: 00FF49H•D6

Indicates the generation of a framing error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

FER is an error flag that indicates the generation of a framing error and becomes "1" when an error has been generated.
When the stop bit for the receiving of the asynchronous mode has become "0", a framing error is generated.
FER is reset to "0" by writing "1".
At initial reset and when RXEN is "0", FER is set to "0" (no error).

PSIF0, PSIF1: 00FF20H•D4, D5

Sets the priority level of the serial interface interrupt. The two bits PSIF0 and PSIF1 are the interrupt priority register corresponding to the serial interface interrupt. Table 5.8.9.4 shows the interrupt priority level which can be set by this register.

Table 5.8.9.4 Interrupt priority level settings

PSIF1	PSIF0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

ESTRA, ESREC, ESERR: 00FF23H•D0, D1, D2

Enables or disables the generation of an interrupt for the CPU.

When "1" is written: Interrupt enabled
When "0" is written: Interrupt disabled
Reading: Valid

ESTRA, ESREC and ESERR are interrupt enable registers that respectively correspond to the interrupt factors for transmitting complete, receiving complete and receiving error. Interrupts set to "1" are enabled and interrupts set to "0" are disabled. At initial reset, this register is set to "0" (interrupt disabled).

FSTRA, FSREC, FSERR: 00FF25H•D0, D1, D2

Indicates the serial interface interrupt generation status.

When "1" is read: Interrupt factor present
When "0" is read: Interrupt factor not present

When "1" is written: Resets factor flag
When "0" is written: Invalid

FSTRA, FSREC and FSERR are interrupt factor flags that respectively correspond to the interrupts for transmitting complete, receiving complete and receiving error and are set to "1" by generation of each factor.
Transmitting complete interrupt factor is generated at the point where the data transmitting of the shift register has been completed.
Receiving complete interrupt factor is generated at the point where the received data has been transferred into the received data buffer.
Receive error interrupt factor is generated when a parity error, framing error or overrun error has been detected during data receiving.
When set in this manner, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU.
Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.
To accept the subsequent interrupt after interrupt generation, re-setting of the interrupt flags (set interrupt flag to lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and interrupt factor flag reset are necessary. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, this flag is reset to "0".

5.8.10 Programming notes

(1) Be sure to initialize the serial interface mode in the transmitting / receiving disable status (TXEN = RXEN = "0").

(2) Do not perform double trigger (writing "1") to TXTRG (RXTRG) when the serial interface is in the transmitting (receiving) operation. Furthermore, do not execute the SLP instruction. (When executing the SLP instruction, set TXEN = RXEN = "0".)

(3) In the clock synchronous mode, since one clock line ($\overline{SCLK}$) is shared for both transmitting and receiving, transmitting and receiving cannot be performed simultaneously. (Half duplex only is possible in clock synchronous mode.) Consequently, be sure not to write "1" to RXTRG (TXTRG) when TXTRG (RXTRG) is "1".

(4) When a parity error or flaming error is generated during receiving in the asynchronous mode, the receiving error interrupt factor flag FSERR is set to "1" prior to the receiving complete interrupt factor flag FSREC for the time indicated in Table 5.8.10.1. Consequently, when an error is generated, you should reset the receiving complete interrupt factor flag FSREC to "0" by providing a wait time in error processing routines and similar routines.
When an overrun error is generated, the receiving complete interrupt factor flag FSREC is not set to "1" and a receiving complete interrupt is not generated.

Table 5.8.10.1 Time difference between FSERR and FSREC on error generation

Clock source	Time difference
f_{OSC3} / n	1/2 cycles of f_{OSC3} / n
Programmable timer	1 cycle of timer 1 underflow

(5) When the demultiplied signal of the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
A time interval of several msec to several 10 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before starting transmitting / receiving of serial interface. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 8, "ELECTRICAL CHARACTERISTICS".)
At initial reset, the OSC3 oscillation circuit is set to OFF status.

5.9 Clock Timer

5.9.1 Configuration of clock timer

The S1C88349 has built in a clock timer that uses the OSC1 oscillation circuit as clock source. The clock timer is composed of an 8-bit binary counter that uses the 256 Hz signal dividing fOSC1 as its input clock and can read the data of each bit (128–1 Hz) by software.
Normally, this clock timer is used for various timing functions such as clocks.
The configuration of the clock timer is shown in Figure 5.9.1.1.

5.9.2 Interrupt function

The clock timer can generate an interrupt by each of the 32 Hz, 8 Hz, 2 Hz and 1 Hz signals.
The configuration of the clock timer interrupt circuit is shown in Figure 5.9.2.1.

Interrupts are generated by respectively setting the corresponding interrupt factor flags FTM32, FTM8, FTM2 and FTM1 at the falling edge of the 32 Hz, 8 Hz, 2 Hz and 1 Hz signals to "1". Interrupt can be prohibited by the setting the interrupt enable registers ETM32, ETM8, ETM2 and ETM1 corresponding to each interrupt factor flag.
In addition, a priority level of the clock timer interrupt for the CPU can be optionally set at levels 0 to 3 by the interrupt priority registers PTM0 and PTM1.
For details on the above mentioned interrupt control register and the operation following generation of an interrupt, see "5.17 Interrupt and Standby Status".

The exception processing vector addresses for each interrupt factor are respectively set as shown below.

32 Hz interrupt:	00001CH
8 Hz interrupt:	00001EH
2 Hz interrupt:	000020H
1 Hz interrupt:	000022H

Figure 5.9.2.2 shows the timing chart for the clock timer.

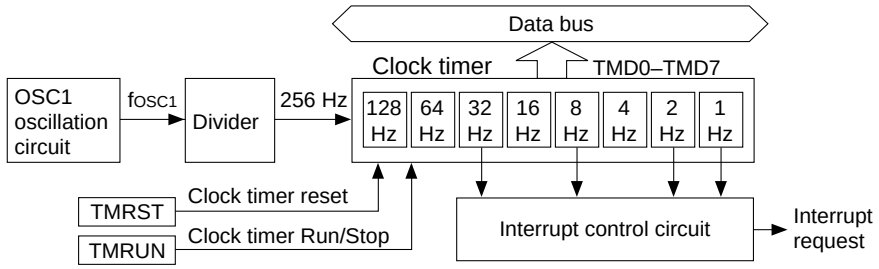


Fig. 5.9.1.1 Configuration of clock timer

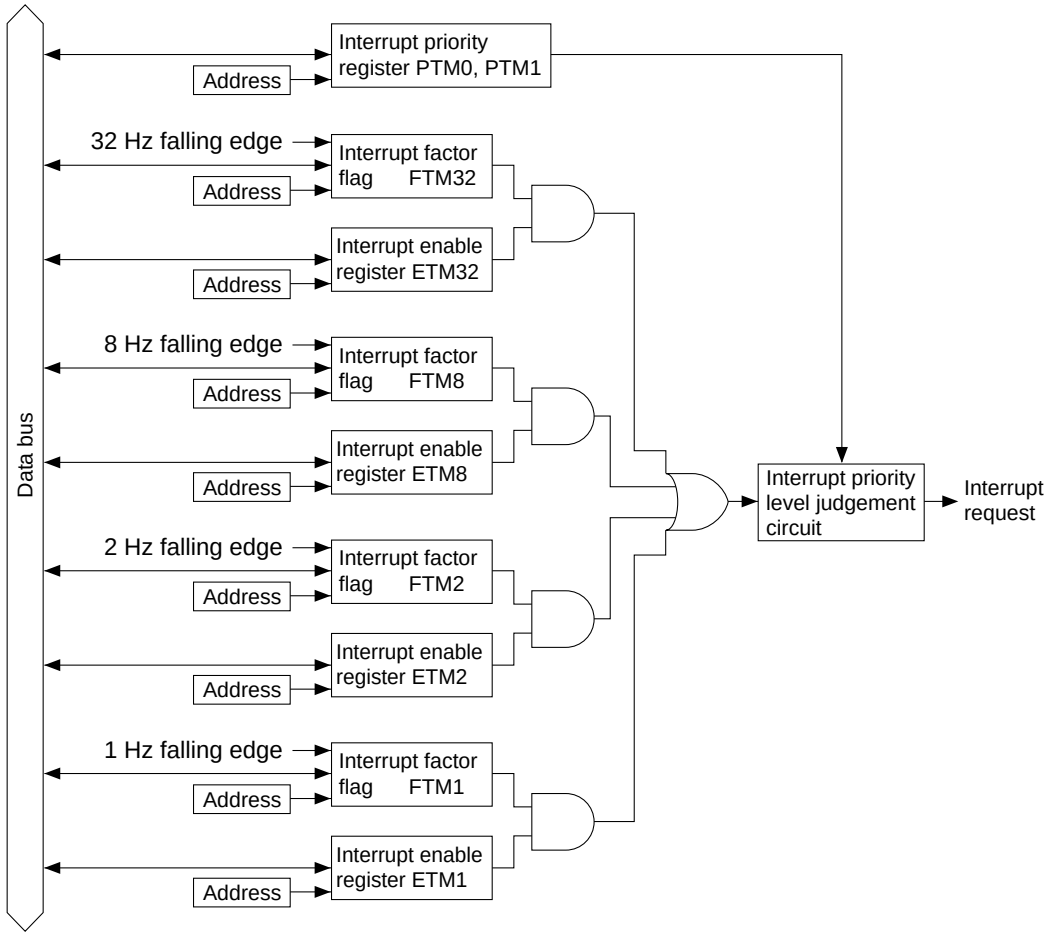


Fig. 5.9.2.1 Configuration of clock timer interrupt circuit

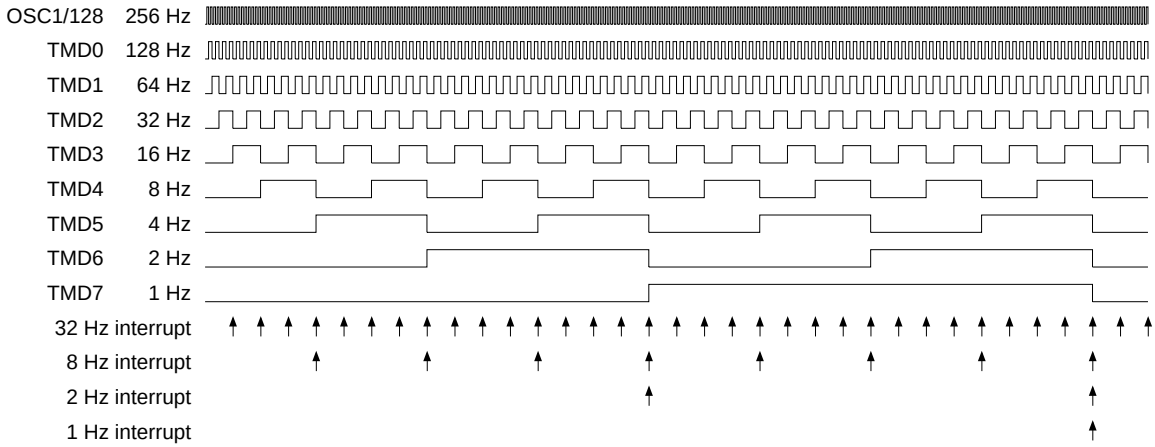


Fig. 5.9.2.2 Timing chart of clock timer

5.9.3 Control of clock timer

Table 5.9.3.1 shows the clock timer control bits.

Table 5.9.3.1 Clock timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF40	D7	–	–	–	–	–		"0" when being read
	D6	FOUT2	FOUT frequency selection FOUT2 FOUT1 FOUT0 Frequency 0 0 0 fOSC1 / 1 0 0 1 fOSC1 / 2 0 1 0 fOSC1 / 4 0 1 1 fOSC1 / 8 1 0 0 fOSC3 / 1 1 0 1 fOSC3 / 2 1 1 0 fOSC3 / 4 1 1 1 fOSC3 / 8			0	R/W	
	D5	FOUT1				0	R/W	
	D4	FOUT0				0	R/W	
	D3	FOUTON	FOUT output control	On	Off	0	R/W	
	D2	WDRST	Watchdog timer reset	Reset	No operation	–	W	Constantly "0" when
	D1	TMRST	Clock timer reset	Reset	No operation	–	W	being read
	D0	TMRUN	Clock timer Run/Stop control	Run	Stop	0	R/W	
00FF41	D7	TMD7	Clock timer data 1 Hz	High	Low	0	R	
	D6	TMD6	Clock timer data 2 Hz					
	D5	TMD5	Clock timer data 4 Hz					
	D4	TMD4	Clock timer data 8 Hz					
	D3	TMD3	Clock timer data 16 Hz					
	D2	TMD2	Clock timer data 32 Hz					
	D1	TMD1	Clock timer data 64 Hz					
	D0	TMD0	Clock timer data 128 Hz					
00FF20	D7	PK01	K00–K07 interrupt priority register	PK01 PK00 Priority level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PK00						
	D5	PSIF1	Serial interface interrupt priority register	PSIF1 PSIF0 Priority level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D4	PSIF0						
	D3	PSW1	Stopwatch timer interrupt priority register	PSW1 PSW0 Priority level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D2	PSW0						
	D1	PTM1	Clock timer interrupt priority register	PTM1 PTM0 Priority level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D0	PTM0						
00FF22	D7	–	–	–	–	–		"0" when being read
	D6	ESW100	Stopwatch timer 100 Hz interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D5	ESW10	Stopwatch timer 10 Hz interrupt enable register					
	D4	ESW1	Stopwatch timer 1 Hz interrupt enable register					
	D3	ETM32	Clock timer 32 Hz interrupt enable register					
	D2	ETM8	Clock timer 8 Hz interrupt enable register					
	D1	ETM2	Clock timer 2 Hz interrupt enable register					
	D0	ETM1	Clock timer 1 Hz interrupt enable register					
00FF24	D7	–	–	–	–	–		"0" when being read
	D6	FSW100	Stopwatch timer 100 Hz interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D5	FSW10	Stopwatch timer 10 Hz interrupt factor flag					
	D4	FSW1	Stopwatch timer 1 Hz interrupt factor flag					
	D3	FTM32	Clock timer 32 Hz interrupt factor flag					
	D2	FTM8	Clock timer 8 Hz interrupt factor flag					
	D1	FTM2	Clock timer 2 Hz interrupt factor flag					
	D0	FTM1	Clock timer 1 Hz interrupt factor flag					

TMD0–TMD7: 00FF41H

The clock timer data can be read out.
Each bit of TMD0–TMD7 and frequency correspondence are as follows:

TMD0:	128 Hz	TMD4:	8 Hz
TMD1:	64 Hz	TMD5:	4 Hz
TMD2:	32 Hz	TMD6:	2 Hz
TMD3:	16 Hz	TMD7:	1 Hz

Since the TMD0–TMD7 is exclusively for reading, the write operation is invalid.
At initial reset, the timer data is set to "00H".

TMRST: 00FF40H•D1

Resets the clock timer.

When "1" is written:	Clock timer reset
When "0" is written:	No operation
Reading:	Always "0"

The clock timer is reset by writing "1" to the TMRST.
When the clock timer is reset in the RUN status, it restarts immediately after resetting. In the case of the STOP status, the reset data "00H" is maintained.
No operation results when "0" is written to the TMRST.
Since the TMRST is exclusively for writing, it always becomes "0" during reading.

TMRUN: 00FF40H•D0

Controls RUN / STOP of the clock timer.

When "1" is written:	RUN
When "0" is written:	STOP
Reading:	Valid

The clock timer starts up-counting by writing "1" to the TMRUN and stops by writing "0".
In the STOP status, the count data is maintained until it is reset or set in the next RUN status. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.
At initial reset, the TMRUN is set to "0" (STOP).

PTM0, PTM1: 00FF20H•D0, D1

Sets the priority level of the clock timer interrupt. The two bits PTM0 and PTM1 are the interrupt priority register corresponding to the clock timer interrupt. Table 5.9.3.2 shows the interrupt priority level which can be set by this register.

Table 5.9.3.2 Interrupt priority level settings

PTM1	PTM0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

ETM1, ETM2, ETM8, ETM32: 00FF22H•D0–D3

Enables or disables the generation of an interrupt for the CPU.

When "1" is written:	Interrupt enabled
When "0" is written:	Interrupt disabled
Reading:	Valid

The ETM1, ETM2, ETM8 and ETM32 are interrupt enable registers that respectively correspond to the interrupt factors for 1 Hz, 2 Hz, 8 Hz and 32 Hz. Interrupts set to "1" are enabled and interrupts set to "0" are disabled.
At initial reset, this register is set to "0" (interrupt disabled).

FTM1, FTM2, FTM8, FTM32: 00FF24H•D0–D3

Indicates the clock timer interrupt generation status.

When "1" is read:	Interrupt factor present
When "0" is read:	Interrupt factor not present
When "1" is written:	Resets factor flag
When "0" is written:	Invalid

The FTM1, FTM2, FTM8 and FTM32 are interrupt factor flags that respectively correspond to the interrupts for 1 Hz, 2 Hz, 8 Hz and 32 Hz and are set to "1" at the falling edge of each signal.
When set in this manner, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU.
Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.
To accept the subsequent interrupt after interrupt generation, re-setting of the interrupt flags (set interrupt flag to lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and interrupt factor flag reset are necessary. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, this flag is reset to "0".

5.9.4 Programming notes

(1) The clock timer is actually made to RUN / STOP in synchronization with the falling edge of the 256 Hz signal after writing to the TMRUN register. Consequently, when "0" is written to the TMRUN, the timer shifts to STOP status when the counter is incremented "1". The TMRUN maintains "1" for reading until the timer actually shifts to STOP status.
Figure 5.9.4.1 shows the timing chart of the RUN / STOP control.

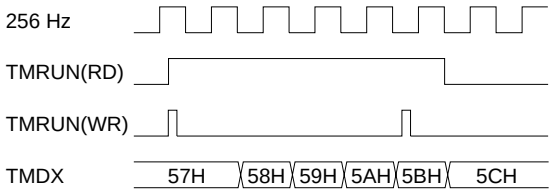


Fig. 5.9.4.1 Timing chart of RUN/STOP control

(2) The SLP instruction is executed when the clock timer is in the RUN status (TMRUN = "1"). The clock timer operation will become unstable when returning from SLEEP status. Therefore, when shifting to SLEEP status, set the clock timer to STOP status (TMRUN = "0") prior to executing the SLP instruction.

5.10 Stopwatch Timer

5.10.1 Configuration of stopwatch timer

The S1C88349 has a built-in 1/100 sec and 1/10 sec stopwatch timer. The stopwatch timer is composed of a 4-bit 2 stage BCD counter (1/100 sec units and 1/10 sec units) that makes the 256 Hz signal that divides the fOSC1 the input clock and it can read the count data by software.
Figure 5.10.1.1 shows the configuration of the stopwatch timer.
The stopwatch timer can be used as a timer different from the clock timer and can easily realize stopwatch and other such functions by software.

5.10.2 Count up pattern

The stopwatch timer is respectively composed of the 4-bit BCD counters SWD0–SWD3 and SWD4–SWD7.

Figure 5.10.2.1 shows the count up pattern of the stopwatch timer.

The feedback dividing circuit generates an approximate 100 Hz signal at 2/256 sec and 3/256 sec intervals from a 256 Hz signal divided from fOSC1.

The 1/100 sec counter (SWD0–SWD3) generates an approximate 10 Hz signal at 25/256 sec and 26/256 sec intervals by counting the approximate 100 Hz signal generated by the feedback dividing circuit in 2/256 sec and 3/256 sec intervals. The count-up is made approximately 1/100 sec counting by the 2/256 sec and 3/256 sec intervals.

The 1/10 sec counter (SWD4–SWD7) generates a 1 Hz signal by counting the approximate 10 Hz signal generated by the 1/100 sec counter at 25/256 sec and 26/256 sec intervals in 4:6 ratios.

The count-up is made approximately 1/10 sec counting by 25/256 sec and 26/256 sec intervals.

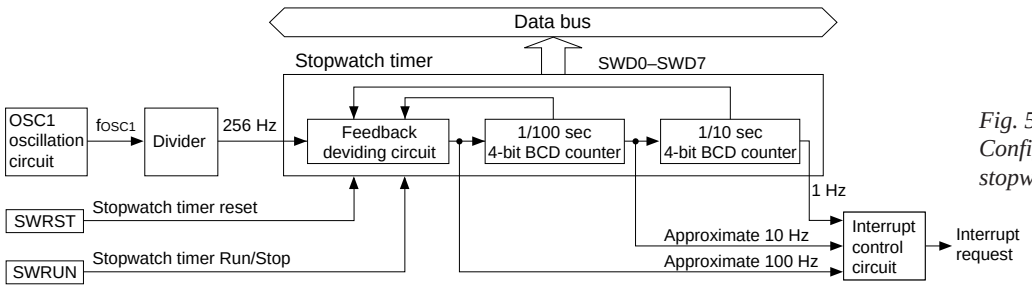


Fig. 5.10.1.1 Configuration of stopwatch timer

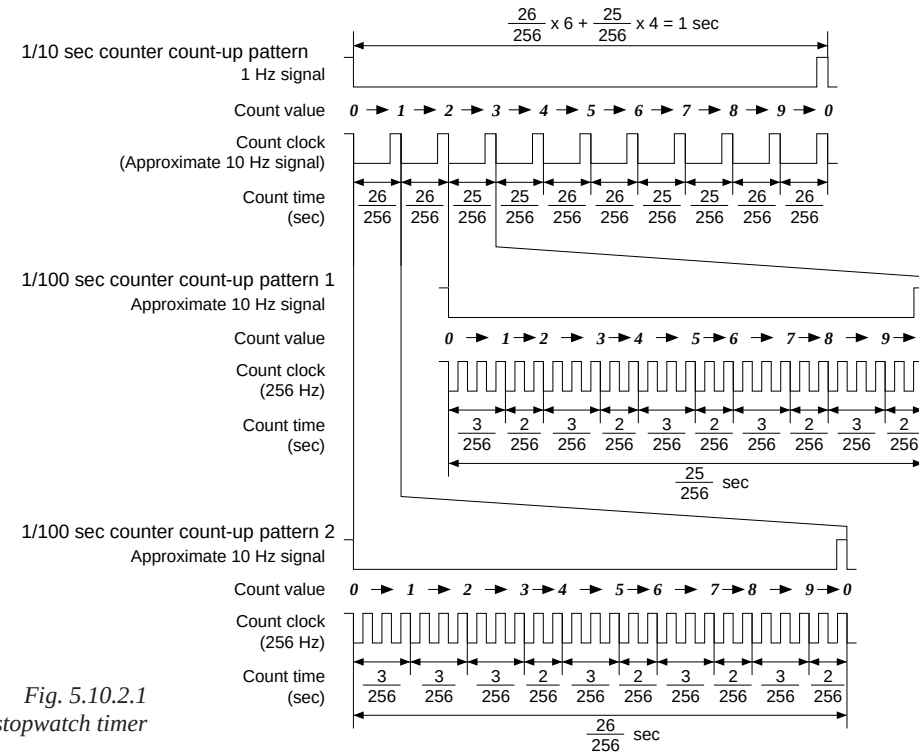


Fig. 5.10.2.1 Count-up pattern of stopwatch timer

5.10.3 Interrupt function

The stopwatch timer can generate an interrupt by each of the 100 Hz (approximately 100 Hz), 10 Hz (approximately 10 Hz) and 1 Hz signals. Figure 5.10.3.1 shows the configuration of the stopwatch timer interrupt circuit.

The corresponding factor flags FSW100, FSW10 and FSW1 are respectively set to "1" at the falling edge of the 100 Hz, 10Hz and 1Hz signal and an interrupt is generated. Interrupt can be prohibited by the setting of the interrupt enable registers ESW100, ESW10 and ESW1 corresponding to each interrupt factor flag.

In addition, a priority level of the stopwatch timer interrupt for the CPU can be optionally set at levels 0 to 3 by the interrupt priority registers PSW0 and PSW1.
For details on the above mentioned interrupt control registers and the operation following generation of an interrupt, see "5.17 Interrupt and Standby Status".
The exception processing vector addresses of each interrupt factor are respectively set as shown below.

100 Hz interrupt:	000016H
10 Hz interrupt:	000018H
1 Hz interrupt:	00001AH

Figure 5.10.3.2 shows the timing chart for the stopwatch timer.

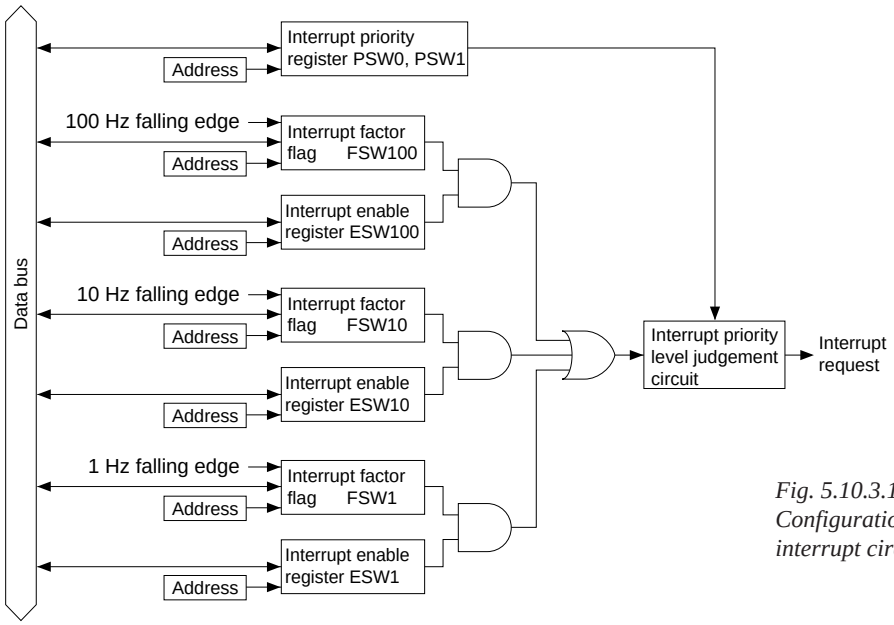


Fig. 5.10.3.1
Configuration of the stopwatch timer interrupt circuit

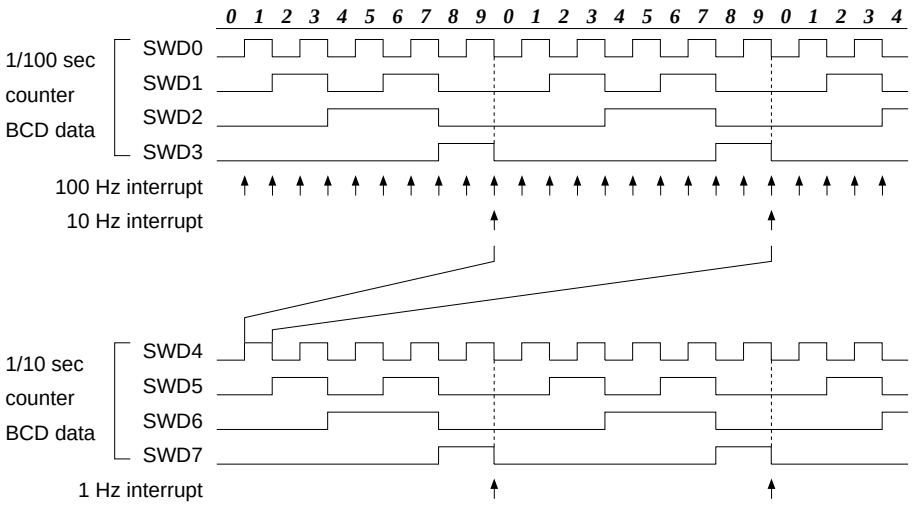


Fig. 5.10.3.2
Stopwatch timer timing chart

5.10.4 Control of stopwatch timer

Table 5.10.4.1 shows the stopwatch timer control bits.

Table 5.10.4.1 Stopwatch timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF42	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	SWRST	Stopwatch timer reset	Reset	No operation	–	W	
	D0	SWRUN	Stopwatch timer Run/Stop control	Run	Stop	0	R/W	
00FF43	D7	SWD7	Stopwatch timer data BCD (1/10 sec)			0	R	
	D6	SWD6						
	D5	SWD5						
	D4	SWD4						
	D3	SWD3	Stopwatch timer data BCD (1/100 sec)					
	D2	SWD2						
	D1	SWD1						
	D0	SWD0						
00FF20	D7	PK01	K00–K07 interrupt priority register	PK01 PK00 PSIF1 PSIF0 PSW1 PSW0 PTM1 PTM0 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PK00						
	D5	PSIF1	Serial interface interrupt priority register			0	R/W	
	D4	PSIF0						
	D3	PSW1	Stopwatch timer interrupt priority register			0	R/W	
	D2	PSW0						
	D1	PTM1	Clock timer interrupt priority register			0	R/W	
	D0	PTM0						
00FF22	D7	–	–	–	–	–		"0" when being read
	D6	ESW100	Stopwatch timer 100 Hz interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D5	ESW10	Stopwatch timer 10 Hz interrupt enable register					
	D4	ESW1	Stopwatch timer 1 Hz interrupt enable register					
	D3	ETM32	Clock timer 32 Hz interrupt enable register					
	D2	ETM8	Clock timer 8 Hz interrupt enable register					
	D1	ETM2	Clock timer 2 Hz interrupt enable register					
	D0	ETM1	Clock timer 1 Hz interrupt enable register					
00FF24	D7	–	–	–	–	–		"0" when being read
	D6	FSW100	Stopwatch timer 100 Hz interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D5	FSW10	Stopwatch timer 10 Hz interrupt factor flag					
	D4	FSW1	Stopwatch timer 1 Hz interrupt factor flag					
	D3	FTM32	Clock timer 32 Hz interrupt factor flag					
	D2	FTM8	Clock timer 8 Hz interrupt factor flag					
	D1	FTM2	Clock timer 2 Hz interrupt factor flag					
	D0	FTM1	Clock timer 1 Hz interrupt factor flag					

SWD0–SWD7: 00FF43H

The stopwatch timer data can be read out.
Higher and lower nibbles and BCD digit correspondence are as follows:

SWD0–SWD3: BCD (1/100 sec)
SWD4–SWD7: BCD (1/10 sec)

Since SWD0–SWD7 are exclusively for reading, the write operation is invalid.
At initial reset, the timer data is set to "00H".

SWRST: 00FF42H•D1

Resets the stopwatch timer.

When "1" is written: Stopwatch timer reset
When "0" is written: No operation
Reading: Always "0"

The stopwatch timer is reset by writing "1" to the SWRST. When the stopwatch timer is reset in the RUN status, it restarts immediately after resetting. In the case of the STOP status, the reset data "00H" is maintained.
No operation results when "0" is written to the SWRST.
Since the SWRST is exclusively for writing, it always becomes "0" during reading.

SWRUN: 00FF42H•D0

Controls RUN/STOP of the stopwatch timer.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The stopwatch timer starts up-counting by writing "1" to the SWRUN and stops by writing "0".
In the STOP status, the timer data is maintained until it is reset or set in the next RUN status. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.
At initial reset, the SWRUN is set at "0" (STOP).

PSW0, PSW1: 00FF20H•D2, D3

Sets the priority level of the stopwatch timer interrupt.
The two bits PSW0 and PSW1 are the interrupt priority register corresponding to the stopwatch timer interrupt. Table 5.10.4.2 shows the interrupt priority level which can be set by this register.

Table 5.10.4.2 Interrupt priority level settings

PSW1	PSW0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

ESW1, ESW10, ESW100: 00FF22H•D4, D5, D6

Enables or disables the generation of an interrupt for the CPU.

When "1" is written: Interrupt enabled
When "0" is written: Interrupt disabled
Reading: Valid

The ESW1, ESW10 and ESW100 are interrupt enable registers that respectively correspond to the interrupt factors for 1 Hz, 10 Hz and 100 Hz. Interrupts set to "1" are enabled and interrupts set to "0" are disabled.
At initial reset, this register is set to "0" (interrupt disabled).

FSW1, FSW10, FSW100: 00FF24H•D4, D5, D6

Indicates the stopwatch timer interrupt generation status.

When "1" is read: Interrupt factor present
When "0" is read: Interrupt factor not present

When "1" is written: Resets factor flag
When "0" is written: Invalid

The FSW1, FSW10 and FSW100 are interrupt factor flags that respectively correspond to the interrupts for 1 Hz, 10 Hz and 100 Hz and are set to "1" in synchronization with the falling edge of each signal. When set in this manner, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU. Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.
To accept the subsequent interrupt after interrupt generation, re-setting of the interrupt flags (set interrupt flag to lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and interrupt factor flag reset are necessary. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, this flag is reset to "0".

5.10.5 Programming notes

(1) The stopwatch timer is actually made to RUN / STOP in synchronization with the falling edge of the 256 Hz signal after writing to the SWRUN register. Consequently, when "0" is written to the SWRUN, the timer shifts to STOP status when the counter is incremented "1". The SWRUN maintains "1" for reading until the timer actually shifts to STOP status.
Figure 5.10.5.1 shows the timing chart of the RUN / STOP control.

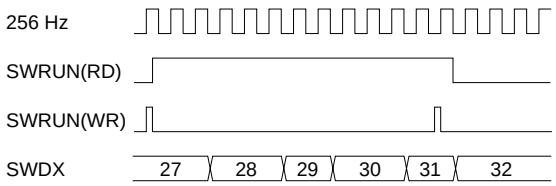


Fig. 5.10.5.1 Timing chart of RUN/STOP control

(2) The SLP instruction is executed when the stopwatch timer is in the RUN status (SWRUN = "1"). The stopwatch timer operation will become unstable when returning from SLEEP status. Therefore, when shifting to SLEEP status, set the clock timer to STOP status (SWRUN = "0") prior to executing the SLP instruction.

5.11 Programmable Timer

5.11.1 Configuration of programmable timer

The S1C88349 has two built-in 8-bit programmable timer systems (timer 0 and timer 1).
Timer 0 and timer 1 are composed of 8-bit presettable down counters and they can be used as 8-bit × 2 channels or 16-bit × 1 channel programmable timer. They also have an event counter function and a pulse width measurement function using the K10 input port terminal.
Figure 5.11.1.1 shows the configuration of the programmable timer.

Programmable setting of the transfer rate is possible, due to the fact that the programmable timer underflow signal can be used as a synchronous clock for the serial interface.
The underflow divided by 1/2 signal can also be output externally from the R27 output port terminal.

5.11.2 Count operation and setting basic mode

Here we will explain the basic operation and setting of the programmable timer.

■ Setting of initial value and counting down

The timers 0 and 1 each have a down counter and reload data register.

The reload data registers RLD00–RLD07 (timer 0) and RLD10–RLD17 (timer 1) are registers that set the initial value of the counter.
By writing "1" to the preset control bit PSET0 (timer 0) or PSET1 (timer 1), the down counter loads the initial value set in the reload register RLD.
Therefore, down-counting is executed from the stored initial value according to the input clock.

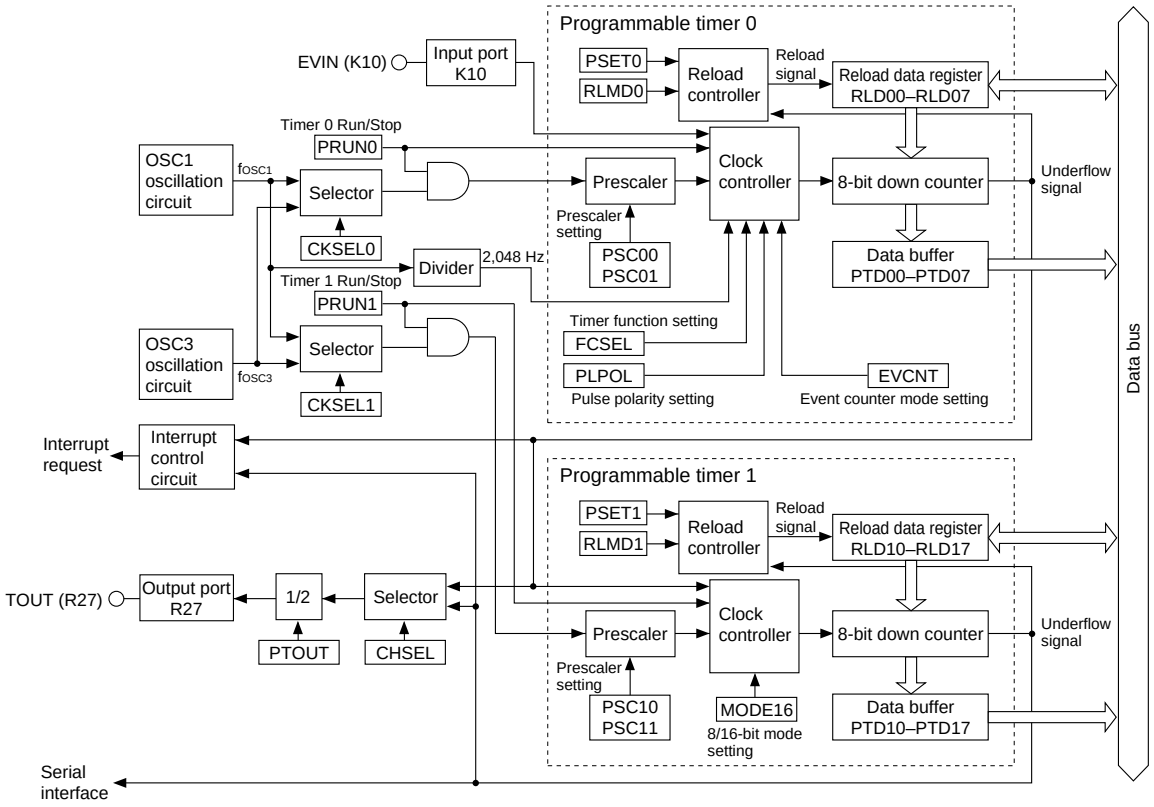


Fig. 5.11.1.1 Configuration of programmable timer

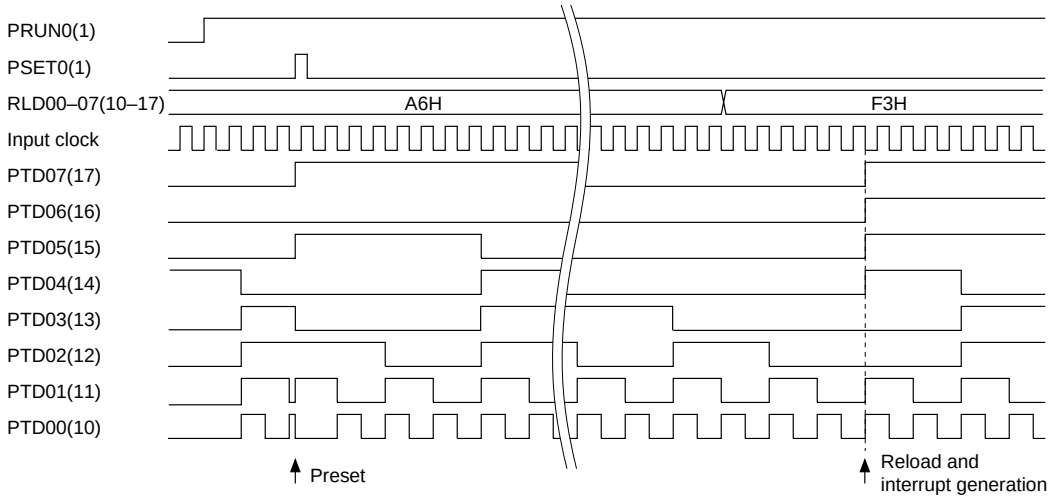


Fig. 5.11.2.1 Basic operation timing of the counter

The registers PRUN0 (timer 0) and PRUN1 (timer 1) are provided to control the RUN / STOP for timers 0 and 1.
After the reload data has been preset into the counter, down-counting is begun by writing "1" to this register. When "0" is written, the clock input is prohibited and the count stops.
The control of this RUN / STOP has no affect on the counter data. The counter data is maintained even during the stoppage of the counter and it can start the count, continuing from that data.

The reading of the counter data can be done through the data buffers PTD00–PTD07 (timer 0) and PTD10–PTD17 (timer 1) with optional timing.
When the down-counting has progressed and an underflow is generated, the counter reloads the initial value set in the reload data register.
This underflow signal controls an interrupt generation, pulse (TOUT signal) output and serial interface clocking, in addition to reloading the counter.

■ Continuous/one-shot mode setting

By writing "1" to the continuous / one-shot mode selection registers CONT0 (timer 0) and CONT1 (timer 1), the programmable timer is set to the continuous mode. In the continuous mode, the initial counter value is automatically loaded when an underflow is generated, and counting is continued. This mode is suitable when programmable intervals are necessary (such as an interrupt and a synchronous clock for the serial interface).
On the other hand, when writing "0" to the registers CONT0 (timer 0) and CONT1 (timer 1), the programmable timer is set to the one-shot mode. The counter loads an initial value and stops when an underflow is generated. At this time, the RUN / STOP control register PRUN0 (timer 0) and PRUN1 (timer 1) are automatically reset to "0". After the counter stops, a one-shot count can be performed once again by writing "1" to registers PRUN0 (timer 0) and PRUN1 (timer 1). This mode is suitable for single time measurement, for example.

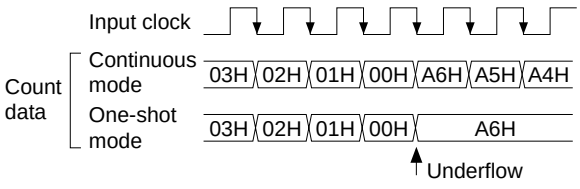


Fig. 5.11.2.2 Continuous mode and one-shot mode

■ 8/16-bit mode setting

By writing "0" to the 8/16-bit mode selection register MODE16, timer 0 and timer 1 are set as independent timers in 8-bit × 2 channels. In this mode, timer 0 and timer 1 can be controlled individually and each of them operates independently.
On the other hand, when writing "1" to the register MODE16, timer 0 and timer1 are set as 1 channel 16-bit timer. This is done by setting timer 0 to the lower 8 bits, and timer 1 to the upper 8 bits. The timer is controlled by timer 0's registers. In this case, the control registers for timer 1 are invalid. (PRUN1 is fixed at "0".)

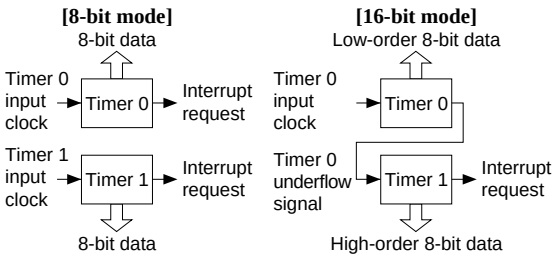


Fig. 5.11.2.3 8/16-bit mode setting and counter configuration

5.11.3 Setting of input clock

Prescalers have been provided for timers 0 and 1. The prescalers generate the input clock for each by dividing the source clock signal from the OSC1 or OSC3 oscillation circuit.
The source clock and the dividing ratio of the prescaler can be selected individually for timer 0 and timer 1 in software.

The input clocks are set by the below sequence.

(1) Selection of source clock

Select the source clock (OSC1 or OSC3) for each prescaler. This is done with the source clock selection registers CKSEL0 (timer 0) and CKSEL1 (timer 1): when "0" is written, OSC1 is selected and when "1" is written, OSC3 is selected. When the 16-bit mode is selected, the source clock is selected by register CKSEL0, and the register CKSEL1 setting becomes invalid.
When the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer.
From the time the OSC3 oscillation circuit is turning ON until oscillation stabilizes, an interval of several msec to several 10 msec is necessary. Consequently, you should allow an adequate waiting time after turning the OSC3 oscillation circuit ON before starting the count of the programmable timer. (The oscillation start time will vary somewhat depending on the oscillator and on external parts. Refer to the oscillation start time example indicated in Chapter 8, "ELECTRICAL CHARACTERISTICS".)
At initial reset, OSC3 oscillation circuit is set to OFF status.

(2) Selection of prescaler dividing ratio

Select the dividing ratio of each prescaler from among 4 types. This selection is done by the prescaler dividing ratio selection registers PSC00/PSC01 (timer 0) and PSC10/PSC11 (timer 1). Setting value and dividing ratio correspondence are shown in Table 5.11.3.1.

Table 5.11.3.1 Selection of prescaler dividing ratio

PSC11 PSC01	PSC10 PSC00	Prescaler dividing ratio
1	1	Source clock / 64
1	0	Source clock / 16
0	1	Source clock / 4
0	0	Source clock / 1

By writing "1" to the register PRUN0 (timer 0) and PRUN1 (timer 1), the source clock is input to the prescaler. Therefore, the clock with selected dividing ratio is input to the timer and the timer starts counting down.
When the 16-bit mode has been selected, the dividing ratio for the source clock is selected by register PSC00/PSC01 and the setting of register PSC10/PSC11 becomes invalid.

5.11.4 Timer mode

The timer mode counts down using the prescaler output as an input clock. In this mode, the programmable timer operates as a timer that obtains fixed cycles using the OSC1 or OSC3 oscillation circuit as a clock source.
See "5.11.2 Count operation and basic mode setting" for basic operation and control, and "5.11.3 Setting input clock" for the clock source and setting of the prescaler.

5.11.5 Event counter mode

Timer 0 includes an even counter function that counts by inputting an external clock (EVIN) to input port K10. This function is selected by writing "1" to the timer 0 counter mode selection register EVCNT.
When the event counter mode is selected, timer 0 operates as an event counter and timer 1 operates as a normal timer in 8-bit mode. In the 16-bit mode, timer 0 and timer 1 operate as 1 channel 16-bit event counter. In the event counter mode, since the timer 0 is clocked externally, the settings of registers PSC00 / PSC01 become invalid.
Count down timing can be controlled by either the falling edge or rising edge selected by the timer 0 pulse polarity selection register PLPOL. When "0" is written to the register PLPOL, the falling edge is selected, and when "1" is written, the rising edge is selected. The timing is shown in Figure 5.11.5.1.

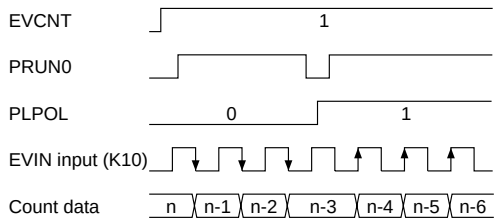


Fig. 5.11.5.1 Timing chart for event counter mode

The event counter also includes a noise rejecter to eliminate noise such as chattering for the external clock (EVIN). This function is selected by writing "1" to the timer 0 function selection register FCSEL.
For a reliable count when "with noise rejecter" is selected, you must allow 0.98 msec or more pulse width for both LOW and HIGH levels. (The noise rejecter allows clocking counter at the second falling edge of the internal 2,048 Hz signal after changing the input level of the K10 input port terminal. Consequently, the pulse width that can reliably be rejected is 0.48 msec.)
Figure 5.11.5.2 shows the count down timing with the noise rejecter selected.

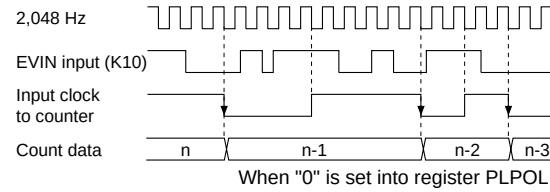


Fig. 5.11.5.2 Count down timing with noise rejecter

The event counter mode is the same as the timer mode except that the clock is external (EVIN).
See "5.11.2 Count operation and setting basic mode" for the basic operation and control.

5.11.6 Pulse width measurement timer mode

Timer 0 includes a pulse width measurement function that measures the width of the input signal to the K10 input port terminal. This function is selected by writing "1" to the timer function selection register FCSEL when in the timer mode (EVCNT = "0").
When the pulse width measurement mode is selected, timer 0 operates as an pulse width measurement and timer 1 operates as a normal timer in 8-bit mode. In the 16-bit mode, timer 0 and timer 1 operate as 1 channel 16-bit pulse width measurement.
The level of the input signal (EVIN) for measurement can be changed either a LOW or HIGH level by the timer 0 pulse polarity selection register PLPOL. When "0" is written to register PLPOL, a LOW level width is measured and when "1" is written, a HIGH level width is measured. The timing is shown in Figure 5.11.6.1.

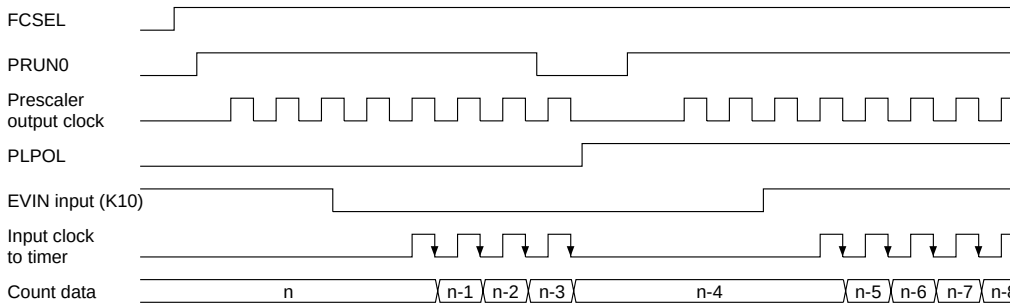


Fig. 5.11.6.1 Timing chart for pulse width measurement timer mode

The pulse width measurement timer mode is the same as the timer mode except that the input clock is controlled by the level of the signal (EVIN) input to the K10 input port terminal.
See "5.11.2 Count operation and setting basic mode" for the basic operation and control.

5.11.7 Interrupt function

The programmable timer can generate an interrupt due to an underflow signal of timer 0 and timer 1. Figure 5.11.7.1 shows the configuration of the programmable timer interrupt circuit.

The respectively corresponding interrupt factor flags FPT0 and FPT1 are set to "1" and an interrupt is generated by an underflow signal of timers 1 and 0. Interrupt can also be prohibited by the setting of the interrupt enable registers EPT0 and EPT1 corresponding to each interrupt flag.

In addition, a priority level of the programmable timer interrupt for the CPU can be optionally set at levels 0 to 3 by the interrupt priority registers PPT0 and PPT1.
For details on the above mentioned interrupt control registers and the operation following generation of an interrupt, see "5.17 Interrupt and Standby Status".

The exception processing vector addresses of each interrupt factor are respectively set as shown below.

Programmable timer 1 interrupt:	000006H
Programmable timer 0 interrupt:	000008H

When the 16-bit mode is selected, the interrupt factor flag FPT0 is not set to "1" and a timer 0 interrupt cannot be generated. (In the 16-bit mode, the interrupt factor flag FPT1 is set to "1" by an underflow of the 16-bit counter.)

5.11.8 Setting of TOUT output

The programmable timer can generate a TOUT signal due to an underflow of timer 0 or timer 1. A TOUT signal is the above mentioned underflow divided by 1/2. The timer underflow which is to be used can be selected by the TOUT output channel selection register CHSEL. When writing "0" to register CHSEL, timer 0 is selected and when "1" is written, timer 1 is selected. However, in the 16-bit mode, it is fixed in timer 1 (underflow of the 16-bit timer) and the setting of register CHSEL becomes invalid.
Figure 5.11.8.1 shows the TOUT signal waveform when channel switching.

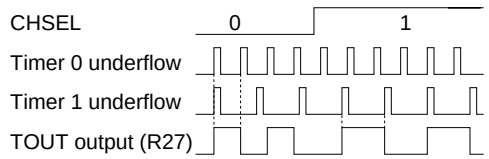


Fig. 5.11.8.1 TOUT signal waveform at channel change

The TOUT signal can be output from the R27 output port terminal and the programmable clock can be supplied to an external device.
The configuration of the output port R27 is shown in Figure 5.11.8.2.

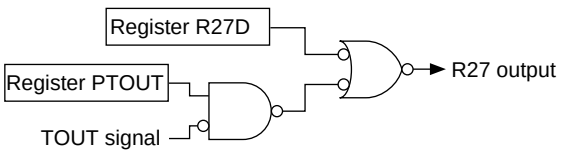


Fig. 5.11.8.2 Configuration of R27

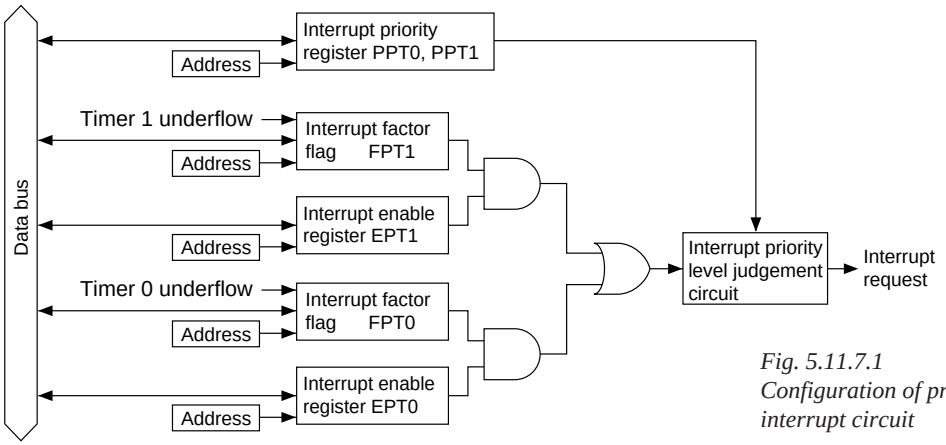


Fig. 5.11.7.1 Configuration of programmable timer interrupt circuit

The output control of the TOUT signal is done by register PTOUT. When "1" is set to the PTOUT, the TOUT signal is output from the R27 output port and when "0" is set, HIGH (V_{DD}) level is output. At this time, "1" must always be set in the data register R27D.

Since the TOUT signal is generated asynchronously from the register PTOUT, when the signal is turned ON or OFF by the register setting, a hazard of a 1/2 cycle or less is generated.
Figure 5.11.8.3 shows the output waveform of TOUT signal.

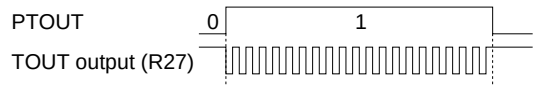


Fig. 5.11.8.3 Output waveform of the TOUT signal

5.11.9 Transmission rate setting of serial interface

The underflow signal of the timer 1 can be used to clock the serial interface.
The transmission rate setting in this case is made in registers PSC1X and PLD1X, and is used to set the count mode to the reload count mode (RLMD1 = "1").
Since the underflow signal of the timer 1 is divided by 1/32 in the serial interface, the value set in register RLD1X which corresponds to the transmission rate is shown in the following expression:

$$RLD1X = fosc / (32*bps*4^{PSC1X}) - 1$$

fosc: Oscillation frequency (OSC1/OSC3)
bps: Transmission rate
PSC1X: Setting value to the register PSC1X (0–3)

(00H can be set to RLD1X)

Table 5.11.9.1 shows an example of the transmission rate setting when the OSC3 oscillation circuit is used as a clock source.

Table 5.11.9.1 Example of transmission rate setting

Transfer rate (bps)	OSC3 oscillation frequency / Programmable timer settings					
	f_{OSC3} = 3.072 MHz		f_{OSC3} = 4.608 MHz		f_{OSC3} = 4.9152 MHz	
	PSC1X	RLD1X	PSC1X	RLD1X	PSC1X	RLD1X
9,600	0 (1/1)	09H	0 (1/1)	0EH	0 (1/1)	0FH
4,800	0 (1/1)	13H	0 (1/1)	1DH	0 (1/1)	1FH
2,400	0 (1/1)	27H	0 (1/1)	3BH	0 (1/1)	3FH
1,200	0 (1/1)	4FH	0 (1/1)	77H	0 (1/1)	7FH
600	0 (1/1)	9FH	0 (1/1)	EFH	0 (1/1)	FFH
300	1 (1/4)	4FH	1 (1/4)	77H	1 (1/4)	7FH
150	1 (1/4)	9FH	1 (1/4)	EFH	1 (1/4)	FFH

5.11.10 Control of programmable timer

Table 5.11.10.1 shows the programmable timer control bits.

Table 5.11.10.1(a) Programmable timer control bits

Address	Bit	Name	Function		1	0	SR	R/W	Comment
00FF30	D7	–	–		–	–	–		Constantry "0" when being read
	D6	–	–		–	–	–		
	D5	–	–		–	–	–		
	D4	MODE16	8/16-bit mode selection		16-bit x 1	8-bit x 2	0	R/W	
	D3	CHSEL	TOUT output channel selection		Timer 1	Timer 0	0	R/W	
	D2	PTOUT	TOUT output control		On	Off	0	R/W	
	D1	CKSEL1	Prescaler 1 source clock selection		f_{OSC3}	f_{OSC1}	0	R/W	
	D0	CKSEL0	Prescaler 0 source clock selection		f_{OSC3}	f_{OSC1}	0	R/W	
00FF31	D7	EVCNT	Timer 0 counter mode selection		Event counter	Timer	0	R/W	
	D6	FCSEL	Timer 0 function selection	In timer mode	Pulse width measurement	Normal mode	0	R/W	
				In event counter mode	With noise rejector	Without noise rejector			
	D5	PLPOL	Timer 0 pulse polarity selection	Down count timing in event counter mode	Rising edge of K10 input	Falling edge of K10 input	0	R/W	
				In pulse width measurement mode	High level measurement for K10 input	Low level measurement for K10 input			
	D4	PSC01	Timer 0 prescaler dividing ratio selection PSC01 PSC00 Prescaler dividing ratio 1 1 Source clock / 64				0	R/W	
	D3	PSC00	1 0 Source clock / 16 0 1 Source clock / 4 0 0 Source clock / 1				0	R/W	
	D2	CONT0	Timer 0 continuous/one-shot mode selection		Continuous	One-shot	0	R/W	
	D1	PSET0	Timer 0 preset		Preset	No operation	–	W	"0" when being read
	D0	PRUN0	Timer 0 Run/Stop control		Run	Stop	0	R/W	
00FF32	D7	–	–		–	–	–		Constantry "0" when being read
	D6	–	–		–	–	–		
	D5	–	–		–	–	–		
	D4	PSC11	Timer 1 prescaler dividing ratio selection PSC11 PSC10 Prescaler dividing ratio 1 1 Source clock / 64				0	R/W	
	D3	PSC10	1 0 Source clock / 16 0 1 Source clock / 4 0 0 Source clock / 1				0	R/W	
	D2	CONT1	Timer 1 continuous/one-shot mode selection		Continuous	One-shot	0	R/W	
	D1	PSET1	Timer 1 preset		Preset	No operation	–	W	"0" when being read
	D0	PRUN1	Timer 1 Run/Stop control		Run	Stop	0	R/W	
00FF33	D7	RLD07	Timer 0 reload data D7 (MSB)		High	Low	1	R/W	
	D6	RLD06	Timer 0 reload data D6						
	D5	RLD05	Timer 0 reload data D5						
	D4	RLD04	Timer 0 reload data D4						
	D3	RLD03	Timer 0 reload data D3						
	D2	RLD02	Timer 0 reload data D2						
	D1	RLD01	Timer 0 reload data D1						
	D0	RLD00	Timer 0 reload data D0 (LSB)						

Table 5.11.10.1(b) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF34	D7	RLD17	Timer 1 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RLD16	Timer 1 reload data D6					
	D5	RLD15	Timer 1 reload data D5					
	D4	RLD14	Timer 1 reload data D4					
	D3	RLD13	Timer 1 reload data D3					
	D2	RLD12	Timer 1 reload data D2					
	D1	RLD11	Timer 1 reload data D1					
	D0	RLD10	Timer 1 reload data D0 (LSB)					
00FF35	D7	PTD07	Timer 0 counter data D7 (MSB)	High	Low	1	R	
	D6	PTD06	Timer 0 counter data D6					
	D5	PTD05	Timer 0 counter data D5					
	D4	PTD04	Timer 0 counter data D4					
	D3	PTD03	Timer 0 counter data D3					
	D2	PTD02	Timer 0 counter data D2					
	D1	PTD01	Timer 0 counter data D1					
	D0	PTD00	Timer 0 counter data D0 (LSB)					
00FF36	D7	PTD17	Timer 1 counter data D7 (MSB)	High	Low	1	R	
	D6	PTD16	Timer 1 counter data D6					
	D5	PTD15	Timer 1 counter data D5					
	D4	PTD14	Timer 1 counter data D4					
	D3	PTD13	Timer 1 counter data D3					
	D2	PTD12	Timer 1 counter data D2					
	D1	PTD11	Timer 1 counter data D1					
	D0	PTD10	Timer 1 counter data D0 (LSB)					
00FF21	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	PPT1	Programmable timer interrupt priority register	PPT1 PK11: 1 1 Level 3; 1 0 Level 2; 0 1 Level 1; 0 0 Level 0		0	R/W	
	D2	PPT0						
	D1	PK11	K10 and K11 interrupt priority register			0	R/W	
	D0	PK10						
00FF23	D7	EPT1	Programmable timer 1 interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D6	EPT0	Programmable timer 0 interrupt enable register					
	D5	EK1	K10 and K11 interrupt enable register					
	D4	EK0H	K04–K07 interrupt enable register					
	D3	EK0L	K00–K03 interrupt enable register					
	D2	ESERR	Serial I/F (error) interrupt enable register					
	D1	ESREC	Serial I/F (receiving) interrupt enable register					
	D0	ESTRA	Serial I/F (transmitting) interrupt enable register					
00FF25	D7	FPT1	Programmable timer 1 interrupt factor flag	(R) Interrupt factor is generated / (W) Reset	(R) No interrupt factor is generated / (W) No operation	0	R/W	
	D6	FPT0	Programmable timer 0 interrupt factor flag					
	D5	FK1	K10 and K11 interrupt factor flag					
	D4	FK0H	K04–K07 interrupt factor flag					
	D3	FK0L	K00–K03 interrupt factor flag					
	D2	FSERR	Serial I/F (error) interrupt factor flag					
	D1	FSREC	Serial I/F (receiving) interrupt factor flag					
	D0	FSTRA	Serial I/F (transmitting) interrupt factor flag					

MODE16: 00FF30H•D4

Selects the 8 / 16-bit mode.

When "1" is written: 16 bits × 1 channel
When "0" is written: 8 bits × 2 channels
Reading: Valid

Select whether timer 0 and timer 1 will be used as 2 channel independent 8-bit timers or as a 1 channel combined 16-bit timer. When "0" is written to MODE16, 8-bit × 2 channels is selected and when "1" is written, 16-bit × 1 channel is selected.
At initial reset, MODE16 is set to "0" (8-bit × 2 channels).

CKSEL0, CKSEL1: 00FF30H•D0, D1

Select the source clock of the prescaler.

When "1" is written: OSC3 clock
When "0" is written: OSC1 clock
Reading: Valid

Select whether the source clock of prescaler 0 will be set to OSC1 or OSC3. When "0" is written to CKSEL0, OSC1 is selected and when "1" is written, OSC3 is selected.
In the same way, the source clock of prescaler 1 is selected by CKSEL1.
When event counter mode has been selected, the setting of the CKSEL0 becomes invalid. In the same way, the CKSEL1 setting becomes invalid when 16-bit mode has been selected.
At initial reset, this register is set to "0" (OSC1 clock).

PSC00, PSC01: 00FF31H•D3, D4
PSC10, PSC11: 00FF32H•D3, D4

Select the dividing ratio of the prescaler.
Two-bit PSC00 and PSC01 is the prescaler dividing ratio selection registers for timer 0, and the two-bit PSC10 and PSC11 correspond to timer 1. The prescaler dividing ratios that can be set by these registers are shown in Table 5.11.10.2.

Table 5.11.10.2 Selection of prescaler dividing ratio

PSC11 PSC01	PSC10 PSC00	Prescaler dividing ratio
1	1	Input clock / 64
1	0	Input clock / 16
0	1	Input clock / 4
0	0	Input clock / 1

When event counter mode has been selected, the setting of the PSC00 and PSC01 becomes invalid. In the same way, the PSC10 and PSC11 setting becomes invalid when 16-bit mode has been selected.
At initial reset, this register is set to "0" (input clock / 1).

EVCNT: 00FF31H•D7

Selects the counter mode for the timer 0.

When "1" is written: Event counter mode
When "0" is written: Timer mode
Reading: Valid

Select whether timer 0 will be used as an event counter or a timer. When "1" is written to EVCNT, the event counter mode is selected and when "0" is written, the timer mode is selected.
At initial reset, EVCNT is set to "0" (timer mode).

FCSEL: 00FF31H•D6

Selects the function for each counter mode of timer 0.

• In timer mode

When "1" is written: Pulse width measurement timer mode
When "0" is written: Normal mode
Reading: Valid

In the timer mode, select whether timer 0 will be used as a pulse width measurement timer or a normal timer. When "1" is written to FCSEL, the pulse width measurement mode is selected and the counting is done according to the level of the signal (EVIN) input to the K10 input port terminal. When "0" is written to FCSEL, the normal mode is selected and the counting is not affected by the K10 input port terminal.

• In event counter mode

When "1" is written: With noise rejecter
When "0" is written: Without noise rejecter
Reading: Valid

In the event counter mode, select whether the noise rejecter for the K10 input port terminal will be selected or not.
When "1" is written to FCSEL, the noise rejecter is selected and counting is done by an external clock (EVIN) with 0.98 msec or more pulse width. (The noise rejecter allows clocking counter at the second falling edge of the internal 2,048 Hz signal after changing the input level of the K10 input port terminal. Consequently, the pulse width that can reliably be rejected is 0.48 msec.)
When "0" is written to FCSEL, the noise rejector is not selected and the counting is done directly by an external clock (EVIN) input to the K10 input port terminal.
At initial reset, FCSEL is set to "0".

PLPOL: 00FF31H•D5

Selects the pulse polarity for the K10 input port terminal.

• In event counter mode

When "1" is written: Rising edge
When "0" is written: Falling edge
Reading: Valid

In the event counter mode, select whether the count timing will be set at the falling edge of the external clock (EVIN) input to the K10 input port terminal or at the rising edge. When "0" is written to PLPOL, the falling edge is selected and when "1" is written, the rising edge is selected.

• In pulse width measurement mode

When "1" is written: High level pulse width measurement
When "0" is written: LOW level pulse width measurement
Reading: Valid

In the pulse width measurement mode, select whether the LOW level width of the signal (EVIN) input to the K10 input port terminal will be measured or the HIGH level will be measured. When "0" is written to PLPOL, the LOW level width measurement is selected and when "1" is written, the HIGH level width measurement is selected.
In the normal mode (EVCNT = FCSEL = "0"), the setting of PLPOL becomes invalid.
At initial reset, PLPOL is set to "0".

CONT0, CONT1: 00FF31H•D2, 00FF32H•D2

Select the continuous / one-shot mode.

When "1" is written: Continuous mode
When "0" is written: One-shot mode
Reading: Valid

Select whether timer 0 will be used in the continuous mode or in the one-shot mode.
By writing "1" to CONT0, the programmable timer is set to the continuous mode. In the continuous mode, the initial counter value is automatically loaded when an underflow is generated, and counting is continued. On the other hand, when writing "0" to CONT0, the programmable timer is set to the one-shot mode. The counter loads an initial value and stops when an underflow is generated. At this time, PRUN0 is automatically reset to "0".
In the same way, the continuous / one-shot mode for timer 1 is selected by CONT1. (In the one-shot mode for timer 1, PRUN1 is automatically reset to "0" when the counter underflow is generated.)
At initial reset, this register is set to "0" (one-shot mode).

RLD00–RLD07: 00FF33H
RLD10–RLD17: 00FF34H

Sets the initial value for the counter.

RLD00–RLD07: Reload data for Timer 0
RLD10–RLD17: Reload data for Timer 1

The reload data set in this register is loaded into the respective counters and is counted down with that as the initial value.
Reload data is loaded to the counter under two conditions, when "1" is written to PSET0 or PSET1 and when the counter underflow automatically loads.
At initial reset, this register is set to "FFH".

PTD00–PTD07: 00FF35H
PTD10–PTD17: 00FF36H

Data of the programmable timer can be read out.

PTD00–PTD07: Timer 0 counter data
PTD10–PTD17: Timer 1 counter data

These bits act as a buffer to maintain the counter data during readout, and the data can be read as optional timing. However, in the 16-bit mode, to avoid a read error, (data error when a borrow from timer 0 to timer 1 is generated in the middle of reading PTD00–PTD07 and PTD10–PTD17), PTD10–PTD17 latches the timer 1 counter data according to the reading of PTD00–PTD07.
The latched status of PTD10–PTD17 is canceled according to the readout of PTD10–PTD17 or when 0.73–1.22 msec (depends on the readout timing) has elapsed. Therefore, in 16-bit mode, be sure to read the counter data of PTD00–PTD07 and PTD10–PTD17 in order.
Since these bits are exclusively for reading, the write operation is invalid.
At initial reset, these bits are set to "FFH".

PSET0, PSET1: 00FF31H•D1, 00FF32H•D1

Presets the reload data to the counter.

When "1" is written: Preset
When "0" is written: No operation
Reading: Always "0"

By writing "1" to PSET0, the reload data in PLD00–PLD07 is preset to the counter of timer 0. When the counter of timer 0 is preset in the RUN status, it restarts immediately after presetting.
In the case of STOP status, the reload data that has been preset is maintained.
No operation results when "0" is written.
In the same way, the reload data in PLD10–PLD17 is preset to the counter of timer 1 by PSET1.
When the 16-bit mode is selected, writing "1" to PSET1 is invalid.
This bit is exclusively for writing, it always becomes "0" during reading.

PRUN0, PRUN1: 00FF31H•D0, 00FF32H•D0

Controls the RUN / STOP of the counter.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The counter of timer 0 starts down-counting by writing "1" to PRUN0 and stops by writing "0". In the STOP status, the counter data is maintained until it is preset or set in the next RUN status. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.
In the same way, the RUN / STOP of the timer 1 counter is controlled by PRUN1.
When the 16-bit mode is selected, PRUN1 is fixed at "0".
At initial reset and when an underflow is generated in the one-shot mode, this register is set to "0" (STOP).

CHSEL: 00FF30H•D3

Selects the channel of the TOUT signal.

When "1" is written: Timer 0 underflow
When "0" is written: Timer 1 underflow
Reading: Valid

Select whether the timer 0 underflow will be used for the TOUT signal or the timer 1 underflow will be used. When "0" is written to CHSEL, timer 0 is selected and when "1" is written, timer 1 is selected. When the 16-bit mode has been selected, it is fixed to timer 1 (underflow of the 16-bit timer), and setting of CHSEL becomes invalid.
At initial reset, CHSEL is set to "0" (timer 1 underflow).

PTOUT: 00FF30H•D2

Controls the TOUT signal output.

When "1" is written: TOUT signal output
When "0" is written: HIGH level (DC) output
Reading: Valid

PTOUT is the output control register for TOUT signal. When "1" is set, the TOUT signal is output from the output port terminal R27 and when "0" is set, HIGH (V_{DD}) level is output. At this time, "1" must always be set for the data register R27D.
At initial reset, PTOUT is set to "0" (HIGH level output).

PPT0, PPT1: 00FF21H•D2, D3

Sets the priority level of the programmable timer interrupt.
The two bits PPT0 and PPT1 are the interrupt priority register corresponding to the programmable timer interrupt. Table 5.11.10.3 shows the interrupt priority level which can be set by this register.

Table 5.11.10.3 Interrupt priority level settings

PPT1	PPT0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

EPT0, EPT1: 00FF23H•D6, D7

Enables or disables the generation of an interrupt for the CPU.

When "1" is written: Interrupt enabled
When "0" is written: Interrupt disabled
Reading: Valid

The EPT0 and EPT1 are interrupt enable registers that respectively correspond to the interrupt factors for timer 0 and timer 1. Interrupts set to "1" are enabled and interrupts set to "0" are disabled.
When the 16-bit mode is selected, setting of EPT0 becomes invalid.
At initial reset, this register is set to "0" (interrupt disabled).

FPT0, FPT1: 00FF25H•D6, D7

Indicates the programmable timer interrupt generation status.

When "1" is read: Interrupt factor present
When "0" is read: Interrupt factor not present

When "1" is written: Resets factor flag
When "0" is written: Invalid

The FPT0 and FPT1 are interrupt factor flags that respectively correspond to the interrupts for timer 0 and timer 1 and are set to "1" in synchronization with the underflow of each counter.
When set in this manner, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU. Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.
To accept the subsequent interrupt after interrupt generation, re-setting of the interrupt flags (set interrupt flag to lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and interrupt factor flag reset are necessary. The interrupt factor flag is reset to "0" by writing "1".
When the 16-bit mode is selected, the interrupt factor flag FPT0 is not set to "1" and a timer 0 interrupt cannot be generated. (In the 16-bit mode, the interrupt factor flag FPT1 is set to "1" by an underflow of the 16-bit counter.)
At initial reset, this flag is reset to "0".

5.11.11 Programming notes

(1) The programmable timer is actually made to RUN / STOP in synchronization with the falling edge of the input clock after writing to the PRUN0(1) register. Consequently, when "0" is written to the PRUN0(1), the timer shifts to STOP status when the counter is decremented "1". The PRUN0(1) maintains "1" for reading until the timer actually shifts to STOP status. Figure 5.11.11.1 shows the timing chart of the RUN / STOP control.

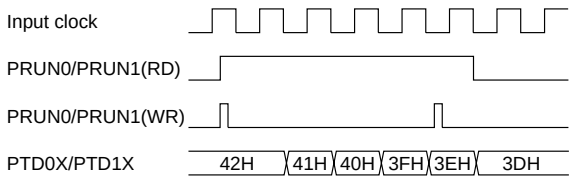


Fig. 5.11.11.1 Timing chart of RUN/STOP control

The event counter mode is excluded from the above note.

(2) The SLP instruction is executed when the programmable timer is in the RUN status (PRUN0(1) = "1"). The programmable timer operation will become unstable when returning from SLEEP status. Therefore, when shifting to SLEEP status, set the clock timer to STOP status (PRUN0(1) = "0") prior to executing the SLP instruction.
In the same way, disable the TOUT signal (PTOUT = "0") to avoid an unstable clock output to the R27 output port terminal.

(3) Since the TOUT signal is generated asynchronously from the register PTOUT, when the signal is turned ON or OFF by the register setting, a hazard of a 1/2 cycle or less is generated.

(4) When the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer.
From the time the OSC3 oscillation circuit is turning ON until oscillation stabilizes, an interval of several msec to several 10 msec is necessary. Consequently, you should allow an adequate waiting time after turning the OSC3 oscillation circuit ON before starting the count of the programmable timer. (The oscillation start time will vary somewhat depending on the oscillator and on external parts. Refer to the oscillation start time example indicated in Chapter 8, "ELECTRICAL CHARACTERISTICS".)
At initial reset, OSC3 oscillation circuit is set to OFF status.

(5) When the 16-bit mode has been selected, be sure to read the counter data in the order of PTD00–PTD07 and PTD10–PTD17. Moreover, the time interval between reading PTD00–PTD07 and PTD10–PTD17 should be 0.73 msec or less.

5.12 LCD Controller

5.12.1 Configuration of LCD controller

The S1C88349 has a built-in dot matrix LCD driver. The S1C88349 allows an LCD panel with a maximum of 1,632 dots (51 segments × 32 commons). It also has an LCD controller for an external LCD driver (S1D15210 or equivalent).
Figure 5.12.1.1 shows the configuration of the LCD controller and the drive power supply.

Note: Refer to the "S1D15000 Series Technical Manual" for the S1D15210 externaly expanded LCD driver.

5.12.2 Mask option

The mask option allows selection of the power source that supplies the LCD drive voltages V_{D1} to V_{D5}. Either the internal power supply configured with a voltage regulator and a voltage booster or an external power supply can be selected.

LCD power source
☐ Internal power supply
☐ External power supply

5.12.3 Switching drive duty

The S1C88349 supports three types of LCD drive duty settings, 1/8, 1/16 and 1/32, and it can be switched using the LDUTY and DUTY8 registers. When "0" is written to the drive duty selection register LDUTY, 1/32 duty is selected and when "1" is written, 1/16 duty is selected.
When "1" is written to DUTY8, the drive duty is fixed at 1/8 and setting of LDUTY becomes invalid.

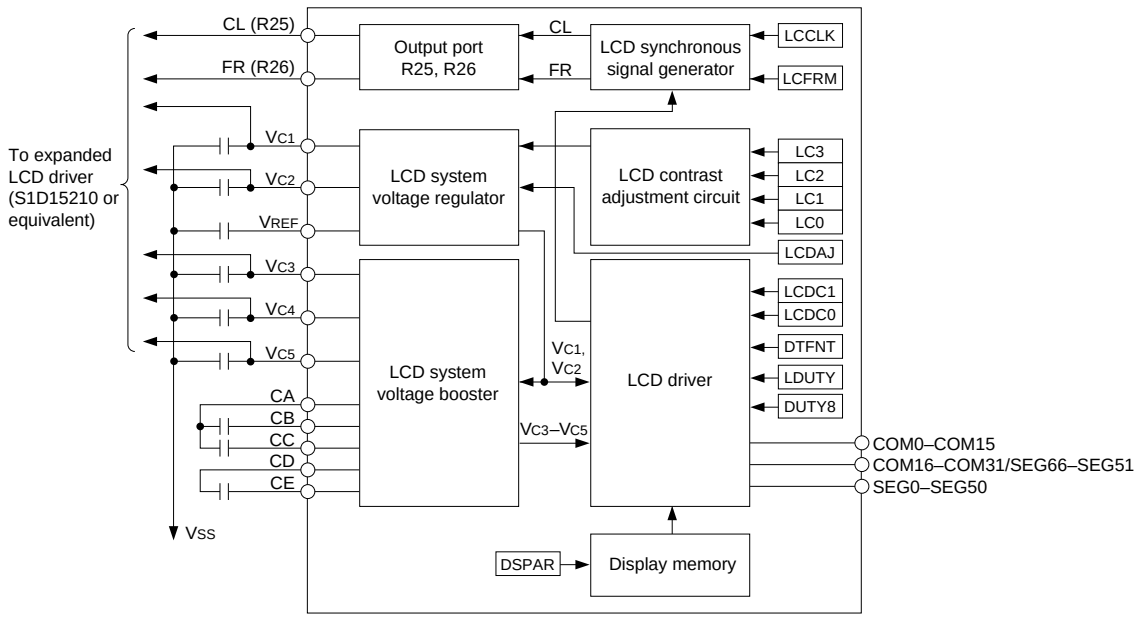
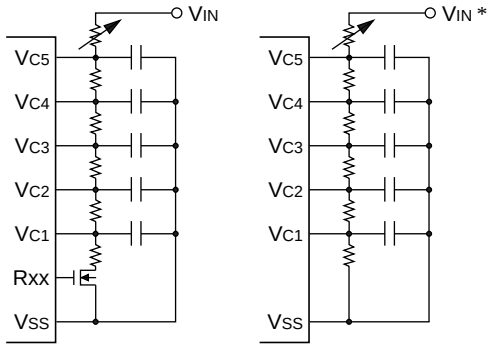


Fig. 5.12.1.1 Configuration of LCD controller and drive power supply

5.12.4 LCD power supply

The LCD drive voltages V_{C1}–V_{C5} can be generated by the internal voltage regulator and voltage booster circuits or can be supplied from an external power supply. The power source is selected by mask option.
The internal power supply generates two types of reference voltage, TYPE A (4.5 V) and TYPE B (5.5 V), and either one can be selected according to the panel characteristics using the LCDAJ register.
The internal power supply is designed for a small scale LCD panel and is not suitable for driving a panel that has large size pixels or for driving a large capacity panel using an external expanded LCD driver. In this case, select external power supply and input the regulated voltage from outside of the IC.
Figure 5.12.4.1 shows the circuit examples when using an external power supply.



* V_{SS} level or high impedance when LCD is not driven.

Fig. 5.12.4.1 Circuit examples when using an external power supply

5.12.5 LCD driver

The maximum number of dots changes according to the drive duty selection.
When 1/32 duty is selected, the combined common/segment output terminal is switched to the common terminal. An LCD panel with 51 segments × 32 commons (maximum 1,632 dots) can be driven in the S1C88349. When 1/16 duty is selected, the combined common/segment output terminal is switched to the segment terminal. An LCD panel with 67 segments × 16 commons (maximum 1,072 dots) in the S1C88349 can be driven. When 1/8 duty is selected, the combined common/segment output terminal is switched to the segment terminal as when 1/16 duty is selected. An LCD panel with 67 segments × 8 commons (maximum 536 dots) in the S1C88349 can be driven. Furthermore, when 1/8 duty is selected, terminals COM8–COM15 become invalid, in that they always output an OFF signal.
Table 5.12.5.1 shows the correspondence between the drive duty and the maximum number of displaying dots. The drive bias is 1/5 (five potentials, V_{C1}–V_{C5}) for any one of the 1/32, 1/16 and 1/8 duties. The respective drive waveforms are shown in Figures 5.12.5.1–5.12.5.3.

Table 5.12.5.1 Correspondence between drive duty and maximum number of displaying dots

DUTY8	LDUTY	Duty	Common terminal	Segment terminal	Maximum number of display dots
0	0	1/32	COM0–COM31	SEG0–SEG50	1,632 dots
0	1	1/16	COM0–COM15	SEG0–SEG66	1,072 dots
1	×	1/8	COM0–COM7	SEG0–SEG66	536 dots

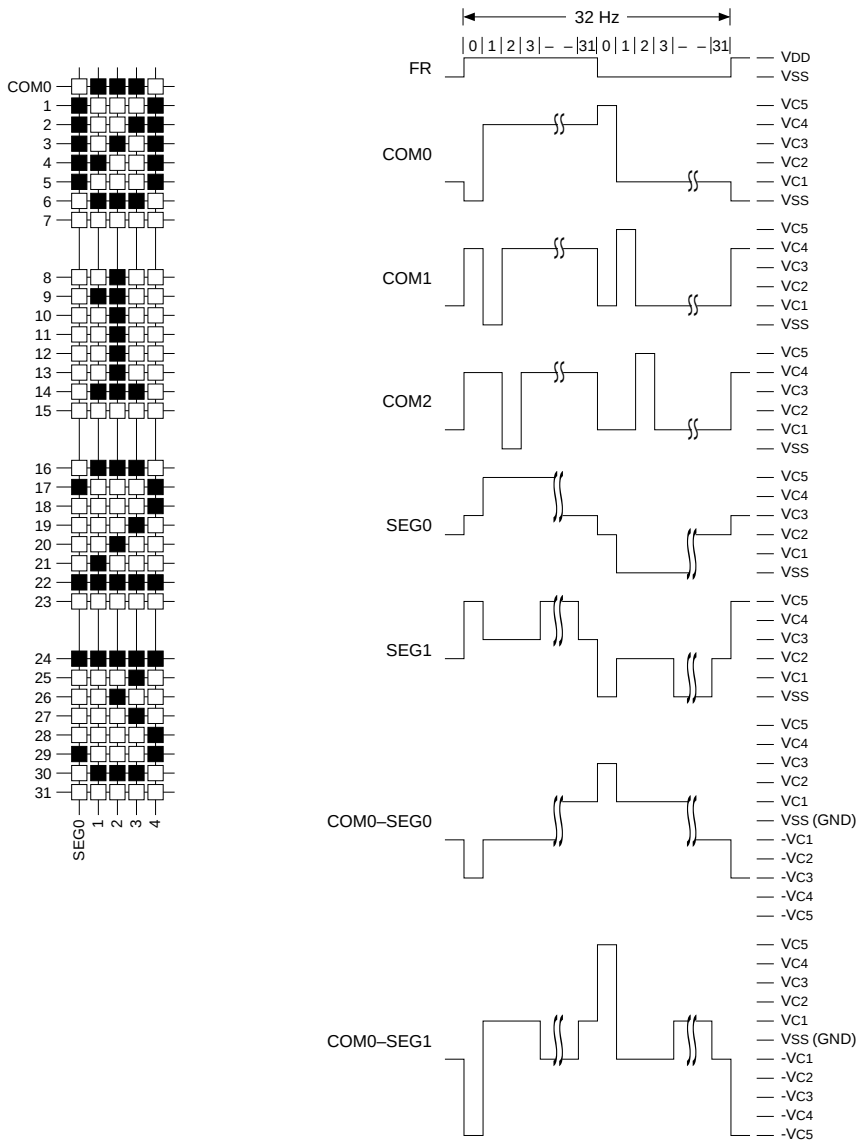


Fig. 5.12.5.1 Drive waveform for 1/32 duty

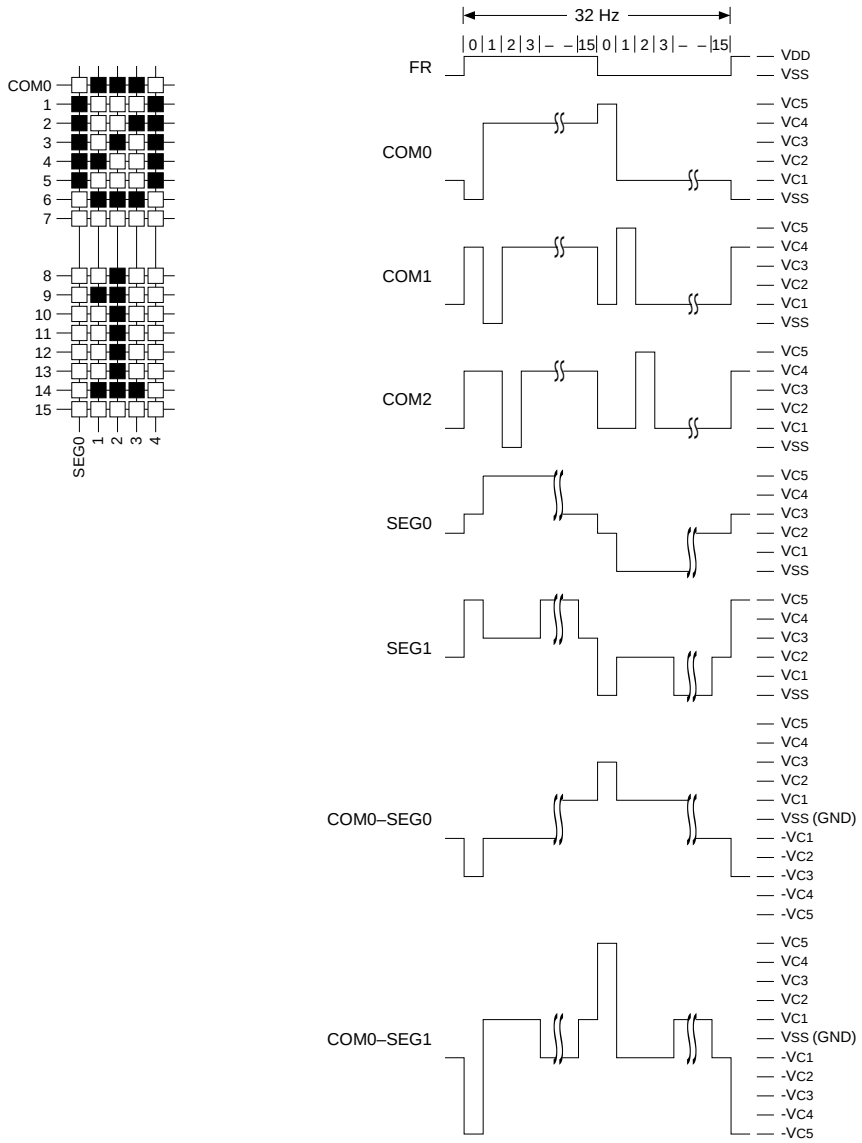


Fig. 5.12.5.2 Drive waveform for 1/16 duty

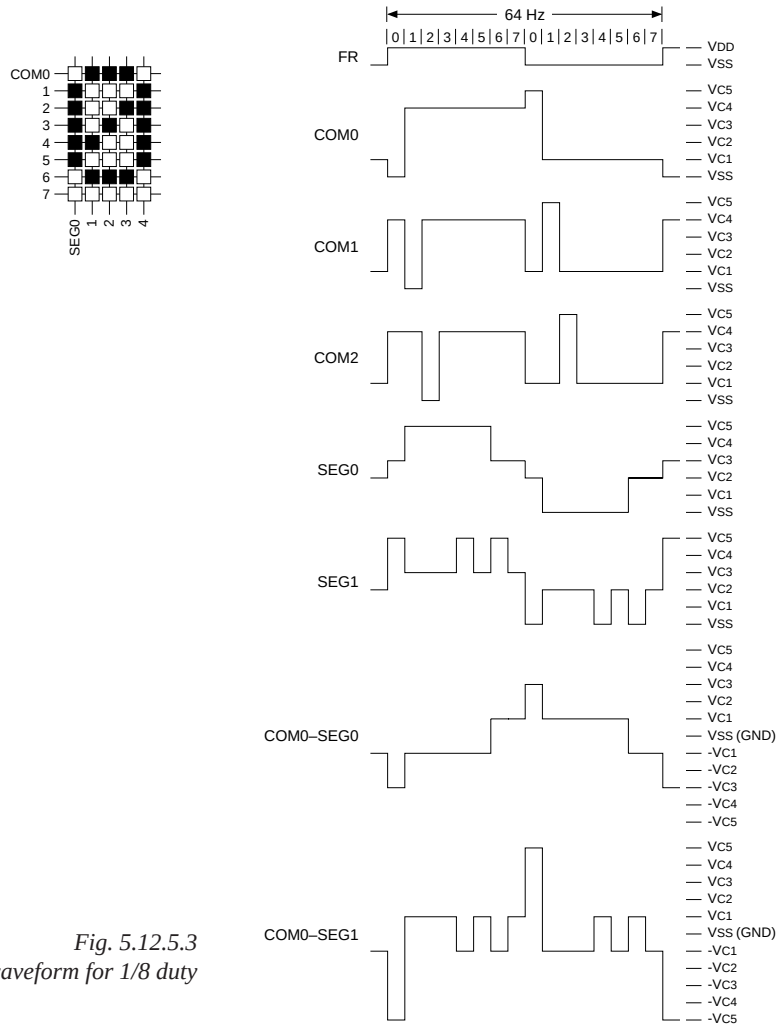


Fig. 5.12.5.3
Drive waveform for 1/8 duty

5.12.6 Display memory

The S1C88349 has a built-in 402-byte display memory. The display memory is allocated to address Fx00H–Fx42H (x = 8–DH) and the correspondence between the memory bits and common / segment terminal is changed according to the selection status of the following items.

(1) Drive duty (1/32, 1/16 or 1/8 duty)
(2) Dot font (5 × 8 or 5 × 5 dots)

When 1/16 or 1/8 duty is selected for drive duty, two-screen memory can be secured, and the two screens can be switched by the display memory area selection register DSPAR. When "0" is written to DSPAR, display area 0 is selected and when "1" is written, display area 1 is selected.
Furthermore, memory allocation for 5 × 8 dots and 5 × 5 dots can be selected in order to easily display 5 x 5-dot font characters on the LCD panel. This selection can be done by the dot font selection register DTFNT: when "0" is written to DTFNT, 5 × 8 dots is selected and when "1" is written, 5 × 5 dots is selected.

The correspondence between the display memory bits set according to the drive duty and font size, and the common / segment terminals are shown in Figures 5.12.6.1–5.12.6.6.
When "1" is written to the display memory bit corresponding to the dot on the LCD panel, the dot goes ON and when "0" is written, it goes OFF. Since display memory is designed to permit reading / writing, it can be controlled in bit units by logical operation instructions and other means (read, modify and write instruction)s.
The display area bits which have not been assigned within the 402-byte display memory can be used as general purpose RAM with read / write capabilities. Even when external memory has expanded into the display memory area, this area is not released to external memory. Access to this area is always via display memory.

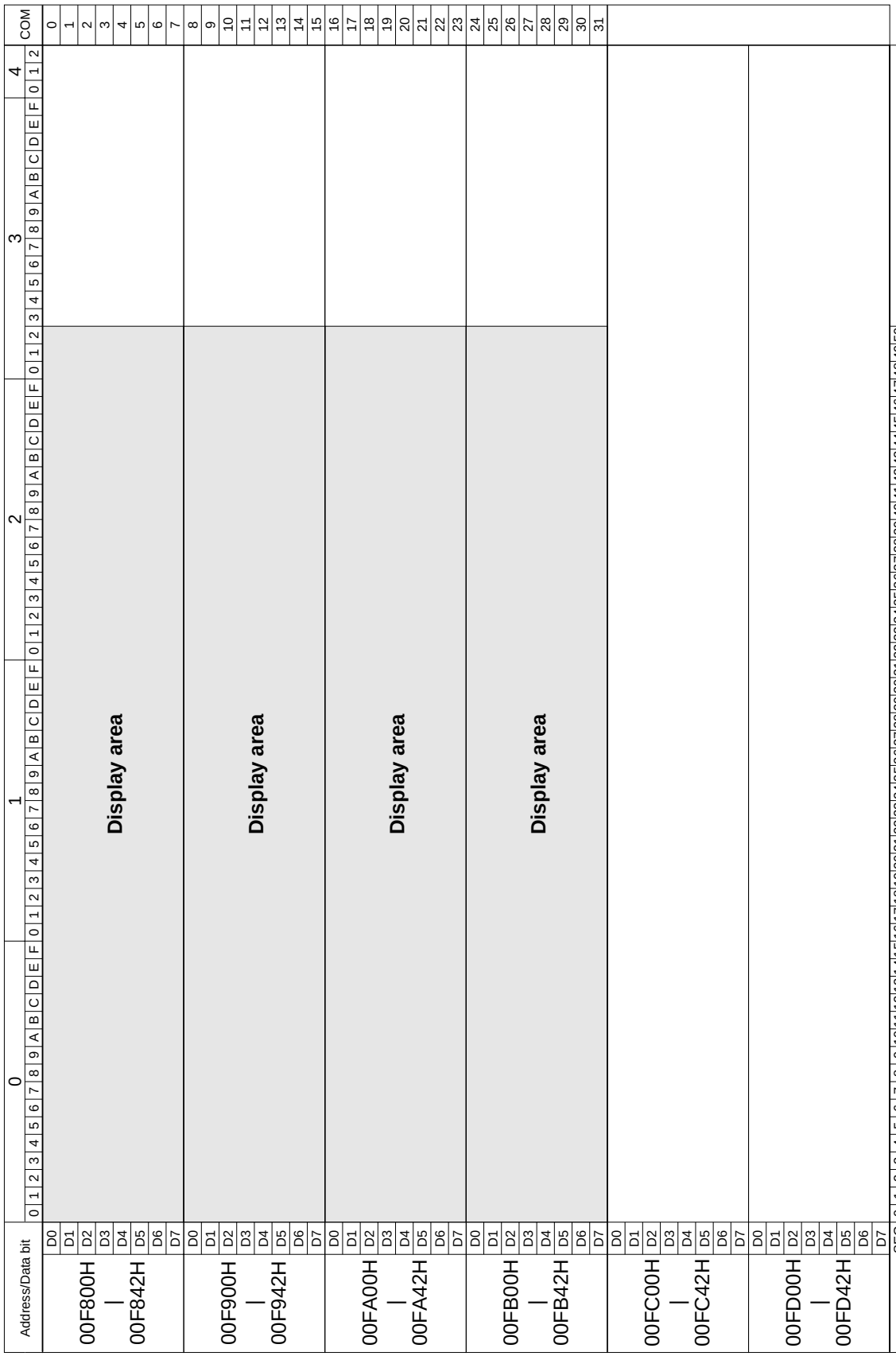


Fig. 5.12.6.1 1/32 duty and 5 × 8 dots display memory map

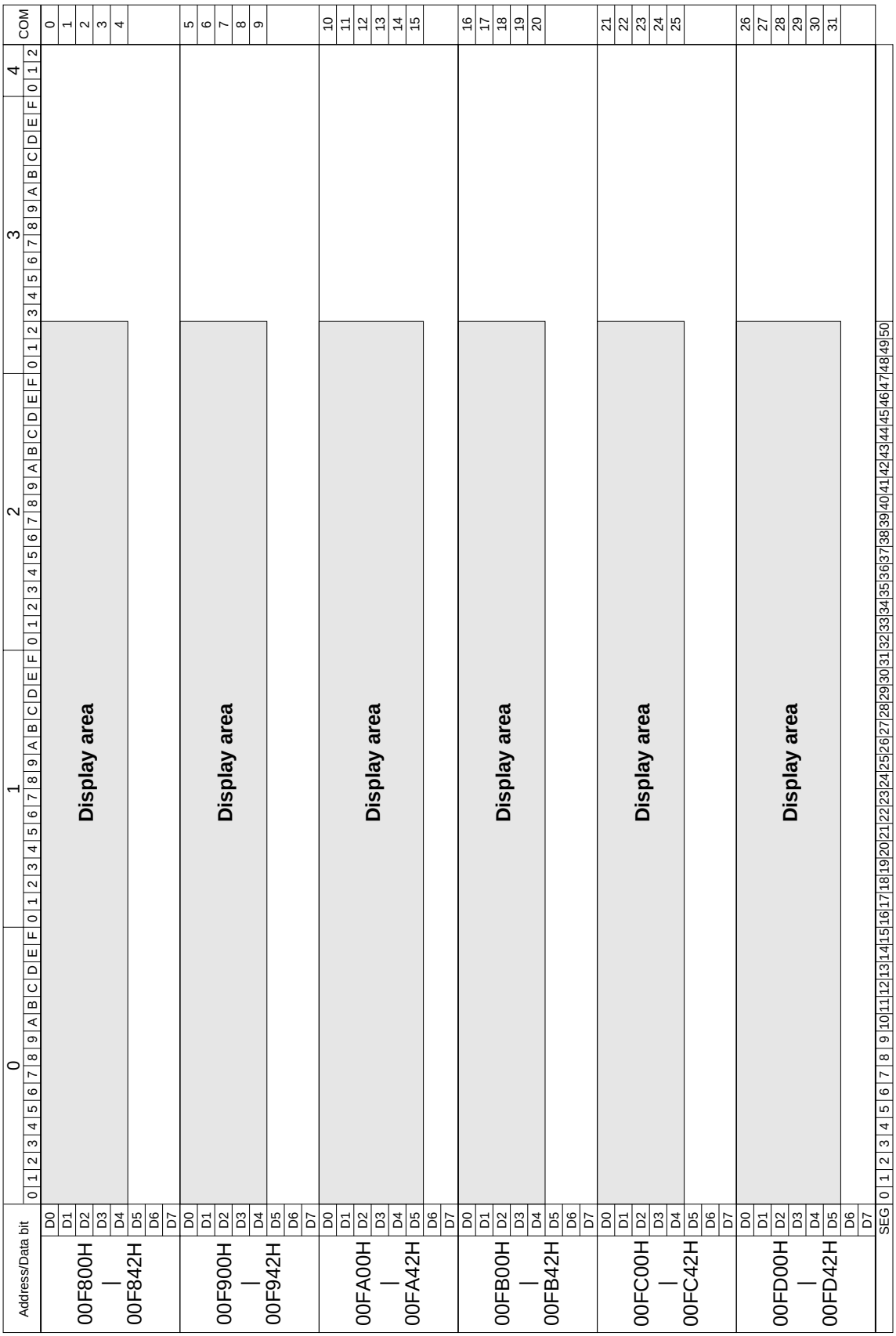


Fig. 5.12.6.2 1/32 duty and 5 ×5 dots display memory map

Fig. 5.12.6.3 1/16 duty and 5 × 8 dots display memory map

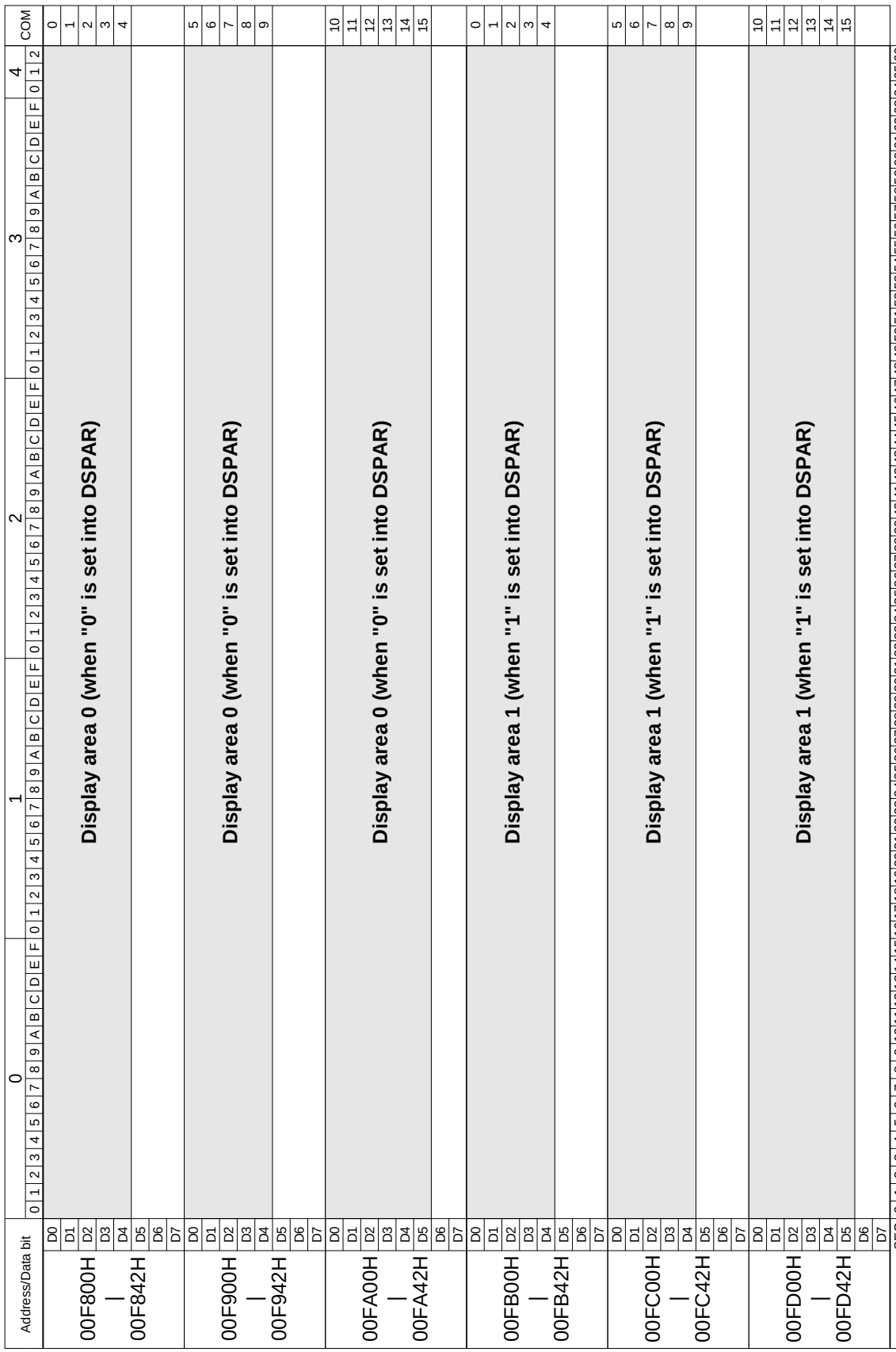


Fig. 5.12.6.4 1/16 duty and 5 ×5 dots display memory map

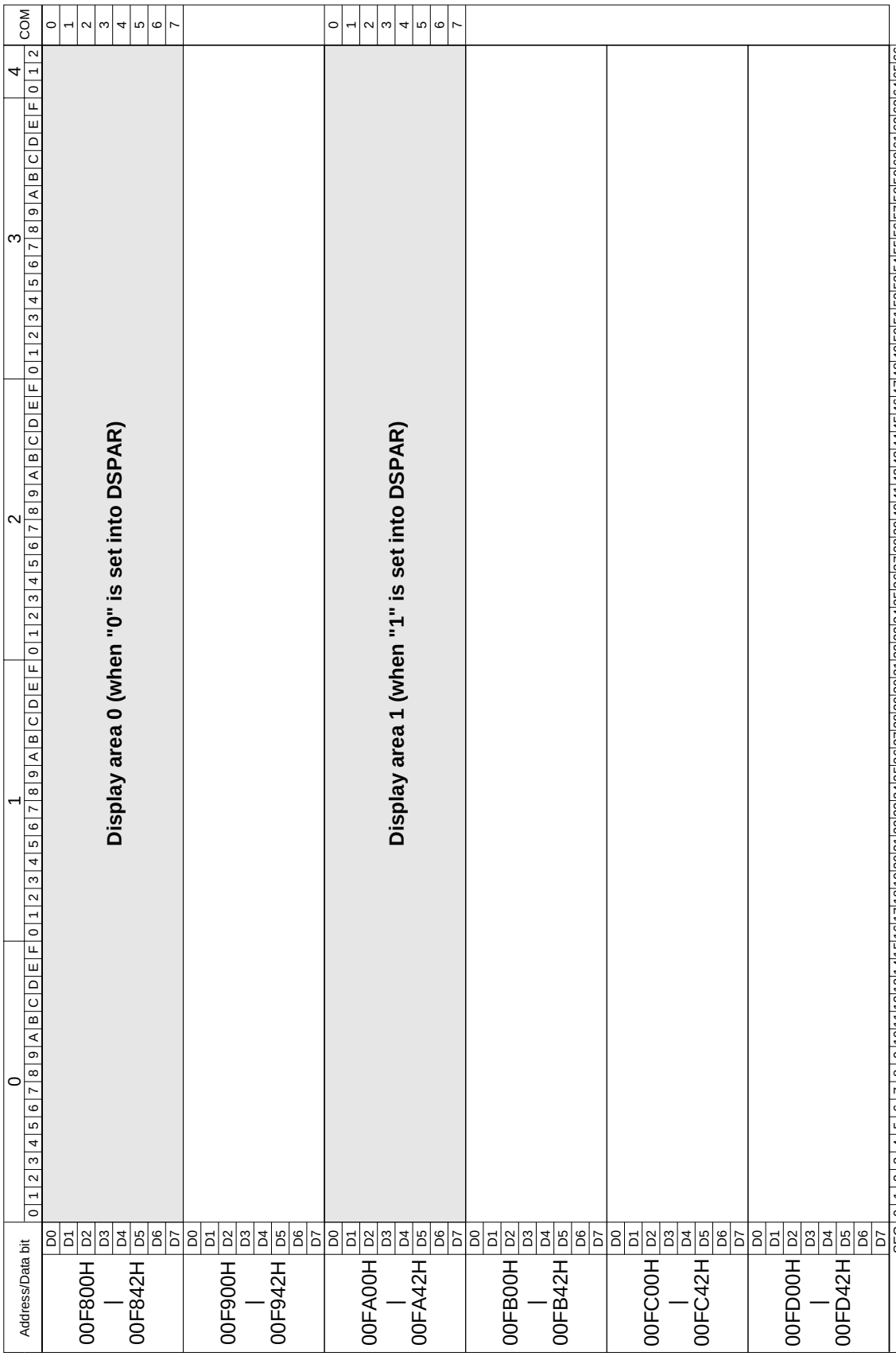


Fig. 5.12.6.5 1/8 duty and 5 × 8 dots display memory map

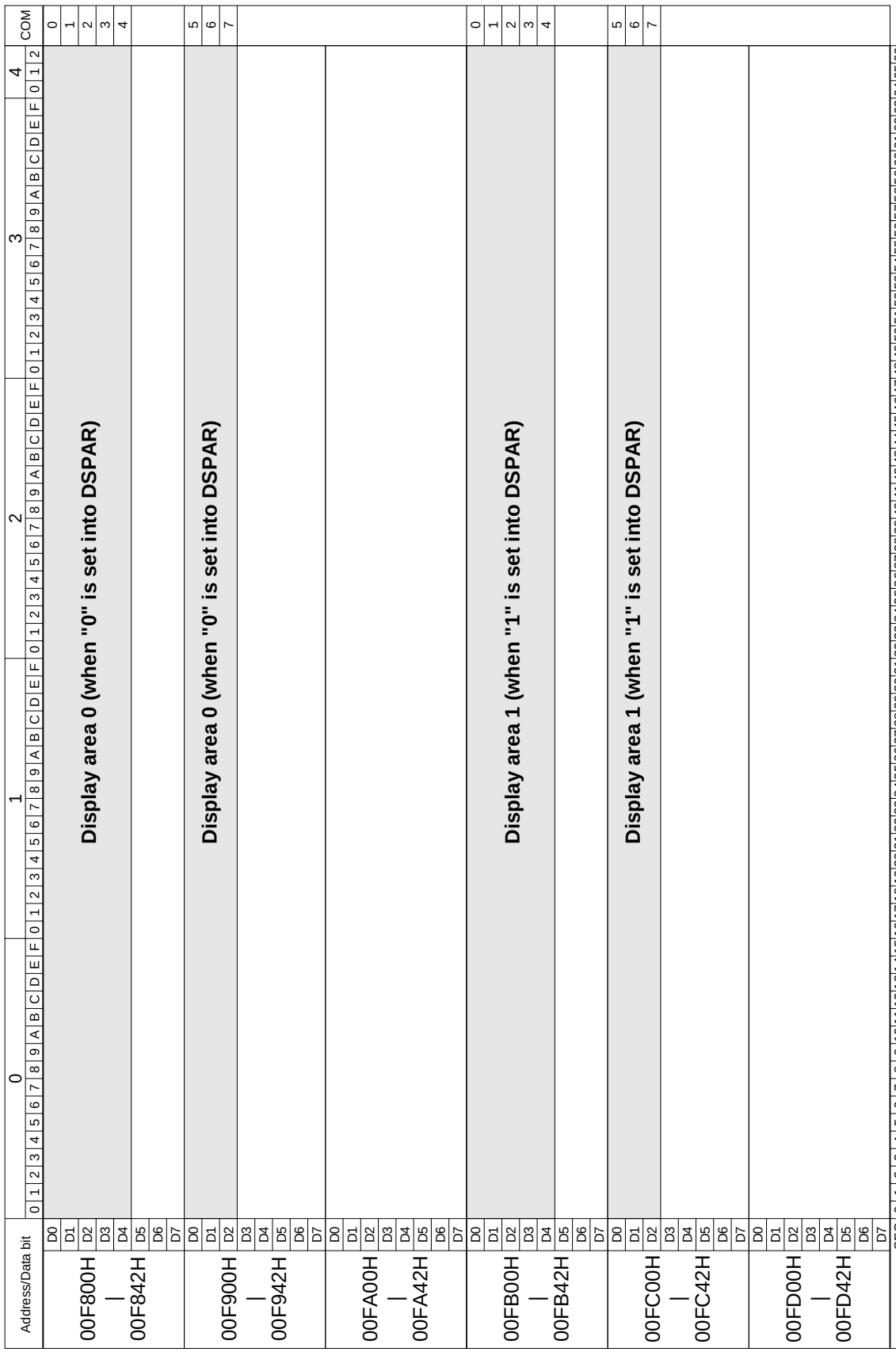


Fig. 5.12.6.6 1/8 duty and 5 × 5 dots display memory map

5.12.7 Display control

The display status of the built-in LCD driver and the contrast adjustment can be controlled with the built-in LCD controller. The LCD display status can be selected by display control registers LCDC0 and LCDC1. Setting the value and display status are shown in Table 5.12.7.1.

Table 5.12.7.1 LCD display control

LCDC1	LCDC0	LCD display
1	1	All LCDs lit (Static)
1	0	All LCDs out (Dynamic)
0	1	Normal display
0	0	Drive OFF

All the dots in the LCD display can be turned on or off directly by the drive waveform output from the LCD driver, and data in the display memory is not changed. Also, since the common terminal at this time is set to static drive when all the dots are on and is set to dynamic drive when they are off, this function can be used as follows:

(1) Since all dots on is binary output (V_{C5} and V_{SS}) with static drive, the common / segment terminal can be used as a monitor terminal for the OSC1 oscillation frequency adjustment.

(2) Since all dots off is dynamic drive, you can brink the entire LCD display without changing display memory data.

Selecting LCD drive OFF turns the LCD drive power circuit OFF and all the V_{C1}–V_{C5} terminals go to V_{SS} level. However, if external power supply has been selected by the mask option, the V_{C1}–V_{C5} shift to floating status when drive is turned OFF. Furthermore, when the SLP instruction is executed, registers LCDC0 and LCDC1 are automatically reset to "0" (set to drive off) by hardware.

The LCD contrast can be adjusted in 16 stages. This adjustment is done by the contrast adjustment register LC0–LC3, and the setting values correspond to the contrast as shown in Table 5.12.7.2. However, if external power supply has been selected by the mask option, the contrast adjustment register LC0–LC3 is ineffective and contrast adjustment cannot be done.

Table 5.12.7.2 LCD contrast adjustment

LC3	LC2	LC1	LC0	Contrast
1	1	1	1	Dark
1	1	1	0	↑
1	1	0	1	
:	:	:	:	
0	0	1	0	
0	0	0	1	↓
0	0	0	0	Light

5.12.8 CL and FR outputs

In order for the S1C88349 to handle connection to an externally expanded LCD driver, output ports R25 and R26 can be used to output a CL signal (LCD synchronous signal) and FR signal (LCD frame signal), respectively.
The configuration of output ports R25 and R26 are shown in Figure 5.12.8.1.

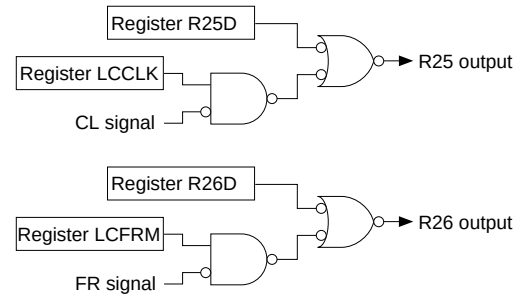


Fig. 5.12.8.1 Configuration of R25 and R26

The output control for the CL signal is done by the register LCCLK. When you set "1" for the LCCLK, the CL signal is output from the output port terminal R25, when "0" is set, the HIGH (V_{DD}) level is output. At this time, "1" must always be set for the data register R25D.
The output control for the FR signal is done by the register LCFRM. When you set "1" for the LCFRM, the FR signal is output from the output port terminal R26, when "0" is set, the HIGH (V_{DD}) level is output. At this time, "1" must always be set for the data register R26D.
The frequencies of each signal are changed as shown in Table 5.12.8.1 according to the drive duty selection.

Table 5.12.8.1 Frequencies of CL and FR signals

Drive duty	CL signal (Hz)	FR signal (Hz)
1/32	2,048	32
1/16	1,024	32
1/8	1,024	64

Since the signals are generated asynchronously from the registers LCCLK and LCFRM, when the signals are turned ON or OFF by the register settings, a hazard of a 1/2 cycle or less is generated. Figure 5.12.8.2 shows the output waveforms of the CL and FR signals.

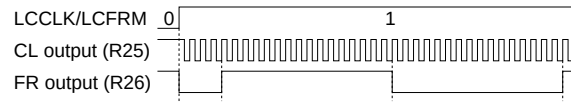


Fig. 5.12.8.2 Output waveforms of CL and FR signals (when 1/16 duty is selected)

5.12.9 Control of LCD controller

Table 5.12.9.1 shows the LCD controller control bits.

Table 5.12.9.1 LCD controller control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF09	D7	–	–	–	–	–		
	D6	–	–	–	–	–		Constantry "0" when being read
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	VCCHG	Reserved	1	0	0	R/W	
	D2	LCDB	Reserved	1	0	0	R/W	
	D1	LCDAJ	Power TYPE A (4.5V)/B (5.5V) switch	TYPE A	TYPE B	0	R/W	
	D0	DUTY8	LCD drive duty switch	1/8 duty	1/16, 1/32	0	R/W	*1
00FF10	D7	–	–	–	–	–		Constantry "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	LCCLK	CL output control for expanded LCD driver	On	Off	0	R/W	
	D3	LCFRM	FR output control for expanded LCD driver	On	Off	0	R/W	
	D2	DTFNT	LCD dot font selection	5 x 5 dots	5 x 8 dots	0	R/W	
	D1	LDUTY	LCD drive duty selection	1/16 duty	1/32 duty	0	R/W	*1
	D0	SGOUT	R/W register	1	0	0	R/W	Reserved register
00FF11	D7	–	–	–	–	–		"0" when being read
	D6	DSPAR	LCD display memory area selection	Display area 1	Display area 0	0	R/W	
	D5	LCDC1	LCD display control LCDC1 LCDC0 LCD display 1 1 All LCDs lit 1 0 All LCDs out 0 1 Normal display 0 0 Drive off			0	R/W	These bits are reset to (0, 0) when SLP instruction is executed.
	D4	LCDC0				0	R/W	
	D3	LC3	LCD contrast adjustment LC3 LC2 LC1 LC0 Contrast 1 1 1 1 Dark 1 1 1 0 : : : : : : 0 0 0 0 Light			0	R/W	
	D2	LC2				0	R/W	
	D1	LC1				0	R/W	
	D0	LC0				0	R/W	

*1 Writing "1" to DUTY8 (FF09•D0) disables 1/16 and 1/32 duty selection using LDUTY (FF10•D1).

LCDAJ: 00FF09H•D1

Switches the internal power supply.

When "1" is written: TYPE A
When "0" is written: TYPE B
Reading: Valid

LCDAJ is the LCD power switching register. When "1" is written, the LCD power supply is set for TYPE A (4.5 V) and when "0" is written the LCD power supply is set for TYPE B (5.5 V).
At initial reset, LCDAJ is set to "0" (TYPE B).

DUTY8: 00FF09H•D0

Switches the drive duty.

When "1" is written: 1/8 duty
When "0" is written: 1/16 or 1/32 duty
Reading: Valid

DUTY8 is the drive duty switching register. When "1" is written, 1/8 duty is selected and when "0" is written, 1/16 or 1/32 duty is selected.
When "1" is written to DUTY8, switching between 1/16 duty and 1/32 duty using LDUTY becomes invalid.
At initial reset, DUTY8 is set to "0" (1/16 or 1/32 duty).

LDUTY: 00FF10H•D1

Selects the drive duty.

When "1" is written: 1/16 duty
When "0" is written: 1/32 duty
Reading: Valid

When "0" is written to LDUTY, 1/32 duty is selected and the combined common/segment output terminal is switched to the common terminal.
When "1" is written to LDUTY, 1/16 duty is selected and the combined common/segment output terminal is switched to the segment terminal.
When "1" is written to DUTY8, the combined common/segment terminals are fixed to the segment terminals and the setting of LDUTY becomes invalid.
The correspondence between the display memory bits set according to the drive duty, and the common/segment terminals are shown in Figures 5.12.6.1–5.12.6.6.
At initial reset, LDUTY is set to "0" (1/32 duty).

DTFNT: 00FF10H•D2

Selects the dot font.

When "1" is written: 5 × 5 dots
When "0" is written: 5 × 8 dots
Reading: Valid

Select 5 × 8 dots or 5 × 5 dots type for the display memory area.
When "0" is written to DTFNT, 5 × 8 dots is selected and when "1" is written, 5 × 5 dots is selected.
The correspondence between the display memory bits set according to the dot font, and the common/segment terminals are shown in Figures 5.12.6.1–5.12.6.6.
At initial reset, DTFNT is set to "0" (5 × 8 dots).

DSPAR: 00FF11H•D6

Selects the display area.

When "1" is written: Display area 1
When "0" is written: Display area 0
Reading: Valid

Selects which display area is secured for two screens in the display memory, will be displayed when 1/16 or 1/8 duty is selected.
When "0" is written to DSPAR, display area 0 is selected and when "1" is written, display area 1 is selected.
When 1/32 duty is selected, since the display area is only for one screen, the setting of DSPAR becomes invalid.
The correspondence between the display memory bits set according to the display area, and the common/segment terminals are shown in Figures 5.12.6.1–5.12.6.6.
At initial reset, DSPAR is set to "0" (display area 0).

LCDC0, LCDC1: 00FF11H•D4, D5

Controls the LCD display.

Table 5.12.9.2 LCD display control

LCDC1	LCDC0	LCD display
1	1	All LCDs lit (Static)
1	0	All LCDs out (Dynamic)
0	1	Normal display
0	0	Drive OFF

The four settings mentioned above can be made without changing the display memory data.
At initial reset and in the SLEEP status, this register is set to "0" (drive off).

LC0–LC3: 00FF11H•D0–D3

Adjusts the LCD contrast.

Table 5.12.9.3 LCD contract adjustment

LC3	LC2	LC1	LC0	Contrast
1	1	1	1	Dark
1	1	1	0	↑
1	1	0	1	
1	1	0	0	
1	0	1	1	
1	0	1	0	
1	0	0	1	
1	0	0	0	
0	1	1	1	
0	1	1	0	
0	1	0	1	
0	1	0	0	
0	0	1	1	
0	0	1	0	
0	0	0	1	↓
0	0	0	0	Light

The contrast can be adjusted in 16 stages as mentioned above. This adjustment changes the drive voltage on terminals V_{C1}–V_{C5}.
At initial reset, this register is set to "0".

LCCLK: 00FF10H•D4

Controls the CL signal output.

When "1" is written: CL signal output
When "0" is written: HIGH level (DC) output
Reading: Valid

LCCLK is the output control register for CL signal. When "1" is set, the CL signal is output from the output port terminal R25 and when "0" is set, HIGH (V_{DD}) level is output. At this time, "1" must always be set for the data register R25D.
At initial reset, LCCLK is set to "0" (HIGH level output).

LCFRM: 00FF10H•D3

Controls the FR signal output.

When "1" is written: FR signal output
When "0" is written: HIGH level (DC) output
Reading: Valid

LCFRM is the output control register for FR signal. When "1" is set, the FR signal is output from the output port terminal R26 and when "0" is set, HIGH (V_{DD}) level is output. At this time, "1" must always be set for the data register R26D.
At initial reset, LCFRM is set to "0" (HIGH level output).

5.12.10 Programming notes

(1) Since the CL and FR signals are generated asynchronously from the output control registers LCCLK and LCFRM, when the signals is turned ON or OFF by setting of the registers LCCLK and LCFRM, a hazard of a 1/2 cycle or less is generated.

(2) When the SLP instruction is executed, display control registers LCDC0 and LCDC1 are automatically reset to "0" by hardware. Furthermore, in the SLEEP status, HIGH (V_{DD}) level is output for the CL and FR signals. (When registers R25D and R26D are set to "1".)

5.13 Sound Generator

5.13.1 Configuration of sound generator

The S1C88349 has a built-in sound generator for generating BZ (buzzer) signal.
BZ signals generated from the sound generator can be output from the R50 output port terminal.
Aside permitting the respective setting of the buzzer signal frequency and sound level (duty adjustment) to 8 stages, it permits the adding of a digital envelope by means of duty ratio control. It also has a one-shot output function for outputting key operated sounds.
Figure 5.13.1.1 shows the configuration of the sound generator.

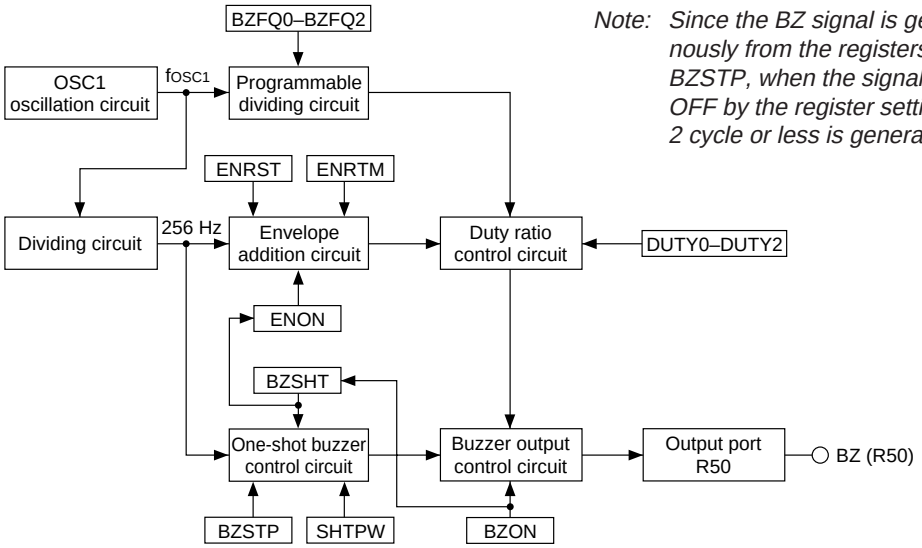


Fig. 5.13.1.1 Configuration of sound generator

5.13.2 Control of buzzer output

BZ signal can be output from the R50 output port terminal.
The configuration of the output port R50 is shown in Figure 5.13.2.1.

The output control for the BZ signal generated by the sound generator is done by the buzzer output control register BZON, one-shot buzzer trigger bit BZSHT and one-shot buzzer forced stop bit BZSTP. When "1" is set to BZON or BZSHT, the BZ signal is output from the R50 output port terminal and when "0" is set to BZON or "1" is set to BZSTP, the LOW (VSS) level is output. At this time, "0" must always be set for the output data register R50D.
Figure 5.13.2.2 shows the output waveform of the BZ signal.

Note: Since the BZ signal is generated asynchronously from the registers BZON, BZSHT and BZSTP, when the signal is turned ON or OFF by the register settings, a hazard of a 1/2 cycle or less is generated.

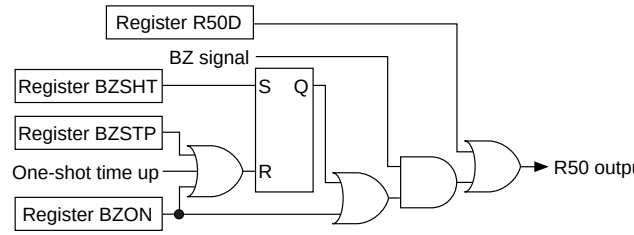


Fig. 5.13.2.1 Configuration of R50

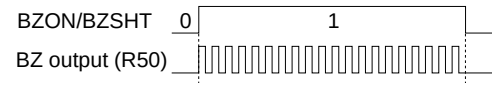


Fig. 5.13.2.2 Output waveform of BZ signal

5.13.3 Setting of buzzer frequency and sound level

The BZ signal is a divided signal using the OSC1 oscillation circuit (32.768 kHz) as the clock source and 8 frequencies can be selected. This selection is done by the buzzer frequency selection register BZFQ0–BZFQ2. The setting value and buzzer frequency correspondence is shown in Table 5.13.3.1. By selecting the duty ratio of the BZ signal from among 8 types, the buzzer sound level can be adjusted. This selection is made in the duty ratio selection register DUTY0–DUTY2. The setting value and duty ratio correspondence is shown in Table 5.13.3.2.

Table 5.13.3.1 Buzzer signal frequency settings

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

Table 5.13.3.2 Duty ratio settings

Level	DUTY2	DUTY1	DUTY0	Duty ratio by buzzer frequencies (Hz)			
				4096.0 2048.0	3276.8 1638.4	2730.7 1365.3	2340.6 1170.3
Level 1 (Max)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (Min)	1	1	1	1/16	1/20	5/24	5/28

Duty ratio refers to the ratio of pulse width to the pulse cycle; given that HIGH level output time is TH, and LOW level output time is TL the BZ signal becomes TH / (TH+TL).
When DUTY0–DUTY2 have all been set to "0", the duty ratio becomes maximum and the sound level also becomes maximum. Conversely, when DUTY0–DUTY2 have all been set to "1", the duty ratio becomes minimum and the sound level also becomes minimum.
Note that the duty ratio setting differ depending on frequency. See Table 5.13.3.2.

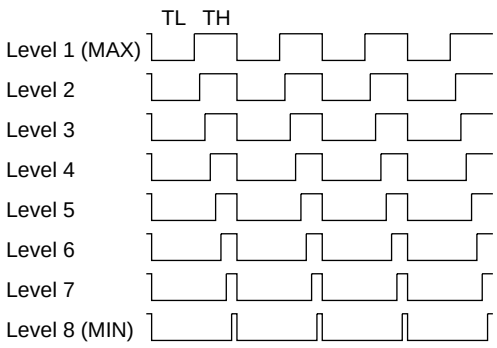


Fig. 5.13.3.1 Duty ratio of buzzer signal waveform

Note: When using the digital envelope, the DUTY0–DUTY2 setting becomes invalid.

5.13.4 Digital envelope

A digital envelope with duty control can be added to the BZ signal.
The envelope can be realized by staged changing of the same duty ratio as detailed in Table 5.13.3.2 in the preceding section from level 1 (maximum) to level 8 (minimum).
The addition of an envelope to the buzzer signal can be done by writing "1" to the envelope control register ENON. When "0" is written, the duty ratio is set at the level selected in DUTY0–DUTY2.
By writing "1" to ENON to turn the buzzer output ON (writing "1" to BZON), a BZ signal with a level 1 duty ratio is output, and then the duty ratio can be attenuated in stages to level 8. The attenuated envelope can be returned to level 1 by writing "1" to the envelope reset bit ENRST. When attenuated to level 8, the duty level remains at level 8 until the buzzer output is turned OFF (writing "0" to BZON) or writing "1" to ENRST.
The stage changing time for the envelope level can be selected either 125 msec or 62.5 msec by the envelope attenuation time selection register ENRTM. Figure 5.13.4.1 shows the timing chart of the digital envelope.

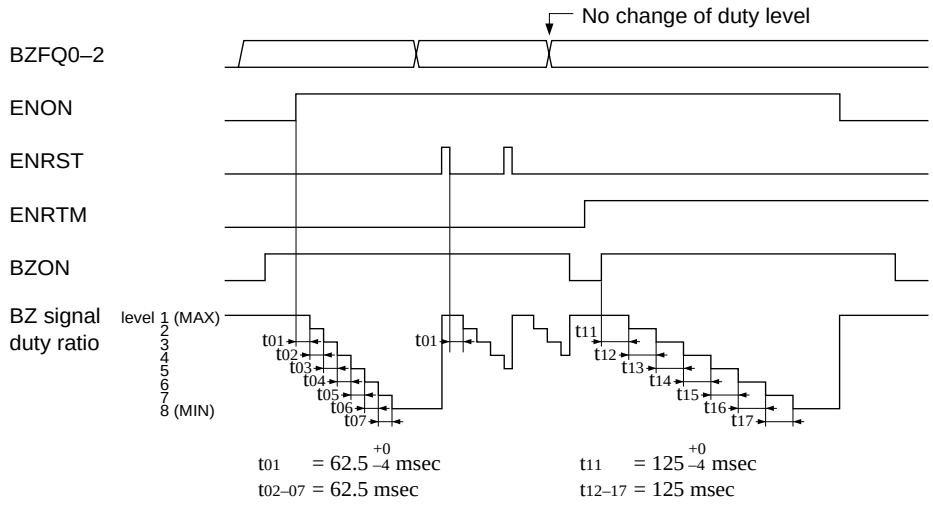


Fig. 5.13.4.1 Timing chart of digital envelope

5.13.5 One-shot output

The sound generator has a built-in one-shot output function for outputting a short duration buzzer signal for key operation sounds and similar effects. Either 125 msec or 31.25 msec can be selected by the one-shot buzzer duration selection register SHTPW for buzzer signal output time.

The output control of the one-shot buzzer is done by writing "1" to the one-shot buzzer trigger BZSHT, then the BZ signal is output in synchronization with the internal 256 Hz signal from the R50 output port terminal. Thereafter, when the set time has elapsed, the BZ signal in synchronization with the 256 Hz signal automatically goes OFF in the same manner.

The BZSHT can be read to determine status. When BZSHT is "1", it indicates a BUSY status (during one-shot output) and when BZSHT is "0", it indicates a READY status (during stop).

When you want to turn the BZ signal OFF prior to the elapse of the set time, the BZ signal can be immediately stopped (goes OFF in asynchonization with 256 Hz signal) by writing "1" to the one-shot forced stop bit BZSTP.

Since the one-shot output has a short duration, an envelope cannot be added. (When "1" is written to BZSHT, ENON is automatically reset to "0".) Consequently, only the frequency and sound level can be set for one-shot output.

The control for the one-shot output is invalid during normal buzzer output.

Figure 5.13.5.1 shows the timing chart of the one-shot output.

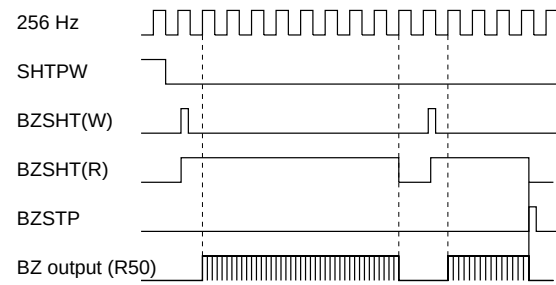


Fig. 5.13.5.1 Timing chart of one-shot output

5.13.6 Control of sound generator

Table 5.13.6.1 shows the sound generator control bits.

Table 5.13.6.1 Sound generator control bits

Address	Bit	Name	Function		1	0	SR	R/W	Comment
00FF44	D7	–	–		–	–	–		Constantry "0" when
	D6	BZSTP	One-shot buzzer forcibly stop		Forcibly stop	No operation	–	W	being read
	D5	BZSHT	One-shot buzzer trigger/status	R	Busy	Ready	0	R/W	
				W	Trigger	No operation			
	D4	SHTPW	One-shot buzzer duration width selection		125 msec	31.25 msec	0	R/W	
	D3	ENRTM	Envelope attenuation time		1 sec	0.5 sec	0	R/W	
	D2	ENRST	Envelope reset		Reset	No operation	–	W	"0" when being read
	D1	ENON	Envelope On/Off control		On	Off	0	R/W	*1
	D0	BZON	Buzzer output control		On	Off	0	R/W	
00FF45	D7	–	–		–	–	–		"0" when being read
	D6	DUTY2	Buzzer signal duty ratio selection				0	R/W	
	D5	DUTY1					0	R/W	
	D4	DUTY0					0	R/W	
	D3	–	–		–	–	–		"0" when being read
	D2	BZFQ2	Buzzer frequency selection				0	R/W	
	D1	BZFQ1					0	R/W	
	D0	BZFQ0					0	R/W	

Buzzer signal duty ratio selection

DUTY2–1			Buzzer frequency (Hz)			
2	1	0	4096.0 2048.0	3276.8 1638.4	2730.7 1365.3	2340.6 1170.3
0	0	0	8/16	8/20	12/24	12/28
0	0	1	7/16	7/20	11/24	11/28
0	1	0	6/16	6/20	10/24	10/28
0	1	1	5/16	5/20	9/24	9/28
1	0	0	4/16	4/20	8/24	8/28
1	0	1	3/16	3/20	7/24	7/28
1	1	0	2/16	2/20	6/24	6/28
1	1	1	1/16	1/20	5/24	5/28

Buzzer frequency selection

BZFQ2	BZFQ1	BZFQ0	Frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

*1 Reset to "0" during one-shot output.

BZON: 00FF44H•D0

Controls the BZ signal output.

When "1" is written: BZ signal output
When "0" is written: LOW level (DC) output
Reading: Valid

BZON is the output control register for BZ signal. When "1" is set, the BZ signal is output from the output port terminal R50 and when "0" is set, LOW (V_{SS}) level is output. At this time, "0" must always be set for the data register R50D.
At initial reset, BZON is set to "0" (LOW level output).

BZFQ0–BZFQ2: 00FF45H•D0–D2

Selects the BZ signal frequency.

Table 5.13.6.2 Buzzer frequency settings

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

The buzzer frequency can be selected from among the above 8 types that have divided the OSC1 clock. At initial reset, this register is set at "0" (4096.0 Hz).

DUTY0–DUTY2: 00FF45H•D4–D6

Selects the duty ratio of the BZ signal.

Table 5.13.6.3 Duty ratio settings

Level	DUTY2	DUTY1	DUTY0	Duty ratio by buzzer frequencies (Hz)			
				4096.0 2048.0	3276.8 1638.4	2730.7 1365.3	2340.6 1170.3
Level 1 (Max)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (Min)	1	1	1	1/16	1/20	5/24	5/28

The buzzer sound level can be adjusted by selecting the duty ratio from among the above 8 types. However, when the envelope has been set to ON (ENON = "1"), this setting becomes invalid.
At initial reset, this register is set to "0" (level 1).

ENRST: 00FF44H•D2

Resets the envelope.

When "1" is written: Reset
When "0" is written: No operation
Reading: Always "0"

The envelope is reset by writing "1" to ENRST and the duty ratio returns to level 1 (maximum). Writing "0" to ENRST and writing "1" when an envelope has not been added become invalid. Since ENRST is exclusively for writing, it always becomes "0" during reading.

ENON: 00FF44H•D1

Controls the addition of an envelope to the BZ signal.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

By writing "1" to ENON, an envelope can be added to BZ signal output. When "0" is written, an envelope is not added and the BZ signal is fixed at the duty ratio selected in DUTY0–DUTY2.
At initial reset and when "1" is written to BZSHT, ENON is set to "0" (OFF).

ENRTM: 00FF44H•D3

Selects the envelope attenuation time that is added to the BZ signal.

When "1" is written: 1.0 sec
(125 msec × 7 = 875 msec)
When "0" is written: 0.5 sec
(62.5 msec × 7 = 437.5 msec)
Reading: Valid

The attenuation time of the digital envelope is determined by the time for changing the duty ratio. The duty ratio is changed in 125 msec (8 Hz) units when "1" is written to ENRTM and in 62.5 msec (16 Hz) units, when "0" is written.
This setting becomes invalid when an envelope has been set to OFF (ENON = "0").
At initial reset, ENRTM is set to "0" (0.5 sec).

SHTPW: 00FF44H•D4

Selects the output duration width of the one-shot buzzer.

When "1" is written: 125 msec
When "0" is written: 31.25 msec
Reading: Valid

The one-shot buzzer output duration width is set to 125 msec when "1" is written to SHTPW and 31.25 msec, when "0" is written.
At initial reset, SHTPW is set to "0" (31.25 msec).

BZSHT: 00FF44H•D5

Controls the one-shot buzzer output.

When "1" is written: Trigger
When "0" is written: No operation

When "1" is read: Busy
When "0" is read: Ready

Writing "1" into BZSHT causes the one-shot output circuit to operate and the BZ signal to be output. The buzzer output is automatically turned OFF after the time set by SHTPW has elapsed. At this time, "0" must always be set for the data register R50D.
The one-shot output is only valid when the normal buzzer output is OFF (BZON = "0") status. The trigger is invalid during ON (BZON = "1") status. When a re-trigger is assigned during a one-shot output, the one-shot output time set with SHTPW is measured again from that point. (time extension)
The operation status of the one-shot output circuit can be confirmed by reading BZSHT, when the one-shot output is ON (busy), BZSHT reads "1" and when the output is OFF (ready), it reads "0".
At initial reset, BZSHT is set to "0" (ready).

BZSTP: 00FF44H•D6

Forcibly stops the one-shot buzzer output.

When "1" is written: Forcibly stop
When "0" is written: No operation
Reading: Constantly "0"

By writing "1" into BZSTP, the one-shot buzzer output can be stopped prior to the elapsing of the time set with SHTPW.
Writing "0" is invalid and writing "1" except during one-shot output is also invalid.
When "1" is written to BZSHT and BZSTP simultaneously, BZSTP takes precedence and one-shot output becomes stop status.
Since BZSTP is for writing only, during readout it is constantly set to "0".

5.13.7 Programming notes

(1) Since the BZ signal is generated asynchronously from the register BZON, when the signal is turned ON or OFF by the register setting, a hazard of a 1/2 cycle or less is generated.

(2) The SLP instruction has executed when the BZ signal is in the enable status (BZON = "1" or BZSHT = "1"), an unstable clock is output from the R50 output port terminal at the time of return from the SLEEP status. Consequently, when shifting to the SLEEP status, you should set the BZ signal to the disable status (BZON = BZSHT = "0") prior to executing the SLP instruction.

(3) The one-shot output is only valid when the normal buzzer output is OFF (BZON = "0") status. The trigger is invalid during ON (BZON = "1") status.

5.14 Analog Comparator

5.14.1 Configuration of analog comparator

The S1C88349 has an MOS input analog comparator built into two channels. The respective analog comparators have two differential input terminals (inverted input terminal CMPMx and non-inverted input terminal CMPPx) that are available for general purpose use.

Figure 5.14.1.1 shows the configuration of the analog comparator.

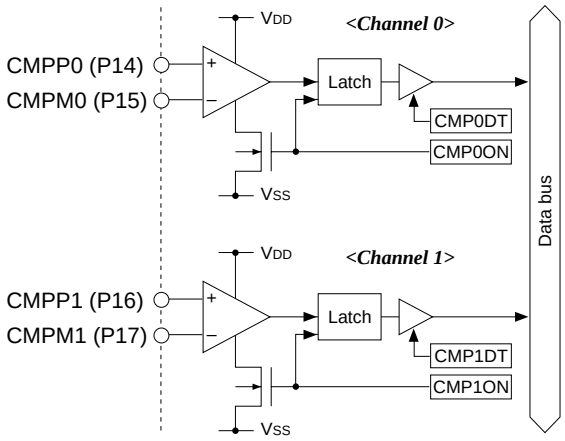


Fig. 5.14.1.1 Configuration of analog comparator

Since the input terminals of the analog comparator CMPP0, CMPM0, CMPP1 and CMPM1 are common to I/O ports P14–P17, when using as the input terminal for the analog comparator, "0" (input mode) must be written to I/O control registers IOC14–IOC17.

Table 5.14.1.1 Input terminal configuration

Terminal	When analog comparator is used
P14	CMPP0
P15	CMPM0
P16	CMPP1
P17	CMPM1

Note: The P14–P17 terminals are shared with the A/D converter input ports. Therefore, do not run the A/D converter when the analog comparator is used.

5.14.2 Mask option

Since the input terminals of the analog comparator are common to the I/O ports, the mask option for the I/O port corresponding to the channel to be used must be set to "Gate direct".

I/O ports pull-up resistor
P14 (CMPP0) ... ☐ With resistor ☑ Gate direct
P15 (CMPM0) .. ☐ With resistor ☑ Gate direct
P16 (CMPP1) ... ☐ With resistor ☑ Gate direct
P17 (CMPM1) .. ☐ With resistor ☑ Gate direct

* "✓" above shows an example of both channels being used.

5.14.3 Analog comparator operation

By writing "1" to the analog comparator control register CMPxON, the analog comparator goes ON, and the analog comparator starts comparing the external voltages that have been input to the two differential input terminals CMPPx and CMPMx. The result can be read from the comparator comparison result detection bit CMPxDT through the latch and when CMPPx (+) > CMPMx (-), it is "1" and when CMPPx (+) < CMPMx (-), it is "0". After the analog comparator has been turned ON, a maximum time of 3 msec is necessary until output stabilizes. Consequently, you should allow an adequate waiting time after turning the analog comparator ON, before reading the comparison result.
When the analog comparator is turned OFF, the comparison result at that point will be latched and the concerned data can be read thereafter, until the analog comparator is turned ON.
You should turn the analog comparator OFF, when it is not necessary, so as to reduce current consumption.
See Chapter 8, "ELECTRICAL CHARACTERISTICS" for the input voltage range.

Note: Since the input terminals of the analog comparator are shared with the I/O ports, the I/O control registers (IOC14–IOC17) corresponding to the channel to be used must be set to the input mode.

5.14.4 Control of analog comparator

Table 5.14.4.1 shows the analog comparator control bits.

Table 5.14.4.1 Analog comparator control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF13	D7	–	–	–	–	–		
	D6	–	–	–	–	–		Constantly "0" when being read
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	CMP1ON	Comparator 1 On/Off control	On	Off	0	R/W	
	D2	CMP0ON	Comparator 0 On/Off control	On	Off	0	R/W	
	D1	CMP1DT	Comparator 1 data	+ > -	+ < -	0	R	
	D0	CMP0DT	Comparator 0 data	+ > -	+ < -	0	R	

CMP0ON, CMP1ON: 00FF13H•D2, D3

Controls the analog comparator ON / OFF.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

The analog comparator 0 goes ON by writing "1" to CMP0ON and goes OFF, when "0" is written. The analog comparator 1 can be controlled with CMP1ON in the same way.
At initial reset, this register is set "0" (OFF).

CMP0DT, CMP1DT: 00FF13H•D0, D1

The comparison result of the analog comparator can be read out.

When "1" is read: CMPPx (+) > CMPMx (-)
When "0" is read: CMPPx (+) < CMPMx (-)
Writing: Invalid

The result of analog comparator 0 can be read from CMP0DT. When the status of external voltage input to differential input terminals CMPP0 and CMPM0 is CMPP0 (+) > CMPM0 (-), CMP0DT becomes "1" and when it is CMPP0 (+) < CMPM0 (-), CMP0DT becomes "0".
As the same way, the comparison result between CMPP1 and CMPM1 can be read from CMP1DT. When the analog comparator is turned OFF, the latched result immediately prior to going OFF is read out.
At initial reset, this bit is set to "1".

5.14.5 Programming notes

(1) To reduce current consumption, turn the analog comparator OFF (CMP0ON = CMP1ON = "0") when it is not necessary.

(2) After the analog comparator has been turned ON, a maximum time of 3 msec is necessary until output stabilizes. Consequently, you should allow an adequate waiting time after turning the analog comparator ON, before reading the comparison result.

(3) Since the input terminals of the analog comparator are common to the I / O ports, the I / O control registers (IOC14–IOC17) corresponding to the channel to be used must be set to the input mode.

(4) The P14–P17 terminals are shared with the A / D converter input ports. Therefore, do not run the A / D converter when the analog comparator is used.

5.15 A/D Converter

5.15.1 Characteristics and configuration of A/D converter

The S1C88349 has a built-in A / D converter with the following characteristics.

- Conversion formula: Successive-approximation type
- Resolution: 10 bits
- Input channel: Maximum 4 channels
- Conversion time: Minimum 11 µsec (in 2 MHz operation)
- Setting of analog conversion voltage range is possible with reference voltage terminal (AVREF)
- A / D conversion result is possible to read from 10-bit data register
- Sample & hold circuit built-in
- A / D conversion completion generates an interrupt

Figure 5.15.1.1 shows the configuration of the A / D converter.

5.15.2 Terminal configuration of A/D converter

The terminals used with the A / D converter are as follows:

■ AVDD, AVSS (power supply input terminal)
The AVDD and AVSS terminals are power supply terminals for the A / D converter. The voltage should be input as AVDD ≤ VDD and AVSS = VSS.

■ AVREF (reference voltage input terminal)
The AVREF terminal is the reference voltage terminal of the analog block. Input voltage range of the A / D conversion is decided by this input. The voltage should be input as AVREF ≤ AVDD.

■ AD4–AD7 (analog input terminal)
The analog input terminals AD4–AD7 are shared with the I / O port terminals P14–P17. Therefore, it is necessary to set them for the A / D converter by software when using them as analog input terminals. This setting can be done for each terminal. (Refer to Section 5.15.4 for setting.)
At initial reset, all the terminals are set in the I / O port terminal.
Analog voltage value AVIN that can be input is in the range of AVSS ≤ AVIN ≤ AVREF.

Note: Since the P14–P17 terminals are shared with the analog comparator, the A/D converter and the analog comparator cannot be used simultaneously. When using the A/D converter, do not run the analog comparator.

5.15.3 Mask option

I/O ports pull-up resistors		
P14 (AD4)	☐ With resistor	☑ Gate direct
P15 (AD5)	☐ With resistor	☑ Gate direct
P16 (AD6)	☐ With resistor	☑ Gate direct
P17 (AD7)	☐ With resistor	☑ Gate direct

* "✓" above shows an example of both channels being used.

The input terminals of the A / D converter are shared with the I / O port terminals P14–P17. Therefore, the terminal specification of the A / D converter is decided by setting the I / O port mask option. Select "Gate direct" for the port corresponding to the channel to be used to obtain the conversion precision.

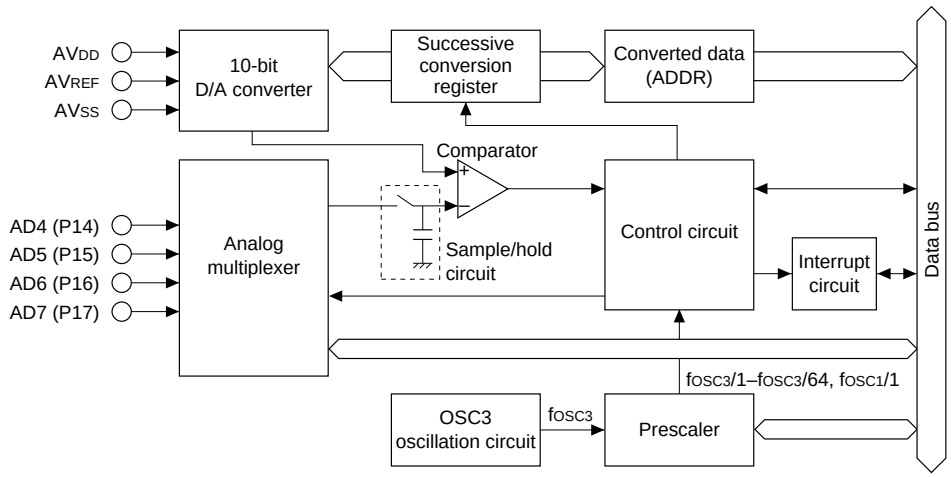


Fig. 5.15.1.1 Configuration of A/D converter

5.15.4 A/D conversion

■ Setting the A/D input terminal

When using the A / D converter, it is necessary to set up the terminals used for analog input from the P14–P17 initialized as the I / O port terminals. Four terminals can all be used as analog input terminals.

The PAD (PAD4–PAD7) register is used to set analog input terminals. When the PAD register bits are set to "1", the corresponding terminals function as the analog input terminals.

Table 5.15.4.1 Correspondence between A/D input terminal and PAD register

Terminal	A/D input control register
P14 (AD4)	PAD4
P15 (AD5)	PAD5
P16 (AD6)	PAD6
P17 (AD7)	PAD7

■ Setting the input clock

The A / D conversion clock can be selected from eight types shown in Table 5.15.4.2. The selection is done using the PSAD register.

Table 5.15.4.2 Input clock selection

Selection register			Division ratio	Output control
PSAD2	PSAD1	PSAD0		
1	1	1	fOSC1/1	PRAD register "1": ON "0": OFF
1	1	0	fOSC3/64	
1	0	1	fOSC3/32	
1	0	0	fOSC3/16	
0	1	1	fOSC3/8	
0	1	0	fOSC3/4	
0	0	1	fOSC3/2	
0	0	0	fOSC3/1	

The selected clock is input to the A / D converter by writing "1" to the PRAD register.

Note:
- *When the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the A/D converter.*
  From the time the OSC3 oscillation circuit is turning ON until oscillation stabilizes, an interval of several msec to several 10 msec is necessary. Consequently, you should allow an adequate waiting time after turning the OSC3 oscillation circuit ON before starting the count of the programmable timer. (The oscillation start time will vary somewhat depending on the oscillator and on external parts. Refer to the oscillation start time example indicated in Chapter 8, "ELECTRICAL CHARACTERISTICS".)
  At initial reset, OSC3 oscillation circuit is set to OFF status.
- *The clock division ratio (see Table 5.15.4.2) must be set so that the A/D conversion clock frequency is 1 MHz or less. Furthermore, the A/D conversion clock frequency should be changed according to the voltage to be used. Refer to Chapter 8, "ELECTRICAL CHARACTERISTICS".*
- *The input clock should be set when the A/D converter stops. Changing in the A/D converter operation may cause a malfunction.*
- *To prevent malfunction, do not start A/D conversion (writing to the CHS register) when the A/D conversion clock is not being output from the prescaler, and do not turn the prescaler output clock off during A/D conversion.*

■ Selecting the input signal

The analog signals from the AD4 (P14)–AD7 (P17) terminals are input to the multiplexer, and the analog input channel for A / D conversion is selected by software. This selection can be done using the CHS register as shown in Table 5.15.4.3.

Table 5.15.4.3 Selection of analog input channel

CHS1	CHS0	Input channel
1	1	AD7
1	0	AD6
0	1	AD5
0	0	AD4

■ A/D conversion operation

An A / D conversion starts by writing data to the ADRUN register. For example, when performing A / D conversion using AD7 as the analog input, write "1" (1, 1) to the CHS register (CHS1, CHS0) and then write "1" to the ADRUN register. The A / D input channel is selected and the A / D conversion starts. However, it is necessary that the P17 terminal has been set as an analog input terminal.
The built-in sample & hold circuit starts sampling of the analog input specified from tAD after writing. When the sampling is completed, the held analog input voltage is converted into a 10-bit digital value in successive-approximation architecture.
The conversion result is loaded into the ADDR (ADDR0–ADDR9) register. ADDR0 is the LSB and ADDR9 is the MSB.

Note: If the CHS register selects an input channel which is not included in the analog input terminals set by the PAD register (the PAD register can select several terminals simultaneously), the A/D conversion does not result in a correct converted value.

Example)
Terminal setting:
PAD5 = 1, PAD7 = PAD6 = PAD4 = 0
(AD5 terminal is used)
Selection of input channel:
CHS1 = 0, CHS0 = 0
(AD4 is selected)

In a setting like this, the A/D conversion result will be invalid because the contents of the settings are not matched.

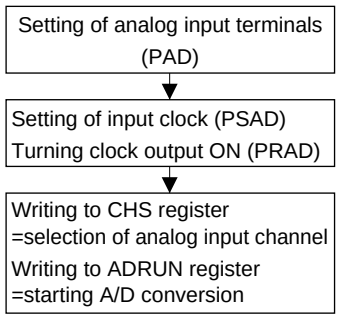


Fig. 5.15.4.1 Flowchart for starting A/D conversion

An A / D conversion is completed when the conversion result is loaded into the ADDR register. At that point, the A / D converter generates an interrupt (explained in the next section).

Figure 5.15.4.2 shows the timing chart of A / D conversion.

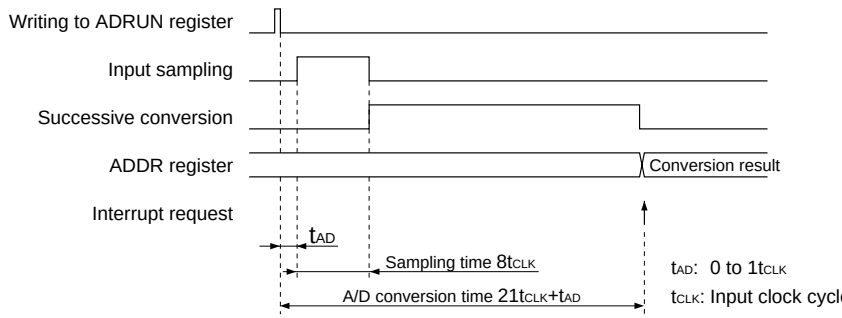


Fig. 5.15.4.2 Timing chart of A/D conversion

5.15.5 Interrupt function

The A / D converter can generate an interrupt when an A / D conversion has completed.
Figure 5.15.5.1 shows the configuration of the A / D converter interrupt circuit.

The A / D converter sets the interrupt factor flag FAD to "1" when it stores the conversion.
At this time, if the interrupt enable register EAD is "1" and the interrupt priority register PADC (2 bits) is set to a higher level than the setting of the interrupt flags (I0 and I1), an interrupt is generated to the CPU.
By setting the EAD register to "0", the interrupt to the CPU can also be disabled. However, the interrupt factor flag is set to "1" when an A / D conversion has completed regardless of the interrupt enable register and interrupt priority register settings.
The interrupt factor flag set in "1" is reset to "0" by writing "1".
Refer to Section 5.17, "Interrupt and Standby Status", for details of the interrupt control registers and operations subsequent to interrupt generation.
The exception processing vector address for the A / D conversion completion interrupt has been set in 000024H.

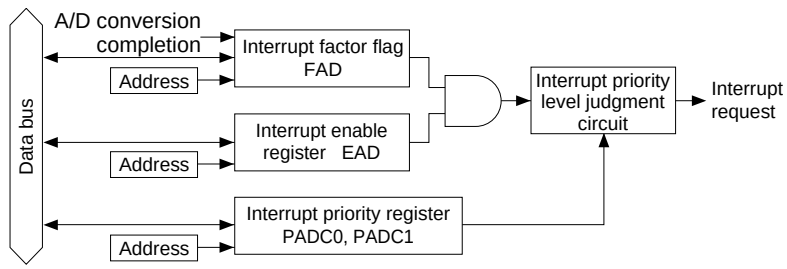


Fig. 5.15.5.1 Configuration of A/D converter interrupt circuit

5.15.6 Control of A/D converter

Table 5.15.6.1 shows the A / D converter control bits.

Table 5.15.6.1(a) A/D converter control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF80	D7	–	–	–	–	–		
	D6	–	–	–	–	–		Constantly "0" when being read
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	PRAD	A/D converter clock control	On	Off	0	R/W	
	D2	PSAD2	A/D converter division ratio PSAD2 PSAD1 PSAD0 Division ratio 1 1 1 fOSC1 / 1 1 1 0 fOSC3 / 64 1 0 1 fOSC3 / 32 1 0 0 fOSC3 / 16 0 1 1 fOSC3 / 8 0 1 0 fOSC3 / 4 0 0 1 fOSC3 / 2 0 0 0 fOSC3 / 1			0	R/W	
	D1	PSAD1				0	R/W	
	D0	PSAD0				0	R/W	
00FF81	D7	PAD7	P17 A/D converter input control	A/D converter input	I/O port	0	R/W	
	D6	PAD6	P16 A/D converter input control			0	R/W	
	D5	PAD5	P15 A/D converter input control			0	R/W	
	D4	PAD4	P14 A/D converter input control			0	R/W	
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		Constantly "0" when being read
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		
00FF82	D7	ADRUN	A/D conversion start control register	Start	Invalid	0	W	
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		Constantry "0" when being read
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	CHS1	Analog input channel selection CHS1 CHS0 Input channel 1 1 AD7 1 0 AD6 0 1 AD5 0 0 AD4			0	R/W	
	D0	CHS0				0	R/W	
00FF83	D7	ADDR9	A/D conversion result D9 (MSB)			–	R	
	D6	ADDR8	A/D conversion result D8					
	D5	ADDR7	A/D conversion result D7					
	D4	ADDR6	A/D conversion result D6					
	D3	ADDR5	A/D conversion result D5					
	D2	ADDR4	A/D conversion result D4					
	D1	ADDR3	A/D conversion result D3					
	D0	ADDR2	A/D conversion result D2					
00FF84	D7	–	–	–	–	–		
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		Constantly "0" when being read
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	ADDR1	A/D conversion result D1			–	R	
	D0	ADDR0	A/D conversion result D0 (LSB)					

Table 5.15.6.1(b) A/D converter control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF28	D7	PADC1	A/D converter interrupt priority register	PADC1 PADC0 Priority 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PADC0				0	R/W	
	D5	–	Reserved	Prohibited	–	0		Do not write "1".
	D4	–	Reserved	Prohibited	–	0		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		Constantly "0" when
	D1	–	–	–	–	–		being read
	D0	–	–	–	–	–		
00FF2A	D7	EAD	A/D converter interrupt enable register	Enable	Disable	0	R/W	
	D6	–	Reserved	–	–	0	R/W	
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		Constantly "0" when
	D2	–	–	–	–	–		being read
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		
00FF2C	D7	FAD	A/D converter interrupt factor flag R)	Generated	Not generated	0	R/W	
			W)	Reset	No operation			
	D6	–	Reserved	–	–	0	R/W	
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		Constantly "0" when
	D2	–	–	–	–	–		being read
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		

PAD4–PAD7: 00FF81H•D4–D7

Sets the P14–P17 terminals as the analog input terminals for the A/D converter.

When "1" is written: A/D converter input
When "0" is written: I/O port
Reading: Valid

When "1" is written to PADn, the P1n terminal is set to the analog input terminal ADn. (n=4–7)
When "0" is written, the terminal is used with the I/O port.
At initial reset, this register is set to "0" (I/O port).

PSAD0–PSAD2: 00FF80H•D0–D2

Selects the clock for the A/D converter.

Table 5.15.6.2 Input clock selection

Selection register			Division ratio	Output control
PSAD2	PSAD1	PSAD0		
1	1	1	f_{OSC1}/1	PRAD
1	1	0	f_{OSC3}/64	register
1	0	1	f_{OSC3}/32	
1	0	0	f_{OSC3}/16	"1": ON
0	1	1	f_{OSC3}/8	"0": OFF
0	1	0	f_{OSC3}/4	
0	0	1	f_{OSC3}/2	
0	0	0	f_{OSC3}/1	

This setting controls the division ratio of the prescaler.
At initial reset, this register is set to "0" (f_{OSC3}/1).

PRAD: 00FF80H•D3

Controls the clock supply to the A / D converter.

When "1" is written: ON
When "0" is written: OFF
Reading: Invalid

By writing "1" to the PRAD register, the clock selected with the PSAD register is input to the A / D converter.
When "0" is written, the clock is not input to the A / D converter.
At initial reset, this register is set to "0" (OFF).

ADRUN: 00FF82H•D7

Starts A / D conversion.

When "1" is written: Start A / D conversion
When "0" is written: Invalid
Reading: Always "0"

By writing "1" to this register, the A / D converter starts A / D conversion of the channel selected by the CHS register, and stores the conversion result to the ADDR register.

CHS0, CHS1: 00FF82H•D0, D1

Selects an analog input channel.

Table 5.15.6.3 Selection of analog input channel

CHS1	CHS0	Input channel
1	1	AD7
1	0	AD6
0	1	AD5
0	0	AD4

At initial reset, this register is set to "0" (AD4).

ADDR0–ADDR9: 00FF84H•D0, D1, 00FF83H

A / D conversion result is stored.
ADDR0 is the LSB and ADDR9 is the MSB.
ADDR0 and ADDR1 are assigned in D0 bit and D1 bit of the address 00FF84H. D2–D7 bits in this address are always "0" when being read.
At initial reset, data is undefined.

PADC0, PADC1: 00FF28H•D6, D7

Sets the priority level of the A / D conversion completion interrupt.
Table 5.15.6.4 shows the interrupt priority level which can be set by the PADC register.

Table 5.15.6.4 Interrupt priority level settings

PADC1	PADC0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

EAD: 00FF2AH•D7

Enables or disables the A / D conversion completion interrupt generation to the CPU.

When "1" is written: Interrupt is enabled
When "0" is written: Interrupt is disabled
Reading: Valid

The EAD register is the interrupt enable register corresponding to the A / D conversion completion interrupt factor. When this register is set to "1", the interrupt is enabled, and when it is set to "0", the interrupt is disabled.
At initial reset, this register is set to "0" (interrupt is disabled).

FAD: 00FF2CH•D7

Indicates the generation of A / D conversion completion interrupt factor.

When "1" is read: Int. factor has generated
When "0" is read: Int. factor has not generated

When "1" is written: Factor flag is reset
When "0" is written: Invalid

FAD is the interrupt factor flag corresponding to the A / D conversion completion interrupt. It is set to "1" when an A / D conversion is completed.
At this point, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of the interrupt flags (I0 and I1), an interrupt is generated to the CPU.
Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag is set to "1" when the interrupt generation condition is met.
To accept the subsequent interrupt after an interrupt generation, it is necessary to re-set the interrupt flags (set the interrupt flag to a lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and to reset the interrupt factor flag. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, the FAD flag is reset to "0".

5.15.7 Programming notes

(1) When the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the A / D converter.
From the time the OSC3 oscillation circuit is turning ON until oscillation stabilizes, an interval of several msec to several 10 msec is necessary. Consequently, you should allow an adequate waiting time after turning the OSC3 oscillation circuit ON before starting the count of the programmable timer. (The oscillation start time will vary somewhat depending on the oscillator and on external parts. Refer to the oscillation start time example indicated in Chapter 8, "ELECTRICAL CHARACTERISTICS".)
At initial reset, OSC3 oscillation circuit is set to OFF status.

(2) When SLEEP mode is set during A / D conversion, correct A / D conversion result cannot be obtained because the OSC3 oscillation circuit stops. Do not set in SLEEP mode during A / D conversion.

(3) The input clock and analog input terminals should be set when the A / D converter stops. Changing in the A / D converter operation may cause a malfunction.

(4) The clock division ratio (see Table 5.15.4.2) must be set so that the A / D conversion clock frequency is 1 MHz or less. Furthermore, the A / D conversion clock frequency should be changed according to the voltage to be used. Refer to Chapter 8, "ELECTRICAL CHARACTERISTICS".

(5) To prevent malfunction, do not start A / D conversion (writing to the CHS register) when the A / D conversion clock is not being output from the prescaler, and do not turn the prescaler output clock off during A / D conversion.

(6) If the CHS register selects an input channel which is not included in the analog input terminals set by the PAD register (the PAD register can select several terminals simultaneously), the A / D conversion does not result in a correct converted value.

(7) During A / D conversion, do not operate the P1n terminals which are not used for analog inputs of the A / D converter (for input / output of digital signal). It affects the A / D conversion precision.

(8) Since the P14–P17 terminals are shared with the analog comparator, the A / D converter and the analog comparator cannot be used simultaneously. When using the A / D converter, do not run the analog comparator.

(9) Note that writing "1" to the A / D converter control bits (FF28H • D5, D4) may cause a malfunction.

5.16 Supply Voltage Detection (SVD) Circuit

5.16.1 Configuration of SVD circuit

The S1C88349 has a built-in supply voltage detection (SVD) circuit configured with a 4-bit successive approximation A / D converter.
The SVD circuit has 16 sampling levels (level 0–level 15) for supply voltage, and this can be controlled by software.
In addition, an initial reset signal can be generated when the supply voltage drops to level 0 or less. This is selected by the mask option.
Figure 5.16.1.1 shows the configuration of the SVD circuit.

5.16.2 Mask option

Initial reset by SVD circuit
☐ Not Use
☐ Use

When the SVD circuit detects that supply voltage has dropped below level 0 four successive times (see Chapter 8, "ELECTRICAL CHARACTERISTICS"), it outputs an initial reset signal until the supply voltage has been restored to level 2.
You can select whether this function is used or not by mask option.

5.16.3 Operation of SVD circuit

■ Sampling control of the SVD circuit

The SVD circuit has two operation modes: continuous sampling and 1 / 4 Hz auto-sampling mode. Operation mode selection is done by the SVD control registers SVDON and SVDSP as shown in Table 5.16.3.1. When both bits of SVDON and SVDSP are set to "1", continuous sampling is selected.

Table 5.16.3.1 Correspondence between control register and operation mode

SVDON	SVDSP	Operating mode
0	0	SVD circuit OFF
0	1	1/4 Hz auto-sampling ON
1	×	Continuous sampling ON

In both operation modes, reading SVDON can confirm whether the SVD circuit is operating (BUSY) or on standby (READY); "1" indicates BUSY and "0" indicates READY.
When executing an SLP instruction while the SVD circuit is operating, the stop operation of the OSC1 oscillation circuit is kept waiting until the sampling is completed. The two bits of SVDON and SVDSP are automatically reset to "0" by hardware while waiting for completion of sampling.
To reduce current consumption, turn the SVD circuit OFF when it is not necessary.

■ Detection result

The SVD circuit A / D converts the supply voltage (V_{DD}–V_{SS}) by 4-bit resolution and sets the result thereof into the SVD0–SVD3 register.
The data in SVD0–SVD3 correspond to the detection levels as shown in Table 5.16.3.2 and the detection data is maintained until the next sampling.

For the correspondence between the detection level and the supply voltage, see Chapter 8, "ELECTRICAL CHARACTERISTICS".
An interval of 7.8 msec (f_{OSC1} = 32.768 kHz) is required from the start of supply voltage sampling by the SVD circuit to completion by writing the result into SVD0–SVD3. Therefore, when reading SVD0–SVD3 before sampling is finished, the previous result will be read.

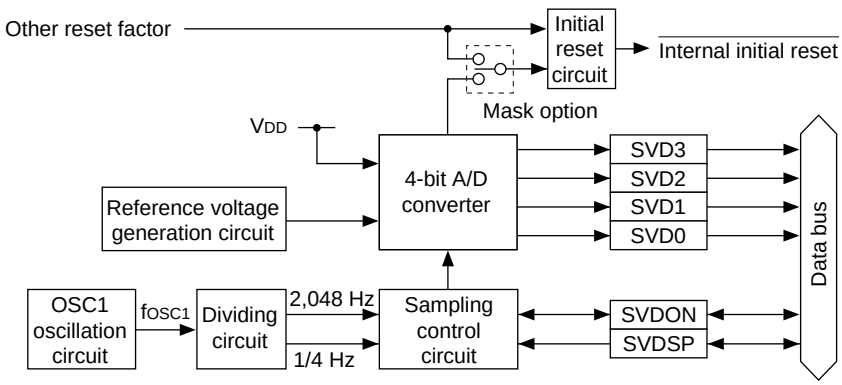


Fig. 5.16.1.1 Configuration of SVD circuit

Table 5.16.3.2 Supply voltage detection results

SVD3	SVD2	SVD1	SVD0	Detection level
1	1	1	1	Level 15
1	1	1	0	Level 14
1	1	0	1	Level 13
1	1	0	0	Level 12
1	0	1	1	Level 11
1	0	1	0	Level 10
1	0	0	1	Level 9
1	0	0	0	Level 8
0	1	1	1	Level 7
0	1	1	0	Level 6
0	1	0	1	Level 5
0	1	0	0	Level 4
0	0	1	1	Level 3
0	0	1	0	Level 2
0	0	0	1	Level 1
0	0	0	0	Level 0

■ Timing of sampling

Next, we will explain the timing for two operation modes.

(1) Continuous sampling mode

This mode is selected when "1" is written to SVDON and sampling of the supply voltage is done continuously in 7.8 msec cycles.
The SVD circuit starts operation in synchronization with the internal 2,048 Hz signal and performs one sampling in 16 clock cycles.
The sampling is done continuously without setting the standby time and the result is latched to SVD0–SVD3 in every 16 clock cycles.
Cancellation of continuous sampling is done by writing "0" to SVDON. The SVD circuit maintains ON status until completion of sampling and then goes OFF.
After writing "0" to SVDON, SVDON reads "1" until the SVD circuit actually goes OFF.
Figure 5.16.3.1 shows the timing chart of the continuous sampling.

(2) 1/4 Hz auto-sampling mode

This mode is selected when "0" is written to SVDON and "1" is written to SVDSP. In this case, supply voltage sampling is done in every 4 seconds.
The sampling time is 7.8 msec as in continuous sampling, and the result in SVD0–SVD3 is updated every 4 seconds.
Cancellation of 1/4 Hz auto-sampling is done by writing "0" to SVDSP. If the SVD circuit is sampling, SVD circuit waits until completion and then turns OFF. In addition, "1" is read from SVDON while the SVD circuit is sampling.
Figure 5.16.3.2 shows the timing chart of the 1/4 Hz auto-sampling.

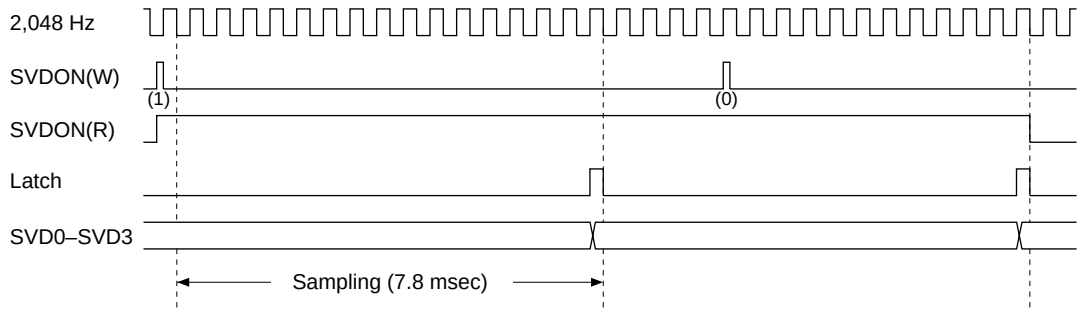


Fig. 5.16.3.1 Timing chart of continuous sampling

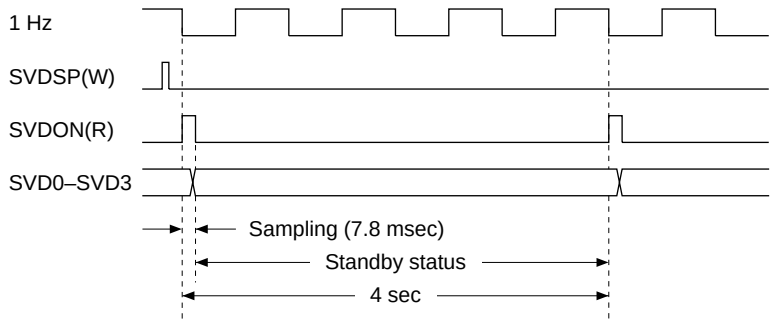


Fig. 5.16.3.2 Timing chart of 1/4 Hz auto-sampling

■ Reset function at low voltage detection

To avoid CPU runaway due to a supply voltage drop, an initial reset function when the supply voltage drops to level 0 or less can be selected by the mask option.
The SVD circuit shifts to continuous sampling status when it detects level 0 (SVD3–SVD0 = 0000B) four successive times. At this time, the internal initial reset signal is generated. The reset status continues until the supply voltage returns to level 2 (SVD3–SVD0 = 0010B) or higher.
When the reset status is canceled by the restoration of the supply voltage, the SVD circuit returns to its previous status. Continuous sampling status continues in case of the previous status was continuous sampling. Then CPU starts the reset exception processing.
Figure 5.16.3.3 shows the timing chart of the initial reset signal generation. (Example when using 1/4 Hz auto-sampling.)

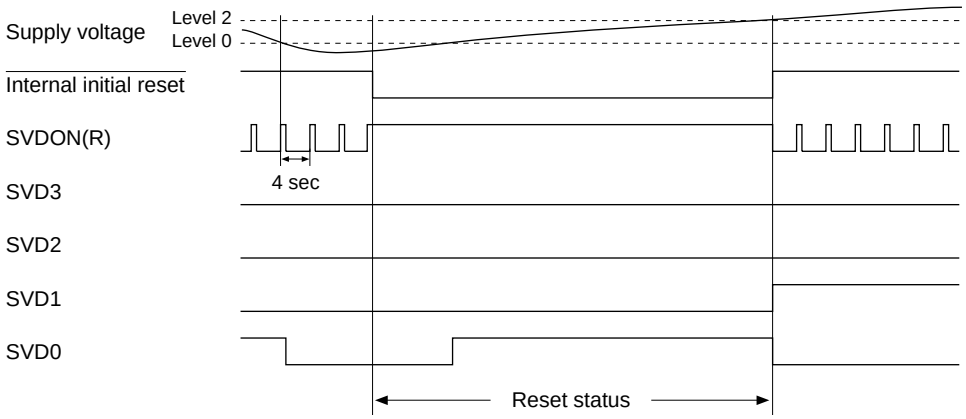


Fig. 5.16.3.3 Timing chart of the initial reset signal generation

5.16.4 Control of SVD circuit

Table 5.16.4.1 shows the SVD circuit control bits.

Table 5.16.4.1 SVD circuit control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF12	D7	–	–	–	–	–		Constantry "0" when
	D6	–	–	–	–	–		being read
	D5	SVDSP	SVD auto-sampling control	On	Off	0	R/W	These registers are reset to "0" when SLP instruction is executed.
	D4	SVDON	SVD continuous sampling control/status R	Busy	Ready	1→0*1	R/W	
			W	On	Off	0		
	D3	SVD3	SVD detection level			X	R	*2
	D2	SVD2				X	R	
	D1	SVD1				X	R	
	D0	SVD0				X	R	

SVD3	SVD2	SVD1	SVD0	Detection level
1	1	1	1	Level 15
1	1	1	0	Level 14
:	:	:	:	:
0	0	0	0	Level 0

*1 After initial reset, this status is set "1" until conclusion of hardware first sampling.
*2 Initial value is set according to the supply voltage detected at first hardware sampling after an initial reset.
Until conclusion of first sampling, SVD0–SVD3 data are undefined.

SVDON: 00FF12H•D4

Controls the turning ON / OFF of the continuous sampling mode.

When "1" is written: Continuous sampling ON
When "0" is written: Continuous sampling OFF

When "1" is read: BUSY
When "0" is read: READY

The continuous sampling mode goes ON when "1" is written to SVDON and goes OFF, when "0" is written.
In the ON status, sampling of the supply voltage is done continuously in 7.8 msec cycles and the detection result is latched to SVD0–SVD3.
SVDON can be read, and "1" indicates SVD circuit operation (BUSY) and "0" indicates standby (READY).
At initial reset and in the SLEEP status, SVDON is set to "0" (continuous sampling OFF / READY).

SVDSP: 00FF12H•D5

Controls the turning ON / OFF of the 1 / 4 Hz auto-sampling mode.

When "1" is written: Auto-sampling ON
When "0" is written: Auto-sampling OFF
Reading: Valid

The 1 / 4 Hz auto-sampling mode goes ON when "1" is written to SVDSP and goes OFF, when "0" is written.
In the ON status, sampling is done in every 4 seconds and "1" is read from SVDON during the actual sampling period (7.8 msec).
At initial reset and in the SLEEP status, SVDSP is set to "0" (auto-sampling OFF).

SVD0–SVD3: 00FF12H•D0–D3

The detection result of the SVD is set.
The reading data correspond to the detection levels as shown in Table 5.16.4.2 and the data is maintained until the next sampling.

Table 5.16.4.2 Supply voltage detection results

SVD3	SVD2	SVD1	SVD0	Detection level
1	1	1	1	Level 15
1	1	1	0	Level 14
1	1	0	1	Level 13
1	1	0	0	Level 12
1	0	1	1	Level 11
1	0	1	0	Level 10
1	0	0	1	Level 9
1	0	0	0	Level 8
0	1	1	1	Level 7
0	1	1	0	Level 6
0	1	0	1	Level 5
0	1	0	0	Level 4
0	0	1	1	Level 3
0	0	1	0	Level 2
0	0	0	1	Level 1
0	0	0	0	Level 0

For the correspondence between the detection level and the supply voltage, see Chapter 8, "ELECTRICAL CHARACTERISTICS".
The initial value at initial reset is set according to the supply voltage detected at first sampling by hardware. Data of this bit is undefined until this sampling is completed.

5.16.5 Programming notes

(1) To reduce current consumption, turn the SVD circuit OFF (SVDON = SVDSP = "0") when it is not necessary.

(2) When executing an SLP instruction while the SVD circuit is operating, the stop operation of the OSC1 oscillation circuit is kept waiting until the sampling is completed. The two bits of SVDON and SVDSP are automatically reset to "0" by hardware while waiting for completion of sampling.

5.17 Interrupt and Standby Status

■ Types of interrupts

7 systems and 16 types of interrupts have been provided for the S1C88349.

External interrupt
- K00–K07 input interrupt (2 types)
- K10 and K11 input interrupt (1 type)

Internal interrupt
- Clock timer interrupt (4 types)
- Stopwatch interrupt (3 types)
- Programmable timer interrupt (2 types)
- Serial interface interrupt (3 types)
- A / D converter interrupt (1 type)

An interrupt factor flag that indicates the generation of an interrupt factor and an interrupt enable register that sets enable / disable for interrupt requests have been provided for each interrupt and interrupt generation can be optionally set for each factor.
In addition, an interrupt priority register has been provided for each system of interrupts and the priority of interrupt processing can be set to 3 levels in each system.
Figure 5.17.1 shows the configuration of the interrupt circuit.

Refer to the explanations of the respective peripheral circuits for details on each interrupt.

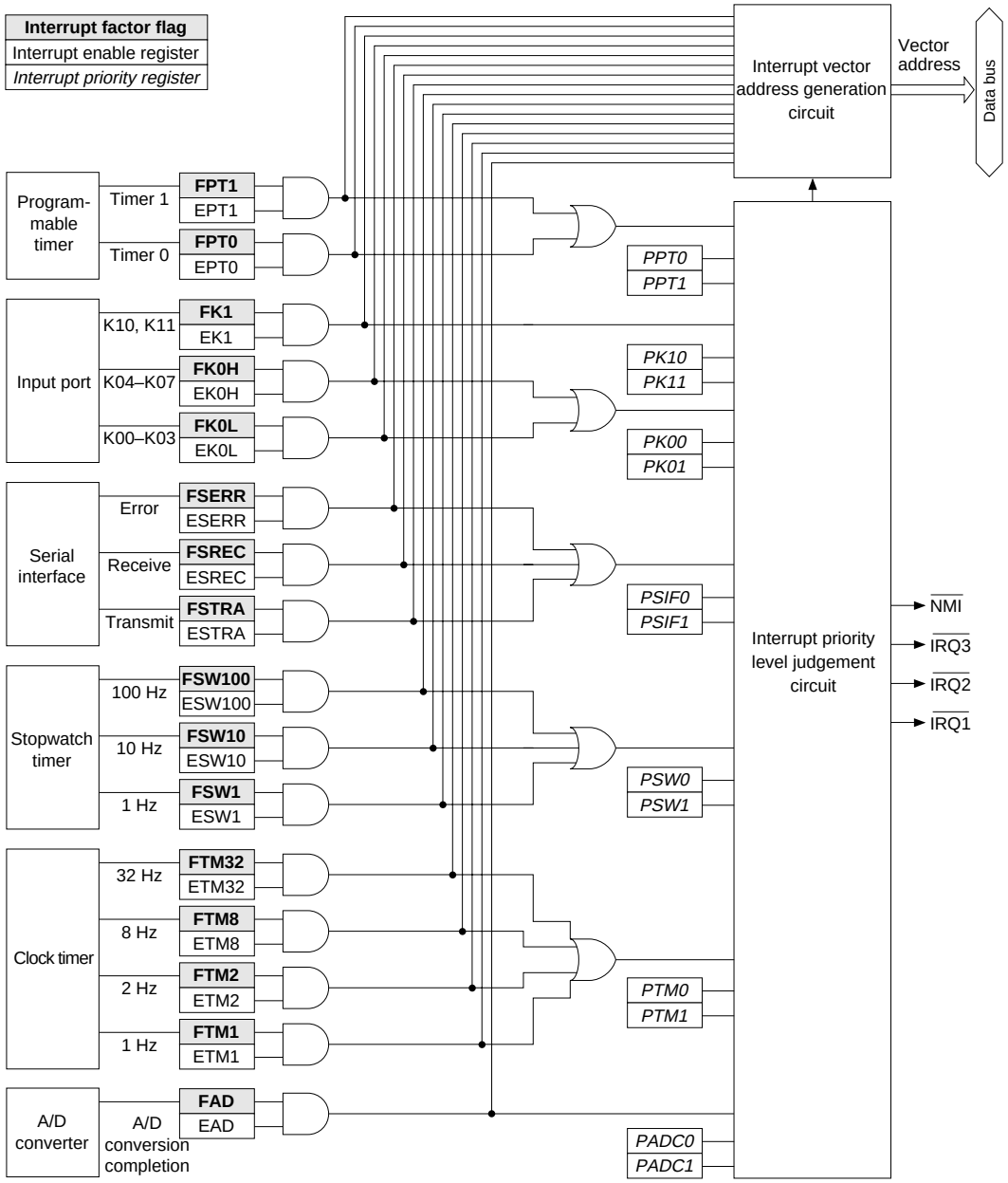


Fig. 5.17.1 Configuration of interrupt circuit

■ HALT status

By executing the program's HALT instruction, the S1C88349 shifts to the HALT status.
Since CPU operation stops in the HALT status, power consumption can be reduced with only peripheral circuit operation.
Cancellation of the HALT status is done by initial reset or an optional interrupt request, and the CPU restarts program execution from an exception processing routine.
See the "S1C88 Core CPU Manual" for the HALT status and reactivation sequence.

■ SLEEP status

By executing the program's SLP instruction, the S1C88349 shifts to the SLEEP status.
Since the operation of the CPU and peripheral circuits stop completely in the SLEEP status, power consumption can be reduced even more than in the HALT status.
Cancellation of the SLEEP status is done by initial reset or an input interrupt from the input port. The CPU reactivates after waiting 8,192 / f_{OSC1} seconds of oscillation stabilization time. At this time, the CPU restarts program execution from an exception processing routine (input interrupt routine).

Note: Since oscillation is unstable for a short time after reactivation from the SLEEP status, the wait time is not always 250 msec even when using the 32.768 kHz crystal oscillator for the OSC1 oscillation circuit.

5.17.1 Interrupt generation conditions

The interrupt factor flags that indicate the generation of their respective interrupt factors are provided for the previously indicated 7 systems and 16 types of interrupts and they will be set to "1" by the generation of a factor.

In addition, interrupt enable registers with a 1 to 1 correspondence to each of the interrupt factor flags are provided. An interrupt is enabled when "1" is written and interrupt is disabled when "0" is written.

The CPU manages the enable / disable of interrupt requests at the interrupt priority level. An interrupt priority register that sets the priority level is provided for each of the interrupts of the 7 systems and the CPU accepts only interrupts above the level that has been indicated with the interrupt flags (I0 and I1).
Consequently, the following three conditions are necessary for the CPU to accept the interrupt.

(1) The interrupt factor flag has been set to "1" by generation of an interrupt factor.
(2) The interrupt enable register corresponding to the above has been set to "1".
(3) The interrupt priority register corresponding to the above has been set to a priority level higher than the interrupt flag (I0 and I1) setting.

The CPU initially samples the interrupt for the first op-code fetch cycle of each instruction. Thereupon, the CPU shifts to the exception processing when the above mentioned conditions have been established.
See the "S1C88 Core CPU Manual" for the exception processing sequence.

5.17.2 Interrupt factor flag

Table 5.17.2.1 shows the correspondence between the factors generating an interrupt and the interrupt factor flags.
The corresponding interrupt factor flags are set to "1" by generation of the respective interrupt factors.
The corresponding interrupt factor can be confirmed by reading the flags through software.

Table 5.17.2.1 Interrupt factors

Interrupt factor	Interrupt factor flag	
Programmable timer 1 underflow	FPT1	(00FF25 D7)
Programmable timer 0 underflow	FPT0	(00FF25 D6)
Non matching of the K10 and K11 inputs and the input comparison registers KCP10 and KCP11	FK1	(00FF25 D5)
Non matching of the K04–K07 inputs and the input comparison registers KCP04–KCP07	FK0H	(00FF25 D4)
Non matching of the K00–K03 inputs and the input comparison registers KCP00–KCP03	FK0L	(00FF25 D3)
Serial interface receiving error (in asynchronous mode)	FSERR	(00FF25 D2)
Serial interface receiving completion	FSREC	(00FF25 D1)
Serial interface transmitting completion	FSTRA	(00FF25 D0)
Falling edge of the stopwatch timer 100 Hz signal	FSW100	(00FF24 D6)
Falling edge of the stopwatch timer 10 Hz signal	FSW10	(00FF24 D5)
Falling edge of the stopwatch timer 1 Hz signal	FSW1	(00FF24 D4)
Rising edge of the clock timer 32 Hz signal	FTM32	(00FF24 D3)
Rising edge of the clock timer 8 Hz signal	FTM8	(00FF24 D2)
Rising edge of the clock timer 2 Hz signal	FTM2	(00FF24 D1)
Rising edge of the clock timer 1 Hz signal	FTM1	(00FF24 D0)
A/D conversion completion	FAD	(00FF2C D7)

Interrupt factor flag that has been set to "1" is reset to "0" by writing "1".
At initial reset, the interrupt factor flags are reset to "0".

Note: When executing the RETE instruction without resetting the interrupt factor flag after an interrupt has been generated, the same interrupt will be generated. Consequently, the interrupt factor flag corresponding to that routine must be reset (writing "1") in the interrupt processing routine.

5.17.3 Interrupt enable register

The interrupt enable register has a 1 to 1 correspondence with each interrupt factor flag and enable / disable of interrupt requests can be set.

When "1" is written to the interrupt enable register, an interrupt request is enabled, and is disabled when "0" is written. This register also permits reading, thus making it possible to confirm that a status has been set.
At initial reset, the interrupt enable registers are set to "0" and shifts to the interrupt disable status.
Table 5.17.3.1 shows the correspondence between the interrupt enable registers and the interrupt factor flags.

5.17.4 Interrupt priority register and interrupt priority level

The interrupt priority registers shown in Table 5.17.4.1 are set to each system of interrupts and the interrupt priority levels for the CPU can be set to the optional priority level (0–3). As a result, it is possible to have multiple interrupts that match the system's interrupt processing priority levels.

The interrupt priority level between each system can optionally be set to three levels by the interrupt priority register. However, when more than one system is set to the same priority level, they are processed according to the default priority level.

Table 5.17.4.2 Setting of interrupt priority level

P*1	P*0	Interrupt priority level	
1	1	Level 3	($\overline{IRQ3}$)
1	0	Level 2	($\overline{IRQ2}$)
0	1	Level 1	($\overline{IRQ1}$)
0	0	Level 0	(non)

Table 5.17.3.1 Interrupt enable registers and interrupt factor flags

Interrupt	Interrupt factor flag		Interrupt enable register	
Programmable timer 1	FPT1	(00FF25 D7)	EPT1	(00FF23 D7)
Programmable timer 0	FPT0	(00FF25 D6)	EPT0	(00FF23 D6)
K10 and K11 input	FK1	(00FF25 D5)	EK1	(00FF23 D5)
K04–K07 input	FK0H	(00FF25 D4)	EK0H	(00FF23 D4)
K00–K03 input	FK0L	(00FF25 D3)	EK0L	(00FF23 D3)
Serial interface receiving error	FSERR	(00FF25 D2)	ESERR	(00FF23 D2)
Serial interface receiving completion	FSREC	(00FF25 D1)	ESREC	(00FF23 D1)
Serial interface transmitting completion	FSTRA	(00FF25 D0)	ESTRA	(00FF23 D0)
Stopwatch timer 100 Hz	FSW100	(00FF24 D6)	ESW100	(00FF22 D6)
Stopwatch timer 10 Hz	FSW10	(00FF24 D5)	ESW10	(00FF22 D5)
Stopwatch timer 1 Hz	FSW1	(00FF24 D4)	ESW1	(00FF22 D4)
Clock timer 32 Hz	FTM32	(00FF24 D3)	ETM32	(00FF22 D3)
Clock timer 8 Hz	FTM8	(00FF24 D2)	ETM8	(00FF22 D2)
Clock timer 2 Hz	FTM2	(00FF24 D1)	ETM2	(00FF22 D1)
Clock timer 1 Hz	FTM1	(00FF24 D0)	ETM1	(00FF22 D0)
A/D conversion completion	FAD	(00FF2C D7)	EAD	(00FF2A D7)

Table 5.17.4.1 Interrupt priority register

Interrupt	Interrupt priority register	
Programmable timer interrupt	PPT0, PPT1	(00FF21 D2, D3)
K10 and K11 input interrupt	PK10, PK11	(00FF21 D0, D1)
K00–K07 input interrupt	PK00, PK01	(00FF20 D6, D7)
Serial interface interrupt	PSIF0, PSIF1	(00FF20 D4, D5)
Stopwatch timer interrupt	PSW0, PSW1	(00FF20 D2, D3)
Clock timer interrupt	PTM0, PTM1	(00FF20 D0, D1)
A/D converter interrupt	PADC0, PADC1	(00FF28 D6, D7)

At initial reset, the interrupt priority registers are all set to "0" and each interrupt is set to level 0. Furthermore, the priority levels in each system have been previously decided and they cannot be changed.
The CPU can mask each interrupt by setting the interrupt flags (I0 and I1). The relation between the interrupt priority level of each system and interrupt flags is shown in Table 5.17.4.3, and the CPU accepts only interrupts above the level indicated by the interrupt flags.
The $\overline{\text{NMI}}$ (watchdog timer) that has level 4 priority, is always accepted regardless of the setting of the interrupt flags.

Table 5.17.4.3 Interrupt mask setting of CPU

I1	I0	Acceptable interrupt
1	1	Level 4 ($\overline{\text{NMI}}$)
1	0	Level 4, Level 3 ($\overline{\text{IRQ3}}$)
0	1	Level 4, Level 3, Level 2 ($\overline{\text{IRQ2}}$)
0	0	Level 4, Level 3, Level 2, Level 1 ($\overline{\text{IRQ1}}$)

After an interrupt has been accepted, the interrupt flags are written to the level of that interrupt. However, interrupt flags after an $\overline{\text{NMI}}$ has been accepted are written to level 3 (I0 = I1 = "1").

Table 5.17.4.4 Interrupt flags after acceptance of interrupt

Accepted interrupt priority level		I1	I0
Level 4	($\overline{\text{NMI}}$)	1	1
Level 3	($\overline{\text{IRQ3}}$)	1	1
Level 2	($\overline{\text{IRQ2}}$)	1	0
Level 1	($\overline{\text{IRQ1}}$)	0	1

The set interrupt flags are reset to their original value on return from the interrupt processing routine. Consequently, multiple interrupts up to 3 levels can be controlled by the initial settings of the interrupt priority registers alone. Additional multiplexing can be realized by rewriting the interrupt flags and interrupt enable register in the interrupt processing routine.

Note: Beware. If the interrupt flags have been rewritten (set to lower priority) prior to resetting an interrupt factor flag after an interrupt has been generated, the same interrupt will be generated again.

5.17.5 Exception processing vectors

When the CPU accepts an interrupt request, it starts exception processing following completion of the instruction being executed. In exception processing, the following operations branch the program.

(1) In the minimum mode, the program counter (PC) and system condition flag (SC) are moved to stack and in the maximum mode, the code bank register (CB), PC and SC are moved.
(2) The branch destination address is read from the exception processing vector corresponding to each exception processing (interrupt) factor and is placed in the PC.

An exception vector is 2 bytes of data in which the top address of each exception (interrupt) processing routine has been stored and the vector addresses correspond to the exception processing factors as shown in Table 5.17.5.1.

Table 5.17.5.1 Vector address and exception processing correspondence

Vector address	Exception processing factor	Priority
000000H	Reset	High ↑
000002H	Zero division	
000004H	Watchdog timer ($\overline{\text{NMI}}$)	
000006H	Programmable timer 1 interrupt	
000008H	Programmable timer 0 interrupt	
00000AH	K10, K11 input interrupt	
00000CH	K04–K07 input interrupt	
00000EH	K00–K03 input interrupt	
000010H	Serial I/F error interrupt	
000012H	Serial I/F receiving complete interrupt	
000014H	Serial I/F transmitting complete interrupt	
000016H	Stopwatch timer 100 Hz interrupt	
000018H	Stopwatch timer 10 Hz interrupt	
00001AH	Stopwatch timer 1 Hz interrupt	
00001CH	Clock timer 32 Hz interrupt	
00001EH	Clock timer 8 Hz interrupt	
000020H	Clock timer 2 Hz interrupt	
000022H	Clock timer 1 Hz interrupt	↓
000024H	A/D converter interrupt	Low
000026H	System reserved (cannot be used)	No priority rating
000028H : 0000FEH	Software interrupt	

Note: An exception processing vector is fixed at 2 bytes, so it cannot specify a branch destination bank address. Consequently, to branch from multiple banks to a common exception processing routine, the top portion of an exception processing routine must be described within the common area (000000H–007FFFH).

5.17.6 Control of interrupt

Table 5.17.6.1 shows the interrupt control bits.

Table 5.17.6.1(a) Interrupt control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF20	D7	PK01	K00–K07 interrupt priority register	PK01 PK00 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PK00						
	D5	PSIF1	Serial interface interrupt priority register	PSIF1 PSIF0 PSW1 PSW0 PTM1 PTM0 Priority level		0	R/W	
	D4	PSIF0						
	D3	PSW1	Stopwatch timer interrupt priority register			0	R/W	
	D2	PSW0						
	D1	PTM1	Clock timer interrupt priority register			0	R/W	
	D0	PTM0						
00FF21	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	PPT1	Programmable timer interrupt priority register	PPT1 PPT0 PK11 PK10 Priority level 1 1 Level 3		0	R/W	
	D2	PPT0						
	D1	PK11	K10 and K11 interrupt priority register	1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D0	PK10						
00FF22	D7	–	–	–	–	–		"0" when being read
	D6	ESW100	Stopwatch timer 100 Hz interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D5	ESW10	Stopwatch timer 10 Hz interrupt enable register					
	D4	ESW1	Stopwatch timer 1 Hz interrupt enable register					
	D3	ETM32	Clock timer 32 Hz interrupt enable register					
	D2	ETM8	Clock timer 8 Hz interrupt enable register					
	D1	ETM2	Clock timer 2 Hz interrupt enable register					
	D0	ETM1	Clock timer 1 Hz interrupt enable register					
00FF23	D7	EPT1	Programmable timer 1 interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D6	EPT0	Programmable timer 0 interrupt enable register					
	D5	EK1	K10 and K11 interrupt enable register					
	D4	EK0H	K04–K07 interrupt enable register					
	D3	EK0L	K00–K03 interrupt enable register					
	D2	ESERR	Serial I/F (error) interrupt enable register					
	D1	ESREC	Serial I/F (receiving) interrupt enable register					
	D0	ESTRA	Serial I/F (transmitting) interrupt enable register					
00FF24	D7	–	–	–	–	–		"0" when being read
	D6	FSW100	Stopwatch timer 100 Hz interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D5	FSW10	Stopwatch timer 10 Hz interrupt factor flag					
	D4	FSW1	Stopwatch timer 1 Hz interrupt factor flag					
	D3	FTM32	Clock timer 32 Hz interrupt factor flag					
	D2	FTM8	Clock timer 8 Hz interrupt factor flag					
	D1	FTM2	Clock timer 2 Hz interrupt factor flag					
	D0	FTM1	Clock timer 1 Hz interrupt factor flag					
00FF25	D7	FPT1	Programmable timer 1 interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D6	FPT0	Programmable timer 0 interrupt factor flag					
	D5	FK1	K10 and K11 interrupt factor flag					
	D4	FK0H	K04–K07 interrupt factor flag					
	D3	FK0L	K00–K03 interrupt factor flag					
	D2	FSERR	Serial I/F (error) interrupt factor flag					
	D1	FSREC	Serial I/F (receiving) interrupt factor flag					
	D0	FSTRA	Serial I/F (transmitting) interrupt factor flag					

Table 5.17.6.1(b) Interrupt control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF28	D7	PADC1	A/D converter interrupt priority register	PADC1 PADC0 Priority 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PADC0				0	R/W	
	D5	–	Reserved	Prohibited	–	0		Do not write "1".
	D4	–	Reserved	Prohibited	–	0		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		Constantly "0" when
	D1	–	–	–	–	–		being read
	D0	–	–	–	–	–		
00FF2A	D7	EAD	A/D converter interrupt enable register	Enable	Disable	0	R/W	
	D6	–	Reserved	–	–	0	R/W	
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		Constantly "0" when
	D2	–	–	–	–	–		being read
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		
00FF2C	D7	FAD	A/D converter interrupt factor flag	R) Generated W) Reset	Not generated No operation	0	R/W	
	D6	–	Reserved	–	–	0	R/W	
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		Constantly "0" when
	D2	–	–	–	–	–		being read
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		

Refer to the explanations on the respective peripheral circuits for the setting content and control method for each bit.

5.17.7 Programming notes

(1) When executing the RETE instruction without resetting the interrupt factor flag after an interrupt has been generated, the same interrupt will be generated. Consequently, the interrupt factor flag corresponding to that routine must be reset (writing "1") in the interrupt processing routine.

(2) Beware. If the interrupt flags (I0 and I1) have been rewritten (set to lower priority) prior to resetting an interrupt factor flag after an interrupt has been generated, the same interrupt will be generated again.

(3) An exception processing vector is fixed at 2 bytes, so it cannot specify a branch destination bank address. Consequently, to branch from multiple banks to a common exception processing routine, the front portion of an exception processing routine must be described within the common area (000000H–007FFFH).

(4) Do not execute the SLP instruction for 2 msec after a $\overline{\text{NMI}}$ interrupt has occurred (when f_{OSC1} is 32.768 kHz).

6 SUMMARY OF NOTES

6.1 Notes for Low Current Consumption

The S1C88349 can turn circuits, which consume a large amount of power, ON or OFF by control registers.
You can reduce power consumption by creating a program that operates the minimum necessary circuits using these control registers.

Next, which circuit systems' operation can be controlled and their control registers (instructions) are explained. You should refer to these when programming.

See Chapter 8, "ELECTRICAL CHARACTERISTICS" for the current consumption.

Refer to "Programming notes" in each peripheral section for precautions of each peripheral circuit.

Table 6.1.1 Circuit systems and control registers

Circuit type	Control register (Instruction)	Status at time of initial resetting
CPU	HALT and SLP instructions	Operation status
Oscillation circuit	CLKCHG, OSCC	OSC1 clock (CLKCHG = "0") OSC3 oscillation OFF (OSCC = "0")
Operating mode	VDC0, VDC1	Normal mode (VDC0 = VDC1 = "0")
LCD controller	LCDC0, LCDC1	Drive OFF (LCDC0 = LCDC1 = "0")
SVD circuit	SVDON, SVDSP	OFF status (SVDON = SVDSP = "0")
Analog comparator	CMP0ON, CMP1ON	OFF status (CMP0ON = CMP1ON = "0")
A/D converter	PRAD, ADRUN	OFF status (PRAD = ADRUN = "0")

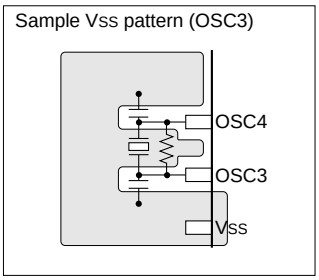
6.2 Precautions on Mounting

<Oscillation Circuit>

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.).
  In particular, when a ceramic or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.
- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC1, OSC2, OSC3 and OSC4 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.

  (2) As shown in the right hand figure, make a VSS pattern as large as possible at circumscription of the OSC1, OSC2, OSC3 and OSC4 terminals and the components connected to these terminals.
  Furthermore, do not use this VSS pattern for any purpose other than the oscillation system.



- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1 / OSC3 and VDD, please keep enough distance between OSC1 / OSC3 and VDD or other signals on the board pattern.

<Reset Circuit>

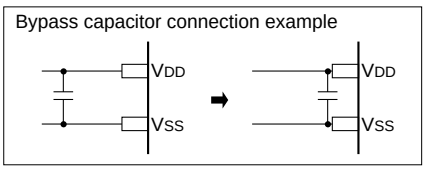
- The power-on reset signal which is input to the $\overline{\text{RESET}}$ terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
  Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product.
  When the built-in pull-up resistor is added to the $\overline{\text{RESET}}$ terminal by mask option, take into consideration dispersion of the resistance for setting the constant.
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the $\overline{\text{RESET}}$ terminal in the shortest line.

<Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

  (1) The power supply should be connected to the VDD, VSS, AVDD, AVSS and AVREF terminal with patterns as short and large as possible.
  In particular, the power supply for AVDD, AVSS and AVREF affects A / D conversion precision.

  (2) When connecting between the VDD and VSS terminals with a bypass capacitor, the terminals should be connected as short as possible.



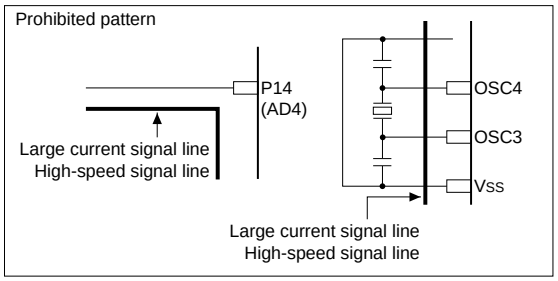
  (3) Components which are connected to the VD1, VC1–VC5 terminals, such as capacitors and resistors, should be connected in the shortest line.
  In particular, the VC1–VC5 voltages affect the display quality.

<A/D Converter>

- When the A / D converter is not used, the power supply terminals for the analog system should be connected as shown below.
  AVDD → VDD
  AVSS → VSS
  AVREF → VSS

<Arrangement of Signal Lines>

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit and analog input unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction.
  Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit and analog input unit.



<Precautions for Visible Radiation (when bare chip is mounted)>

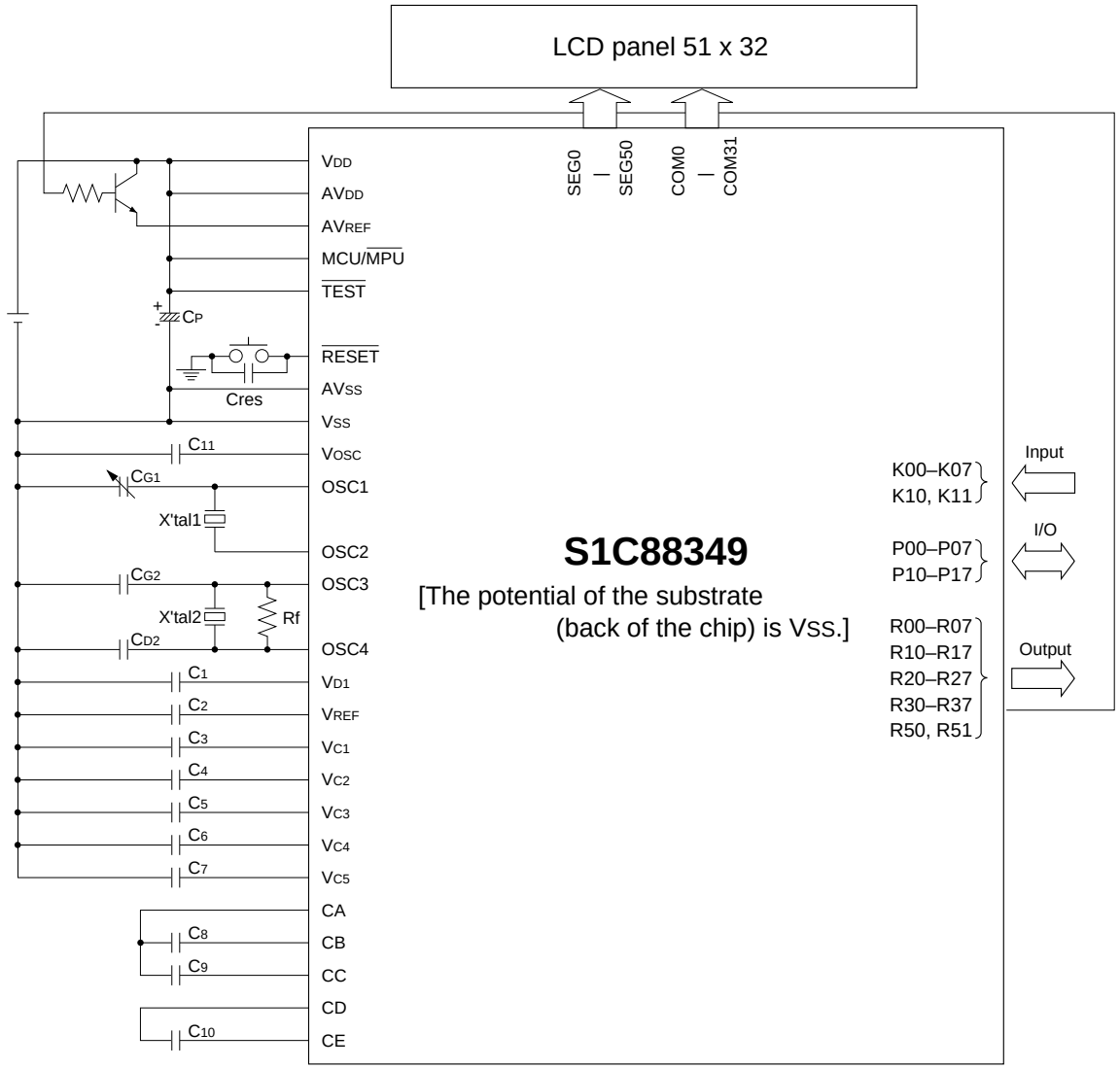
- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

  (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

  (3) As well as the face of the IC, shield the back and side too.

7 BASIC EXTERNAL WIRING DIAGRAM



Recommended values for external parts

Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768 kHz, CI (Max.) = 35 kΩ
X'tal2	Crystal oscillator	4.9152 MHz
Rf	Feedback resistor	1 MΩ
C_{G1}	Trimmer capacitor	5–25 pF
C_{G2}	Gate capacitor	15–30 pF
C_{D2}	Drain capacitor	15–30 pF
C_1	Capacitor between V_{SS} and V_{D1}	0.1 µF
C_2	Capacitor between V_{SS} and V_{REF}	0.1 µF

Symbol	Name	Recommended value
C_3	Capacitor between V_{SS} and V_{C1}	0.1 µF
C_4	Capacitor between V_{SS} and V_{C2}	0.1 µF
C_5	Capacitor between V_{SS} and V_{C3}	0.1 µF
C_6	Capacitor between V_{SS} and V_{C4}	0.1 µF
C_7	Capacitor between V_{SS} and V_{C5}	0.1 µF
C_8–C_{10}	Booster capacitors	0.1 µF
C_{11}	Capacitor between V_{SS} and V_{OSC}	0.1 µF
C_P	Capacitor for power supply	3.3 µF
Cres	Capacitor for $\overline{\text{RESET}}$ terminal	0.47 µF

Note: The above table is simply an example, and is not guaranteed to work.

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Rating

(V_{SS} = 0 V)

Item	Symbol	Condition	Rated value	Unit	Note
Power voltage	V_{DD}		-0.3 to +7.0	V	
Liquid crystal power voltage	V_{C5}		-0.3 to +7.0	V	
Input voltage	V_I		-0.3 to V_{DD} + 0.3	V	
Output voltage	V_O		-0.3 to V_{DD} + 0.3	V	1
High level output current	I_{OH}	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Low level output current	I_{OL}	1 terminal	5	mA	
		Total of all terminals	20	mA	
Permitted loss	P_D		200	mW	2
Operating temperature	Topr		-40 to +85	°C	
Storage temperature	Tstg		-65 to +150	°C	
Soldering temperature / time	Tsol		260°C, 10sec (lead section)	–	

Note) 1 Case that to Nch open drain output by the mask option is included.
2 In case of plastic package.

8.2 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating power voltage (Normal mode)	V_{DD}		2.4		5.5	V	
Operating power voltage (Low power mode)	V_{DD}		1.8		3.5	V	
Operating power voltage (High speed mode)	V_{DD}		3.5		5.5	V	
Operating frequency (Normal mode)	f_{OSC1}	V_{DD} = 2.4 to 5.5 V	30.000	32.768	80.000	kHz	1
	f_{OSC3}		0.03		4.2	MHz	1
Operating frequency (Low power mode)	f_{OSC1}	V_{DD} = 1.8 to 3.5 V	30.000	32.768	80.000	kHz	1
Operating frequency (High speed mode)	f_{OSC1}	V_{DD} = 3.5 to 5.5 V	30.000	32.768	80.000	kHz	1
	f_{OSC3}		0.03		8.2	MHz	1
Liquid crystal power voltage	V_{C5}	$V_{C5} \geq V_{C4} \geq V_{C3} \geq V_{C2} \geq V_{C1} \geq V_{SS}$			7.0	V	2
Capacitor between V_{D1} and V_{SS}	C_1			0.1		µF	
Capacitor between V_{REF} and V_{SS}	C_2			0.1		µF	3
Capacitor between V_{C1} and V_{SS}	C_3			0.1		µF	3
Capacitor between V_{C2} and V_{SS}	C_4			0.1		µF	3
Capacitor between V_{C3} and V_{SS}	C_5			0.1		µF	3
Capacitor between V_{C4} and V_{SS}	C_6			0.1		µF	3
Capacitor between V_{C5} and V_{SS}	C_7			0.1		µF	3
Capacitor between CA and CB	C_8			0.1		µF	3
Capacitor between CA and CC	C_9			0.1		µF	3
Capacitor between CD and CE	C_{10}			0.1		µF	3
Capacitor between V_{OSC} and V_{SS}	C_{11}			0.1		µF	3

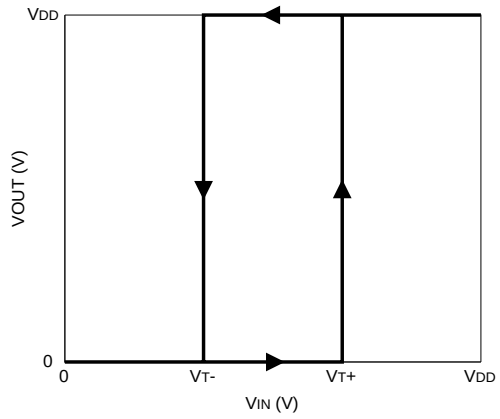
Note) 1 When an external clock is input from the OSC1 terminal by the mask option, leave the OSC2 terminal open, and when an external clock is input from the OSC3 terminal, leave the OSC4 terminal open.
2 When external power supply is selected by the mask option.
3 When LCD drive power is not used, the capacitor is not necessary.
In this case, leave the V_{C1} to V_{C5} and CA to CE terminals open.

8.3 DC Characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
High level input voltage (1)	V_{IH1}	Kxx, Pxx, MCU/$\overline{MPU}$	0.8V_{DD}		V_{DD}	V	
Low level input voltage (1)	V_{IL1}	Kxx, Pxx, MCU/$\overline{MPU}$	0		0.2V_{DD}	V	
High level input voltage (2) (Normal mode)	V_{IH2}	OSC1, OSC3	1.6		V_{DD}	V	1
High level input voltage (2) (Low power mode)	V_{IH2}	OSC1	1.0		V_{DD}	V	1
High level input voltage (2) (High speed mode)	V_{IH2}	OSC1, OSC3	2.4		V_{DD}	V	1
Low level input voltage (2) (Normal mode)	V_{IL2}	OSC1, OSC3	0		0.6	V	1
Low level input voltage (2) (Low power mode)	V_{IL2}	OSC1	0		0.3	V	1
Low level input voltage (2) (High speed mode)	V_{IL2}	OSC1, OSC3	0		0.9	V	1
High level schmitt input voltage	V_{T+}	$\overline{RESET}$	0.5V_{DD}		0.9V_{DD}	V	
Low level schmitt input voltage	V_{T-}	$\overline{RESET}$	0.1V_{DD}		0.5V_{DD}	V	
High level output current	I_{OH}	Pxx, Rxx, V_{OH} = 0.9 V_{DD}			-0.5	mA	
Low level output current	I_{OL}	Pxx, Rxx, V_{OL} = 0.1 V_{DD}	0.5			mA	
Input leak current	I_{LI}	Kxx, Pxx, $\overline{RESET}$, MCU/$\overline{MPU}$	-1		1	µA	
Output leak current	I_{LO}	Pxx, Rxx	-1		1	µA	
Input pull-up resistance	R_{IN}	Kxx, Pxx, $\overline{RESET}$, MCU/$\overline{MPU}$	100		500	kΩ	2
Input terminal capacitance	C_{IN}	Kxx, Pxx V_{IN} = 0 V, f = 1 MHz, Ta = 25°C			15	pF	
Segment/Common output current	I_{SEGH}	SEGxx, COMxx, V_{SEGH} = V_{C5}-0.1 V			-5	µA	
	I_{SEGL}	SEGxx, COMxx, V_{SEGL} = 0.1 V	5			µA	

Note) 1 When external clock is selected by mask option.
2 When addition of pull-up resistor is selected by mask option.



8.4 Analog Circuit Characteristics

■ LCD drive circuit

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, C_1–C_{11} = 0.1 µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
LCD drive voltage	V_{C1}	*1		0.19V_{C5}		0.23V_{C5}	V	
	V_{C2}	*2		0.39V_{C5}		0.43V_{C5}	V	
	V_{C3}	*3		0.59V_{C5}		0.62V_{C5}	V	
	V_{C4}	*4		0.78V_{C5}		0.82V_{C5}	V	
	V_{C5} TYPE A (4.5V)	*5	LCX = 0H		3.89		V	
			LCX = 1H		3.96		V	
			LCX = 2H		4.04		V	
			LCX = 3H		4.11		V	
			LCX = 4H		4.18		V	
			LCX = 5H		4.26		V	
			LCX = 6H		4.34		V	
			LCX = 7H	Typ×0.94	4.42	Typ×1.06	V	
			LCX = 8H		4.50		V	
			LCX = 9H		4.58		V	
			LCX = AH		4.66		V	
			LCX = BH		4.74		V	
			LCX = CH		4.82		V	
			LCX = DH		4.90		V	
			LCX = EH		4.99		V	
			LCX = FH		5.08		V	
	V_{C5} TYPE B (5.5V)	*5	LCX = 0H		4.73		V	
			LCX = 1H		4.83		V	
			LCX = 2H		4.92		V	
			LCX = 3H		5.02		V	
			LCX = 4H		5.11		V	
			LCX = 5H		5.21		V	
			LCX = 6H		5.30		V	
			LCX = 7H	Typ×0.94	5.40	Typ×1.06	V	
			LCX = 8H		5.50		V	
			LCX = 9H		5.60		V	
			LCX = AH		5.70		V	
			LCX = BH		5.81		V	
			LCX = CH		5.93		V	
			LCX = DH		6.05		V	
			LCX = EH		6.17		V	
			LCX = FH		6.29		V	

*1 Connects 1 MΩ load resistor between V_{DD} and V_{C1} (V_{C1} has no capability to drive the load connected to V_{SS} due to its property).

*2 Connects 1 MΩ load resistor between V_{SS} and V_{C2}.

*3 Connects 1 MΩ load resistor between V_{SS} and V_{C3}.

*4 Connects 1 MΩ load resistor between V_{SS} and V_{C4}.

*5 Connects 1 MΩ load resistor between V_{SS} and V_{C5}.

■ SVD circuit

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SVD voltage	V_{SVD}	Level 1 → Level 0	Typ×0.92	1.83	Typ×1.08	V	1
		Level 2 → Level 1		2.00		V	1
		Level 3 → Level 2		2.17		V	1
		Level 4 → Level 3		2.33		V	1
		Level 5 → Level 4		2.50		V	2
		Level 6 → Level 5		2.67		V	2
		Level 7 → Level 6		2.83		V	2
		Level 8 → Level 7		3.00		V	2
		Level 9 → Level 8		3.17		V	2
		Level 10 → Level 9		3.33		V	2
		Level 11 → Level 10		3.50		V	3
		Level 12 → Level 11		3.67		V	3
		Level 13 → Level 12		3.83		V	3
		Level 14 → Level 13		4.00		V	3
		Level 15 → Level 14		4.17		V	3

$V_{SVD\ (Level\ 0)} < V_{SVD\ (Level\ 1)} < V_{SVD\ (Level\ 2)} < V_{SVD\ (Level\ 3)} < V_{SVD\ (Level\ 4)} < V_{SVD\ (Level\ 5)} < V_{SVD\ (Level\ 6)} < V_{SVD\ (Level\ 7)}$
$< V_{SVD\ (Level\ 8)} < V_{SVD\ (Level\ 9)} < V_{SVD\ (Level\ 10)} < V_{SVD\ (Level\ 11)} < V_{SVD\ (Level\ 12)} < V_{SVD\ (Level\ 13)} < V_{SVD\ (Level\ 14)} < V_{SVD\ (Level\ 15)}$

Note) 1 Low power operating mode only
2 Low power operating mode or Normal operating mode
3 Normal operating mode or High speed operating mode

■ Analog comparator circuit

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Analog comparator operating voltage input range	V_{CMIP}	Non-inverted input (CMPP)	0.7		V_{DD} - 0.7	V	1
	V_{CMIM}	Inverted input (CMPM)	0.7		V_{DD} - 0.7	V	1
Analog comparator offset voltage	V_{CMOF}	V_{CMIP} = 0.7 V to V_{DD} - 0.7 V V_{CMIM} = 0.7 V to V_{DD} - 0.7 V			20	mV	1
Analog comparator stability time	t_{CMP1}				1	mS	2
Analog comparator response time	t_{CMP2}	V_{CMIP} = 0.7 V to V_{DD} - 0.7 V V_{CMIM} = 0.7 V to V_{DD} - 0.7 V $V_{CMIP} = V_{CMIM} \pm 0.025$ V			2	mS	1 3

Note) 1 When "no pull-up resistor" (for comparator input) is selected by mask option.
2 Stability time is the time from turning the circuit ON until the circuit is stabilized.
3 Response time is the time that the output result responds to the input signal.

■ A/D converter circuit

Unless otherwise specified: V_{DD} = AV_{DD} = AV_{REF} = 5.0 V, V_{SS} = AV_{SS} =0 V, f_{OSC1} = 32.768 kHz, f_{OSC3} = 4.0 MHz, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Zero-scale error	Ezs	V_{DD} = AV_{DD} = AV_{REF} = 2.4 to 5.5 V, ADCLK = 1 MHz, Ta = 25°C	-1.5		+1.5	LSB	
Full-scale error	Efs		-1.5		+1.5	LSB	
Non-linearity error	El		-5		+5	LSB	
Total error	Et		-5		+5	LSB	
A/D converter current consumption	I_{AD}	V_{DD} = AV_{DD} = AV_{REF} = 3.0 V, ADCLK = 1 MHz, Ta = 25°C AV_{REF} and ADCLK divider current not included		70	130	µA	1
		V_{DD} = AV_{DD} = AV_{REF} = 5.0 V, ADCLK = 1 MHz, Ta = 25°C AV_{REF} and ADCLK divider current not included		250	350	µA	1
A/D conversion clock	f	V_{DD} = AV_{DD} = AV_{REF} = 2.4 to 5.5 V, Ta = 25°C			1	MHz	2
		V_{DD} = AV_{DD} = AV_{REF} = 2.0 to 2.4 V, Ta = 25°C			32	kHz	2

∗ Zero-scale error: Ezs = deviation from the ideal value at zero point

∗ Full-scale error: Efs = deviation from the ideal value at the full scale point

∗ Non-linearity error: El = deviation of the real conversion curve from the end point line

∗ Total error: Et = max (Ezs, Efs, Eabs), Eabs = deviation from the ideal line (including quantization error)

Note) 1 Average current during conversion

2 See Table 5.15.4.2 in "5.15 A/D Converter" for setting the A/D conversion clock.

8.5 Power Current Consumption

Unless otherwise specified: V_{DD} = Within the operating voltage in each operating mode, V_{SS} = 0 V, Ta = 25°C,
OSC1 = 32.768 kHz crystal oscillation, C_G = 25pF, C_1–C_{11} = 0.1 µF, No panel load

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power current (Normal mode)	I_{DD1}	In SLEEP status *1		0.3	1.5	µA	
	I_{DD2}	In HALT status *2		1.5	4	µA	
	I_{DD3}	CPU is in operating (32.768 kHz) *3		9	15	µA	
	I_{DD4}	CPU is in operating (4 MHz) *4		1.1	1.4	mA	
Power current (Low power mode)	I_{DD1}	In SLEEP status *1		0.2	1	µA	
	I_{DD2}	In HALT status *2		1	3	µA	
	I_{DD3}	CPU is in operating (32.768 kHz) *3		5	7	µA	
Power current (High speed mode)	I_{DD1}	In SLEEP status *1		0.6	3	µA	
	I_{DD2}	In HALT status *2		2	6	µA	
	I_{DD3}	CPU is in operating (32.768 kHz) *3		13	20	µA	
	I_{DD4}	CPU is in operating (8 MHz) *4		3.7	4.8	mA	
LCD drive circuit current	I_{LCDN}			3	5	µA	
SVD circuit current	I_{SVDN}	V_{DD} = 3 V		30	60	µA	1
Analog comparator circuit current	I_{CMP1}	CMPXDT = "1"		35	60	µA	
	I_{CMP2}	CMPXDT = "0"		2	4	µA	

*1 OSC1: Stop, OSC3: Stop, CPU, ROM, RAM: SLEEP status, Clock timer: Stop, Others: Stop status
*2 OSC1: Oscillating, OSC3: Stop, CPU, ROM, RAM: HALT status, Clock timer: Operating, Others: Stop status
*3 OSC1: Oscillating, OSC3: Stop, CPU, ROM, RAM: Operating in 32.768 kHz, Clock timer: Operating, Others: Stop status
*4 OSC1: Oscillating, OSC3: Oscillating, CPU, ROM, RAM: Operating in 1 MHz, Clock timer: Operating, Others: Stop status

Note) 1 The value in ***x*** V can be found by the following expression: I_{SVDN} (V_{DD} = ***x*** V) = (***x*** × 60) - 150 (Max. value)

8.6 AC Characteristics

■ Operating range

Condition: V_{DD} = Within the operating voltage in each operating mode, V_{SS} = 0 V, Ta = -40 to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating frequency (Normal mode)	f_{OSC1}	V_{DD} = 2.4 to 5.5 V	30.000	32.768	80.000	kHz	
	f_{OSC3}		0.03		4.2	MHz	
Operating frequency (Low power mode)	f_{OSC1}	V_{DD} = 1.8 to 3.5 V	30.000	32.768	80.000	kHz	
Operating frequency (High speed mode)	f_{OSC1}	V_{DD} = 3.5 to 5.5 V	30.000	32.768	80.000	kHz	
	f_{OSC3}		0.03		8.2	MHz	
Instruction execution time (during operation with OSC1 clock)	tcy	1-cycle instruction	25	61	67	µS	
		2-cycle instruction	50	122	133	µS	
		3-cycle instruction	75	183	200	µS	
		4-cycle instruction	100	244	267	µS	
		5-cycle instruction	125	305	333	µS	
		6-cycle instruction	150	366	400	µS	
Instruction execution time Normal mode (during operation with OSC3 clock)	tcy	1-cycle instruction	0.5		66.7	µS	
		2-cycle instruction	1.0		133.3	µS	
		3-cycle instruction	1.4		200.0	µS	
		4-cycle instruction	1.9		266.7	µS	
		5-cycle instruction	2.4		333.3	µS	
		6-cycle instruction	2.9		400.0	µS	
Instruction execution time High speed mode (during operation with OSC3 clock)	tcy	1-cycle instruction	0.2		66.7	µS	
		2-cycle instruction	0.5		133.3	µS	
		3-cycle instruction	0.7		200.0	µS	
		4-cycle instruction	1.0		266.7	µS	
		5-cycle instruction	1.2		333.3	µS	
		6-cycle instruction	1.5		400.0	µS	

■ External memory access

• Read cycle (Normal operating mode)

Condition: V_{DD} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{IH2} = 1.6 V, V_{IL2} = 0.6 V, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}, C_L = 100 pF (load capacitance)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Address set-up time in read cycle	tras	tc+tl-100+n•tc/2			nS	1
Address hold time in read cycle	trah	th-80			nS	
Read signal pulse width	trp	tc-20+n•tc/2			nS	1
Data input set-up time in read cycle	trds	300			nS	
Data input hold time in read cycle	trdh	0			nS	

Note) 1 Substitute the number of states for wait insertion in n.

• Read cycle (High speed operating mode)

Condition: V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{IH2} = 2.4 V, V_{IL2} = 0.9 V, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}, C_L = 100 pF (load capacitance)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Address set-up time in read cycle	tras	tc+tl-50+n•tc/2			nS	1
Address hold time in read cycle	trah	th-40			nS	
Read signal pulse width	trp	tc-10+n•tc/2			nS	1
Data input set-up time in read cycle	trds	150			nS	
Data input hold time in read cycle	trdh	0			nS	

Note) 1 Substitute the number of states for wait insertion in n.

• Read cycle (Low power operating mode)

Condition: V_{DD} = 1.8 to 3.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{IH2} = 1.0 V, V_{IL2} = 0.3 V, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}, C_L = 100 pF (load capacitance)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Address set-up time in read cycle	tras	15			µS	
Address hold time in read cycle	trah	5			µS	
Read signal pulse width	trp	10			µS	
Data input set-up time in read cycle	trds	10			µS	
Data input hold time in read cycle	trdh	0			µS	

• Write cycle (Normal operating mode)

Condition: V_{DD} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{IH2} = 1.6 V, V_{IL2} = 0.6 V, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}, C_L = 100 pF (load capacitance)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Address set-up time in write cycle	twas	tc-180			nS	
Address hold time in write cycle	twah	th-80			nS	
Write signal pulse width	twp	tl-40+n•tc/2			nS	1
Data output set-up time in write cycle	twds	tc-180+n•tc/2			nS	1
Data output hold time in write cycle	twdh	th-80		th+80	nS	

Note) 1 Substitute the number of states for wait insertion in n.

• Write cycle (High speed operating mode)

Condition: V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{IH2} = 2.4 V, V_{IL2} = 0.9 V, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}, C_L = 100 pF (load capacitance)

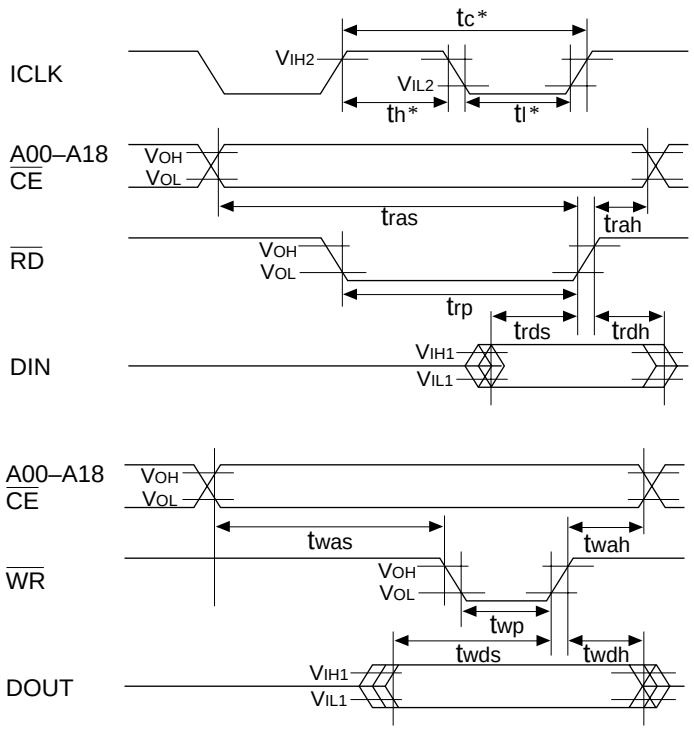
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Address set-up time in write cycle	twas	tc-90			nS	
Address hold time in write cycle	twah	th-40			nS	
Write signal pulse width	twp	tl-20+n•tc/2			nS	1
Data output set-up time in write cycle	twds	tc-90+n•tc/2			nS	1
Data output hold time in write cycle	twdh	th-40		th+40	nS	

Note) 1 Substitute the number of states for wait insertion in n.

• Write cycle (Low power operating mode)

Condition: V_{DD} = 1.8 to 3.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{IH2} = 1.0 V, V_{IL2} = 0.3 V, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}, C_L = 100 pF (load capacitance)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Address set-up time in write cycle	twas	10			µS	
Address hold time in write cycle	twah	5			µS	
Write signal pulse width	twp	5			µS	
Data output set-up time in write cycle	twds	10			µS	
Data output hold time in write cycle	twdh	5		20	µS	



* In the case of crystal oscillation and ceramic oscillation: th = 0.5tc ± 0.05tc, tl = tc - th (1/tc: oscillation frequency)

* In the case of CR oscillation: th = 0.5tc ± 0.10tc, tl = tc - th (1/tc: oscillation frequency)

■ Serial interface

• Clock synchronous master mode (Normal operating mode)

Condition: V_{DD} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tsmd			200	nS	
Receiving data input set-up time	tsms	500			nS	
Receiving data input hold time	tsmh	200			nS	

• Clock synchronous master mode (High speed operating mode)

Condition: V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tsmd			100	nS	
Receiving data input set-up time	tsms	250			nS	
Receiving data input hold time	tsmh	100			nS	

• Clock synchronous master mode (Low power operating mode)

Condition: V_{DD} = 1.8 to 3.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tsmd			5	µS	
Receiving data input set-up time	tsms	10			µS	
Receiving data input hold time	tsmh	5			µS	

• Clock synchronous slave mode (Normal operating mode)

Condition: V_{DD} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tssd			500	nS	
Receiving data input set-up time	tsss	200			nS	
Receiving data input hold time	tssh	200			nS	

• Clock synchronous slave mode (High speed operating mode)

Condition: V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tssd			250	nS	
Receiving data input set-up time	tsss	100			nS	
Receiving data input hold time	tssh	100			nS	

• Clock synchronous slave mode (Low power operating mode)

Condition: V_{DD} = 1.8 to 3.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tssd			10	µS	
Receiving data input set-up time	tsss	5			µS	
Receiving data input hold time	tssh	5			µS	

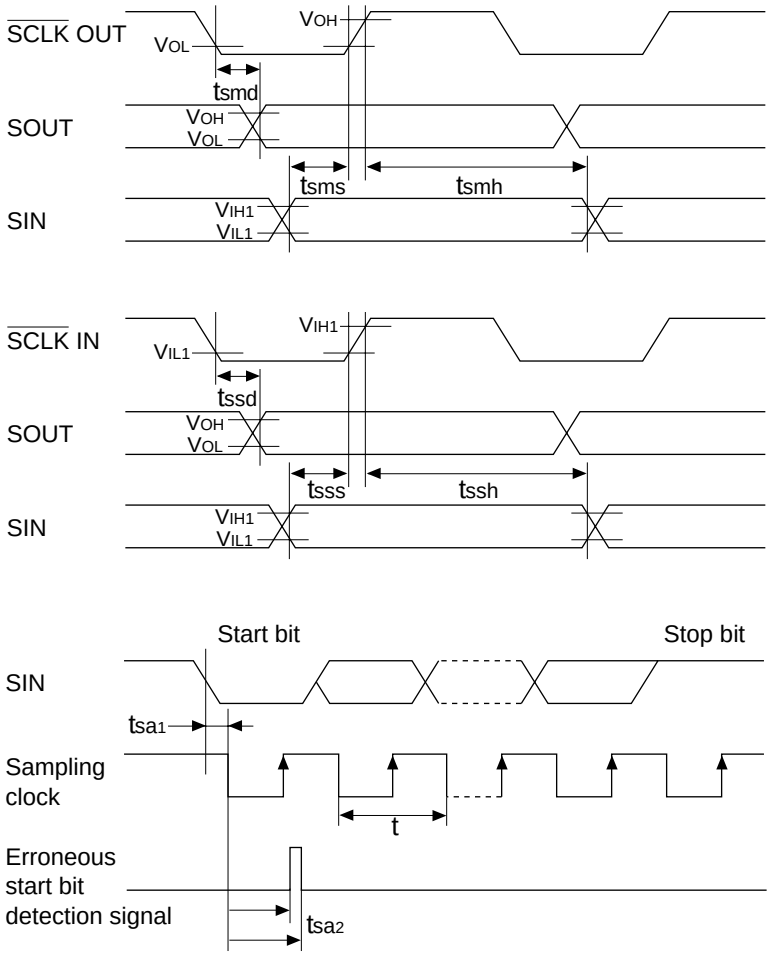
• Asynchronous system (All operating mode)

Condition: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Start bit detection error time	t_{sa1}	0		t/16	S	1
Erroneous start bit detection range time	t_{sa2}	9t/16		10t/16	S	2

Note) 1 Start bit detection error time is a logical delay time from inputting the start bit until internal sampling begins operating. (Time as far as AC is excluded.)

2 Erroneous start bit detection range time is a logical range to detect whether a LOW level (start bit) has been input again after a start bit has been detected and the internal sampling clock has started.
When a HIGH level is detected, the start bit detection circuit is reset and goes into a wait status until the next start bit. (Time as far as AC is excluded.)



■ Input clock

• OSC1, OSC3 external clock (Normal operating mode)

Condition: V_{DD} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C, V_{IH2} = 1.6 V, V_{IL2} = 0.6 V

Item		Symbol	Min.	Typ.	Max.	Unit	Note
OSC1 input clock time	Cycle time	t_{O1CY}	20		32	µS	
	"H" pulse width	t_{O1H}	10		16	µS	
	"L" pulse width	t_{O1L}	10		16	µS	
OSC3 input clock time	Cycle time	t_{O3CY}	250		32,000	nS	
	"H" pulse width	t_{O3H}	125		16,000	nS	
	"L" pulse width	t_{O3L}	125		16,000	nS	
Input clock rising time		t_{OSR}			25	nS	
Input clock falling time		t_{OSF}			25	nS	

• OSC1, OSC3 external clock (High speed operating mode)

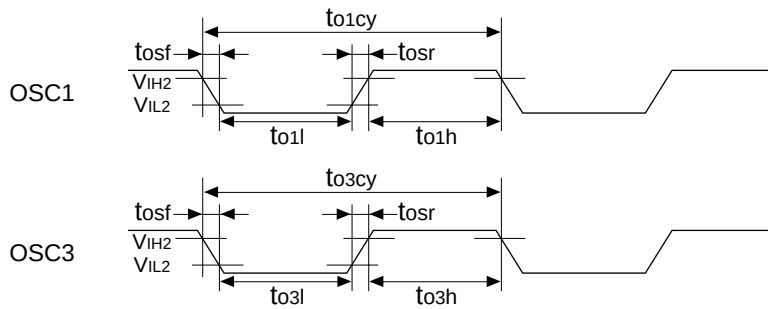
Condition: V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C, V_{IH2} = 2.4 V, V_{IL2} = 0.9 V

Item		Symbol	Min.	Typ.	Max.	Unit	Note
OSC1 input clock time	Cycle time	t_{O1CY}	20		32	µS	
	"H" pulse width	t_{O1H}	10		16	µS	
	"L" pulse width	t_{O1L}	10		16	µS	
OSC3 input clock time	Cycle time	t_{O3CY}	125		32,000	nS	
	"H" pulse width	t_{O3H}	62.5		16,000	nS	
	"L" pulse width	t_{O3L}	62.5		16,000	nS	
Input clock rising time		t_{OSR}			25	nS	
Input clock falling time		t_{OSF}			25	nS	

• OSC1, OSC3 external clock (Low power operating mode)

Condition: V_{DD} = 1.8 to 3.5 V, V_{SS} = 0 V, Ta = -40 to 85°C, V_{IH2} = 1.0 V, V_{IL2} = 0.3 V

Item		Symbol	Min.	Typ.	Max.	Unit	Note
OSC1 input clock time	Cycle time	t_{O1CY}	20		32	µS	
	"H" pulse width	t_{O1H}	10		16	µS	
	"L" pulse width	t_{O1L}	10		16	µS	
Input clock rising time		t_{OSR}			25	nS	
Input clock falling time		t_{OSF}			25	nS	



• $\overline{SCLK}$, EVIN input clock (Normal operating mode)

Condition: V_{DD} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}

Item		System	Min.	Typ.	Max.	Unit	Note
$\overline{SCLK}$ input clock time	Cycle time	tsccy	4			µS	
	"H" pulse width	tsch	2			µS	
	"L" pulse width	tscl	2			µS	
EVIN input clock time (With noise rejector)	Cycle time	tevcy	64 / f_{OSC1}			S	
	"H" pulse width	tevh	32 / f_{OSC1}			S	
	"L" pulse width	tevl	32 / f_{OSC1}			S	
EVIN input clock time (Without noise rejector)	Cycle time	tevcy	4			µS	
	"H" pulse width	tevh	2			µS	
	"L" pulse width	tevl	2			µS	
Input clock rising time		tckr			25	nS	
Input clock falling time		tckf			25	nS	

• $\overline{SCLK}$, EVIN input clock (High speed operating mode)

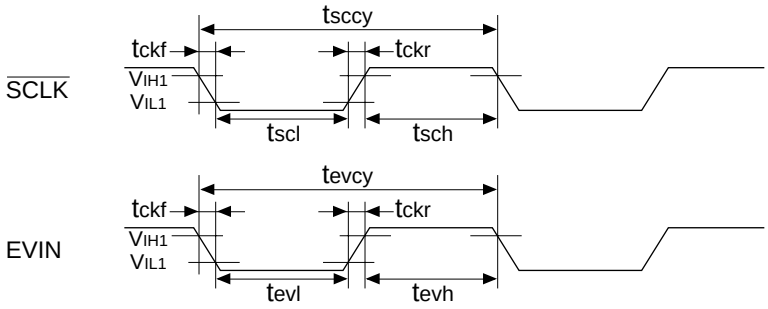
Condition: V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}

Item		System	Min.	Typ.	Max.	Unit	Note
$\overline{SCLK}$ input clock time	Cycle time	tsccy	2			µS	
	"H" pulse width	tsch	1			µS	
	"L" pulse width	tscl	1			µS	
EVIN input clock time (With noise rejector)	Cycle time	tevcy	64 / f_{OSC1}			S	
	"H" pulse width	tevh	32 / f_{OSC1}			S	
	"L" pulse width	tevl	32 / f_{OSC1}			S	
EVIN input clock time (Without noise rejector)	Cycle time	tevcy	2			µS	
	"H" pulse width	tevh	1			µS	
	"L" pulse width	tevl	1			µS	
Input clock rising time		tckr			25	nS	
Input clock falling time		tckf			25	nS	

• $\overline{SCLK}$, EVIN input clock (Low power operating mode)

Condition: V_{DD} = 1.8 to 3.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}

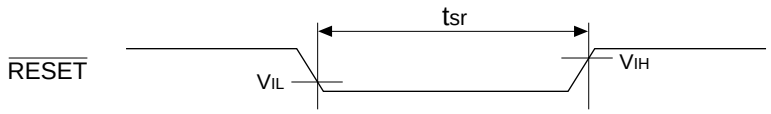
Item		System	Min.	Typ.	Max.	Unit	Note
$\overline{SCLK}$ input clock time	Cycle time	tsccy	100			µS	
	"H" pulse width	tsch	50			µS	
	"L" pulse width	tscl	50			µS	
EVIN input clock time (With noise rejector)	Cycle time	tevcy	64 / f_{OSC1}			S	
	"H" pulse width	tevh	32 / f_{OSC1}			S	
	"L" pulse width	tevl	32 / f_{OSC1}			S	
EVIN input clock time (Without noise rejector)	Cycle time	tevcy	100			µS	
	"H" pulse width	tevh	50			µS	
	"L" pulse width	tevl	50			µS	
Input clock rising time		tckr			25	nS	
Input clock falling time		tckf			25	nS	



- **$\overline{\text{RESET}}$ input clock (All operating mode)**

Condition: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH} = 0.5V_{DD}, V_{IL} = 0.1V_{DD}

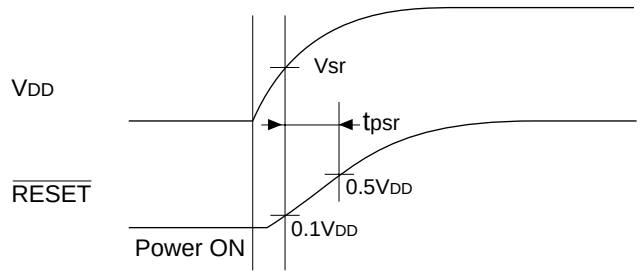
Item	Symbol	Min.	Typ.	Max.	Unit	Note
$\overline{\text{RESET}}$ input time	tsr	100			µS	

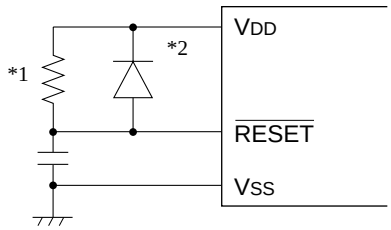


■ Power ON reset

Condition: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Operating power voltage	Vsr	2.4			V	
$\overline{\text{RESET}}$ input time	tpsr	10			mS	





*1 When the built-in pull up resistor is not used.

*2 Because the potential of the $\overline{\text{RESET}}$ terminal not reached V_{DD} level or higher.

■ Operating mode switching

Condition: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Stabilization time	tvdc	5			mS	1

Note) 1 Stabilization time is the time from switching on the operating mode until operating mode is stabilized. For example, when turning the OSC3 oscillation circuit on, stabilization time is needed after the operating mode is switched on.

8.7 Oscillation Characteristics

Oscillation characteristics change depending on conditions (board pattern, components used, etc.). Use the following characteristics as reference values. In particular, when a ceramic oscillator is used for OSC3, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance. The oscillation start time is important because it becomes the wait time when OSC3 clock is used. (If OSC3 is used as CPU clock before oscillation stabilizes, the CPU may malfunction.)

■ OSC1 (Crystal)

Unless otherwise specified: V_{DD} = Within the operating voltage in each operating mode, V_{SS} = 0 V, Ta = 25°C,
Crystal oscillator = Q12C2*, C_{G1} = 25 pF, C_{D1} = Built-in

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				3	S	
External gate capacitance	C_{G1}	Including board capacitance	5		25	pF	1
Built-in gate capacitance	C_{G1}	In case of the chip		17		pF	2
Built-in drain capacitance	C_{D1}	In case of the chip		10		pF	
Frequency/IC deviation	∂f/∂IC	V_{DD} = constant	-10		10	ppm	
Frequency/power voltage deviation	∂f/∂V				1	ppm/V	
Frequency adjustment range	∂f/∂C_G	V_{DD} = constant, C_G = 5 to 25pF	25			ppm	

* Q12C2 Made by Seiko Epson corporation

Note) 1 When crystal oscillation is selected by the mask option.
2 When crystal oscillation (gate capacitor built-in) is selected by the mask option.

■ OSC1 (CR)

Unless otherwise specified: V_{DD} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				100	µS	
Frequency/IC deviation	∂f/∂IC	R_{CR} = constant	-25		25	%	

■ OSC3 (Crystal)

Unless otherwise specified: V_{DD} = Within the operating voltage in each operating mode, V_{SS} = 0 V, Ta = 25°C,
Crystal oscillator = Q21CA301xxx*, R_F = 1MΩ, C_{G2} = C_{D2} = 15pF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time (Normal mode)	tsta	4.0 MHz crystal oscillator			10	mS	1
Oscillation start time (High speed mode)	tsta	8.0 MHz crystal oscillator			10	mS	1

* Q21CA301xxx Made by Seiko Epson corporation

Note) 1 The crystal oscillation start time changes by the crystal oscillator to be used, C_{G2} and C_{D2}.

■ OSC3 (Ceramic)

Unless otherwise specified: V_{DD} = Within the operating voltage in each operating mode, V_{SS} = 0 V, Ta = 25°C,
Ceramic oscillator = CSA4.00MG / CSA8.00MTZ*, R_F = 1MΩ, C_{G2} = C_{D2} = 30pF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time (Normal mode)	tsta	4.0 MHz ceramic oscillator			1	mS	1
Oscillation start time (High speed mode)	tsta	8.0 MHz ceramic oscillator			1	mS	1

* CSA4.00MG / CSA8.00MTZ Made by Murata Mfg. corporation

Note) 1 The ceramic oscillation start time changes by the ceramic oscillator to be used, C_{G2} and C_{D2}.

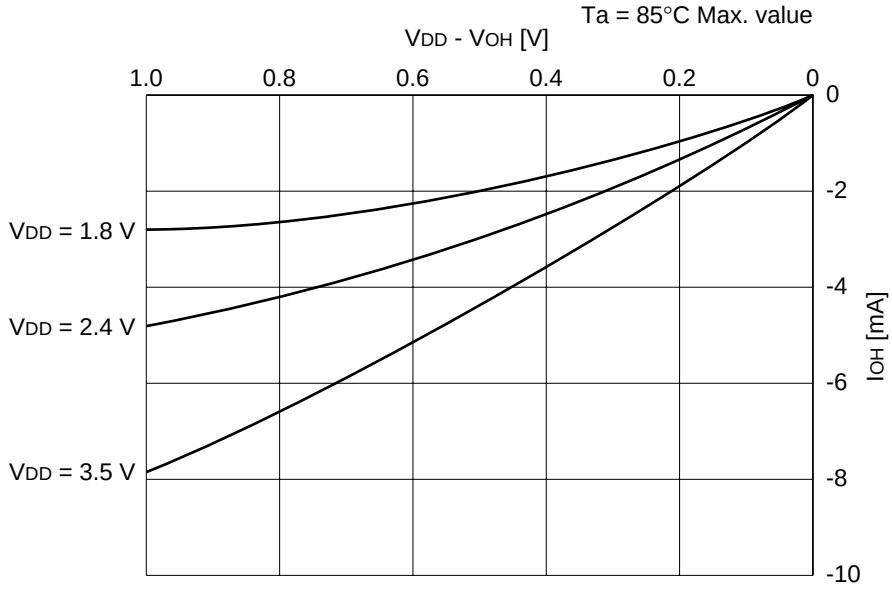
■ OSC3 (CR)

Unless otherwise specified: V_{DD} = Within the operating voltage in each operating mode, V_{SS} = 0 V, Ta = 25°C

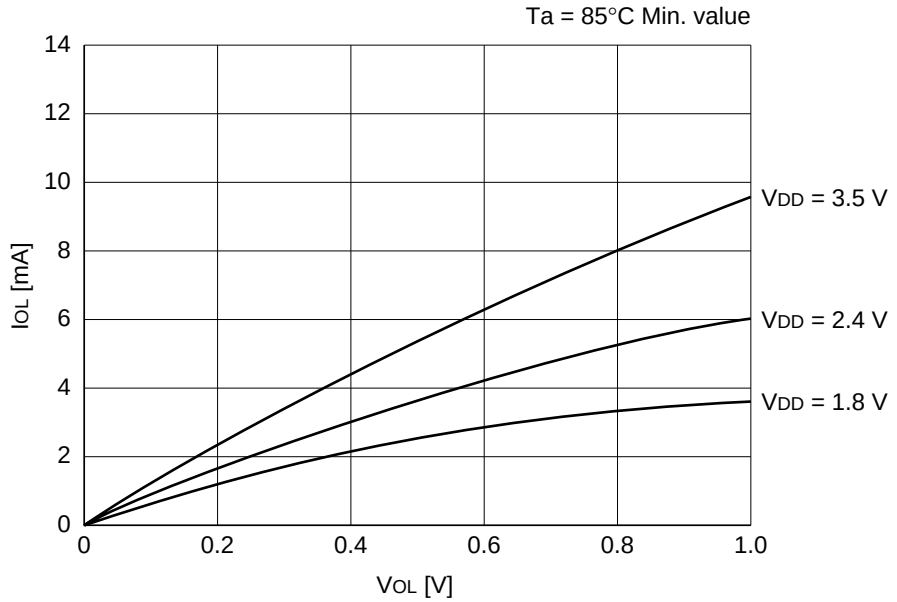
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time (Normal mode)	tsta				100	µS	
Oscillation start time (High speed mode)	tsta				100	µS	
Frequency/IC deviation (Normal mode)	∂f/∂IC	R_{CR} = constant	-25		25	%	
Frequency/IC deviation (High speed mode)	∂f/∂IC	R_{CR} = constant	-25		25	%	

8.8 Characteristics Curves (reference value)

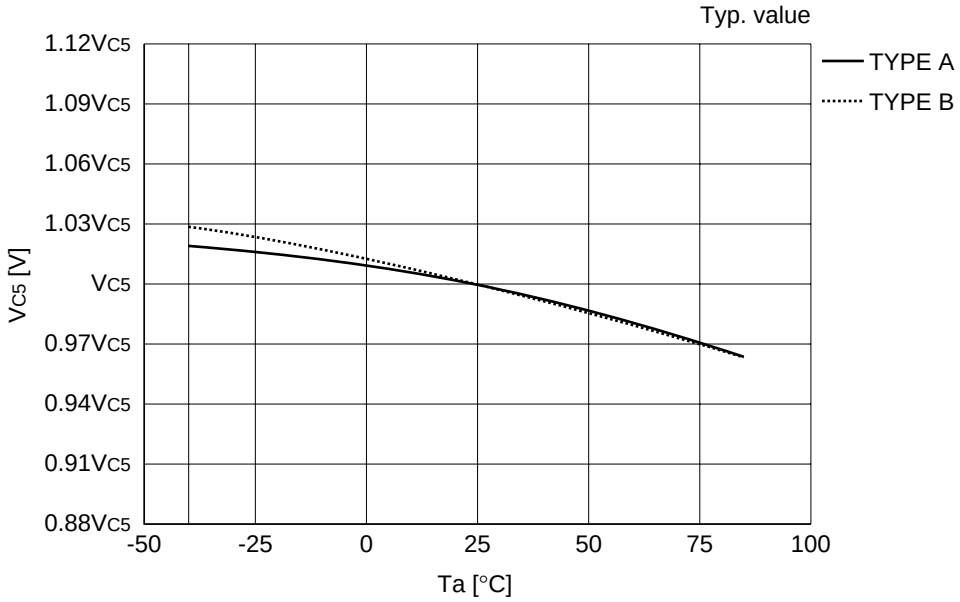
■ **High level output current-voltage characteristic**



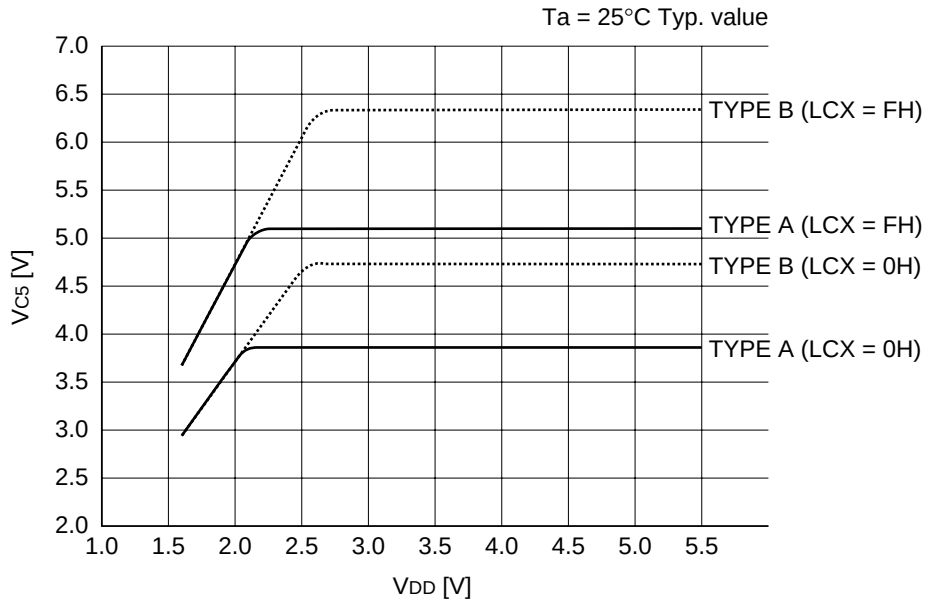
■ **Low level output current-voltage characteristic**



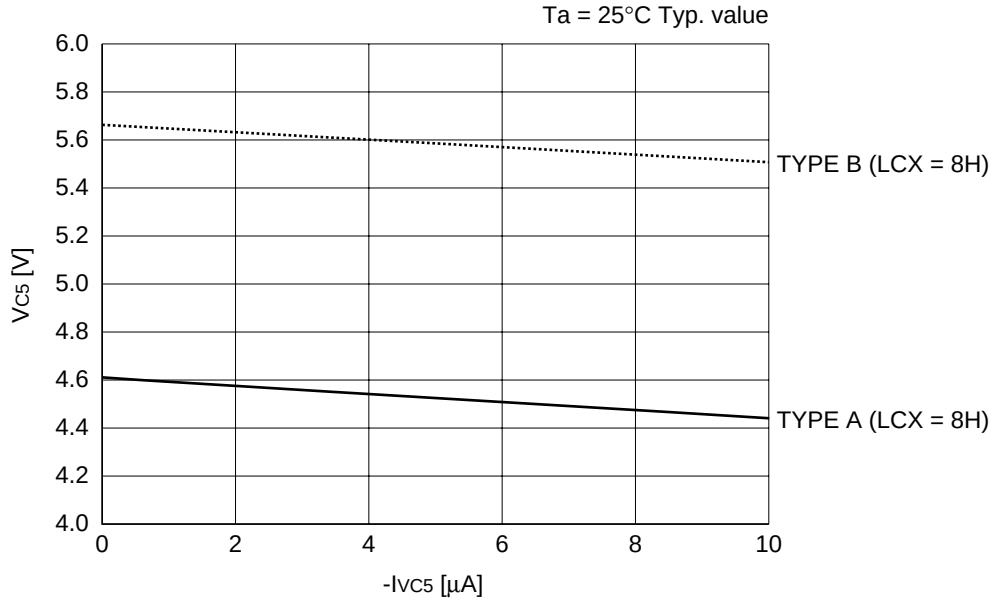
■ LCD drive voltage-ambient temperature characteristic



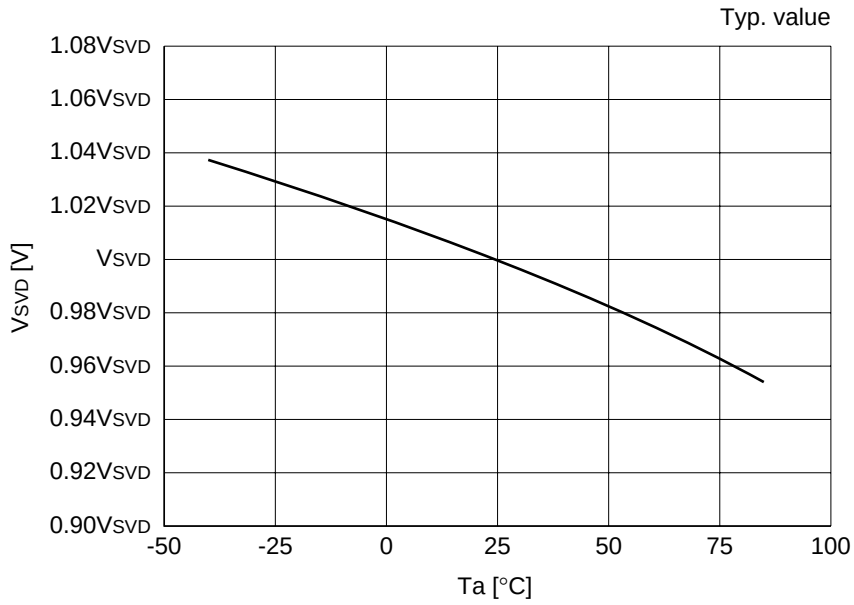
■ LCD drive voltage-supply voltage characteristic



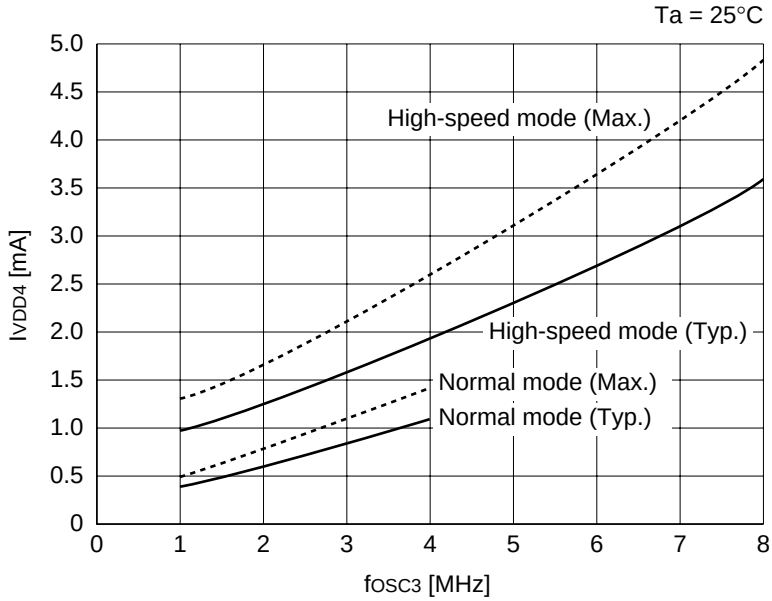
■ LCD drive voltage-load characteristic



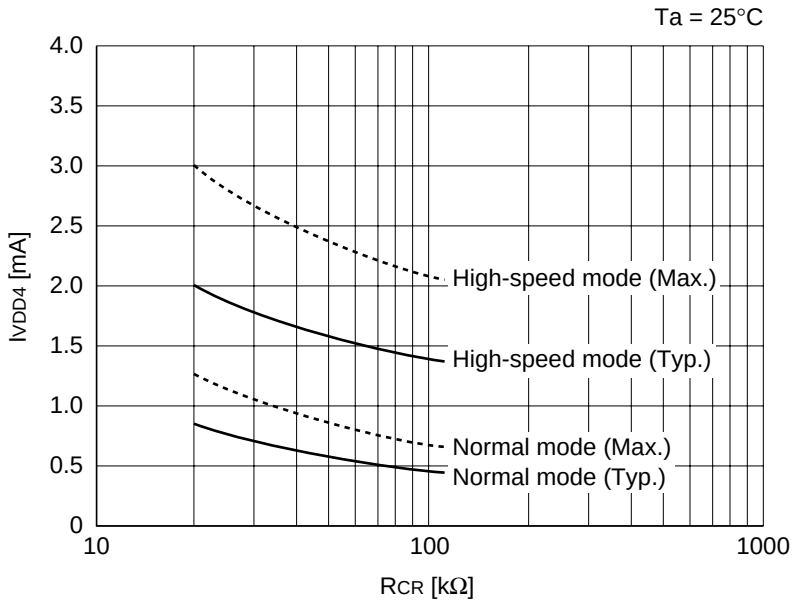
■ SVD voltage-ambient temperature characteristic



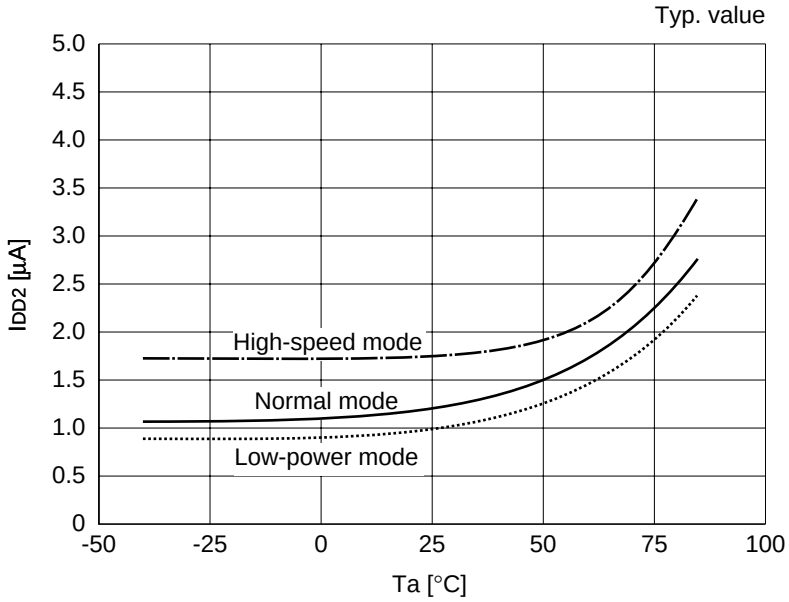
■ Power current (During operation with OSC3) <Crystal/ceramic oscillation>



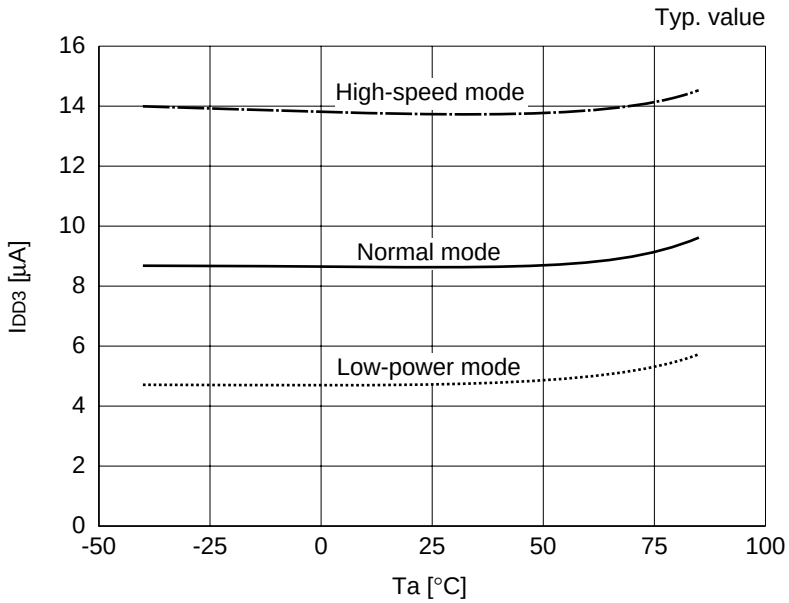
■ Power current (During operation with OSC3) <CR oscillation>



■ **Power current-ambient temperature characteristic (In HALT status)**



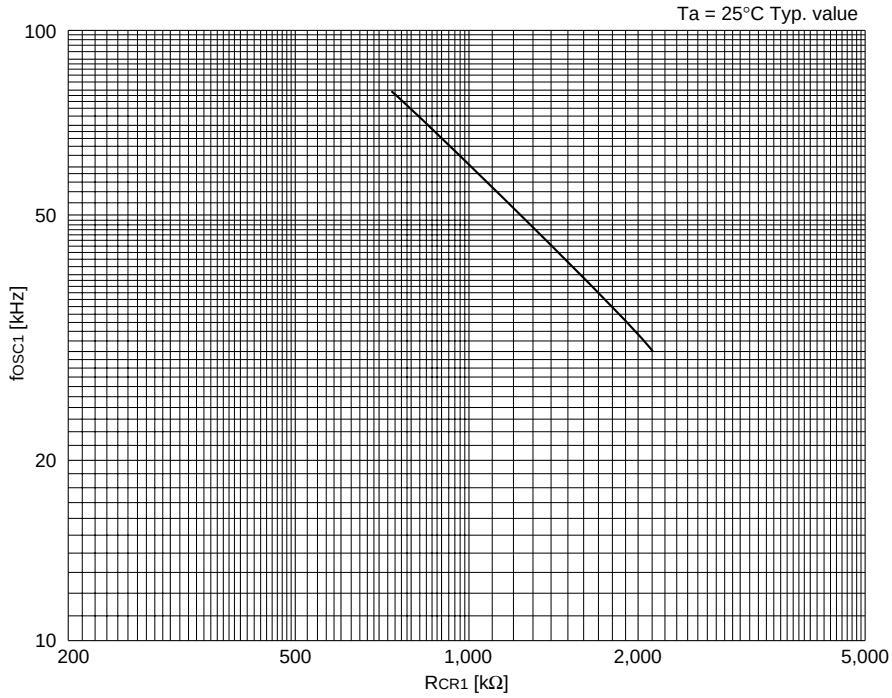
■ **Power current-ambient temperature characteristic (CPU is under 32.768 kHz operation)**



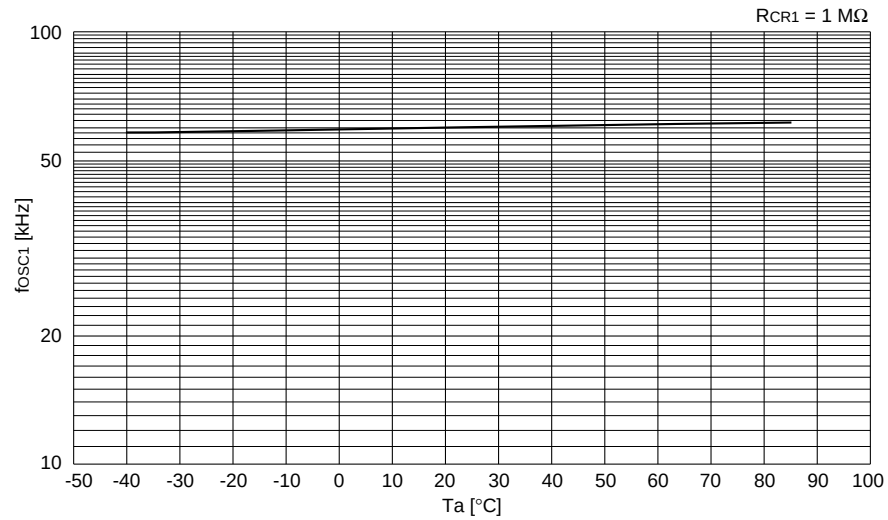
■ CR oscillation frequency characteristic

Note: Oscillation frequency changes depending on the conditions (components used, board pattern, etc.). In particular, the OSC3 oscillation frequency changes extensively depending on the product form (chip, plastic package or ceramic package) and board capacitance. Therefore, use the following charts for reference only and select the resistance value after evaluating the actual product. (The resistance value should be set to $R_{CR} \geq 15$ kΩ.)

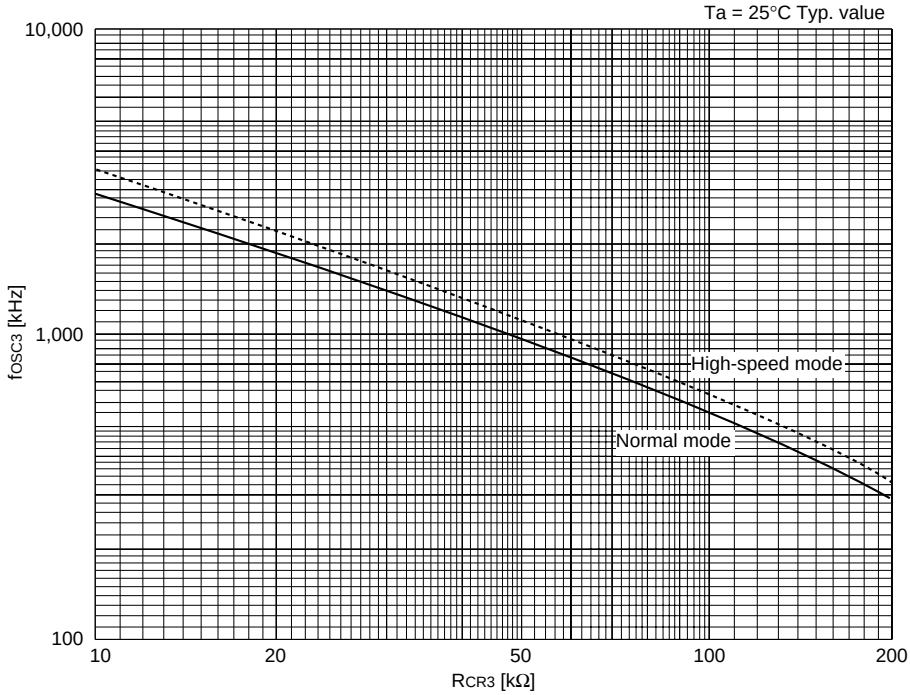
• OSC1 oscillation frequency-resistor characteristic



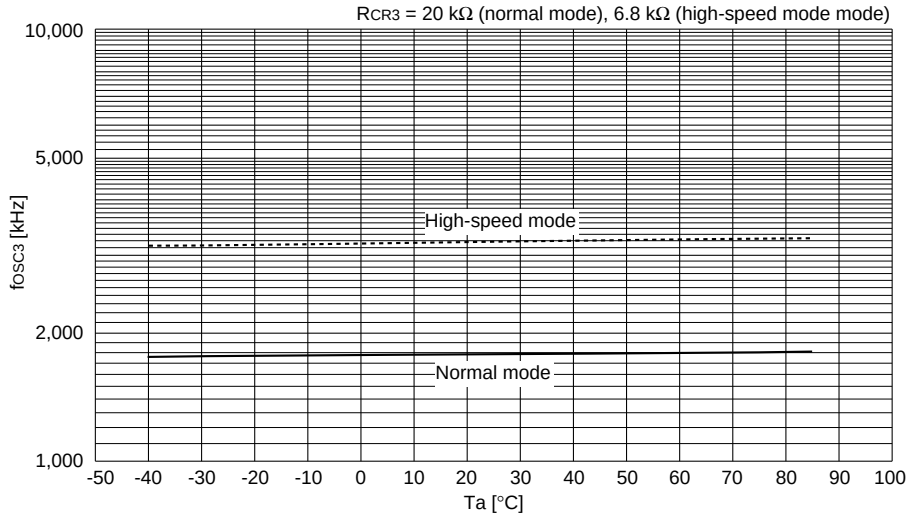
• OSC1 CR oscillation frequenc-ambient temperature characteristic



- **OSC3 oscillation frequency-resistor characteristic**



- **OSC3 CR oscillation frequenc-ambient temperature characteristic**

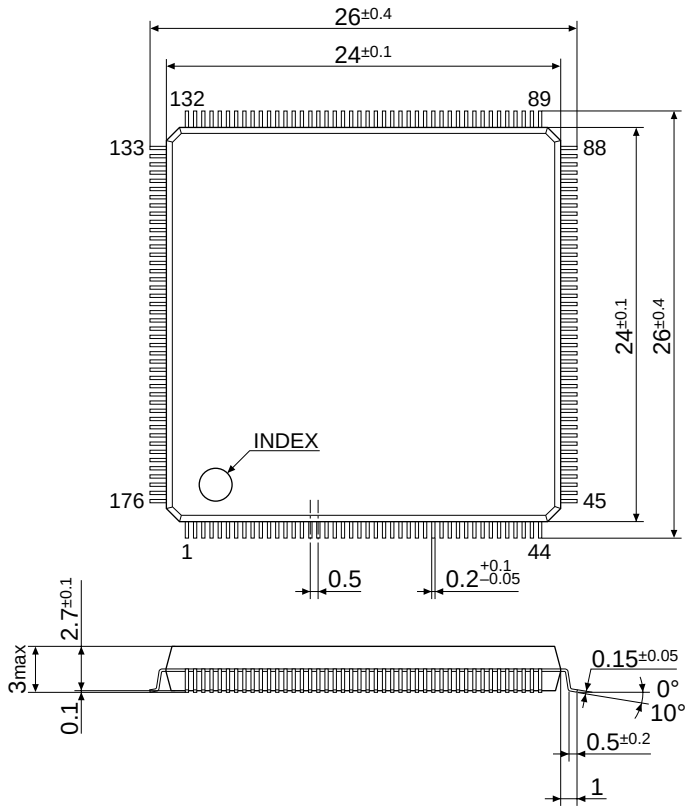


9 PACKAGE

9.1 Plastic Package

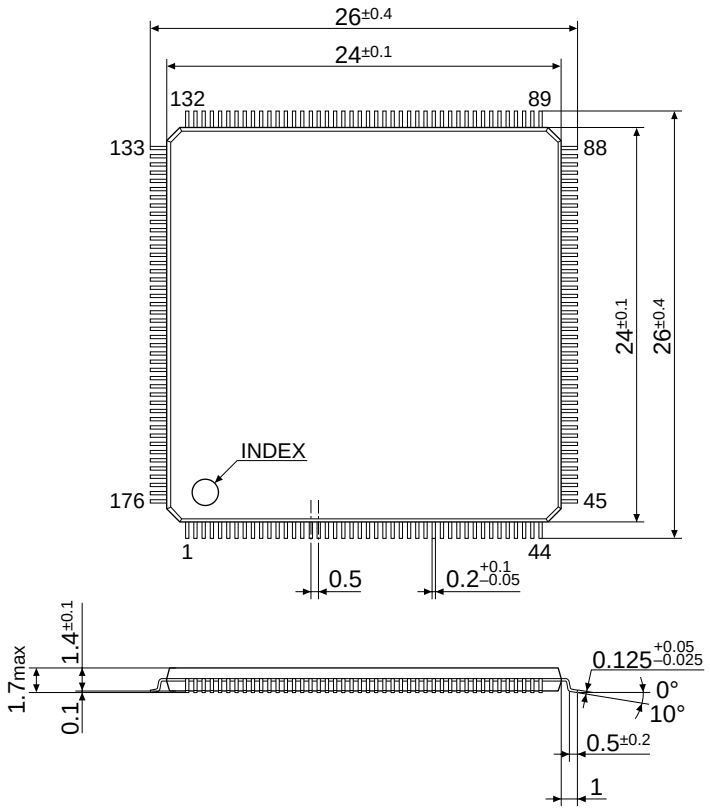
QFP18-176pin

(Unit: mm)



QFP21-176pin

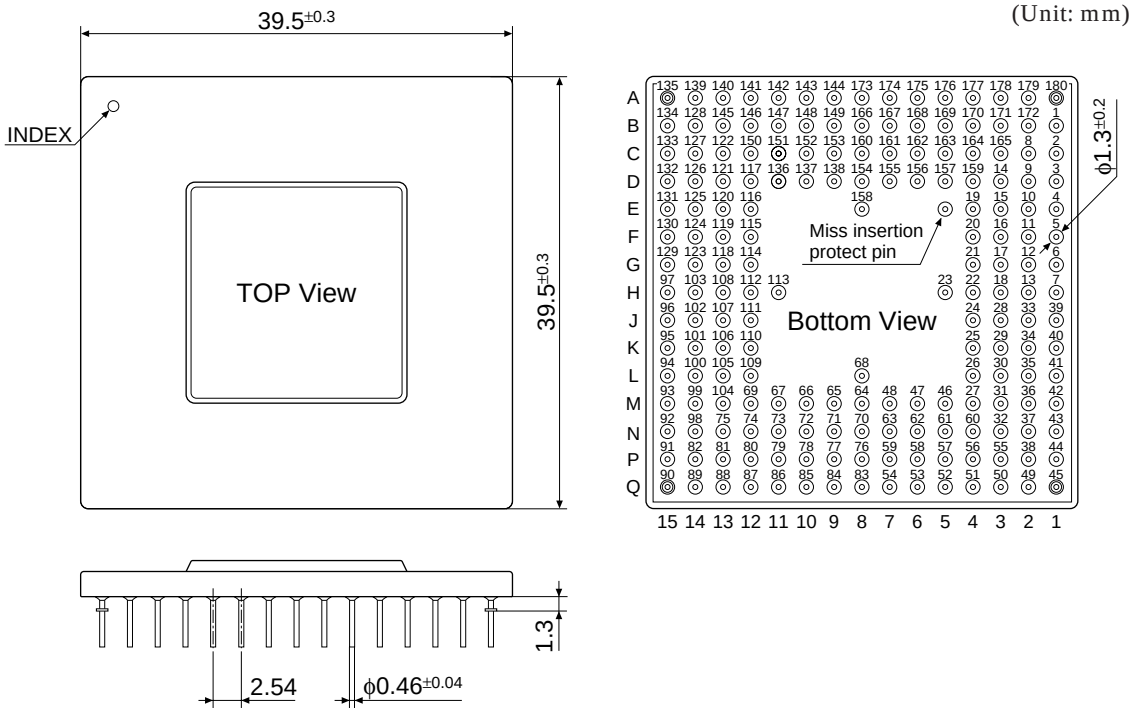
(Unit: mm)



9.2 Ceramic Package for Test Samples

PGA-181pin

(Unit: mm)

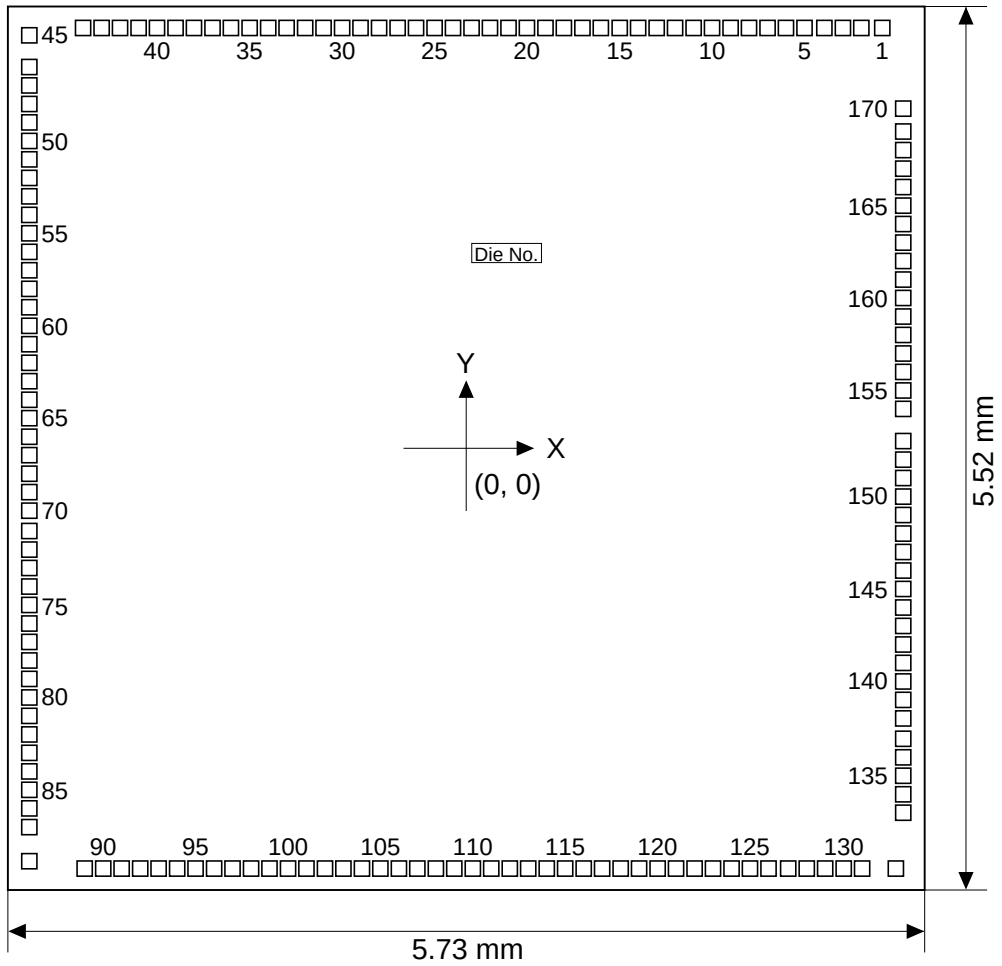


Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	N.C.	37	SEG37	73	CD	109	P14/CMPP0/AD4	145	R22/A18
2	SEG2	38	SEG38	74	CC	110	P13/$\overline{\text{SRDY}}$	146	R23/$\overline{\text{RD}}$
3	SEG3	39	SEG39	75	CB	111	P12/$\overline{\text{SCLK}}$	147	R24/$\overline{\text{WR}}$
4	SEG4	40	SEG40	76	CA	112	P11/SOUT	148	R25/CL
5	SEG5	41	SEG41	77	V_{C5}	113	P10/SIN	149	R26/FR
6	SEG6	42	SEG42	78	V_{C4}	114	AV_{DD}	150	R27/TOUT
7	SEG7	43	SEG43	79	V_{C3}	115	AV_{SS}	151	R30/$\overline{\text{CE0}}$
8	SEG8	44	SEG44	80	V_{C2}	116	AV_{REF}	152	R31/$\overline{\text{CE1}}$
9	SEG9	45	SEG45	81	V_{C1}	117	V_{DD}	153	R32/$\overline{\text{CE2}}$
10	SEG10	46	N.C.	82	OSC3	118	P07/D7	154	R33/$\overline{\text{CE3}}$
11	SEG11	47	N.C.	83	OSC4	119	P06/D6	155	R34/FOUT
12	SEG12	48	N.C.	84	V_{D1}	120	P05/D5	156	R35
13	SEG13	49	N.C.	85	V_{DD}	121	P04/D4	157	R36
14	SEG14	50	SEG46	86	V_{SS}	122	P03/D3	158	R37
15	SEG15	51	SEG47	87	V_{OSC}	123	P02/D2	159	V_{SS}
16	SEG16	52	SEG48	88	N.C.	124	P01/D1	160	R50/$\overline{\text{BZ}}$
17	SEG17	53	SEG49	89	N.C.	125	P00/D0	161	R51/$\overline{\text{BACK}}$
18	SEG18	54	SEG50	90	N.C.	126	R00/A0	162	COM0
19	SEG19	55	COM31/SEG51	91	OSC1	127	R01/A1	163	COM1
20	SEG20	56	COM30/SEG52	92	$\overline{\text{OSC2}}$	128	R02/A2	164	COM2
21	SEG21	57	COM29/SEG53	93	$\overline{\text{TEST}}$	129	R03/A3	165	COM3
22	SEG22	58	COM28/SEG54	94	$\overline{\text{RESET}}$	130	R04/A4	166	COM4
23	SEG23	59	COM27/SEG55	95	MCU/$\overline{\text{MPU}}$	131	R05/A5	167	COM5
24	SEG24	60	COM26/SEG56	96	K11/$\overline{\text{BREQ}}$	132	R06/A6	168	COM6
25	SEG25	61	COM25/SEG57	97	K10/EVIN	133	R07/A7	169	COM7
26	SEG26	62	COM24/SEG58	98	K07	134	R10/A8	170	COM8
27	SEG27	63	COM23/SEG59	99	K06	135	N.C.	171	COM9
28	SEG28	64	COM22/SEG60	100	K05	136	R11/A9	172	COM10
29	SEG29	65	COM21/SEG61	101	K04	137	R12/A10	173	COM11
30	SEG30	66	COM20/SEG62	102	K03	138	R13/A11	174	COM12
31	SEG31	67	COM19/SEG63	103	K02	139	R14/A12	175	COM13
32	SEG32	68	COM18/SEG64	104	K01	140	R15/A13	176	COM14
33	SEG33	69	COM17/SEG65	105	K00	141	R16/A14	177	COM15
34	SEG34	70	COM16/SEG66	106	P17/CMPM1/AD7	142	R17/A15	178	SEG0
35	SEG35	71	V_{REF}	107	P16/CMPP1/AD6	143	R20/A16	179	SEG1
36	SEG36	72	CE	108	P15/CMPM0/AD5	144	R21/A17	180	N.C.

N.C.: No Connection

10 PAD LAYOUT

10.1 Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 100 µm

10.2 Pad Coordinates

Table 10.2.1 Pad coordinates

(Unit: μm)

Pad		Coordinates		Pad		Coordinates		Pad		Coordinates	
No.	Name	X	Y	No.	Name	X	Y	No.	Name	x	Y
1	OSC1	2,600	2,626	58	R26/FR/$\overline{\text{TOUT}}$	-2,731	996	115	SEG28	618	-2,626
2	OSC2	2,469	2,626	59	R27/TOUT	-2,731	881	116	SEG29	734	-2,626
3	$\overline{\text{TEST}}$	2,354	2,626	60	R30/$\overline{\text{CE0}}$	-2,731	765	117	SEG30	849	-2,626
4	$\overline{\text{RESET}}$	2,238	2,626	61	R31/$\overline{\text{CE1}}$	-2,731	650	118	SEG31	965	-2,626
5	MCU/$\overline{\text{MPU}}$	2,114	2,626	62	R32/$\overline{\text{CE2}}$	-2,731	534	119	SEG32	1,080	-2,626
6	K11/BREQ	1,998	2,626	63	R33/$\overline{\text{CE3}}$	-2,731	419	120	SEG33	1,196	-2,626
7	K10/EVIN	1,883	2,626	64	R34/FOUT	-2,731	303	121	SEG34	1,311	-2,626
8	K07	1,767	2,626	65	R35	-2,731	188	122	SEG35	1,427	-2,626
9	K06	1,652	2,626	66	R36	-2,731	72	123	SEG36	1,542	-2,626
10	K05	1,536	2,626	67	R37	-2,731	-43	124	SEG37	1,658	-2,626
11	K04	1,421	2,626	68	V_{SS}	-2,731	-159	125	SEG38	1,773	-2,626
12	K03	1,305	2,626	69	R50/BZ	-2,731	-274	126	SEG39	1,889	-2,626
13	K02	1,190	2,626	70	R51/$\overline{\text{BACK}}$/$\overline{\text{BZ}}$	-2,731	-390	127	SEG40	2,012	-2,626
14	K01	1,074	2,626	71	COM0	-2,731	-517	128	SEG41	2,128	-2,626
15	K00	959	2,626	72	COM1	-2,731	-633	129	SEG42	2,243	-2,626
16	P17/CMPM1/AD7	841	2,626	73	COM2	-2,731	-748	130	SEG43	2,359	-2,626
17	P16/CMPP1/AD6	726	2,626	74	COM3	-2,731	-864	131	SEG44	2,474	-2,626
18	P15/CMPM0/AD5	610	2,626	75	COM4	-2,731	-979	132	SEG45	2,685	-2,626
19	P14/CMPP0/AD4	495	2,626	76	COM5	-2,731	-1,095	133	SEG46	2,731	-2,277
20	P13/$\overline{\text{SRDY}}$	379	2,626	77	COM6	-2,731	-1,210	134	SEG47	2,731	-2,162
21	P12/$\overline{\text{SCLK}}$	264	2,626	78	COM7	-2,731	-1,326	135	SEG48	2,731	-2,046
22	P11/SOUT	148	2,626	79	COM8	-2,731	-1,441	136	SEG49	2,731	-1,931
23	P10/SIN	33	2,626	80	COM9	-2,731	-1,557	137	SEG50	2,731	-1,815
24	AV_{DD}	-83	2,626	81	COM10	-2,731	-1,672	138	COM31/SEG51	2,731	-1,688
25	AV_{SS}	-198	2,626	82	COM11	-2,731	-1,788	139	COM30/SEG52	2,731	-1,572
26	AV_{REF}	-314	2,626	83	COM12	-2,731	-1,903	140	COM29/SEG53	2,731	-1,457
27	V_{DD}	-429	2,626	84	COM13	-2,731	-2,019	141	COM28/SEG54	2,731	-1,341
28	P07/D7	-545	2,626	85	COM14	-2,731	-2,134	142	COM27/SEG55	2,731	-1,226
29	P06/D6	-661	2,626	86	COM15	-2,731	-2,250	143	COM26/SEG56	2,731	-1,110
30	P05/D5	-776	2,626	87	SEG0	-2,731	-2,367	144	COM25/SEG57	2,731	-995
31	P04/D4	-892	2,626	88	SEG1	-2,731	-2,580	145	COM24/SEG58	2,731	-879
32	P03/D3	-1,007	2,626	89	SEG2	-2,385	-2,626	146	COM23/SEG59	2,731	-764
33	P02/D2	-1,123	2,626	90	SEG3	-2,269	-2,626	147	COM22/SEG60	2,731	-648
34	P01/D1	-1,238	2,626	91	SEG4	-2,154	-2,626	148	COM21/SEG61	2,731	-533
35	P00/D0	-1,354	2,626	92	SEG5	-2,038	-2,626	149	COM20/SEG62	2,731	-417
36	R00/A0	-1,471	2,626	93	SEG6	-1,923	-2,626	150	COM19/SEG63	2,731	-302
37	R01/A1	-1,586	2,626	94	SEG7	-1,807	-2,626	151	COM18/SEG64	2,731	-186
38	R02/A2	-1,702	2,626	95	SEG8	-1,692	-2,626	152	COM17/SEG65	2,731	-71
39	R03/A3	-1,817	2,626	96	SEG9	-1,576	-2,626	153	COM16/SEG66	2,731	45
40	R04/A4	-1,933	2,626	97	SEG10	-1,461	-2,626	154	V_{REF}	2,731	246
41	R05/A5	-2,048	2,626	98	SEG11	-1,345	-2,626	155	CE	2,731	361
42	R06/A6	-2,164	2,626	99	SEG12	-1,230	-2,626	156	CD	2,731	477
43	R07/A7	-2,279	2,626	100	SEG13	-1,114	-2,626	157	CC	2,731	592
44	R10/A8	-2,395	2,626	101	SEG14	-999	-2,626	158	CB	2,731	708
45	R11/A9	-2,731	2,580	102	SEG15	-883	-2,626	159	CA	2,731	823
46	R12/A10	-2,731	2,382	103	SEG16	-768	-2,626	160	V_{C5}	2,731	939
47	R13/A11	-2,731	2,267	104	SEG17	-652	-2,626	161	V_{C4}	2,731	1,054
48	R14/A12	-2,731	2,151	105	SEG18	-537	-2,626	162	V_{C3}	2,731	1,170
49	R15/A13	-2,731	2,036	106	SEG19	-421	-2,626	163	V_{C2}	2,731	1,285
50	R16/A14	-2,731	1,920	107	SEG20	-306	-2,626	164	V_{C1}	2,731	1,401
51	R17/A15	-2,731	1,805	108	SEG21	-190	-2,626	165	OSC3	2,731	1,516
52	R20/A16	-2,731	1,689	109	SEG22	-75	-2,626	166	OSC4	2,731	1,632
53	R21/A17	-2,731	1,574	110	SEG23	41	-2,626	167	V_{D1}	2,731	1,747
54	R22/A18	-2,731	1,458	111	SEG24	156	-2,626	168	V_{DD}	2,731	1,863
55	R23/$\overline{\text{RD}}$	-2,731	1,343	112	SEG25	272	-2,626	169	V_{SS}	2,731	1,979
56	R24/$\overline{\text{WR}}$	-2,731	1,227	113	SEG26	387	-2,626	170	V_{OSC}	2,731	2,212
57	R25/CL	-2,731	1,112	114	SEG27	503	-2,626	–	–	–	–

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