MF1131-02

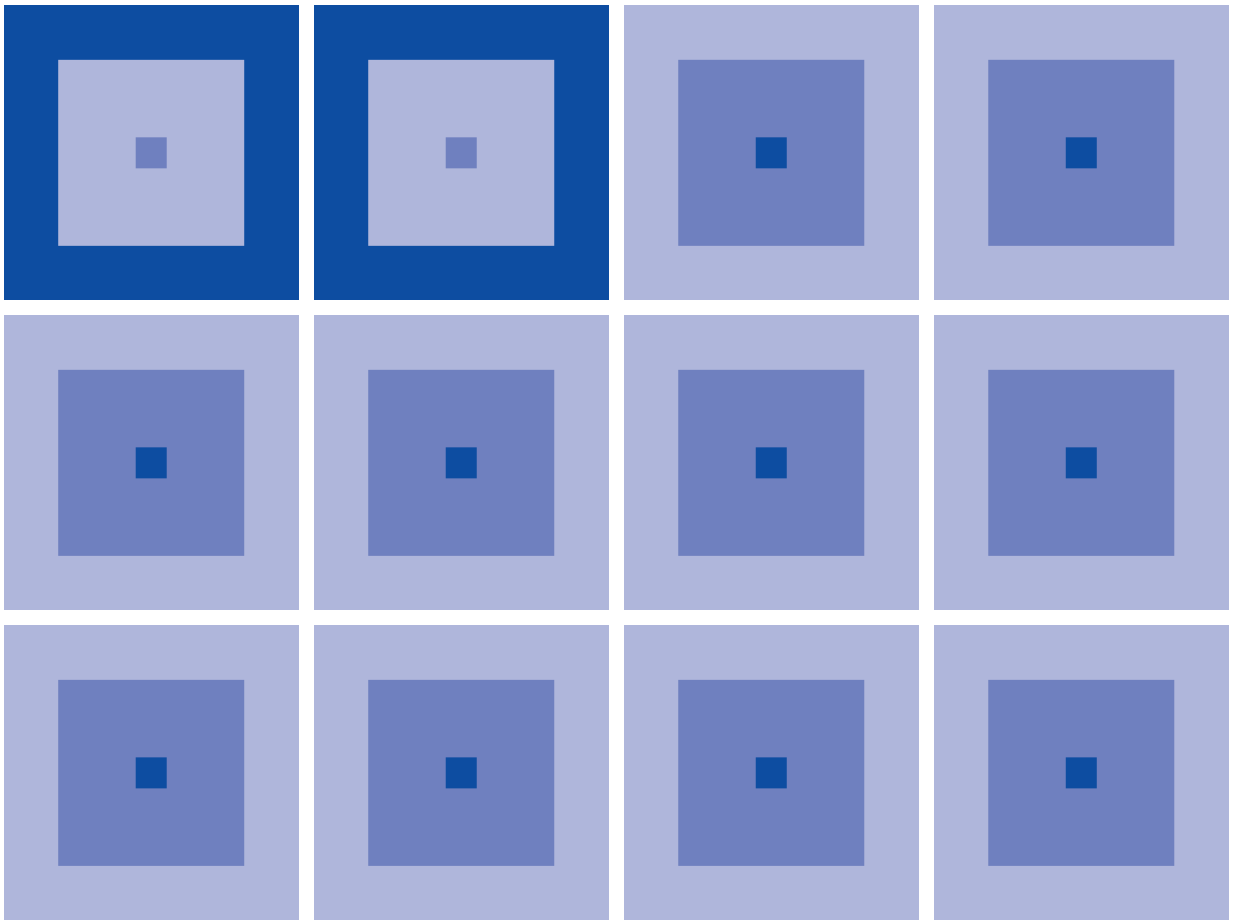
EPSON

CMOS 8-BIT SINGLE CHIP MICROCOMPUTER

S1C88408

Technical Manual

S1C88408 Technical Hardware



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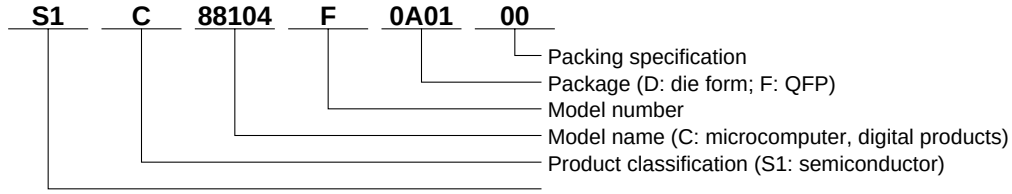
The information of the product number change

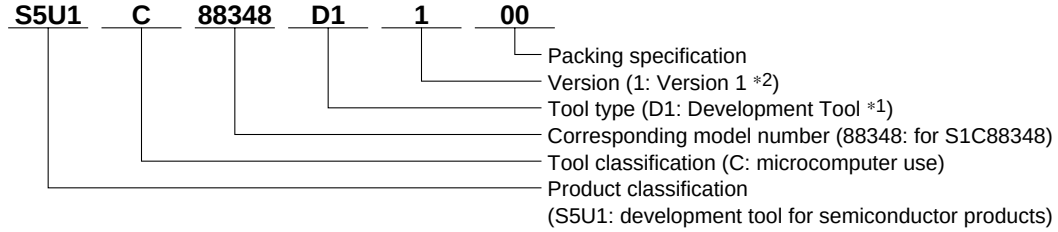
Starting April 1, 2001, the product number will be changed as listed below. To order from April 1, 2001 please use the new product number. For further information, please contact Epson sales representative.

Configuration of product number

Devices



Development tools



*1: For details about tool types, see the tables below. (In some manuals, tool types are represented by one digit.)
*2: Actual versions are not written in the manuals.

Comparison table between new and previous number

S1C88 Family processors

Previous No.	New No.
E0C88104	S1C88104
E0C88112	S1C88112
E0C88308	S1C88308
E0C88316	S1C88316
E0C88317	S1C88317
E0C88348	S1C88348
E0C88P348	S1C8P348
E0C88349	S1C88349

Previous No.	New No.
E0C88365	S1C88365
E0C88F360	S1C8F360
E0C88408	S1C88408
E0C88409	S1C88409
E0C88816	S1C88816
E0C88832	S1C88832
E0C88862	S1C88862
E0C88F816	S1C8F816

Comparison table between new and previous number of development tools

Development tools for the S1C88 Family

Previous No.	New No.
88ISAIF	S5U1C88000H4
ADP88348	S5U1C88348X
ADP88360	S5U1C88360X
DEV88104	S5U1C88104D
DEV88112	S5U1C88112D
DEV88308	S5U1C88308D
DEV88316	S5U1C88316D
DEV88317	S5U1C88317D
DEV88348	S5U1C88348D
DEV88365	S5U1C88365D
DEV88408	S5U1C88408D
DEV88409	S5U1C88409D

Previous No.	New No.
DEV88816	S5U1C88816D
DEV88832	S5U1C88832D
DEV88862	S5U1C88862D
DMT88348-DB	S5U1C88348T
ICE88UR	S5U1C88000H5
PRC88316	S5U1C88316P
PRC88348	S5U1C88348P
PRC88365	S5U1C88365P
PRC88409	S5U1C88409P
PRC88816	S5U1C88816P
SAP88	S5U1C88000S
URS88348	S5U1C88348Y

Development tools for the S1C63/88 Family

Previous No.	New No.
ADS00002	S5U1C88000X1
GWH00002	S5U1C88000W2
URM00002	S5U1C88000W1

CONTENTS

CHAPTER 1 OUTLINE

The S1C88408 is a single chip microcomputer which consists of a CMOS 8-bit core CPU S1C88 (MODEL3), 8KB ROM, 3.75KB RAM, dot-matrix LCD controller, 3 types of timers / counters, serial interface (IR input / output function is available). The S1C88408 operates faster even with low supply voltage, and is most suitable for various application equipment such as information terminals needing low power operation. Furthermore, the S1C88408 can control up to 4M × 3 bytes of memory with the 22-bit outside address bus and 3-bit chip enable signals, therefore it can also be applied to systems such as electronic dictionaries and organizers.

1.1 Features

Table 1.1.1 Features

Core CPU		CMOS 8-bit core CPU S1C88 (MODEL3)
OSC1 oscillation circuit		Crystal oscillation circuit/CR oscillation circuit/external clock input 32.768 kHz (Typ.)
OSC3 oscillation circuit		Crystal oscillation circuit/ceramic oscillation circuit/CR oscillation circuit/external clock input 8 MHz (Max.)
Instruction set		Basic instruction: 54 types, Total: 608 types (multiplication/division instructions are usable) Addressing mode: 12 types
Min. instruction execution time		0.25 µsec/8 MHz (2 clocks)
Internal ROM capacity		8K bytes
Internal RAM capacity		3.75K bytes (display memory is included; data/display memory size can be set by mask option)
Bus line		Address bus: 22 bits Data bus: 8 bits $\overline{CE}$ signal: 3 bits $\overline{WR}$ signal: 1 bit $\overline{RD}$ signal: 1 bit (usable as general output port or I/O port when it is not used as a bus signal)
Input port		12 bits • 2 bits are usable for event counter input
Output port		30 bits • They are used as address bus and bus control signals when external bus is set • Usable for clock output and buzzer output
I/O port		28 bits • 8 bits are used as data bus when external bus is set • Usable for serial interface input/output
Serial interface		1 channel • Clock synchronous mode/asynchronous mode selectable • Usable as IrDA interface
16-bit programmable timer		1 channel • Usable for 16 bits × 1 channel or 8 bits × 2 channels • Usable as event counter
8-bit programmable timer		1 channel • Usable as baud rate generator for serial interface
Clock timer		1 channel • Generating 1 sec signal with 32 kHz oscillation • 60S counter available
LCD controller		Dot-matrix type • B&W or 4 gray scale display • A 240 × 100 dot LCD panel can be driven with external drivers (S1D16305 or S1D16700, S1D16006 or S1D15700) • Scroll function available
Sound generator		Equipped with envelope and volume control functions
Supply voltage detection (SVD)		Possible to detect 3 voltage levels
Watchdog timer		Possible to generate NMI
Address match jump		Up to 4 addresses can be specified to generate vector jumps
Interrupt		External: Input interrupt 2 systems (5 types) Internal: 16-bit programmable timer interrupt 2 systems (4 types) 8-bit programmable timer interrupt 1 system (1 type) Clock timer interrupt 1 system (5 types) Watchdog timer interrupt 1 system (1 type) Serial interface interrupt 1 system (3 types) LCD controller interrupt 1 system (1 type)
Supply voltage		1.8 V to 5.5 V (operating frequency Max. 1.1 MHz) 2.6 V to 5.5 V (operating frequency Max. 4.4 MHz) 3.5 V to 5.5 V (operating frequency Max. 8.2 MHz)
Current consumption	SLEEP	0.6 µA Typ. (at 3.0 V) (Normal mode)
	HALT (32 kHz)	3.0 µA Typ. (at 3.0 V) (Normal mode)
	Run (32 kHz)	15 µA Typ. (at 3.0 V) (Normal mode)
	Run (4 MHz)	2 mA Typ. (at 3.0 V) (Normal mode)
Supply form		QFP15-100pin or chip

1.2 Block Diagram

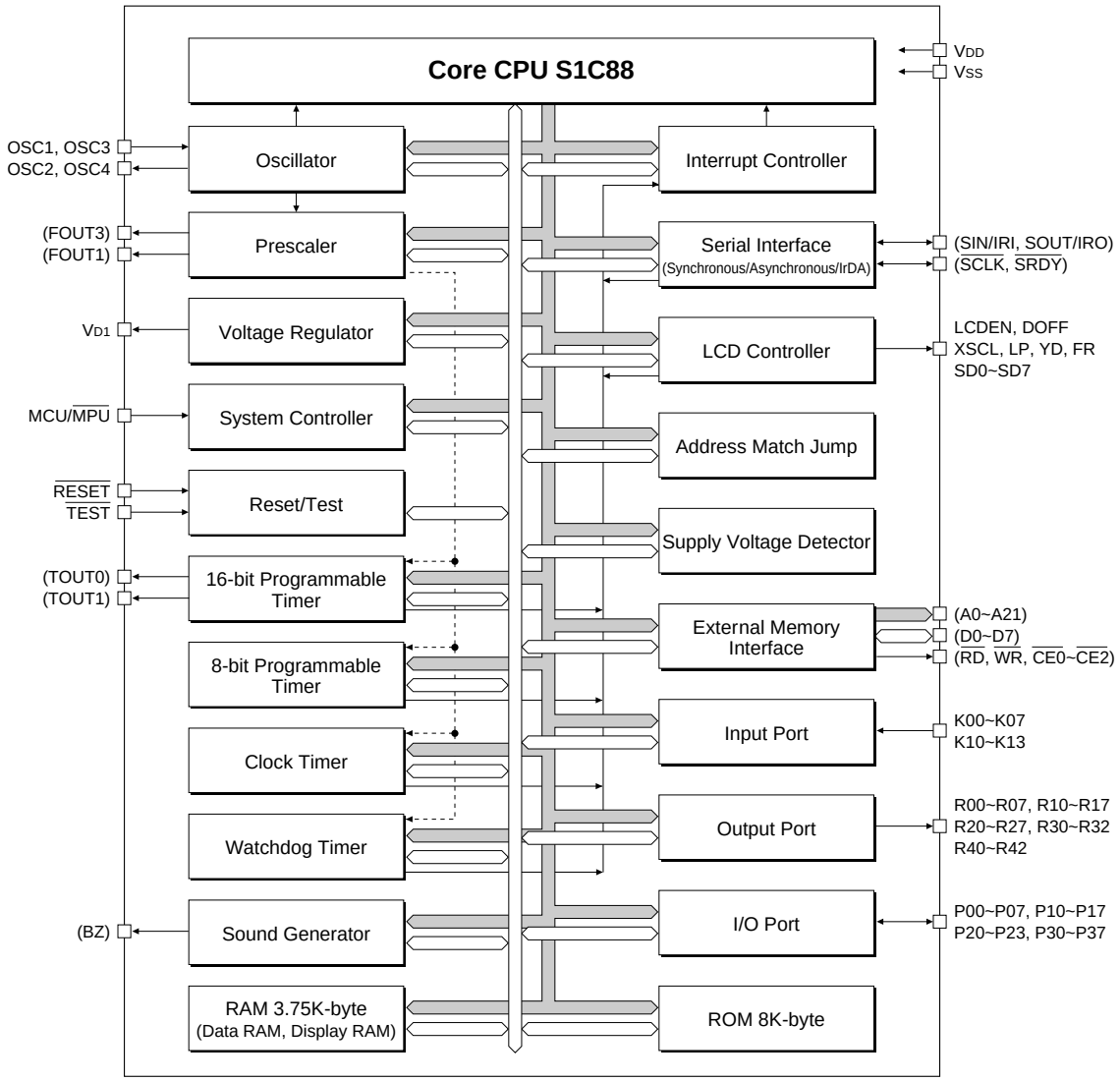


Fig. 1.2.1 S1C88408 block diagram

∗ The terminals that are shown in ( ) are shared with Pxx or Rxx terminals.

1.3 System Configuration

System configuration of the S1C88408 is classified in 2 types according to use.

1) Single-chip system
2) Multi-chip system

To construct these systems, the S1C88408 has been designed to switch the bus mode (configuration of the external bus) by software and / or mask option.

1.3.1 Single-chip system

The single-chip system has the smallest configuration that uses the S1C88408 as the CPU of the system and does not expand any memory and devices outside. It is suitable for various controller systems.

Since it does not use an external bus, the bus mode of the S1C88408 should be set to the MCU / single-chip mode (see Section 3.5). (Initial setting)
The memory that can be used is limited to the built-in area.

ROM ...8KB
RAM ...3.75KB (display memory is included)

The I / O ports shared with the external bus can be used entirely as general-purpose I / O ports.

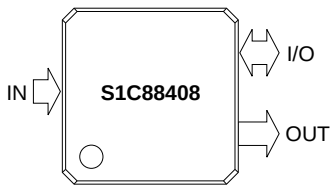


Fig. 1.3.1.1 Configuration of single-chip system

1.3.2 Multi-chip system

With the S1C88408 as the CPU, the multi-chip system has expanded memory as well as other expanded devices. It covers a wide range of applications. Memory and devices are connected to the external bus of the S1C88408 and are all controlled by the S1C88408.
The bus mode of the S1C88408 can be set to the expanded mode (see Section 3.5) according to scale of the system.

MCU or MPU* / Expanded 64K mode
For systems with 64KB or less expanded memory

MCU or MPU* / Expanded 4M minimum mode
For systems with 64KB to 12MB (4M × 3) expanded memory (However, program memory is 64KB or less)

MCU or MPU* / Expanded 4M maximum mode
For systems with 64KB to 12MB (4M × 3) expanded memory (For systems that require 64KB or more program memory)

* The MCU mode is set when the internal ROM is used, and the MPU mode is set when the internal ROM is not used.

Refer to Section 3.6, "External Bus", for the bus configuration.

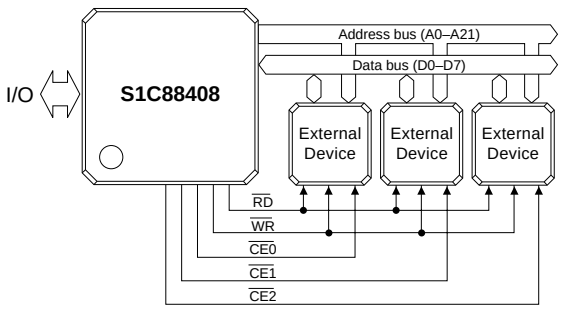


Fig. 1.3.2.1 Configuration of multi-chip system

1.4 Pin Layout Diagram

• Pin layout for single chip mode (initial setting)

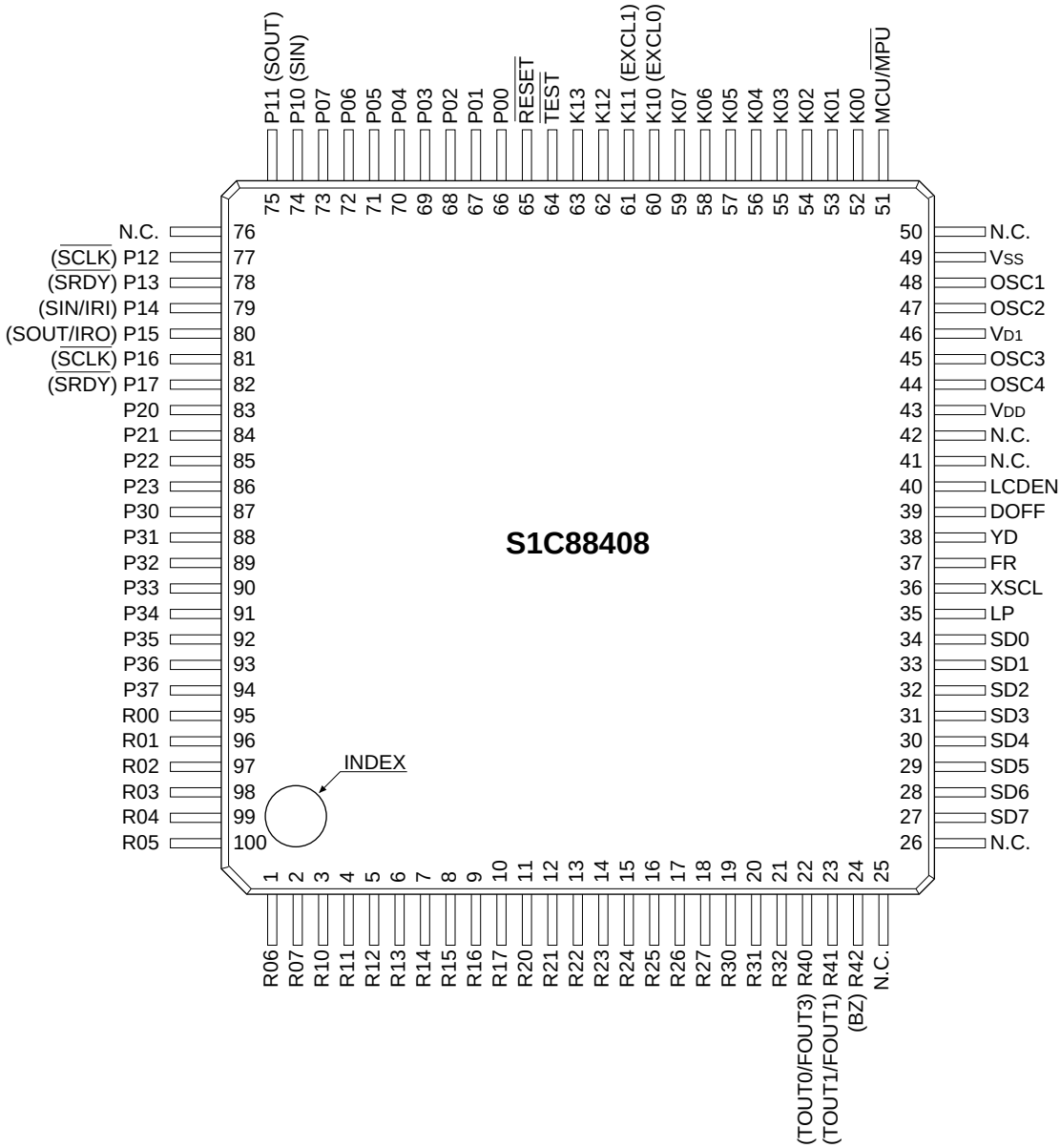


Fig. 1.4.1 S1C88408 pin layout (single chip mode)

Table 1.4.1 S1C88408 pin description (single chip mode)

Pin name	Pin No.	I/O	Function
VDD	43	–	Power supply (+) pin
VSS	49	–	Power supply (GND) pin
VD1	46	O	Voltage regulator output pin
OSC1	48	I	OSC1 oscillation input pin (32 kHz crystal, CR oscillation, external clock input)
OSC2	47	O	OSC1 oscillation output pin
OSC3	45	I	OSC3 oscillation input pin (crystal/ceramic, CR oscillation, external clock input)
OSC4	44	O	OSC3 oscillation output pin
MCU/$\overline{\text{MPU}}$	51	I	MCU/MPU mode stting pin*1
K00–K07	52–59	I	Input port pin
K10 (EXCL00)	60	I	Input port pin or external clock input pin for event counter (Timer 0)
K11 (EXCL01)	61	I	Input port pin or external clock input pin for event counter (Timer 1)
K12–K13	62–63	I	Input port pin
R00–R07	95–100, 1,2	O	Output port pin
R10–R17	3–10	O	Output port pin
R20–R27	11–18	O	Output port pin
R30–R32	19–21	O	Output port pin
R40 (TOUT0/FOUT3)	22	O	Output port pin or TOUT0/FOUT3 clock output pin
R41 (TOUT1/FOUT1)	23	O	Output port pin or TOUT1/FOUT1 clock output pin
R42 (BZ)	24	O	Output port pin or buzzer signal output pin
P00–P07	66–73	I/O	I/O port pin
P10 (SIN)	74	I/O	I/O port pin or serial I/F data input pin
P11 (SOUT)	75	I/O	I/O port pin or serial I/F data output pin
P12 ($\overline{\text{SCLK}}$)	77	I/O	I/O port pin or serial I/F clock input/output pin
P13 ($\overline{\text{SRDY}}$)	78	I/O	I/O port pin or serial I/F ready signal output pin
P14 (SIN/IRI)	79	I/O	I/O port pin, serial I/F data input or IR receiver input pin
P15 (SOUT/IRO)	80	I/O	I/O port pin, serial I/F data output or IR transmitter output pin
P16 ($\overline{\text{SCLK}}$)	81	I/O	I/O port pin or serial I/F clock input/output pin
P17 ($\overline{\text{SRDY}}$)	82	I/O	I/O port pin or serial I/F ready signal output pin
P20–P23	83–86	I/O	I/O port pin
P30–P37	87–94	I/O	I/O port pin
LCDEN	40	O	LCD controller enable signal output pin
DOFF	39	O	LCD controller forced blank signal output pin
YD	38	O	LCD controller scan start pulse output pin
FR	37	O	LCD controller frame signal output pin
XSCL	36	O	LCD controller shift clock output pin
LP	35	O	LCD controller latch pulse output pin
SD0–SD7	34–27	O	LCD controller data output pin
$\overline{\text{RESET}}$	65	I	Initial reset input pin
$\overline{\text{TEST}}$	64	I	Test input pin*2

∗1 The MCU / $\overline{\text{MPU}}$ terminal should be connected to VDD.

∗2 $\overline{\text{TEST}}$ is the terminal used for factory inspection of the IC. For normal operation, be sure to connect the $\overline{\text{TEST}}$ terminal to VDD.

• Pin layout for expanded 64K mode (for multi-chip system)

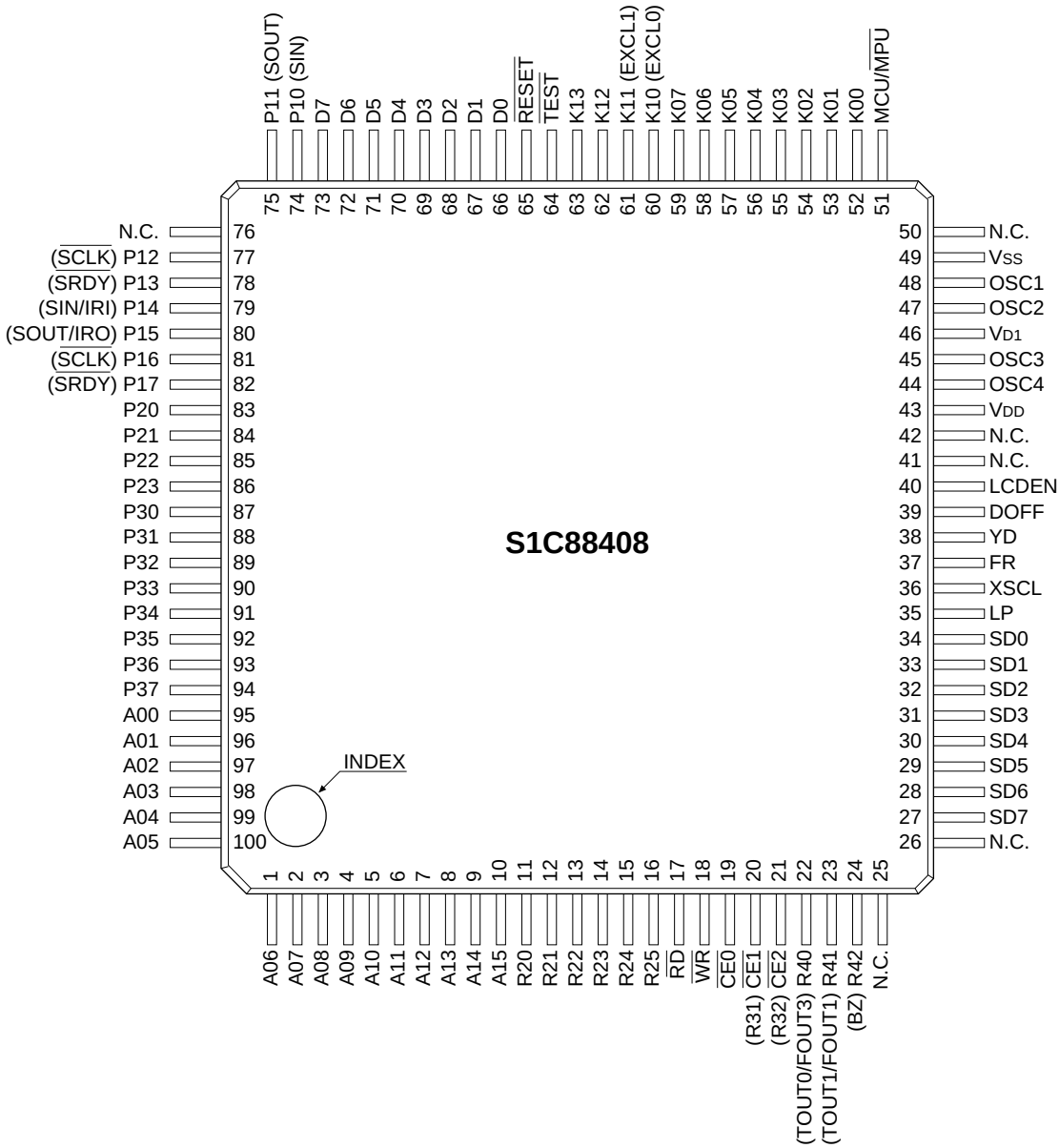


Fig. 1.4.2 S1C88408 pin layout (expanded 64K mode)

Table 1.4.2 S1C88408 pin description (expanded 64K mode)

Pin name	Pin No.	I/O	Function
VDD	43	–	Power supply (+) pin
VSS	49	–	Power supply (GND) pin
VD1	46	O	Voltage regulator output pin
OSC1	48	I	OSC1 oscillation input pin (32 kHz crystal, CR oscillation, external clock input)
OSC2	47	O	OSC1 oscillation output pin
OSC3	45	I	OSC3 oscillation input pin (crystal/ceramic, CR oscillation, external clock input)
OSC4	44	O	OSC3 oscillation output pin
MCU/$\overline{\text{MPU}}$	51	I	MCU/MPU mode stting pin
K00–K07	52–59	I	Input port pin
K10 (EXCL00)	60	I	Input port pin or external clock input pin for event counter (Timer 0)
K11 (EXCL01)	61	I	Input port pin or external clock input pin for event counter (Timer 1)
K12–K13	62–63	I	Input port pin
A00–A15	95–100, 1–10	O	Address bus
R20–R25	11–16	O	Output port pin
$\overline{\text{RD}}$	17	O	Read signal output pin
$\overline{\text{WR}}$	18	O	Write signal output pin
$\overline{\text{CE0}}$	19	O	Chip enable signal output pin
$\overline{\text{CE1}}$ (R31)	20	O	Chip enable signal output pin or output port pin
$\overline{\text{CE2}}$ (R32)	21	O	Chip enable signal output pin or output port pin
R40 (TOUT0/FOUT3)	22	O	Output port pin or TOUT0/FOUT3 clock output pin
R41 (TOUT1/FOUT1)	23	O	Output port pin or TOUT1/FOUT1 clock output pin
R42 (BZ)	24	O	Output port pin or buzzer signal output pin
D0–D7	66–73	I/O	Data bus
P10 (SIN)	74	I/O	I/O port pin or serial I/F data input pin
P11 (SOUT)	75	I/O	I/O port pin or serial I/F data output pin
P12 ($\overline{\text{SCLK}}$)	77	I/O	I/O port pin or serial I/F clock input/output pin
P13 ($\overline{\text{SRDY}}$)	78	I/O	I/O port pin or serial I/F ready signal output pin
P14 (SIN/IRI)	79	I/O	I/O port pin, serial I/F data input or IR receiver input pin
P15 (SOUT/IRO)	80	I/O	I/O port pin, serial I/F data output or IR transmitter output pin
P16 ($\overline{\text{SCLK}}$)	81	I/O	I/O port pin or serial I/F clock input/output pin
P17 ($\overline{\text{SRDY}}$)	82	I/O	I/O port pin or serial I/F ready signal output pin
P20–P23	83–86	I/O	I/O port pin
P30–P37	87–94	I/O	I/O port pin
LCDEN	40	O	LCD controller enable signal output pin
DOFF	39	O	LCD controller forced blank signal output pin
YD	38	O	LCD controller scan start pulse output pin
FR	37	O	LCD controller frame signal output pin
XSCL	36	O	LCD controller shift clock output pin
LP	35	O	LCD controller latch pulse output pin
SD0–SD7	34–27	O	LCD controller data output pin
$\overline{\text{RESET}}$	65	I	Initial reset input pin
$\overline{\text{TEST}}$	64	I	Test input pin*1

*1 $\overline{\text{TEST}}$ is the terminal used for factory inspection of the IC. For normal operation, be sure to connect the $\overline{\text{TEST}}$ terminal to VDD.

• Pin layout for expanded 4M mode (for multi-chip system)

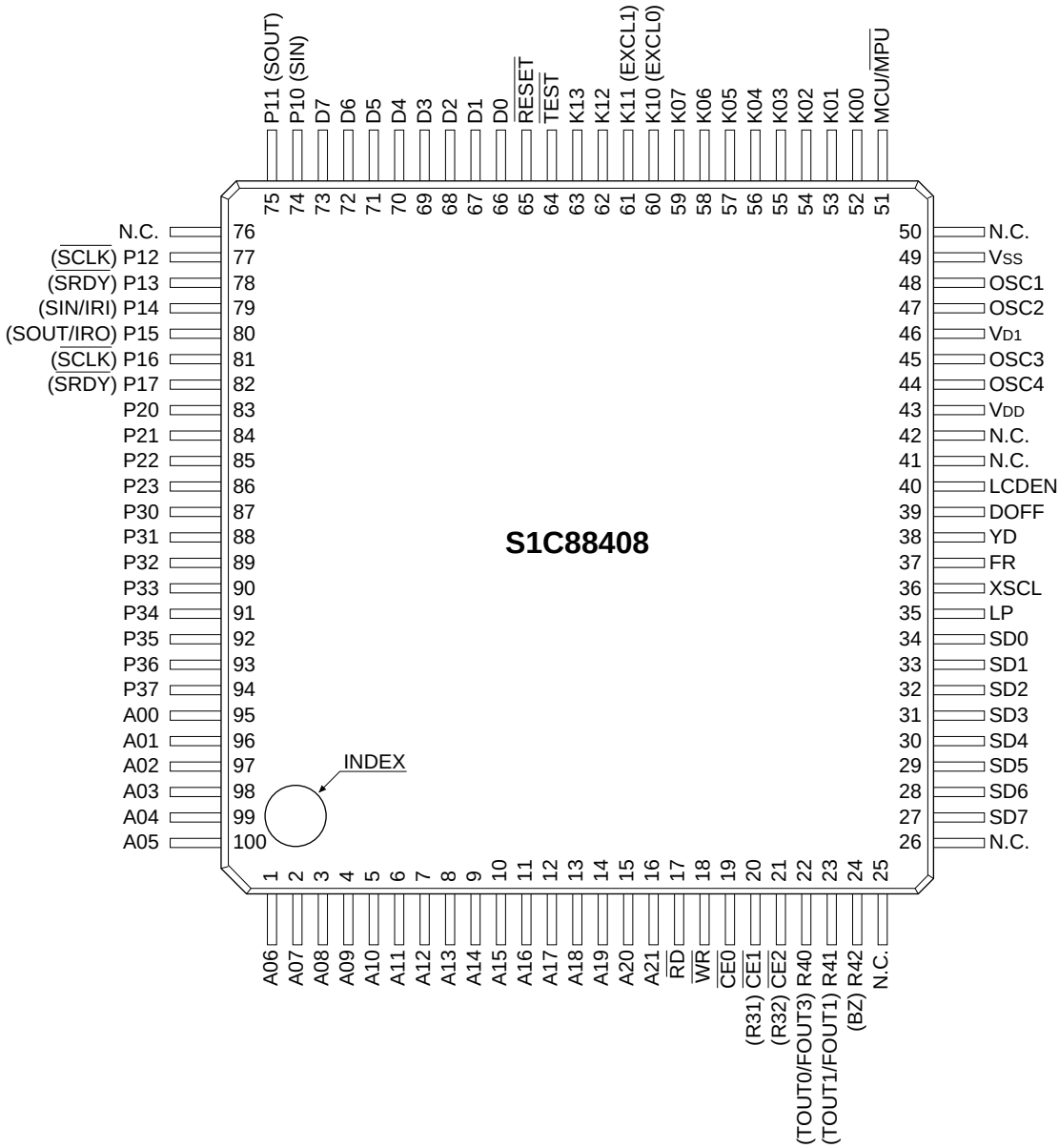


Fig. 1.4.3 S1C88408 pin layout (expanded 4M mode)

Table 1.4.3 S1C88408 pin description (expanded 4M mode)

Pin name	Pin No.	I/O	Function
VDD	43	–	Power supply (+) pin
VSS	49	–	Power supply (GND) pin
VD1	46	O	Voltage regulator output pin
OSC1	48	I	OSC1 oscillation input pin (32 kHz crystal, CR oscillation, external clock input)
OSC2	47	O	OSC1 oscillation output pin
OSC3	45	I	OSC3 oscillation input pin (crystal/ceramic, CR oscillation, external clock input)
OSC4	44	O	OSC3 oscillation output pin
MCU/$\overline{\text{MPU}}$	51	I	MCU/MPU mode stting pin
K00–K07	52–59	I	Input port pin
K10 (EXCL00)	60	I	Input port pin or external clock input pin for event counter (Timer 0)
K11 (EXCL01)	61	I	Input port pin or external clock input pin for event counter (Timer 1)
K12–K13	62–63	I	Input port pin
A00–A21	95–100, 1–16	O	Address bus
$\overline{\text{RD}}$	17	O	Read signal output pin
$\overline{\text{WR}}$	18	O	Write signal output pin
$\overline{\text{CE0}}$	19	O	Chip enable signal output pin
$\overline{\text{CE1}}$ (R31)	20	O	Chip enable signal output pin or output port pin
$\overline{\text{CE2}}$ (R32)	21	O	Chip enable signal output pin or output port pin
R40 (TOUT0/FOUT3)	22	O	Output port pin or TOUT0/FOUT3 clock output pin
R41 (TOUT1/FOUT1)	23	O	Output port pin or TOUT1/FOUT1 clock output pin
R42 (BZ)	24	O	Output port pin or buzzer signal output pin
D0–D7	66–73	I/O	Data bus
P10 (SIN)	74	I/O	I/O port pin or serial I/F data input pin
P11 ($\overline{\text{SOUT}}$)	75	I/O	I/O port pin or serial I/F data output pin
P12 ($\overline{\text{SCLK}}$)	77	I/O	I/O port pin or serial I/F clock input/output pin
P13 (SRDY)	78	I/O	I/O port pin or serial I/F ready signal output pin
P14 (SIN/IRI)	79	I/O	I/O port pin, serial I/F data input or IR receiver input pin
P15 ($\overline{\text{SOUT}}$/IRO)	80	I/O	I/O port pin, serial I/F data output or IR transmitter output pin
P16 ($\overline{\text{SCLK}}$)	81	I/O	I/O port pin or serial I/F clock input/output pin
P17 (SRDY)	82	I/O	I/O port pin or serial I/F ready signal output pin
P20–P23	83–86	I/O	I/O port pin
P30–P37	87–94	I/O	I/O port pin
LCDEN	40	O	LCD controller enable signal output pin
DOFF	39	O	LCD controller forced blank signal output pin
YD	38	O	LCD controller scan start pulse output pin
FR	37	O	LCD controller frame signal output pin
XSCL	36	O	LCD controller shift clock output pin
LP	35	O	LCD controller latch pulse output pin
SD0–SD7	34–27	O	LCD controller data output pin
$\overline{\text{RESET}}$	65	I	Initial reset input pin
$\overline{\text{TEST}}$	64	I	Test input pin*1

*1 $\overline{\text{TEST}}$ is the terminal used for factory inspection of the IC. For normal operation, be sure to connect the $\overline{\text{TEST}}$ terminal to VDD.

1.5 Mask Option

Mask options shown below are provided for the S1C88408. Several hardware specifications are prepared in each mask option, and one of them can be selected according to the application. The function option generator FOG88408, that has been prepared as the development software tool of the S1C88408, is used for this selection. Mask pattern of the IC is finally generated based on the data created by the FOG88408. Refer to the "S5U1C88408D Manual" for details on the FOG88408.

<Functions selectable with S1C88408 mask options>

(1) Bus mode

The bus mode that is set at initial reset can be selected. It is necessary to select it when using the S1C88408 in the MPU mode. Refer to Section 5.2, "System Controller and Bus Control", for details.

(2) OSC1 oscillation circuit

The specification of the OSC1 oscillation circuit can be selected from among four types: "Crystal oscillation", "CR oscillation", "Crystal oscillation (gate capacitor built-in)" and "External clock input". Refer to Section 5.4.3, "OSC1 oscillation circuit", for details.

(3) OSC3 oscillation circuit

The specification of the OSC3 oscillation circuit can be selected from among four types: "Crystal oscillation", "Ceramic oscillation", "CR oscillation" and "External clock input". Refer to Section 5.4.4, "OSC3 oscillation circuit", for details.

(4) MCU/$\overline{\text{MPU}}$ terminal pull-up resistor

This mask option can select whether the pull-up resistor for the MCU / $\overline{\text{MPU}}$ terminal is used or not.

(5) $\overline{\text{RESET}}$ terminal pull-up resistor

This mask option can select whether the pull-up resistor for the $\overline{\text{RESET}}$ terminal is used or not.

(6) Input port pull-up resistor

This mask option can select whether the pull-up resistor for the input port terminal is used or not. It is possible to select for each bit of the input ports. Refer to Section 5.6.2, "Mask option", for details.

(7) I/O port pull-up resistor

This mask option can select whether the pull-up resistor for the I / O port terminal (it works during input mode) is used or not. It is possible to select for each bit of the input ports. Refer to Section 5.8.3, "Mask option", for details.

(8) Data RAM, Display RAM capacity

The S1C88408 has built-in 3.75KB RAM. The data memory / display memory size can be selected from seven types (256 / 3584, 512 / 3328, 768 / 3072, 1024 / 2816, 1280 / 2560, 1536 / 2304, 1792 / 2048 bytes) according to the LCD panel to be used. Refer to Section 3.2.2, "RAM (Data Memory, Display Memory)", for details.

CHAPTER 2 POWER SUPPLY

This section explains the operating voltage and the configuration of the internal power supply circuit of the S1C88408.

2.1 Operating Voltage

Table 2.1.1 shows the operating voltage of the S1C88408.
Using a low voltage for VDD according to operating speed needs can reduce power consumption.

Table 2.1.1 Correspondence between operating voltage and operating frequency

Operatable voltage range (VDD)	Max. clock frequency (OSC3)
1.8 V to 5.5 V	1.1 MHz
2.6 V to 5.5 V	4.4 MHz
3.5 V to 5.5 V	8.2 MHz

Note: I/O signal levels (high and low) that are described in this manual show the following voltage level if not otherwise noted.

High level = VDD
Low level = VSS

2.2 Internal Power Supply Circuit

The S1C88408 has the built-in power supply circuit shown in Figure 2.2.1. The power supply circuit generates the voltage VD1 for the internal circuits by supplying a voltage within the range mentioned above between the VDD (+) and VSS (GND) terminals.

VD1 voltage can be selected from among three types: 3.2 V (Max. 8.2 MHz), 2.4 V (Max. 4.4 MHz) and 1.6 V (Max. 1.1 MHz).
It should be selected by a program to switch according to the supply voltage and oscillation frequency.
Refer to Section 5.4, "Oscillation Circuit" for switching VD1.

Note: Be sure not to use the VD1 terminal output for driving external circuits.

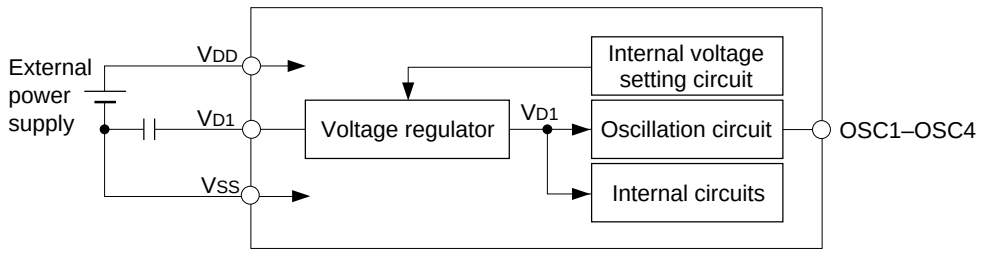


Fig. 2.2.1 Configuration of power supply circuit

2.3 Heavy Load Protection Mode

The S1C88408 has a heavy load protection function for stable operation even when the supply voltage fluctuates by driving a heavy load. The heavy load protection mode becomes valid when the peripheral circuits are in the following status:

(1) The OSC3 oscillation circuit is switched ON (OSCC = "1" and not in SLEEP)

(2) The buzzer output is switched ON (BZON = "1" or BZSHT = "1")

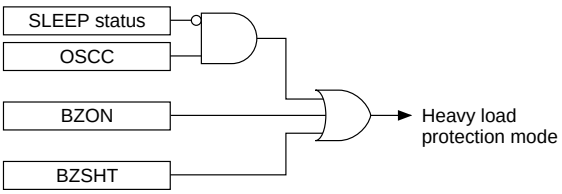


Fig. 2.3.1 Configuration of heavy load protection mode control circuit

For details of the OSC3 oscillation circuit and buzzer output, refer to Section 5.4, "Oscillation Circuit" and Section 5.15, "Sound Generator", respectively.

CHAPTER 3 CPU AND MEMORY

This section explains the CPU, operating mode and bus configuration.

3.1 CPU

The S1C88408 employs the 8-bit core CPU S1C88 as the CPU, so that register configuration, instructions and so on are virtually identical to those in other family processors using the S1C88.

Refer to the "S1C88 Core CPU Manual" for details of the S1C88.

The S1C88 CPU model used is Model 3 and has up to 4M × 3 address space that can be used for extended memory.

3.2 Internal Memory

The S1C88408 has built-in ROM and RAM as shown in Figure 3.2.1.
Small-scale applications can be realized with only this chip. The internal memory can be used together with the external memory.
Furthermore, the internal ROM can be disconnected from the bus so that the space is released to external memory.

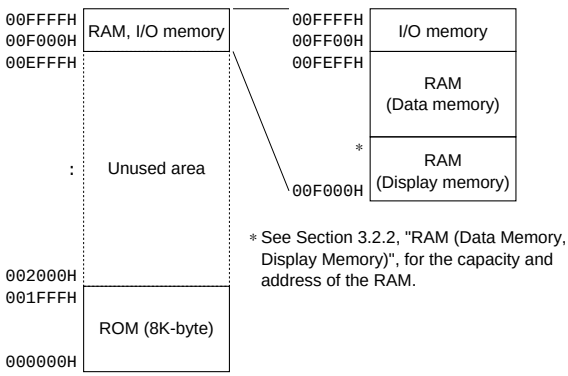


Fig. 3.2.1 Internal memory map

3.2.1 ROM

The internal ROM has a capacity of 8KB.
Depending on the setting of the MCU / $\overline{\text{MPU}}$ terminal, the internal ROM area can be released to external memory. (See Section 3.5, "Chip Mode".)

3.2.2 RAM (Data Memory, Display Memory)

The internal RAM has a capacity of 3.75KB.
The data memory size and display memory size can be selected as shown in Table 3.2.2.1 by mask option.

Table 3.2.2.1 RAM size setting by mask option

	Data memory	Display memory
1	1792 bytes 00F800H–00FEFFH	2048 bytes 00F000H–00F7FFH
2	1536 bytes 00F900H–00FEFFH	2304 bytes 00F000H–00F8FFH
3	1280 bytes 00FA00H–00FEFFH	2560 bytes 00F000H–00F9FFH
4	1024 bytes 00FB00H–00FEFFH	2816 bytes 00F000H–00FAFFH
5	768 bytes 00FC00H–00FEFFH	3072 bytes 00F000H–00FBFFH
6	512 bytes 00FD00H–00FEFFH	3328 bytes 00F000H–00FCFFH
7	256 bytes 00FE00H–00FEFFH	3584 bytes 00F000H–00FDFFH

The internal RAM area is not released to external memory even when the external memory which overlaps the internal RAM area is expanded. Access to this area affects the internal RAM.

Note: The display memory area configured by mask option may be used as data memory. However, the stack area cannot be assigned there.

Refer to Section 5.10, "LCD Controller", for details of the display memory.

3.2.3 I/O memory

A memory mapped I/O method is adopted in the S1C88408 for interface with internal peripheral circuits. The control bits and data registers of the peripheral circuits are arranged in the data memory space. Control and data transfer can be done with normal memory access instructions.
I/O memory area is arranged in 00FF00H–00FFFFH. Refer to Section 5.1, "I/O Memory Map", for details of the I/O memory.
The I/O memory area is not released to the external memory even when the external memory which overlaps the I/O memory area is expanded. Access to this area affects the I/O memory.

3.3 Exception Processing Vectors

In the S1C88408, 000000H–000029H in the program area are assigned as exception processing vectors. Furthermore, from 000034H to 0000FFH, software interrupt vectors are assignable to any two bytes which begin with an even address.
Table 3.3.1 shows the correspondence between the vector addresses and the exception processing factors.

The start address of the exception processing routine should be written to the respective vector address and the next address in order of low and high-order start address. When an exception processing factor is generated, the exception processing routine which starts from the recorded address is executed.
When multiple exception processing factors are generated at the same time, the exception processing is executed according to priority.

The priority of interrupts shown in Table 3.3.1 assumes that the interrupt priority levels are all the same. The interrupt priority levels can be set by software in each interrupt system. (See Section 5.18, "Interrupt and Standby Mode".)

Note: The exception processing not including reset saves the SC (system condition flag) and PC (program counter) to the stack before branching to the exception processing routine. Consequently, when returning to the main routine from exception processing routines, use the RETE instruction.

Refer to the "S1C88 Core CPU Manual" for CPU operation when an exception processing factor is generated.

Table 3.3.1 Correspondence between vector addresses and exception processing factors

Vector address	Symbol	Exception processing factor		Priority
000000H	RESET	Reset		High ↑
000002H	ZDIV	Zero division		
000004H	NMI	NMI (Watchdog timer)		
000006H	IRK10	Input port K1	K10 input interrupt	
000008H	IRK11		K11 input interrup	
00000AH	IRK12		K12 input interrup	
00000CH	IRK13		K13 input interrup	
00000EH	IRK0	Input port K0	K00–K07 input interrup	
000010H	IRTU0	16-bit programmable timer 0	Underflow interrupt	
000012H	IRTC0		Compare match interrupt	
000014H	IRTU1	16-bit programmable timer 1	Underflow interrupt	
000016H	IRTC1		Compare match interrupt	
000018H	IRTU2	8-bit programmable timer	Underflow interrupt	
00001AH	IRSER	Serial interface	Receive error interrupt	
00001CH	IRSRX		Receive completion interrupt	
00001EH	IRSTX		Receive error interrupt	
000024H	IRLCD	LCD controller	Data transfer completion interrupt	↓
000028H	IRRTC	Clock timer	32Hz/8Hz/2Hz/1Hz/60S interrupt	Low
000032H	–	System reserved (cannot be used)		No Priority rating
000034H ↓ 0000FEH	–	Software interrupt		

3.4 CC (Customized Condition Flag)

The S1C88408 does not use the customized condition flag (CC) in the core CPU. Accordingly, it cannot be used as a branching condition for the conditional branching instruction (JRS, CARS).

3.5 Chip Mode

3.5.1 MCU mode and MPU mode

The S1C88408 is set in two chip operating mode by the MCU / $\overline{\text{MPU}}$ terminal.

- **MCU mode...Set the MCU/$\overline{\text{MPU}}$ terminal to HIGH (V_{DD})**

  The MCU mode should be set when using the internal ROM. External memory can be expanded to the addressable space except for the internal memory area. Refer to Section 3.5.2, "Bus mode", for the memory map.

  In the MCU mode, an initial reset activates the S1C88408 as a system with the internal memory only. The internal ROM is allocated to the top of the common area (logical space 0000H–7FFFH) in the program memory. Exception processing vectors are assigned in the internal ROM.
  Furthermore, the application initial routine that starts with reset exception processing must likewise be written to the internal ROM. Bus and other settings corresponding to the expanded memory can be done by software. This processing is executed in the initial routine written in the internal ROM. The external memory can be accessed after the bus mode setting.

  In this mode, accessing the internal memory area does not output the chip enable ($\overline{\text{CE}}$) or the read ($\overline{\text{RD}}$) / write ($\overline{\text{WR}}$) signals to the external memory, and it sets the data bus (D0–D7) to high impedance status (or pull-up status when the pull-up resistors for P00–P07 are available by setting the mask option). Consequently, the external memory addresses that overlap with the internal memory are invalid.

- **MPU mode...Set the MCU/$\overline{\text{MPU}}$ terminal to LOW (V_{SS})**

  The MPU mode releases the internal ROM area to an external memory, so the internal ROM cannot be used. When this area is accessed, a chip enable ($\overline{\text{CE}}$) signal and a read ($\overline{\text{RD}}$) / write ($\overline{\text{WR}}$) signal are output to the external memory and the data bus (D0–D7) goes to active status. Accessing other internal memory (RAM, I/O memory) does not output these signals outside of the IC.

  In the MPU mode, the system is activated by the external memory. Therefore, the initial setting for the system configuration can be selected with mask option so that the bus is set according to the external memory at initial reset. (See Section 3.5.2, "Bus mode".)

  When setting this mode, the exception processing vectors and the initial routine must be assigned within the common area (000000H–007FFFH).

  The MCU / $\overline{\text{MPU}}$ terminal has a built-in pull-up resistor, and it can be selected for use or not by the mask option.

Note: The MCU/$\overline{\text{MPU}}$ terminal status is latched at the rising edge of the $\overline{\text{RESET}}$ input signal. Therefore, apply a low pulse to the $\overline{\text{RESET}}$ terminal when switching the mode.

3.5.2 Bus mode

The S1C88408 has four kind of bus modes in order to set the bus specification to match the configuration of expanded external memory. The four bus modes are as follows, and one of them can be selected with software.

- **Single chip mode**

  The single chip mode should be set when using the S1C88408 as a single chip microcomputer without external memory expansion.
  This mode is available only in the MCU mode shown in the previous section because the internal ROM is used. In the MPU mode, the single chip mode cannot be set.

  The single chip mode does not need an external bus line. The terminals for the external bus can be used as general-purpose output ports or I/O ports. Accordingly, the output port consists of 30 bits and the I/O port consists of 28 bits.

  This mode is equivalent to the Model 3/ minimum mode of the S1C88 core CPU. Memory access is valid only for the internal memory area within the physical space 000000H to 00FFFFH.

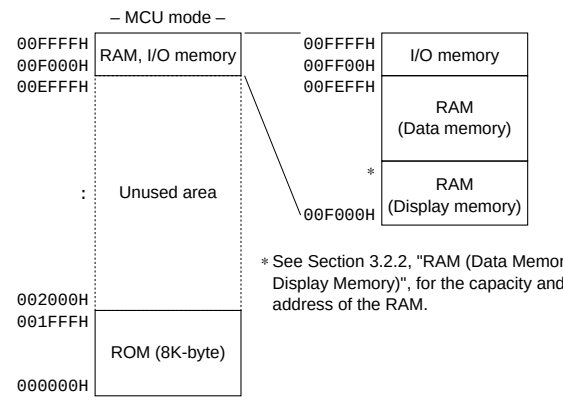


Fig. 3.5.2.1 Memory map for single chip mode

- **Expanded 64K mode**

  The expanded 64K mode should be set when 64KB or less of external memory is expanded to the S1C88408. This mode can be set regardless of the MCU / MPU mode setting.

  In the MCU mode, the internal ROM is used. Therefore, the external memory in that area cannot be accessed. External memory can be assigned to the area from 007000H to 00EFFFH in the MCU / expanded 64K mode.
  In the MPU mode, the internal ROM area is released to the external memory. Thus, external memory can be assigned to the area from 000000H to 00EFFFH in the MPU / expanded 64K mode.
  The area from 00F000H to 00FFFFH is assigned to the internal RAM and I / O memory, therefore the area cannot be accessed as an external memory.

  The expanded 64K mode is suitable for small- to mid-scale systems. This mode can output three (MCU mode) or four (MPU mode) kinds of chip enable ($\overline{CE}$) signals for 8KB to 64KB memory chips. It can be selected by software according to the memory chip to be used. Refer to Section 3.6.4, "Chip enable ($\overline{CE}$) signal", for details of the $\overline{CE}$ signal.

  This mode is equivalent to the Model 3 / minimum mode of the S1C88 core CPU. Memory access is valid only for the physical space 000000H to 00FFFFH.

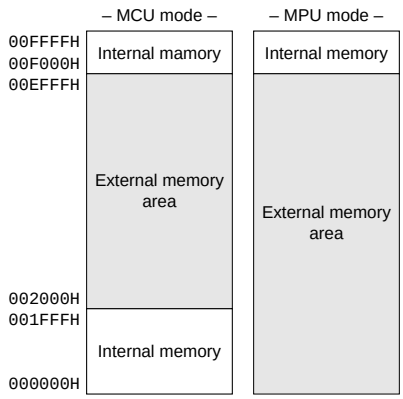


Fig. 3.5.2.2 Memory map for expanded 64K mode

- **Expanded 4M minimum mode**

  The expanded 4M minimum mode should be set when 64KB–4MB × 3 of external memory is expanded to the S1C88408. This mode can be set regardless of the MCU / MPU mode setting.

  In the MCU mode, the internal ROM is used. External memory can be assigned to the area from 400000H to FFFFFFH in the MCU / expanded 4M minimum mode.
  In the MPU mode, the internal ROM area is released to the external memory. Thus, external memory can be assigned to the area from 000000H to BFFFFFH in the MPU / expanded 4M minimum mode.
  However, the area from 00F000H to 00FFFFH is assigned to the internal RAM and I / O memory, therefore the area cannot be accessed as an external memory.

  This mode is equivalent to the Model 3 / minimum mode of the S1C88 core CPU. Memory access is valid for the physical space 000000H to BFFFFFH in the MPU mode or 400000H to FFFFFFH + internal memory in the MCU mode. However, program memory expansion is limited to 64KB.
  In the MPU mode, program memory can be assigned to the common area (000000H to 007FFFH) and one optional bank (32K) area.
  In the MCU mode, since the internal ROM is assigned to the common area, external program memory can be assigned to one optional bank (32K) only.
  This mode is suitable for small- to mid-scale program memories and large-scale data memory systems.

  This mode outputs the chip enable ($\overline{CE}$) signals for the 4MB memory chip.

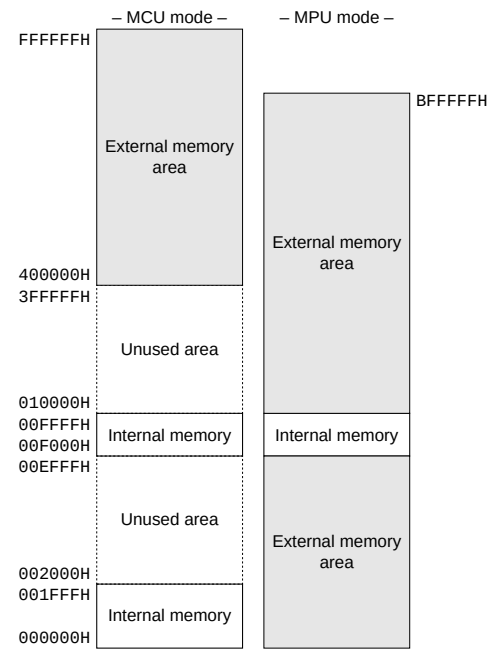


Fig. 3.5.2.3 Memory map for expanded 4M minimum mode

- **Expanded 4M maximum mode**

  The expanded 4M maximum mode should be set when 64KB–4MB × 3 of external memory is expanded to the S1C88408. This mode can be set regardless of the MCU / MPU mode setting.

  In the MCU mode, the internal ROM is used. External memory can be assigned to the area from 400000H to FFFFFFH in the MCU / expanded 4M maximum mode.
  In the MPU mode, the internal ROM area is released to the external memory. Thus, external memory can be assigned to the area from 000000H to BFFFFFH in the MPU / expanded 4M maximum mode.
  However, the area from 00F000H to 00FFFFH is assigned to the internal RAM and I / O memory, therefore the area cannot be accessed as an external memory.

  This mode is equivalent to the Model 3 / maximum mode of the S1C88 core CPU. Memory access is valid for the physical space 000000H to BFFFFFH in the MPU mode or 400000H to FFFFFFH + internal memory in the MCU mode.
  Program memory and data memory can be assigned with an optional size (up to 4MB × 3 together), so this mode is suitable for systems with large-scale program and data capacity.

  This mode outputs the chip enable ($\overline{CE}$) signals for the 4MB memory chip.

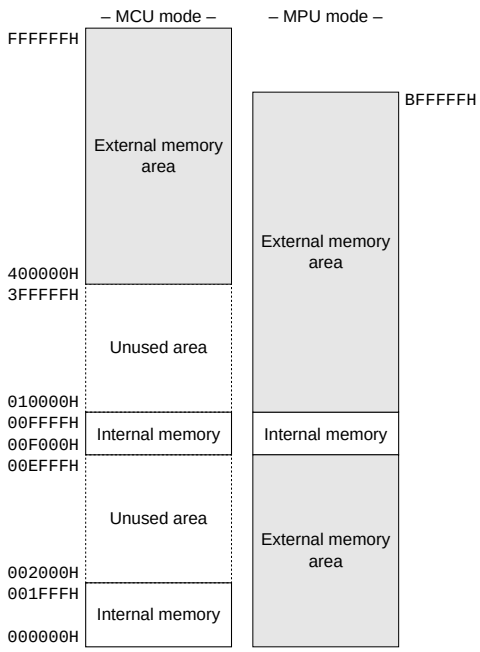


Fig. 3.5.2.4 Memory map for expanded 4M maximum mode

Refer to Section 5.2, "System Controller and Bus Control", for setting the mode.

3.6 External Bus

The S1C88408 has bus terminals that can address a maximum 4MB × 3 external memory. Memory and other devices can be expanded outside according to the range of each bus mode shown in the previous section.

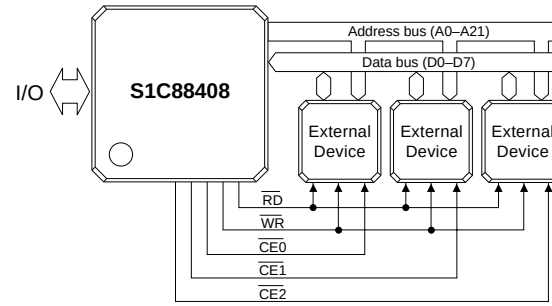


Fig. 3.6.1 External bus lines

The following explains the outline of the external bus terminals. Refer to Section 5.2, "System Controller and Bus Control", for controlling them.

3.6.1 Data bus

The S1C88408 has an 8-bit external data bus (D0–D7). The terminals and I / O circuits of the data bus D0–D7 are shared with the I / O port P00–P07, and the function switches according to the bus mode setting.
In the single chip mode, the 8-bit terminals are all set as the I / O port terminals P00–P07 and in the other expanded modes, they are set as the data bus (D0–D7).
When the data bus is set, the data register and I / O control register of the I / O port P00–P07 are disconnected from the I / O circuit and can be used as general purpose data registers with the ability to read / write.

Each data bus line has a built-in pull-up resistor that is activated during the input mode, and it can be selected for use or not by the mask option.

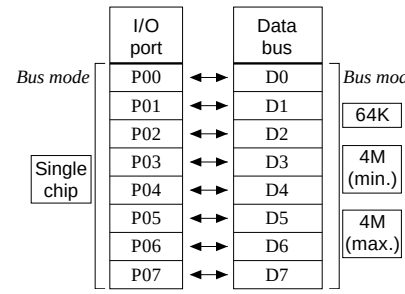


Fig. 3.6.1.1 Correspondence between data bus and I/O port

3.6.2 Address bus

The S1C88408 has a 22-bit external address bus (A0–A21). The terminals and output circuits of the address bus A0–A21 are shared with the output ports R00–R07 (=A0–A7), R10–R17 (=A8–A15) and R20–R25 (=A16–A21), and the function switches according to the bus mode setting.
In the single chip mode, the 22-bit terminals are all set as the output port terminals R00–R07, R10–R17 and R20–R25.
In the expanded 64K mode, 16-bit terminals within the 22 bits are set as the address bus A0–A15, while the remaining 6 bits, A16–A21, are set as output port R20–R25.
In the expanded 4M minimum and maximum modes, all of the 22-bit terminals are set as the address bus (A0–A21).

When the address bus is set, the data register and high impedance control register of each output port are disconnected from the output circuit and can be used as general-purpose data registers with the ability to read / write.

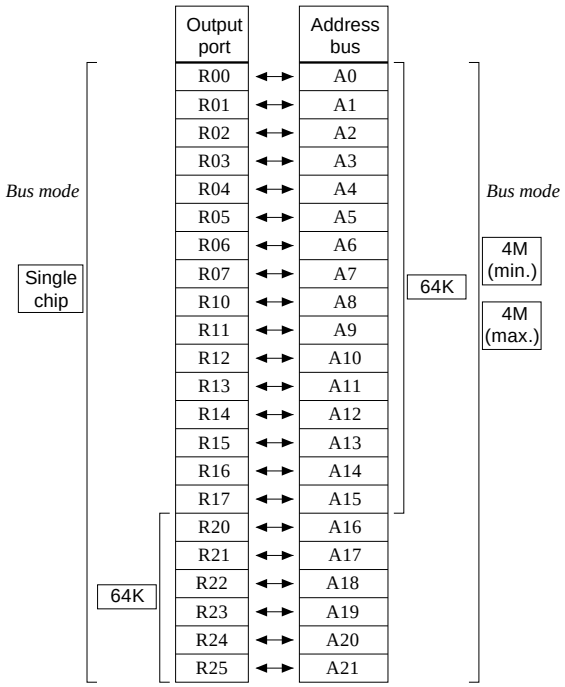


Fig. 3.6.2.1 Correspondence between address bus and output ports

3.6.3 Read ($\overline{RD}$)/write ($\overline{WR}$) signals

The output terminals and output circuits for the read ($\overline{RD}$) / write ($\overline{WR}$) signals are shared with the output ports R26 and R27, and the function switches according to the bus mode setting.
In the single chip mode, both the terminals are set as output port terminals and in other expanded modes, they are set as read ($\overline{RD}$) / write ($\overline{WR}$) signal output terminals. When they are set as read ($\overline{RD}$) / write ($\overline{WR}$) signal output terminals, the data register and high impedance control register for each output port (R26, R27) are disconnected from the output circuit and can be used as a general-purpose data register with the ability to read / write.

These two signals are output only when the memory area for the external device is being accessed. They are not output when the internal memory is accessed.
Refer to Section 3.6.5, "WAIT control", for the signal output timing.

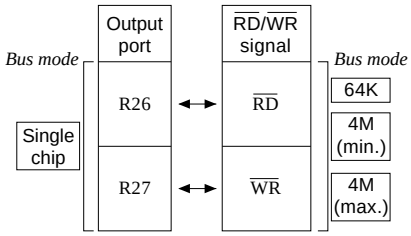


Fig. 3.6.3.1 Correspondence between read ($\overline{RD}$)/write ($\overline{WR}$) signal and output port

3.6.4 Chip enable ($\overline{CE}$) signal

The S1C88408 has a built-in address decoder which can output up to three chip enable ($\overline{CE}$) signals. Consequently, three devices equipped with a chip enable ($\overline{CE}$) or chip select ($\overline{CS}$) terminal can be directly connected without an external address decoder.

The three chip enable ($\overline{CE0}$–$\overline{CE2}$) signal output terminals and output circuits are shared with output ports R30–R32. In the expanded modes, the function, either $\overline{CE}$ or output port, can independently be selected by software according to the chips to be expanded.
When the chip enable ($\overline{CE}$) output is set, the data register and high impedance control register of the output port are disconnected from the output circuit and can be used as general-purpose data registers with the ability to read / write.
In the single chip mode, they can be used as the output ports R30–R32.

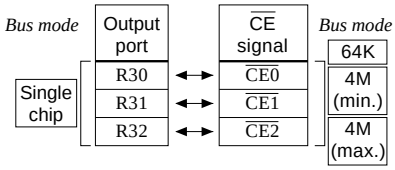


Fig. 3.6.4.1 Correspondence between $\overline{CE}$ signals and output ports

The memory size assigned to three chip enable ($\overline{CE}$) signals is determined by the bus mode setting.
In the expanded 64K mode, four decoder outputs can be selected by software according to the memory expanded.
Table 3.6.4.1 shows the addressable ranges which are assigned to the chip enable ($\overline{CE}$) signal in each mode.

When the internal memory area is accessed, the $\overline{CE}$ signal is not output. Be aware that the part has been irregular setting.
External devices can be allocated to an area selected by an optional chip enable signal. It is not necessary to continue from a lower address of the memory space.

The chip enable signal is output only when the external memory area is being accessed. It is not output when the internal memory is accessed. Furthermore, when the CPU is in standby status (HALT, SLEEP), all the $\overline{CE}$ signals go HIGH. It prohibits external memory access and gets the CPU into power save mode.
Refer to Section 3.6.5, "WAIT control", for the signal output timing.

Table 3.6.4.1 $\overline{CE0}$–$\overline{CE2}$ address settings

(1) Expanded 64K mode + MCU mode

$\overline{CE}$ signal	Addressing range (selected with software)		
	8KB	16KB	32KB
$\overline{CE0}$	008000H–009FFFH	007000H–00AFFFH	008000H–00EFFFH
$\overline{CE1}$	00A000H–00BFFFH	00B000H–00EFFFH	–
$\overline{CE2}$	00C000H–00DFFFH	–	–

(2) Expanded 64K mode + MPU mode

$\overline{CE}$ signal	Addressing range (selected with software)			
	8KB	16KB	32KB	64KB
$\overline{CE0}$	000000H–001FFFH	000000H–003FFFH	000000H–007FFFH	000000H–00EFFFH
$\overline{CE1}$	002000H–003FFFH	004000H–007FFFH	008000H–00EFFFH	–
$\overline{CE2}$	004000H–005FFFH	008000H–00BFFFH	–	–

(3) Expanded 4M minimum/maximum mode

$\overline{CE}$ signal	Addressing range (selected with software)	
	MCU mode	MPU mode
$\overline{CE0}$	C00000H–FFFFFFH	000000H–00EFFFH, 010000H–3FFFFFH
$\overline{CE1}$	400000H–7FFFFFH	400000H–7FFFFFH
$\overline{CE2}$	800000H–BFFFFFH	800000H–BFFFFFH

3.6.5 WAIT control

In order to guarantee accessing of external low speed devices during high speed operation, the S1C88408 is equipped with a WAIT function that prolongs access time. (Refer to the "S1C88 Core CPU Manual" for details of the WAIT function.)

The WAIT state numbers to be inserted can be selected with software from four values as shown in Table 3.6.5.1.

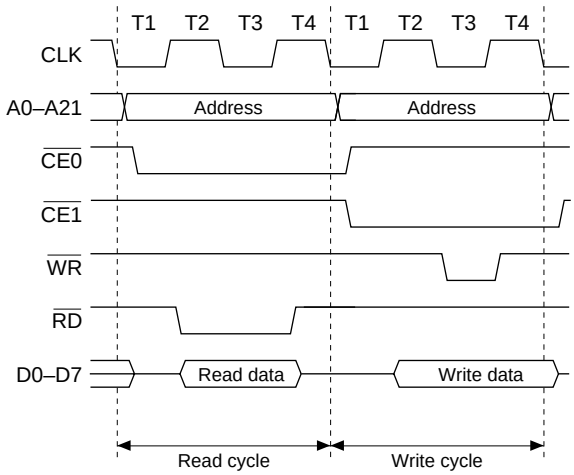
Table 3.6.5.1 Selectable WAIT state numbers

Selection No.	1	2	3	4
Insert states	0	4	8	12

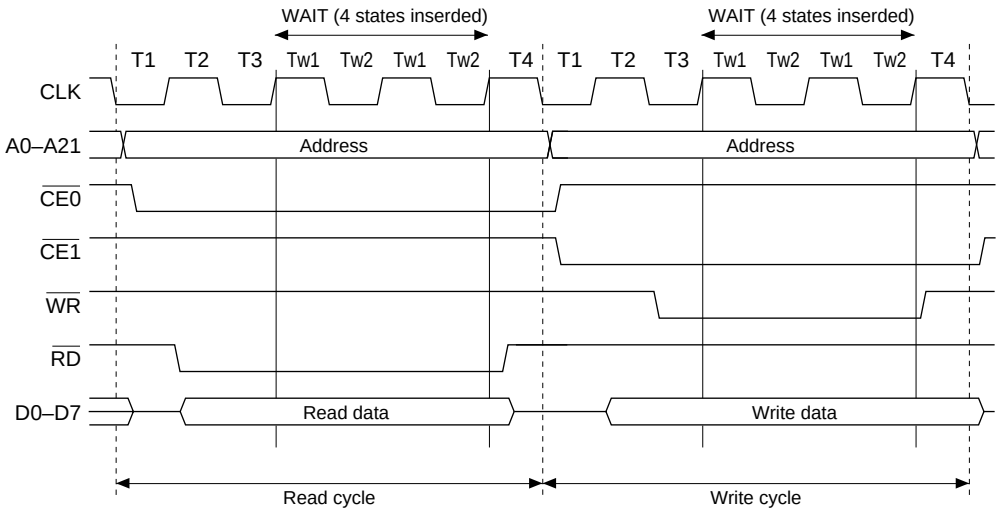
∗ The length of one state is 1/2 a cycle of the clock.

The WAIT states that are set with software are inserted between bus cycle states T3 and T4. Note, however, that WAIT states cannot be inserted when an internal register or internal memory is being accessed and when the CPU operates with the OSC1 oscillation clock (see Section 5.4, "Oscillation Circuit"). Consequently, WAIT state settings are invalid in the single chip mode.

Figure 3.6.5.1 shows the memory read / write timing charts.



(1) No WAIT



(2) WAIT state insertion

Fig. 3.6.5.1 Memory read/write cycle

CHAPTER 4 INITIAL RESET

To initialize the S1C88408 circuits, initial reset must be executed. This section explains the initial reset factor and the initial settings for internal registers.

4.1 Initial Reset Factors

There are two initial reset factors for the S1C88408 as shown below.

(1) $\overline{\text{RESET}}$ terminal
(2) Simultaneous LOW level input at input port terminals K00–K03.

Figure 4.1.1 shows the configuration of the initial reset circuit.

The CPU and peripheral circuits are initialized by means of initial reset factors. When the factor is canceled, the CPU commences reset exception processing. (See "S1C88 Core CPU Manual".)

When this occurs, reset exception processing vectors, Bank 0, 000000H–000001H from program memory are read out and the program (initialization routine) which begins at the readout address is executed.

4.1.1 $\overline{\text{RESET}}$ terminal

Initial reset can be done by executed externally inputting a LOW level to the $\overline{\text{RESET}}$ terminal.
Be sure to maintain the $\overline{\text{RESET}}$ terminal at LOW level for the regulation time after the power on to assure the initial reset.
In addition, be sure to use the $\overline{\text{RESET}}$ terminal for the first initial reset after the power is turned on.
The $\overline{\text{RESET}}$ terminal is equipped with a pull-up resistor. You can select whether or not to use by mask option.

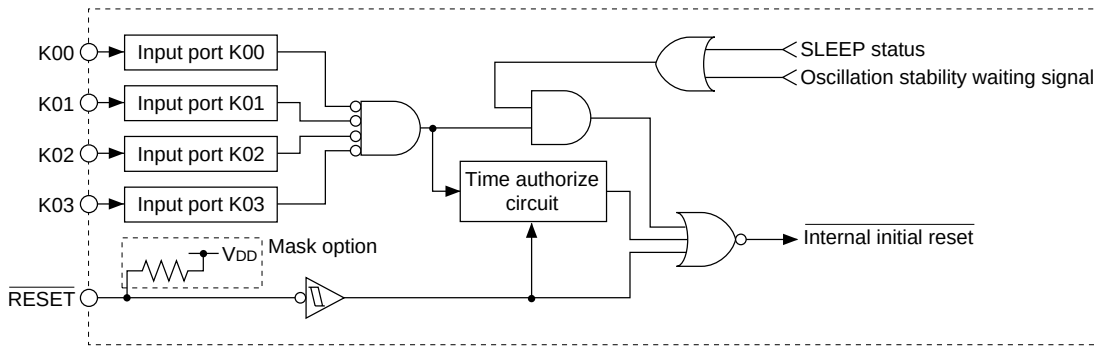


Fig. 4.1.1 Configuration of initial reset circuit

4.1.2 Simultaneous LOW level input at input port terminals K00–K03

Another way of executing initial reset externally is to input a LOW level simultaneously to the input ports (K00–K03) selected by mask option.
Since there is a built-in time authorize circuit, be sure to maintain the designated input port terminal at LOW level for two seconds (when the oscillation frequency is fOSC1 = 32.768 kHz) or more to perform the initial reset by means of this function.
However, the time authorize circuit is bypassed during the SLEEP (standby) status and oscillation stabilization waiting period, and initial reset is executed immediately after the simultaneous LOW level input to the designated input ports.
The combination of input ports (K00–K03) that can be selected by mask option are as follows:
(1) Not use
(2) K00 & K01
(3) K00 & K01 & K02
(4) K00 & K01 & K02 & K03

For instance, let's say that mask option (4) "K00 & K01 & K02 & K03" is selected.
When the input level at input ports K00–K03 is simultaneously LOW, initial reset will take place.

When using this function, make sure that the designated input ports do not simultaneously switch to LOW level while the system is in normal operation.

4.2 Initial Reset Sequence

After cancellation of the LOW level input to the $\overline{\text{RESET}}$ terminal, when the power is turned on, the start-up of the CPU is held back until the oscillation stabilization waiting time (8,192 / fOSC1 sec.) has elapsed.
Figure 4.2.1 shows the operating sequence following initial reset release.

Also, when using the initial reset by simultaneous LOW level input into the input port, you should be careful of the following points.

(1) During SLEEP status, since the time authorization circuit is bypassed, an initial reset is triggered immediately after a LOW level simultaneous input value. In this case, the CPU starts after waiting the oscillation stabilization time, following cancellation of the LOW level simultaneous input.

(2) Other than during SLEEP status, an initial reset will be triggered 1–2 seconds after a LOW level simultaneous input. In this case, since a reset differential pulse (64 / fOSC1 sec.) is generated inside the S1C88408, the CPU will start even if the LOW level simultaneous input status is not canceled.

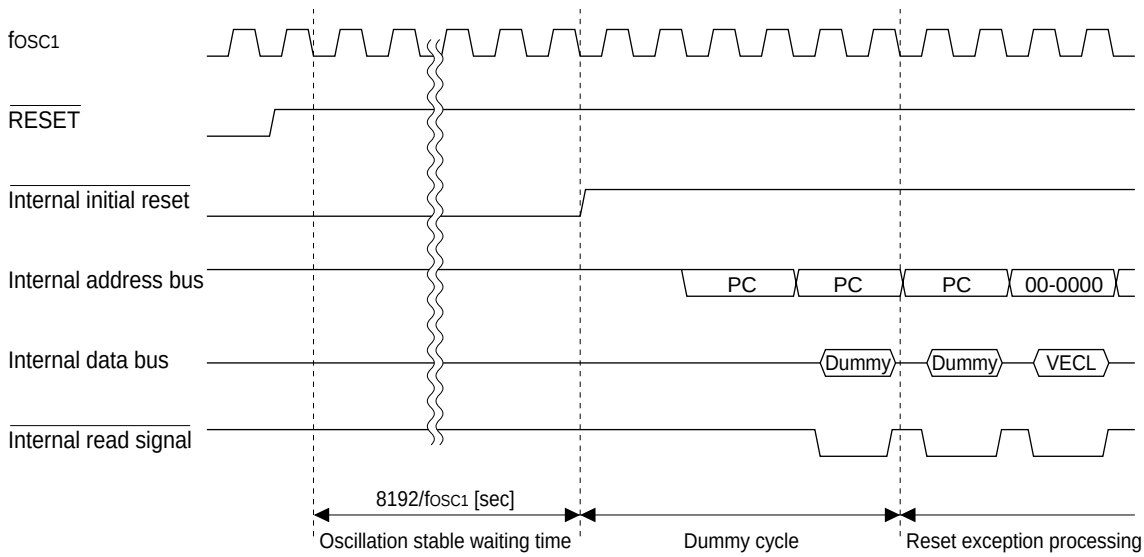


Fig. 4.2.1 Initial reset sequence

4.3 Initial Settings at Initial Reset

Initial settings of internal registers

The internal registers in the CPU are initialized as follows during initial reset.

Table 4.3.1 Initial settings

Register name	Symbol	Bit length	Initial value
Data register A	A	8	Undefined
Data register B	B	8	Undefined
Index (data) register L	L	8	Undefined
Index (data) register H	H	8	Undefined
Index register IX	IX	16	Undefined
Index register IY	IY	16	Undefined
Program counter	PC	16	Undefined*
Stack pointer	SP	16	Undefined
Base register	BR	8	Undefined
Zero flag	Z	1	0
Carry flag	C	1	0
Overflow flag	V	1	0
Negative flag	N	1	0
Decimal flag	D	1	0
Unpack flag	U	1	0
Interrupt flag 0	I0	1	1
Interrupt flag 1	I1	1	1
New code bank register	NB	8	01H
Code bank register	CB	8	Undefined*
Expand page register	EP	8	00H
Expand page register for IX	XP	8	00H
Expand page register for IY	YP	8	00H

* The reset exception processing loads the value stored in Bank 0, 00000H–000001H into the PC. At the same time, the NB initial value 01H is loaded into CB.

Registers which are not initialized at initial reset should be initialized using software.

Stack

The stack pointer SP is undefined at initial reset. Be sure to initialize SP before subroutines and interrupts generate.
In the S1C88408, the stack page is fixed at Page 0. Therefore, reserve the stack area in the RAM expanded in Page 0 or the data memory area of the internal RAM (–00FEFFH).

Note: The display memory area configured by mask option may be used as data memory. However, the stack area cannot be assigned there.

Internal RAM (Data memory, Display memory)

Since the internal RAM is not initialized at initial reset, initialize with software.

System and terminal configuration

When the S1C88408 is used in the MCU mode, the bus mode is set to the single chip mode at initial reset. In the MPU mode, it is set to the mode selected by the mask option.
Refer to Section 1.4, "Pin Layout Diagram", for the terminal configuration depending on the bus mode setting.

Internal peripheral circuit

The internal peripheral circuits are initialized to prescribed status. Initialize with software if necessary.
Especially the input/output terminals of the peripheral circuits are all set as the output port terminals and the I/O port terminals. Switch them according to the peripheral circuit to be used.
Refer to Section 5.1, "I/O Memory Map", or respective sections of the peripheral circuits for details of the status and initial values.

Interrupt

After initial reset, all the interrupts including NMI are masked until the appropriate values are written to the I/O memory addresses "00FF00H" and "00FF01H" to prevent malfunctions that may occur before setting the system configuration.
Refer to Section 5.2, "System Controller and Bus Control", for the contents of the addresses.

CHAPTER 5 PERIPHERAL CIRCUITS AND OPERATION

The peripheral circuits of the S1C88408 are interfaced with the CPU in the memory mapped I/O method. Thus, the peripheral circuits can be controlled by using the memory operation instructions to access the I/O memory. This chapter explains the operation and control of the peripheral circuits, individually.

5.1 I/O Memory Map

Table 5.1.1(a) I/O Memory map (00FF00H, 00FF01H)

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF00 MCU mode	D7	BSMD1	Bus mode (CPU mode) selection BSMD1 BSMD0 Mode 1 1 4M(Maximum) 1 0 4M(Minimum) 0 1 64K 0 0 Single chip			0	R/W	
	D6	BSMD0				0	R/W	
	D5	CEMD1	Expanded 64K chip enable mode CEMD1 CEMD0 Mode 1 1 – 1 0 32K($\overline{CE0}$) 0 1 16K($\overline{CE0}$, $\overline{CE1}$) 0 0 8K($\overline{CE0}$–$\overline{CE2}$)			1	R/W	Only for 64K bus mode
	D4	CEMD0				1	R/W	
	D3	–	–	–	–	–	–	"0" when being read
	D2	CE2	$\overline{CE2}$(R32) $\overline{CE}$ signal output enable/disable	$\overline{CE2}$ enable	$\overline{CE2}$ disable	1	R/W	In the single chip
	D1	CE1	$\overline{CE1}$(R31) enable: $\overline{CE}$ signal output	$\overline{CE1}$ enable	$\overline{CE1}$ disable	1	R/W	mode, these setting
	D0	CE0	$\overline{CE0}$(R30) disable: DC output (R3x)	$\overline{CE0}$ enable	$\overline{CE0}$ disable	1	R/W	are fixed at DC output
00FF00 MPU mode	D7	BSMD1	Bus mode (CPU mode) selection BSMD1 BSMD0 Mode 1 1 4M(Maximum) 1 0 4M(Minimum) 0 1 64K 0 0 Option selection ◄			*	R/W	Initial setting can be selected from 3 types (64K, 4M min, 4M max) by mask option
	D6	BSMD0				*	R/W	
	D5	CEMD1	Expanded 64K chip enable mode CEMD1 CEMD0 Mode 1 1 64K($\overline{CE0}$) 1 0 32K($\overline{CE0}$, $\overline{CE1}$) 0 1 16K($\overline{CE0}$–$\overline{CE2}$) 0 0 8K($\overline{CE0}$–$\overline{CE2}$)			1	R/W	Only for 64K bus mode
	D4	CEMD0				1	R/W	
	D3	–	–	–	–	–	–	"0" when being read
	D2	CE2	$\overline{CE2}$(R32) $\overline{CE}$ signal output enable/disable	$\overline{CE2}$ enable	$\overline{CE2}$ disable	1	R/W	
	D1	CE1	$\overline{CE1}$(R31) enable: $\overline{CE}$ signal output	$\overline{CE1}$ enable	$\overline{CE1}$ disable	1	R/W	
	D0	CE0	$\overline{CE0}$(R30) disable: DC output (R3x)	$\overline{CE0}$ enable	$\overline{CE0}$ disable	1	R/W	
00FF01	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	WT1	Wait state control WT1 WT0 Number of states 1 1 12(3 cycles) 1 0 8(2 cycles) 0 1 4(1 cycle) 0 0 No wait			0	R/W	
	D4	WT0				0	R/W	
	D3	CLKCHG	CPU operating clock switch	OSC3	OSC1	0	R/W	
	D2	OSCC	OSC3 oscillation ON/OFF control	On	Off	0	R/W	
	D1	VD1C1	V_{D1} output level setting VD1C1 VD1C0 V_{D1} (Typ.) 1 × 3.2 V 0 1 1.6 V 0 0 2.4 V			0	R/W	
	D0	VD1C0				0	R/W	

Note: All the interrupts including NMI are masked until the appropriate values are written to both the "00FF00H" and "00FF01H" addresses.

Table 5.1.1(b) I/O Memory map (00FF10H–00FF12H)

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF10	D7	PRPRT1	16-bit programmable timer 1 clock control	On	Off	0	R/W	
	D6	PST12	16-bit programmable timer 1 division ratio			0	R/W	
	D5	PST11	PST12 PST11 PST10 (OSC3) (OSC1) 1 1 1 fOSC3 / 4096 fOSC1 / 128 1 1 0 fOSC3 / 1024 fOSC1 / 64 1 0 1 fOSC3 / 256 fOSC1 / 32 1 0 0 fOSC3 / 128 fOSC1 / 16 0 1 1 fOSC3 / 64 fOSC1 / 8 0 1 0 fOSC3 / 32 fOSC1 / 4 0 0 1 fOSC3 / 8 fOSC1 / 2 0 0 0 fOSC3 / 2 fOSC1 / 1			0	R/W	
	D4	PST10				0	R/W	
	D3	PRPRT0	16-bit programmable timer 0 clock control	On	Off	0	R/W	
	D2	PST02	16-bit programmable timer 0 division ratio			0	R/W	
	D1	PST01	PST02 PST01 PST00 (OSC3) (OSC1) 1 1 1 fOSC3 / 4096 fOSC1 / 128 1 1 0 fOSC3 / 1024 fOSC1 / 64 1 0 1 fOSC3 / 256 fOSC1 / 32 1 0 0 fOSC3 / 128 fOSC1 / 16 0 1 1 fOSC3 / 64 fOSC1 / 8 0 1 0 fOSC3 / 32 fOSC1 / 4 0 0 1 fOSC3 / 8 fOSC1 / 2 0 0 0 fOSC3 / 2 fOSC1 / 1			0	R/W	
	D0	PST00				0	R/W	
00FF11	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	PRPRT2	8-bit programmable timer clock control	On	Off	0	R/W	
	D2	PST22	8-bit programmable timer division ratio			0	R/W	
	D1	PST21	PST22 PST21 PST20 Division ratio 1 1 1 fOSC3 / 256 1 1 0 fOSC3 / 128 1 0 1 fOSC3 / 64 1 0 0 fOSC3 / 32 0 1 1 fOSC3 / 16 0 1 0 fOSC3 / 8 0 0 1 fOSC3 / 4 0 0 0 fOSC3 / 2			0	R/W	
	D0	PST20				0	R/W	
00FF12	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	–	–	–	–	–	–	
	D1	PRTF1	16-bit programmable timer 1 source clock selection	fOSC1	fOSC3	0	R/W	
	D0	PRTF0	16-bit programmable timer 0 source clock selection	fOSC1	fOSC3	0	R/W	

Table 5.1.1(c) I/O Memory map (00FF14H, 00FF15H)

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF14	D7	PRFO1	FOUT1 output control	On	Off	0	R/W	
	D6	PSF12	FOUT1 division ratio			0	R/W	
	D5	PSF11				0	R/W	
	D4	PSF10				0	R/W	
	D3	PRFO3	FOUT3 output control	On	Off	0	R/W	
	D2	PSF32	FOUT3 division ratio			0	R/W	
	D1	PSF31				0	R/W	
	D0	PSF30				0	R/W	
00FF15	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	–	–	–	–	–	–	
	D1	PK11ON	EXCL01 input clock ON/OFF control	On	Off	0	R/W	
	D0	PK10ON	EXCL00 input clock ON/OFF control	On	Off	0	R/W	

FOUT1 division ratio

PSF12	PSF11	PSF10	Division ratio
1	1	1	$fosc_1$ / 128
1	1	0	$fosc_1$ / 64
1	0	1	$fosc_1$ / 32
1	0	0	$fosc_1$ / 16
0	1	1	$fosc_1$ / 8
0	1	0	$fosc_1$ / 4
0	0	1	$fosc_1$ / 2
0	0	0	$fosc_1$ / 1

FOUT3 division ratio

PSF32	PSF31	PSF30	Division ratio
1	1	1	$fosc_3$ / 128
1	1	0	$fosc_3$ / 64
1	0	1	$fosc_3$ / 32
1	0	0	$fosc_3$ / 16
0	1	1	$fosc_3$ / 8
0	1	0	$fosc_3$ / 4
0	0	1	$fosc_3$ / 2
0	0	0	$fosc_3$ / 1

Table 5.1.1(d) I/O Memory map (00FF20H, 00FF21H, 00FF23H–00FF25H)

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF20	D7	PK11	K10–K13	PK11	PK10	0	R/W	
	D6	PK10	interrupt priority register	PK01	PK00	0	R/W	
	D5	PK01	K00–K07	PTM11	PTM10	0	R/W	
	D4	PK00	interrupt priority register	PTM01	PTM00	0	R/W	
	D3	PTM11	16-bit programmable timer 1	1	1	0	R/W	
	D2	PTM10	interrupt priority register	1	0	0	R/W	
	D1	PTM01	16-bit programmable timer 0	0	1	0	R/W	
	D0	PTM00	interrupt priority register	0	0	0	R/W	
00FF21	D7	PTM21	8-bit programmable timer	PTM21	PTM20	0	R/W	
	D6	PTM20	interrupt priority register	PSI1	PSI0	0	R/W	
	D5	PSI1	Serial interface	PCTM1	PCTM0	0	R/W	
	D4	PSI0	interrupt priority register	PLCD1	PLCD0	0	R/W	
	D3	PCTM1	Clock timer	1	1	0	R/W	
	D2	PCTM0	interrupt priority register	1	0	0	R/W	
	D1	PLCD1	LCD controller	0	1	0	R/W	
	D0	PLCD0	interrupt priority register	0	0	0	R/W	
00FF23	D7	EK13	K13 interrupt enable register	Interrupt is enabled	Interrupt is disabled	0	R/W	
	D6	EK12	K12 interrupt enable register			0	R/W	
	D5	EK11	K11 interrupt enable register			0	R/W	
	D4	EK10	K10 interrupt enable register			0	R/W	
	D3	EK0	K00–K07 interrupt enable register			0	R/W	
	D2	–	–			–	–	"0" when being read
	D1	–	–			–	–	
	D0	–	–			–	–	
00FF24	D7	ETU2	8-bit programmable timer underflow interrupt enable register	Interrupt is enabled	Interrupt is disabled	0	R/W	
	D6	ETC1	16-bit programmable timer 1 compare match interrupt enable register			0	R/W	
	D5	ETU1	16-bit programmable timer 1 underflow interrupt enable register			0	R/W	
	D4	ETC0	16-bit programmable timer 0 compare match interrupt enable register			0	R/W	
	D3	ETU0	16-bit programmable timer 0 underflow interrupt enable register			0	R/W	
	D2	ESTX	Serial interface transmit completion interrupt enable register			0	R/W	
	D1	ESRX	Serial interface receive completion interrupt enable register			0	R/W	
	D0	ESERR	Serial interface receive error interrupt enable register			0	R/W	
00FF25	D7	ET60S	Clock timer 60 S interrupt enable register	Interrupt is enabled	Interrupt is disabled	0	R/W	
	D6	ECTM1	Clock timer 1 Hz interrupt enable register			0	R/W	
	D5	ECTM2	Clock timer 2 Hz interrupt enable register			0	R/W	
	D4	ECTM8	Clock timer 8 Hz interrupt enable register			0	R/W	
	D3	ECTM32	Clock timer 32 Hz interrupt enable register			0	R/W	
	D2	ELCD	LCD controller interrupt enable register			0	R/W	
	D1	–	–			–	–	"0" when being read
	D0	–	–			–	–	

Table 5.1.1(e) I/O Memory map (00FF27H–00FF29H)

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF27	D7	FK13	K13 interrupt factor flag	(R)	(R)	0	R/(W)	
	D6	FK12	K12 interrupt factor flag	Interrupt	Interrupt	0	R/(W)	
	D5	FK11	K11 interrupt factor flag	factor has	factor has not	0	R/(W)	
	D4	FK10	K10 interrupt factor flag	generated	generated	0	R/(W)	
	D3	FK0	K00–K07 interrupt factor flag			0	R/(W)	
	D2	–	–	(W)	(W)	–	–	"0" when being read
	D1	–	–	Reset	Invalid	–	–	
	D0	–	–			–	–	
00FF28	D7	FTU2	8-bit programmable timer underflow interrupt factor flag			0	R/(W)	
	D6	FTC1	16-bit programmable timer 1 compare match interrupt factor flag	(R) Interrupt factor has generated	(R) Interrupt factor has not generated	0	R/(W)	
	D5	FTU1	16-bit programmable timer 1 underflow interrupt factor flag			0	R/(W)	
	D4	FTC0	16-bit programmable timer 0 compare match interrupt factor flag			0	R/(W)	
	D3	FTU0	16-bit programmable timer 0 underflow interrupt factor flag			0	R/(W)	
	D2	FSTX	Serial interface transmit completion interrupt factor flag	(W) Reset	(W) Invalid	0	R/(W)	
	D1	FSRX	Serial interface receive completion interrupt factor flag			0	R/(W)	
	D0	FSERR	Serial interface receive error interrupt factor flag			0	R/(W)	
00FF29	D7	FT60S	Clock timer 60 S interrupt factor flag	(R)	(R)	0	R/(W)	
	D6	FCTM1	Clock timer 1 Hz interrupt factor flag	Interrupt	Interrupt	0	R/(W)	
	D5	FCTM2	Clock timer 2 Hz interrupt factor flag	factor has	factor has not	0	R/(W)	
	D4	FCTM8	Clock timer 8 Hz interrupt factor flag	generated	generated	0	R/(W)	
	D3	FCTM32	Clock timer 32 Hz interrupt factor flag			0	R/(W)	
	D2	FLCD	LCD controller interrupt factor flag	(W)	(W)	0	R/(W)	
	D1	–	–	Reset	Invalid	–	–	"0" when being read
	D0	–	–			–	–	

Table 5.1.1(f) I/O Memory map (00FF30H–00FF37H)

Address	Bit	Name	Function		1	0	Init	R/W	Comment
00FF30	D7	MODE16	16-bit PTM 8-/16-bit mode selection		16-bit	8-bit × 2	0	R/W	
	D6	–	–		–	–	–	–	"0" when being read
	D5	–	–		–	–	–	–	
	D4	–	–		–	–	–	–	
	D3	PTOUT0	16-bit PTM0 clock output control		On	Off	0	R/W	
	D2	PTRUN0	16-bit PTM0 RUN/STOP control		Run	Stop	0	R/W	
	D1	PSET0	16-bit PTM0 preset		Preset	Invalid	0	W	"0" when being read
	D0	CKSEL0	16-bit PTM0 input clock selection		External clock	Internal clock	0	R/W	
00FF31	D7	–	–		–	–	–	–	"0" when being read
	D6	–	–		–	–	–	–	
	D5	–	–		–	–	–	–	
	D4	–	–		–	–	–	–	
	D3	PTOUT1	16-bit PTM1 clock output control		On	Off	0	R/W	
	D2	PTRUN1	16-bit PTM1 RUN/STOP control		Run	Stop	0	R/W	
	D1	PSET1	16-bit PTM1 preset		Preset	Invalid	0	W	"0" when being read
	D0	CKSEL1	16-bit PTM1 input clock selection		External clock	Internal clock	0	R/W	
00FF32	D7	RDR07	16-bit programmable timer 0	D7(MSB)			1	R/W	Low-order 8 bits data
	D6	RDR06	reload data register	D6			1	R/W	in 16-bit mode
	D5	RDR05		D5			1	R/W	
	D4	RDR04		D4			1	R/W	
	D3	RDR03		D3			1	R/W	
	D2	RDR02		D2			1	R/W	
	D1	RDR01		D1			1	R/W	
	D0	RDR00		D0(LSB)			1	R/W	
00FF33	D7	RDR17	16-bit programmable timer 1	D7(MSB)			1	R/W	High-order 8 bits data
	D6	RDR16	reload data register	D6			1	R/W	in 16-bit mode
	D5	RDR15		D5			1	R/W	
	D4	RDR14		D4			1	R/W	
	D3	RDR13		D3			1	R/W	
	D2	RDR12		D2			1	R/W	
	D1	RDR11		D1			1	R/W	
	D0	RDR10		D0(LSB)			1	R/W	
00FF34	D7	CDR07	16-bit programmable timer 0	D7(MSB)			0	R/W	Low-order 8 bits data
	D6	CDR06	compare data register	D6			0	R/W	in 16-bit mode
	D5	CDR05		D5			0	R/W	
	D4	CDR04		D4			0	R/W	
	D3	CDR03		D3			0	R/W	
	D2	CDR02		D2			0	R/W	
	D1	CDR01		D1			0	R/W	
	D0	CDR00		D0(LSB)			0	R/W	
00FF35	D7	CDR17	16-bit programmable timer 1	D7(MSB)			0	R/W	High-order 8 bits data
	D6	CDR16	compare data register	D6			0	R/W	in 16-bit mode
	D5	CDR15		D5			0	R/W	
	D4	CDR14		D4			0	R/W	
	D3	CDR13		D3			0	R/W	
	D2	CDR12		D2			0	R/W	
	D1	CDR11		D1			0	R/W	
	D0	CDR10		D0(LSB)			0	R/W	
00FF36	D7	PTM07	16-bit programmable timer 0	D7(MSB)			1	R	Low-order 8 bits data
	D6	PTM06	data register	D6			1	R	in 16-bit mode
	D5	PTM05		D5			1	R	
	D4	PTM04		D4			1	R	
	D3	PTM03		D3			1	R	
	D2	PTM02		D2			1	R	
	D1	PTM01		D1			1	R	
	D0	PTM00		D0(LSB)			1	R	
00FF37	D7	PTM17	16-bit programmable timer 1	D7(MSB)			1	R	High-order 8 bits data
	D6	PTM16	data register	D6			1	R	in 16-bit mode
	D5	PTM15		D5			1	R	
	D4	PTM14		D4			1	R	
	D3	PTM13		D3			1	R	
	D2	PTM12		D2			1	R	
	D1	PTM11		D1			1	R	
	D0	PTM10		D0(LSB)			1	R	

Table 5.1.1(g) I/O Memory map (00FF38H–00FF3AH)

Address	Bit	Name	Function		1	0	Init	R/W	Comment
00FF38	D7	–	–		–	–	–	–	"0" when being read
	D6	–	–		–	–	–	–	
	D5	–	–		–	–	–	–	
	D4	–	–		–	–	–	–	
	D3	–	–		–	–	–	–	
	D2	PTOUT	8-bit programmable timer clock output control		On	Off	0	R/W	
	D1	PSET	8-bit programmable timer preset		Preset	Invalid	–	W	"0" when being read
	D0	PRUN	8-bit programmable timer RUN/STOP control		Run	Stop	0	R/W	
00FF39	D7	RLD7	8-bit programmable timer	D7(MSB)			1	R/W	
	D6	RLD6	reload data register	D6			1	R/W	
	D5	RLD5		D5			1	R/W	
	D4	RLD4		D4			1	R/W	
	D3	RLD3		D3			1	R/W	
	D2	RLD2		D2			1	R/W	
	D1	RLD1		D1			1	R/W	
	D0	RLD0		D0(LSB)			1	R/W	
00FF3A	D7	PTD7	8-bit programmable timer	D7(MSB)			1	R	
	D6	PTD6	data register	D6			1	R	
	D5	PTD5		D5			1	R	
	D4	PTD4		D4			1	R	
	D3	PTD3		D3			1	R	
	D2	PTD2		D2			1	R	
	D1	PTD1		D1			1	R	
	D0	PTD0		D0(LSB)			1	R	

Table 5.1.1(h) I/O Memory map (00FF40H–00FF43H)

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF40	D7	SIOSEL	Serial I/F terminal selection	P14–P17	P10–P13	0	R/W	
	D6	EPR	Serial I/F parity enable	With parity	No parity	0	R/W	
	D5	PMD	Serial I/F parity mode selection	Odd	Even	0	R/W	
	D4	STPB	Serial I/F stop bit selection	2 bits	1 bit	0	R/W	
	D3	–	–	–	–	–	–	"0" when being read
	D2	SMD1	Serial I/F mode selection SMD1 SMD0 Mode 1 1 8-bit asynchronous			0	R/W	
	D1	SMD0	1 0 7-bit asynchronous 0 1 Clock synchronous slave 0 0 Clock synchronous master			0	R/W	
	D0	ESIF	Serial I/F enable	Serial I/F	I/O port	0	R/W	
00FF41	D7	–	–	–	–	–	–	"0" when being read
	D6	FER	Serial I/F framing error flag	Error Reset (0)	No error Invalid	0	R W	
	D5	PER	Serial I/F parity error flag	Error Reset (0)	No error Invalid	0	R W	
	D4	OER	Serial I/F overrun error flag	Error Reset (0)	No error Invalid	0	R W	
	D3	RXTRG	Serial I/F receive trigger/status	Run Trigger	Stop Invalid	0	R W	
	D2	RXEN	Serial I/F receive enable	Enable	Disable	0	R/W	
	D1	TXTRG	Serial I/F transmit trigger/status	Run Trigger	Stop Invalid	0	R W	
	D0	TXEN	Serial I/F transmit enable	Enable	Disable	0	R/W	
00FF42	D7	TRXD7	Serial I/F transmit/receive data register D7(MSB)	High	Low	×	R/W	TRXD7 is invalid in 7-bit asynchronous mode
	D6	TRXD6	D6			×	R/W	
	D5	TRXD5	D5			×	R/W	
	D4	TRXD4	D4			×	R/W	
	D3	TRXD3	D3			×	R/W	
	D2	TRXD2	D2			×	R/W	
	D1	TRXD1	D1			×	R/W	
	D0	TRXD0	D0(LSB)			×	R/W	
00FF43	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	IRTL	IrDA interface output logic inversion	Inverse	Normal	0	R/W	
	D2	IRIL	IrDA interface input logic inversion	Inverse	Normal	0	R/W	
	D1	IRST1	IrDA interface setting IRST1 IRST0 Setting 1 1 Reserved (do not set)			0	R/W	Valid only when SIOSEL = "1" in asynchronous mode
	D0	IRST0	1 0 IrDA interface 0 1 Reserved (do not set) 0 0 Normal interface			0	R/W	

Table 5.1.1(i) I/O Memory map (00FF50H–00FF53H)

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF50	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	–	–	–	–	–	–	
	D1	TMRST	Clock timer reset	Reset	Invalid	–	W	
	D0	TMRUN	Clock timer RUN/STOP	Run	Stop	0	R/W	
00FF51	D7	TMD7	Clock timer data 1 Hz	High	Low	0	R	
	D6	TMD6	Clock timer data 2 Hz			0	R	
	D5	TMD5	Clock timer data 4 Hz			0	R	
	D4	TMD4	Clock timer data 8 Hz			0	R	
	D3	TMD3	Clock timer data 16 Hz			0	R	
	D2	TMD2	Clock timer data 32 Hz			0	R	
	D1	TMD1	Clock timer data 64 Hz			0	R	
	D0	TMD0	Clock timer data 128 Hz			0	R	
00FF52	D7	–	–	–	–	–	–	"0" when being read
	D6	TMMD6	Clock timer data 10 sec (BCD)			0	R/W	
	D5	TMMD5				0	R/W	
	D4	TMMD4				0	R/W	
	D3	TMMD3	Clock timer data 1 sec (BCD)			0	R/W	
	D2	TMMD2				0	R/W	
	D1	TMMD1				0	R/W	
	D0	TMMD0				0	R/W	
00FF53	D7	WRWD	EWD, WDCL write enable	Write enable	Write disable	0	R/W	∗1
	D6	EWD	Watchdog timer NMI enable	NMI enable	NMI disable	1	R/W	∗1
	D5	WDCL	Watchdog timer input clock selection	f_{OSC3}/16	f_{OSC1}/16	0	R/W	∗1
	D4	–	–	–	–	–	–	"0" when being read
	D3	–	–	–	–	–	–	
	D2	–	–	–	–	–	–	
	D1	–	–	–	–	–	–	
	D0	WDRST	Watchdog timer reset	Reset	Invalid	–	W	

∗1 Writing to EWD or WDCL is valid after "1" is written to WRWD. WRWD is automatically returns to "0" after writing to EWD or WDCL.

Table 5.1.1(j) I/O Memory map (00FF54H, 00FF55H)

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF54	D7	–	–	–	–	–	–	"0" when being read
	D6	BZSTP	One-shot buzzer forcibly stop	Forcibly stop	No operation	–	W	
	D5	BZSHT	One-shot buzzer trigger/status	Busy	Ready	0	R	
				Trigger	No operation	0	W	
	D4	SHTPW	One-shot buzzer duration width selection	125 msec	31.25 msec	0	R/W	
	D3	ENRTM	Envelope attenuation time	1 sec	0.5 sec	0	R/W	
	D2	ENRST	Envelope reset	Reset	No operation	–	W	"0" when being read
	D1	ENON	Envelope On/Off control	On	Off	0	R/W	∗1
	D0	BZON	Buzzer output control	On	Off	0	R/W	
00FF55	D7	–	–	–	–	–	–	"0" when being read
	D6	DUTY2	Buzzer signal duty ratio selection			0	R/W	
	D5	DUTY1				0	R/W	
	D4	DUTY0				0	R/W	
	D3	–	–	–	–	–	–	"0" when being read
	D2	BZFQ2	Buzzer frequency selection			0	R/W	
	D1	BZFQ1				0	R/W	
	D0	BZFQ0				0	R/W	

DUTY2–1 / Buzzer frequency (Hz)

2	1	0	4096.0 2048.8	3276.8 1638.4	2730.7 1365.3	2340.6 1170.3
0	0	0	8/16	8/20	12/24	12/28
0	0	1	7/16	7/20	11/24	11/28
0	1	0	6/16	6/20	10/24	10/28
0	1	1	5/16	5/20	9/24	9/28
1	0	0	4/16	4/20	8/24	8/28
1	0	1	3/16	3/20	7/24	7/28
1	1	0	2/16	2/20	6/24	6/28
1	1	1	1/16	1/20	5/24	5/28

Buzzer frequency selection

BZFQ2	BZFQ1	BZFQ0	Frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

∗1 ENON is reset to "0" during one-shot output.

Table 5.1.1(k) I/O Memory map (00FF56H)

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF56	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	SVD1	SVD criteria voltage setting			0	R/W	
	D2	SVD0				0	R/W	
	D1	SVDDT	SVD data	Low	Normal	0	R	
	D0	SCDON	SVD On/Off control	On	Off	0	R/W	

SVD1	SVD0	Voltage (V)
1	×	3.4 V
0	1	2.8 V
0	0	1.9 V

Table 5.1.1(l) I/O Memory map (00FF60H–00FF65H)

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF60	D7	DISP	Display On/Off control	On	Off	0	R/W	
	D6	REV	Normal/Inverse display control	Inverse	Normal	0	R/W	
	D5	CKCN2	Scanning line frequency selection			0	R/W	
	D4	CKCN1	CKCN2 CKCN1 CKCN0 POINT5 Frequency 0 0 0 0 fosc1 0 0 0 1 fosc1 / 1.5 0 0 1 0 fosc1 / 2 0 0 1 1 fosc1 / 2.5 0 1 0 0 fosc1 / 3 0 1 0 1 fosc1 / 3.5 0 1 1 0 fosc1 / 4			0	R/W	
	D3	CKCN0	0 1 1 1 fosc1 / 4.5 1 0 0 0 fosc1 / 5 1 0 0 1 fosc1 / 5.5 1 0 1 0 fosc1 / 6 1 0 1 1 fosc1 / 6.5			0	R/W	
	D2	POINT5	1 1 0 0 fosc1 / 7 1 1 0 1 fosc1 / 7.5 1 1 1 0 fosc1 / 8 1 1 1 1 fosc1 / 8.5			0	R/W	
	D1	GRAY	Gray/B&W mode selection	Gray	B&W	0	R/W	
	D0	BITNO	8-bit/4-bit transfer selection	8 bits	4 bits	0	R/W	
00FF61	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	S1570AS	Hardware auto-transfer status	Busy	Standby	0	R	
	D3	LCDEN	LCD power On/Off control	On	Off	0	R/W	
	D2	S1570A	Hardware auto-transfer control	On	Off	0	R/W	
	D1	S1570O	One-shot transfer trigger/status	Busy	Standby	0	R	
				Trigger	Invalid	0	W	
	D0	S1606	Continuous refresh transfer control	On	Off	1	R/W	
00FF62	D7	–	–	–	–	–	–	"0" when being read
	D6	LBC6	Number of bytes per display line D6(MSB)	High	Low	0	R/W	
	D5	LBC5	D5			0	R/W	
	D4	LBC4	D4			0	R/W	
	D3	LBC3	D3			0	R/W	
	D2	LBC2	D2			0	R/W	
	D1	LBC1	D1			0	R/W	
	D0	LBC0	D0(LSB)			0	R/W	
00FF63	D7	SAD7	Display start address (lower 8 bits) D7	High	Low	0	R/W	
	D6	SAD6	D6			0	R/W	
	D5	SAD5	D5			0	R/W	
	D4	SAD4	D4			0	R/W	
	D3	SAD3	D3			0	R/W	
	D2	SAD2	D2			0	R/W	
	D1	SAD1	D1			0	R/W	
	D0	SAD0	D0			0	R/W	
00FF64	D7	SAD15	Display start address (upper 8 bits) D15	High	Low	0	R/W	
	D6	SAD14	D14			0	R/W	
	D5	SAD13	D13			0	R/W	
	D4	SAD12	D12			0	R/W	
	D3	SAD11	D11			0	R/W	
	D2	SAD10	D10			0	R/W	
	D1	SAD9	D9			0	R/W	
	D0	SAD8	D8			0	R/W	
00FF65	D7	SLT7	Total display lines D7	High	Low	0	R/W	
	D6	SLT6	D6			0	R/W	
	D5	SLT5	D5			0	R/W	
	D4	SLT4	D4			0	R/W	
	D3	SLT3	D3			0	R/W	
	D2	SLT2	D2			0	R/W	
	D1	SLT1	D1			0	R/W	
	D0	SLT0	D0			0	R/W	

Table 5.1.1(m) I/O Memory map (00FF66H–00FF6AH)

Address	Bit	Name	Function		1	0	Init	R/W	Comment
00FF66	D7	–	–		–	–	–	–	"0" when being read
	D6	–	–		–	–	–	–	
	D5	–	–		–	–	–	–	
	D4	–	–		–	–	–	–	
	D3	–	–		–	–	–	–	
	D2	–	–		–	–	–	–	
	D1	–	–		–	–	–	–	
	D0	SLT8	Total display lines (MSB)		High	Low	0	R/W	
00FF67	D7	APADJ7	Address pitch adjustment	D7	High	Low	0	R/W	
	D6	APADJ6		D6			0	R/W	
	D5	APADJ5		D5			0	R/W	
	D4	APADJ4		D4			0	R/W	
	D3	APADJ3		D3			0	R/W	
	D2	APADJ2		D2			0	R/W	
	D1	APADJ1		D1			0	R/W	
	D0	APADJ0		D0			0	R/W	
00FF68	D7	GS17	Gray scale (0,1) conversion code	D7	High	Low	0	R/W	
	D6	GS16		D6			0	R/W	
	D5	GS15		D5			0	R/W	
	D4	GS14		D4			0	R/W	
	D3	GS13		D3			0	R/W	
	D2	GS12		D2			0	R/W	
	D1	GS11		D1			0	R/W	
	D0	GS10		D0			0	R/W	
00FF69	D7	GS27	Gray scale (1,0) conversion code	D7	High	Low	0	R/W	
	D6	GS26		D6			0	R/W	
	D5	GS25		D5			0	R/W	
	D4	GS24		D4			0	R/W	
	D3	GS23		D3			0	R/W	
	D2	GS22		D2			0	R/W	
	D1	GS21		D1			0	R/W	
	D0	GS20		D0			0	R/W	
00FF6A	D7	GS37	Gray scale (1,1) conversion code	D7	High	Low	0	R/W	
	D6	GS36		D6			0	R/W	
	D5	GS35		D5			0	R/W	
	D4	GS34		D4			0	R/W	
	D3	GS33		D3			0	R/W	
	D2	GS32		D2			0	R/W	
	D1	GS31		D1			0	R/W	
	D0	GS30		D0			0	R/W	

Table 5.1.1(n) I/O Memory map (00FF70H–00FF77H)

Address	Bit	Name	Function		1	0	Init	R/W	Comment
00FF70	D7	MA0A07	Match address set 0	A07	High	Low	0	R/W	Address match jump 0 does not occur when FF71 and FF70 are set to 0000H.
	D6	MA0A06	Address (Lower 8 bits)	A06			0	R/W	
	D5	MA0A05		A05			0	R/W	
	D4	MA0A04		A04			0	R/W	
	D3	MA0A03		A03			0	R/W	
	D2	MA0A02		A02			0	R/W	
	D1	MA0A01		A01			0	R/W	
	D0	MA0A00		A00			0	R/W	
00FF71	D7	MA0A15	Match address set 0	A15	High	Low	0	R/W	Address match jump 0 does not occur when FF71 and FF70 are set to 0000H.
	D6	MA0A14	Address (Upper 8 bits)	A14			0	R/W	
	D5	MA0A13		A13			0	R/W	
	D4	MA0A12		A12			0	R/W	
	D3	MA0A11		A11			0	R/W	
	D2	MA0A10		A10			0	R/W	
	D1	MA0A09		A09			0	R/W	
	D0	MA0A08		A08			0	R/W	
00FF72	D7	MA1A07	Match address set 1	A07	High	Low	0	R/W	Address match jump 1 does not occur when FF73 and FF72 are set to 0000H.
	D6	MA1A06	Address (Lower 8 bits)	A06			0	R/W	
	D5	MA1A05		A05			0	R/W	
	D4	MA1A04		A04			0	R/W	
	D3	MA1A03		A03			0	R/W	
	D2	MA1A02		A02			0	R/W	
	D1	MA1A01		A01			0	R/W	
	D0	MA1A00		A00			0	R/W	
00FF73	D7	MA1A15	Match address set 1	A15	High	Low	0	R/W	Address match jump 1 does not occur when FF73 and FF72 are set to 0000H.
	D6	MA1A14	Address (Upper 8 bits)	A14			0	R/W	
	D5	MA1A13		A13			0	R/W	
	D4	MA1A12		A12			0	R/W	
	D3	MA1A11		A11			0	R/W	
	D2	MA1A10		A10			0	R/W	
	D1	MA1A09		A09			0	R/W	
	D0	MA1A08		A08			0	R/W	
00FF74	D7	MA2A07	Match address set 2	A07	High	Low	0	R/W	Address match jump 2 does not occur when FF75 and FF74 are set to 0000H.
	D6	MA2A06	Address (Lower 8 bits)	A06			0	R/W	
	D5	MA2A05		A05			0	R/W	
	D4	MA2A04		A04			0	R/W	
	D3	MA2A03		A03			0	R/W	
	D2	MA2A02		A02			0	R/W	
	D1	MA2A01		A01			0	R/W	
	D0	MA2A00		A00			0	R/W	
00FF75	D7	MA2A15	Match address set 2	A15	High	Low	0	R/W	Address match jump 2 does not occur when FF75 and FF74 are set to 0000H.
	D6	MA2A14	Address (Upper 8 bits)	A14			0	R/W	
	D5	MA2A13		A13			0	R/W	
	D4	MA2A12		A12			0	R/W	
	D3	MA2A11		A11			0	R/W	
	D2	MA2A10		A10			0	R/W	
	D1	MA2A09		A09			0	R/W	
	D0	MA2A08		A08			0	R/W	
00FF76	D7	MA3A07	Match address set 3	A07	High	Low	0	R/W	Address match jump 3 does not occur when FF77 and FF76 are set to 0000H.
	D6	MA3A06	Address (Lower 8 bits)	A06			0	R/W	
	D5	MA3A05		A05			0	R/W	
	D4	MA3A04		A04			0	R/W	
	D3	MA3A03		A03			0	R/W	
	D2	MA3A02		A02			0	R/W	
	D1	MA3A01		A01			0	R/W	
	D0	MA3A00		A00			0	R/W	
00FF77	D7	MA3A15	Match address set 3	A15	High	Low	0	R/W	Address match jump 3 does not occur when FF77 and FF76 are set to 0000H.
	D6	MA3A14	Address (Upper 8 bits)	A14			0	R/W	
	D5	MA3A13		A13			0	R/W	
	D4	MA3A12		A12			0	R/W	
	D3	MA3A11		A11			0	R/W	
	D2	MA3A10		A10			0	R/W	
	D1	MA3A09		A09			0	R/W	
	D0	MA3A08		A08			0	R/W	

Table 5.1.1(o) I/O Memory map (00FFC0H–00FFC4H)

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FFC0	D7	SIK07	K07 interrupt selection register	Interrupt is enabled	Interrupt is disabled	0	R/W	
	D6	SIK06	K06 interrupt selection register			0	R/W	
	D5	SIK05	K05 interrupt selection register			0	R/W	
	D4	SIK04	K04 interrupt selection register			0	R/W	
	D3	SIK03	K03 interrupt selection register			0	R/W	
	D2	SIK02	K02 interrupt selection register			0	R/W	
	D1	SIK01	K01 interrupt selection register			0	R/W	
	D0	SIK00	K00 interrupt selection register			0	R/W	
00FFC1	D7	KCP07	K07 input comparison register	Falling edge generates interrupt	Rising edge generates interrupt	1	R/W	
	D6	KCP06	K06 input comparison register			1	R/W	
	D5	KCP05	K05 input comparison register			1	R/W	
	D4	KCP04	K04 input comparison register			1	R/W	
	D3	KCP03	K03 input comparison register			1	R/W	
	D2	KCP02	K02 input comparison register			1	R/W	
	D1	KCP01	K01 input comparison register			1	R/W	
	D0	KCP00	K00 input comparison register			1	R/W	
00FFC2	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	KCP13	K13 input comparison register	Falling edge generates interrupt	Rising edge generates interrupt	1	R/W	
	D2	KCP12	K12 input comparison register			1	R/W	
	D1	KCP11	K11 input comparison register			1	R/W	
	D0	KCP10	K10 input comparison register			1	R/W	
00FFC3	D7	K07D	K07 input port data	High	Low	–	R	
	D6	K06D	K06 input port data			–	R	
	D5	K05D	K05 input port data			–	R	
	D4	K04D	K04 input port data			–	R	
	D3	K03D	K03 input port data			–	R	
	D2	K02D	K02 input port data			–	R	
	D1	K01D	K01 input port data			–	R	
	D0	K00D	K00 input port data			–	R	
00FFC4	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	K13D	K13 input port data	High	Low	–	R	
	D2	K12D	K12 input port data			–	R	
	D1	K11D	K11 input port data			–	R	
	D0	K10D	K10 input port data			–	R	

Table 5.1.1(p) I/O Memory map (00FFD0H–00FFD4H)

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FFD0	D7	HZR07	R07 high impedance control register	High impedance	Complementary	1	R/W	
	D6	HZR06	R06 high impedance control register			1	R/W	
	D5	HZR05	R05 high impedance control register			1	R/W	
	D4	HZR04	R04 high impedance control register			1	R/W	
	D3	HZR03	R03 high impedance control register			1	R/W	
	D2	HZR02	R02 high impedance control register			1	R/W	
	D1	HZR01	R01 high impedance control register			1	R/W	
	D0	HZR00	R00 high impedance control register			1	R/W	
00FFD1	D7	HZR17	R17 high impedance control register	High impedance	Complementary	1	R/W	
	D6	HZR16	R16 high impedance control register			1	R/W	
	D5	HZR15	R15 high impedance control register			1	R/W	
	D4	HZR14	R14 high impedance control register			1	R/W	
	D3	HZR13	R13 high impedance control register			1	R/W	
	D2	HZR12	R12 high impedance control register			1	R/W	
	D1	HZR11	R11 high impedance control register			1	R/W	
	D0	HZR10	R10 high impedance control register			1	R/W	
00FFD2	D7	HZR27	R27 high impedance control register	High impedance	Complementary	1	R/W	
	D6	HZR26	R26 high impedance control register			1	R/W	
	D5	HZR25	R25 high impedance control register			1	R/W	
	D4	HZR24	R24 high impedance control register			1	R/W	
	D3	HZR23	R23 high impedance control register			1	R/W	
	D2	HZR22	R22 high impedance control register			1	R/W	
	D1	HZR21	R21 high impedance control register			1	R/W	
	D0	HZR20	R20 high impedance control register			1	R/W	
00FFD3	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	HZR32	R32 high impedance control register	High impedance	Complementary	1	R/W	
	D1	HZR31	R31 high impedance control register			1	R/W	
	D0	HZR30	R30 high impedance control register			1	R/W	
00FFD4	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	HZR42	R42 high impedance control register	High impedance	Complementary	1	R/W	
	D1	HZR41	R41 high impedance control register			1	R/W	
	D0	HZR40	R40 high impedance control register			1	R/W	

Table 5.1.1(q) I/O Memory map (00FFD5H–00FFD9H)

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FFD5	D7	R07D	R07 output port data register	High	Low	1	R/W	
	D6	R06D	R06 output port data register			1	R/W	
	D5	R05D	R05 output port data register			1	R/W	
	D4	R04D	R04 output port data register			1	R/W	
	D3	R03D	R03 output port data register			1	R/W	
	D2	R02D	R02 output port data register			1	R/W	
	D1	R01D	R01 output port data register			1	R/W	
	D0	R00D	R00 output port data register			1	R/W	
00FFD6	D7	R17D	R17 output port data register	High	Low	1	R/W	
	D6	R16D	R16 output port data register			1	R/W	
	D5	R15D	R15 output port data register			1	R/W	
	D4	R14D	R14 output port data register			1	R/W	
	D3	R13D	R13 output port data register			1	R/W	
	D2	R12D	R12 output port data register			1	R/W	
	D1	R11D	R11 output port data register			1	R/W	
	D0	R10D	R10 output port data register			1	R/W	
00FFD7	D7	R27D	R27 output port data register	High	Low	1	R/W	
	D6	R26D	R26 output port data register			1	R/W	
	D5	R25D	R25 output port data register			1	R/W	
	D4	R24D	R24 output port data register			1	R/W	
	D3	R23D	R23 output port data register			1	R/W	
	D2	R22D	R22 output port data register			1	R/W	
	D1	R21D	R21 output port data register			1	R/W	
	D0	R20D	R20 output port data register			1	R/W	
00FFD8	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	R32D	R32 output port data register	High	Low	1	R/W	
	D1	R31D	R31 output port data register			1	R/W	
	D0	R30D	R30 output port data register			1	R/W	
00FFD9	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	R42D	R42 output port data register	High	Low	1	R/W	
	D1	R41D	R41 output port data register			1	R/W	
	D0	R40D	R40 output port data register			1	R/W	

Table 5.1.1(r) I/O Memory map (00FFE0H–00FFE5H)

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FFE0	D7	IOC07	P07 I/O control register	Output	Input	0	R/W	
	D6	IOC06	P06 I/O control register			0	R/W	
	D5	IOC05	P05 I/O control register			0	R/W	
	D4	IOC04	P04 I/O control register			0	R/W	
	D3	IOC03	P03 I/O control register			0	R/W	
	D2	IOC02	P02 I/O control register			0	R/W	
	D1	IOC01	P01 I/O control register			0	R/W	
	D0	IOC00	P00 I/O control register			0	R/W	
00FFE1	D7	IOC17	P17 I/O control register	Output	Input	0	R/W	
	D6	IOC16	P16 I/O control register			0	R/W	
	D5	IOC15	P15 I/O control register			0	R/W	
	D4	IOC14	P14 I/O control register			0	R/W	
	D3	IOC13	P13 I/O control register			0	R/W	
	D2	IOC12	P12 I/O control register			0	R/W	
	D1	IOC11	P11 I/O control register			0	R/W	
	D0	IOC10	P10 I/O control register			0	R/W	
00FFE2	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	IOC23	P23 I/O control register	Output	Input	0	R/W	
	D2	IOC22	P22 I/O control register			0	R/W	
	D1	IOC21	P21 I/O control register			0	R/W	
	D0	IOC20	P20 I/O control register			0	R/W	
00FFE3	D7	IOC37	P37 I/O control register	Output	Input	0	R/W	
	D6	IOC36	P36 I/O control register			0	R/W	
	D5	IOC35	P35 I/O control register			0	R/W	
	D4	IOC34	P34 I/O control register			0	R/W	
	D3	IOC33	P33 I/O control register			0	R/W	
	D2	IOC32	P32 I/O control register			0	R/W	
	D1	IOC31	P31 I/O control register			0	R/W	
	D0	IOC30	P30 I/O control register			0	R/W	
00FFE4	D7	P07D	P07 I/O port data register	High	Low	1	R/W	
	D6	P06D	P06 I/O port data register			1	R/W	
	D5	P05D	P05 I/O port data register			1	R/W	
	D4	P04D	P04 I/O port data register			1	R/W	
	D3	P03D	P03 I/O port data register			1	R/W	
	D2	P02D	P02 I/O port data register			1	R/W	
	D1	P01D	P01 I/O port data register			1	R/W	
	D0	P00D	P00 I/O port data register			1	R/W	
00FFE5	D7	P17D	P17 I/O port data register	High	Low	1	R/W	
	D6	P16D	P16 I/O port data register			1	R/W	
	D5	P15D	P15 I/O port data register			1	R/W	
	D4	P14D	P14 I/O port data register			1	R/W	
	D3	P13D	P13 I/O port data register			1	R/W	
	D2	P12D	P12 I/O port data register			1	R/W	
	D1	P11D	P11 I/O port data register			1	R/W	
	D0	P10D	P10 I/O port data register			1	R/W	

Note: At initial reset, the data registers at addresses "00FFE4H" and "00FFE5H" are set to "1".

Table 5.1.1(s) I/O Memory map (00FFE6H, 00FFE7H)

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FFE6	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	P23D	P23 I/O port data register	High	Low	1	R/W	
	D2	P22D	P22 I/O port data register			1	R/W	
	D1	P21D	P21 I/O port data register			1	R/W	
	D0	P20D	P20 I/O port data register			1	R/W	
00FFE7	D7	P37D	P37 I/O port data register	High	Low	1	R/W	
	D6	P36D	P36 I/O port data register			1	R/W	
	D5	P35D	P35 I/O port data register			1	R/W	
	D4	P34D	P34 I/O port data register			1	R/W	
	D3	P33D	P33 I/O port data register			1	R/W	
	D2	P32D	P32 I/O port data register			1	R/W	
	D1	P31D	P31 I/O port data register			1	R/W	
	D0	P30D	P30 I/O port data register			1	R/W	

Note: At initial reset, the data register at addresses "00FFE6H" and "00FFE7H" are set to "1".

5.2 System Controller and Bus Control

The system controller is a control unit which sets the bus mode according to the system configuration such as the external memory.
The software can set the following items to control the system.

(1) Bus mode (CPU mode)
(2) Chip enable ($\overline{CE}$) signal output
(3) WAIT state for external memory

The following explains the settings.

5.2.1 Bus mode settings

The S1C88408 has four bus modes as shown in Section 3.5.2, "Bus mode". The bus mode should be set according to the capacity of the memory expanded.

The bus mode can be set by writing to the BSMD register (two bits) as shown in Table 5.2.1.1.

At initial reset, the bus mode is set as follows:

MCU mode:

At initial reset, the S1C88408 is set in the single chip mode.
Accordingly, the system is activated by the program written to the internal ROM in the MCU mode even if the external memory has been expanded.
When the external memory has been expanded, set the corresponding bus mode with the initial routine written in the internal ROM.

MPU mode:

When the MPU mode is used, the expanded mode (expanded 64K mode, expanded 4M minimum mode or expanded 4M maximum mode) at initial reset, has to have been previously selected by the mask option.
Set it according to the system configuration.

The function of I/O terminals is set as shown in Table 5.2.1.2 depending on the mode selection.

Table 5.2.1.1 Bus mode settings

Setting value		Bus mode	Configuration of external memory
BSMD1	BSMD0		
1	1	Expanded 4M maximum mode	ROM+RAM>64K bytes (Program>64K bytes)
1	0	Expanded 4M minimum mode	ROM+RAM>64K bytes (Program≤64K bytes)
0	1	Expanded 64K mode	ROM+RAM≤64K bytes
0	0	Single chip mode (MCU)	None
		Optional setting of one of the expanded modes (MPU)	See above

∗ The single chip mode can be set only when the S1C88408 is used in the MCU mode.

In the MPU mode, the single chip mode cannot be set since the MPU mode does not use the internal ROM.

When using the S1C88408 in the MPU mode, it is necessary to select the bus mode at initial reset (and when the BSMD register is set to "0") by mask option from the three types of expanded modes: expanded 64K mode, expanded 4M minimum mode and expanded 4M maximum mode.
Select the expanded 4M maximum mode, when the MPU mode is not used.

Table 5.2.1.2 I/O terminal settings

Terminal	Bus mode		
	Single chip	Expanded 64K	Expanded 4M
R00	Output port R00	Address bus A0	
R01	Output port R01	Address bus A1	
R02	Output port R02	Address bus A2	
R03	Output port R03	Address bus A3	
R04	Output port R04	Address bus A4	
R05	Output port R05	Address bus A5	
R06	Output port R06	Address bus A6	
R07	Output port R07	Address bus A7	
R10	Output port R10	Address bus A8	
R11	Output port R11	Address bus A9	
R12	Output port R12	Address bus A10	
R13	Output port R13	Address bus A11	
R14	Output port R14	Address bus A12	
R15	Output port R15	Address bus A13	
R16	Output port R16	Address bus A14	
R17	Output port R17	Address bus A15	
R20	Output port R20		Address bus A16
R21	Output port R21		Address bus A17
R22	Output port R22		Address bus A18
R23	Output port R23		Address bus A19
R24	Output port R24		Address bus A20
R25	Output port R25		Address bus A21
R26	Output port R26	$\overline{RD}$ signal	
R27	Output port R27	$\overline{WR}$ signal	
P00	I/O port P00	Data bus D0	
P01	I/O port P01	Data bus D1	
P02	I/O port P02	Data bus D2	
P03	I/O port P03	Data bus D3	
P04	I/O port P04	Data bus D4	
P05	I/O port P05	Data bus D5	
P06	I/O port P06	Data bus D6	
P07	I/O port P07	Data bus D7	

5.2.2 Address decoder ($\overline{CE}$ output) settings

As explained in Section 3.6.4, the S1C88408 has a built-in address decoder that can output up to three chip enable signals ($\overline{CE0}$–$\overline{CE2}$) to external devices.

The output terminals and output circuits for $\overline{CE0}$–$\overline{CE2}$ are shared with the output ports R30–R32. At initial reset, they are set as the $\overline{CE}$ terminals. Unused $\overline{CE}$ terminals can be set to general-purpose output port terminals by writing "0" to the CE0–CE2 registers.
Table 5.2.2.1 shows the address range assigned to the chip enable ($\overline{CE}$) signals.
External devices can be allocated to an area selected with an optional chip enable signal.

It is not necessary to continue from a lower address of the memory space. However in the MPU mode, the program memory must be assigned to $\overline{CE0}$.
In the expanded 4M mode, the address range of each $\overline{CE}$ signal is fixed.
In the expanded 64K mode, four address ranges can be selected using the CEMD register (two bits) according to the memory to be used.

These signals are output only when the corresponding external memory area is accessed and are not output when the internal memory is accessed. Furthermore, when the CPU is in standby status (HALT, SLEEP), all the $\overline{CE}$ signals go HIGH to disable external memory access.

Table 5.2.2.1 Address settings of $\overline{CE0}$–$\overline{CE2}$

(1) Expanded 64K mode + MCU mode

CEMD1	CEMD0	Chip size	$\overline{CE0}$	$\overline{CE1}$	$\overline{CE2}$
1	1	–	–	–	–
1	0	32KB	008000H–00EFFFH	–	–
0	1	16KB	007000H–00AFFFH	00B000H–00EFFFH	–
0	0	8KB	008000H–009FFFH	00A000H–00BFFFH	00C000H–00DFFFH

(2) Expanded 64K mode + MPU mode

CEMD1	CEMD0	Chip size	$\overline{CE0}$	$\overline{CE1}$	$\overline{CE2}$
1	1	64KB	000000H–00EFFFH	–	–
1	0	32KB	000000H–007FFFH	008000H–00EFFFH	–
0	1	16KB	000000H–003FFFH	004000H–007FFFH	008000H–00BFFFH
0	0	8KB	000000H–001FFFH	002000H–003FFFH	004000H–005FFFH

(3) Expanded 4M minimum/maximum mode

$\overline{CE}$ signal	Address range	
	MCU mode	MPU mode
$\overline{CE0}$	C00000H–FFFFFFH	000000H–00EFFFH, 010000H–3FFFFFH
$\overline{CE1}$	400000H–7FFFFFH	400000H–7FFFFFH
$\overline{CE2}$	800000H–BFFFFFH	800000H–BFFFFFH

5.2.3 WAIT state settings

In order to guarantee accessing of external low speed devices during high speed operation, the S1C88408 is equipped with a WAIT function that prolongs access time.
The number of wait states to be inserted can be selected from four values by the WT register (two bits) as shown in Table 5.2.3.1.

The WAIT states that are set with software are inserted between the bus cycle states T3 and T4. Note, however, that WAIT states cannot be inserted when an internal register or internal memory are being accessed and when the CPU operates with the OSC1 oscillation clock (see Section 5.4, "Oscillation Circuit").

Consequently, WAIT state settings are invalid in the single chip mode.

Table 5.2.3.1 Setting the number of WAIT states

WT1	WT0	Number of inserted states
1	1	12
1	0	8
0	1	4
0	0	No wait

* The length of one state is 1/2 a cycle of the clock.

Refer to Section 3.6.5, "WAIT control", for the timing chart for WAIT insertion.

5.2.4 I/O memory of system controller

Table 5.2.4.1 shows the control bits for the system controller.

Table 5.2.4.1 System controller control bits

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF00 MCU mode	D7	BSMD1	Bus mode (CPU mode) selection BSMD1 BSMD0 Mode 1 1 4M(Maximum) 1 0 4M(Minimum) 0 1 64K 0 0 Single chip			0	R/W	
	D6	BSMD0				0	R/W	
	D5	CEMD1	Expanded 64K chip enable mode CEMD1 CEMD0 Mode 1 1 – 1 0 32K($\overline{CE0}$) 0 1 16K($\overline{CE0}$, $\overline{CE1}$) 0 0 8K($\overline{CE0}$–$\overline{CE2}$)			1	R/W	Only for 64K bus mode
	D4	CEMD0				1	R/W	
	D3	–	–	–	–	–	–	"0" when being read
	D2	CE2	$\overline{CE2}$(R32)	$\overline{CE2}$ enable	$\overline{CE2}$ disable	1	R/W	In the single chip
	D1	CE1	$\overline{CE1}$(R31) enable: $\overline{CE}$ signal output	$\overline{CE1}$ enable	$\overline{CE1}$ disable	1	R/W	mode, these setting
	D0	CE0	$\overline{CE0}$(R30) disable: DC output (R3x)	$\overline{CE0}$ enable	$\overline{CE0}$ disable	1	R/W	are fixed at DC output
00FF00 MPU mode	D7	BSMD1	Bus mode (CPU mode) selection BSMD1 BSMD0 Mode 1 1 4M(Maximum) 1 0 4M(Minimum) 0 1 64K 0 0 Option selection			*	R/W	Initial setting can be selected from 3 types (64K, 4M min, 4M max) by mask option
	D6	BSMD0				*	R/W	
	D5	CEMD1	Expanded 64K chip enable mode CEMD1 CEMD0 Mode 1 1 64K($\overline{CE0}$) 1 0 32K($\overline{CE0}$, $\overline{CE1}$) 0 1 16K($\overline{CE0}$–$\overline{CE2}$) 0 0 8K($\overline{CE0}$–$\overline{CE2}$)			1	R/W	Only for 64K bus mode
	D4	CEMD0				1	R/W	
	D3	–	–	–	–	–	–	"0" when being read
	D2	CE2	$\overline{CE2}$(R32)	$\overline{CE2}$ enable	$\overline{CE2}$ disable	1	R/W	
	D1	CE1	$\overline{CE1}$(R31) enable: $\overline{CE}$ signal output	$\overline{CE1}$ enable	$\overline{CE1}$ disable	1	R/W	
	D0	CE0	$\overline{CE0}$(R30) disable: DC output (R3x)	$\overline{CE0}$ enable	$\overline{CE0}$ disable	1	R/W	
00FF01	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	WT1	Wait state control WT1 WT0 Number of states 1 1 12(3 cycles) 1 0 8(2 cycles) 0 1 4(1 cycle) 0 0 No wait			0	R/W	
	D4	WT0				0	R/W	
	D3	CLKCHG	CPU operating clock switch	OSC3	OSC1	0	R/W	
	D2	OSCC	OSC3 oscillation ON/OFF control	On	Off	0	R/W	
	D1	VD1C1	V_{D1} output level setting VD1C1 VD1C0 V_{D1} (Typ.) 1 × 3.2 V 0 1 1.6 V 0 0 2.4 V			0	R/W	
	D0	VD1C0				0	R/W	

Note: All the interrupts including NMI are masked until the appropriate values are written to both the "00FF00H" and "00FF01H" addresses.

BSMD0, BSMD1: Bus mode selection register (00FF00H•D6, D7)

Sets the bus mode as shown in Table 5.2.4.2.

Table 5.2.4.2 Bus mode settings

Setting value		Bus mode
BSMD1	BSMD0	
1	1	Expanded 4M maximum mode
1	0	Expanded 4M minimum mode
0	1	Expanded 64K mode
0	0	Single chip mode (MCU)
		Optional setting of one of the expanded mode (MPU)

The single chip mode can be set only when the S1C88408 is used in the MCU mode.
When using the external MPU interface, only the single chip mode can be set.

In the MPU mode, the single chip mode cannot be set since the MPU mode does not use the internal ROM.

When using the S1C88408 in the MPU mode, it is necessary to select the bus mode set at initial reset (and when the BSMD register is set to "0") by mask option from the three types of expanded modes: expanded 64K mode, expanded 4M minimum mode and expanded 4M maximum mode. Select the expanded 4M maximum mode, when the MPU mode is not used.
At initial reset, the BSMD register is set to "0" (single chip mode in the MCU mode or an expanded mode selected by mask option in the MPU mode).

Note: After initial reset, all the interrupts including NMI are masked until the appropriate values are written to the I/O memory addresses "00FF00H" and "00FF01H" to prevent malfunctions that may occur before setting the system configuration. Therefore, write data to the addresses in the initial routine even though operating the S1C88408 in the initial settings (single chip mode). Furthermore, set the stack pointer SP prior to writing so that interrupt processing will operate normally.

CEMD0, CEMD1: Expanded 64K chip enable mode selection register (00FF00H•D4, D5)

Sets the $\overline{CE}$ signal address range (valid only in the expanded 64K mode).
Set this register according to the external memory chip size as shown in Table 5.2.4.3.

Table 5.2.4.3 $\overline{CE}$ signal settings

CEMD1	CEMD0	Address range	Usable terminals	
			MCU mode	MPU mode
1	1	64K bytes	Invalid	$\overline{CE0}$
1	0	32K bytes	$\overline{CE0}$	$\overline{CE0}$, $\overline{CE1}$
0	1	16K bytes	$\overline{CE0}$, $\overline{CE1}$	$\overline{CE0}$–$\overline{CE2}$
0	0	8K bytes	$\overline{CE0}$–$\overline{CE2}$	$\overline{CE0}$–$\overline{CE2}$

This setting is invalid for modes other than the expanded 64K mode.
At initial reset, the CEMD register is set to "11B". However, since "11B" is invalid in the MCU mode, set it to another value.

CE0–CE2: $\overline{CE}$ signal output enable register (00FF00H•D0–D2)

Sets the $\overline{CE}$ output terminals to be used.

When "1" is written: $\overline{CE}$ output enabled
When "0" is written: $\overline{CE}$ output disabled
Reading: Valid

Writing "1" to the CE0–CE2 register enables the corresponding $\overline{CE}$ signal to output.
Writing "0" to the register disables the $\overline{CE}$ signal to output, and the terminal functions as the output port (R30–R32).
At initial reset, the CE registers are all set to "1".

WT0, WT1: WAIT state control register (00FF01H•D4, D5)

Controls the WAIT state insertion.
Table 5.2.4.4 shows the register setting and the number of WAIT states inserted.

Table 5.2.4.4 WAIT state settings

WT1	WT0	Number of inserted states
1	1	12
1	0	8
0	1	4
0	0	No wait

∗ The length of one state is 1/2 a cycle of the clock.

At initial reset, the WT register is set to "0" (no wait).

5.2.5 Programming note

After initial reset, all the interrupts including NMI are masked until the appropriate values are written to the I/O memory addresses "00FF00H" and "00FF01H" to prevent malfunctions that may occur before setting the system configuration. Therefore, write data to the addresses in the initial routine even though the initial settings are used. Furthermore, set the stack pointer SP prior to writing so that interrupt processing will operate normally.

5.3 Watchdog Timer

5.3.1 Configuration of watchdog timer

The S1C88408 has a built-in watchdog timer that detects CPU runaway.

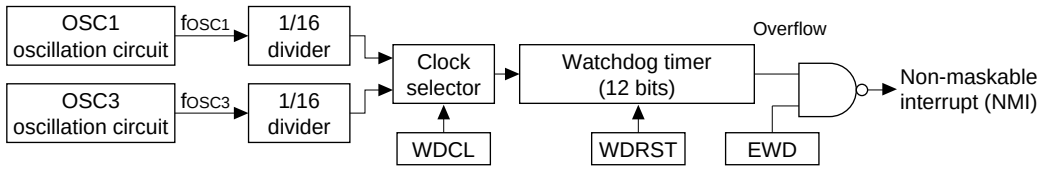


Fig. 5.3.1.1 Block diagram of watchdog timer

The watchdog timer is composed of a 12-bit up-counter that uses the OSC1 or OSC3 oscillation circuit as a clock source. This counter must be reset cyclically by software. If the counter is not reset and an overflow occurs, the watchdog timer generates NMI (non-maskable interrupt) to the CPU.
Figure 5.3.1.1 is a block diagram of the watchdog timer.

5.3.2 Control of watchdog timer

Input clock selection

The input clock of the watchdog timer can be selected using the input clock selection register WDCL from the two listed below.

WDCL = "1": 1/16 OSC1 dividing clock
WDCL = "0": 1/16 OSC3 dividing clock

At initial reset, the input clock is set to f_{OSC1}/16. The following shows an example of a watchdog timer reset cycle according to the input clock selected.

When f_{OSC1}/16 is selected:

f_{OSC1} = 32.768 kHz	within 2 sec

When f_{OSC3}/16 is selected:

f_{OSC3} = 1 MHz	within 64 msec
f_{OSC3} = 6 MHz	within 10 msec
f_{OSC3} = 8 MHz	within 8 msec

The WDCL register is set to write disabling status usually to prevent modification of the reset cycle by a wrong writing. To change the input clock, it is necessary to set the WDCL register in write authorized status by writing "1" to the write enable register WRWD beforehand. The write authorization by the WRWD register enables only one write for the WDCL register. When data is written to the WDCL register after setting in write authorization, the WRWD register returns to "0", and the WDCL register is also returned to write disabling status.

Resetting the watchdog timer

When the watchdog timer is used, it is necessary to reset the counter before an overflow is generated. The watchdog timer is reset by writing "1" to the watchdog timer reset bit WDRST.
By resetting the watchdog timer on the main routine, program runaway that does not pass the reset routine can be detected. Ordinarily this routine is incorporated to a place where it is executed regularly.

Operation in HALT/SLEEP status

(1) HALT status

The OSC1 oscillation circuit and the OSC3 oscillation circuit operate in HALT status. Therefore, the watchdog timer also operates. The watchdog timer generates NMI when HALT status continues more than a reset cycle. HALT status is released at that point.

(2) SLEEP status

The OSC1 oscillation circuit and the OSC3 oscillation circuit stop in SLEEP status. Therefore, the watchdog timer also stops. Since the counter maintains the value at the point it stops, the counter resumes counting from the value after SLEEP status is canceled. However, the oscillation clock becomes unstable immediately after SLEEP is canceled. Therefore, reset the watchdog timer before shifting to SLEEP status and after SLEEP status is canceled so that an unnecessary NMI will not be generated.

When watchdog timer is not used

The watchdog timer always operates unless the oscillation circuit specified for the input clock stops. If monitoring the system by the watchdog timer is unnecessary, it is possible to disable the watchdog timer interrupt (NMI) by writing "0" to the watchdog timer enable register EWD.
At initial reset, the watchdog timer starts counting by inputting the fOSC1 / 16 clock and is set to generate NMI. When the watchdog timer is not used, write "0" to the EWD register before the first overflow is generated.

The EWD register is set to write disabling status same as the WDCL register. Set it in write authorized status using the WRWD register before writing to the EWD register. In this case, only one write is enabled for the EWD register.

5.3.3 Interrupt function

When the watchdog timer is not reset cyclically by software, the watchdog timer outputs an interrupt signal to the NMI (level 4) input of the core CPU. This interrupt cannot be masked and the exception processing has priority over other interrupts.
Refer to the "S1C88 Core CPU Manual" for details of the NMI exception processing.
This exception processing vector address is set to 000004H.

When the EWD register is set to "0", this interrupt is not generated.

5.3.4 I/O memory of watchdog timer

Table 5.3.4.1 shows the control bits for the watchdog timer.

Table 5.3.4.1 Watchdog timer control bits

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF53	D7	WRWD	EWD, WDCL write enable	Write enable	Write disable	0	R/W	*1
	D6	EWD	Watchdog timer NMI enable	NMI enable	NMI disable	1	R/W	*1
	D5	WDCL	Watchdog timer input clock selection	fOSC3/16	fOSC1/16	0	R/W	*1
	D4	–	–	–	–	–	–	"0" when being read
	D3	–	–	–	–	–	–	
	D2	–	–	–	–	–	–	
	D1	–	–	–	–	–	–	
	D0	WDRST	Watchdog timer reset	Reset	Invalid	–	W	

*1 Writing to EWD or WDCL is valid after "1" is written to WRWD. WRWD is automatically returns to "0" after writing to EWD or WDCL.

WRWD: EWD, WDCL write enable register (00FF53H•D7)

Enables writing to the EWD and WDCL register.

When "1" is written: Write is enabled
When "0" is written: Write is disabled
Reading: Valid

The EWD and WDCL registers are set to write disabling status usually to prevent unnecessary modification. When "1" is written to the WRWD register, only one write is permitted. When data is written to either the EWD or WDCL registers or both, the WRWD register returns to "0", and the EWD and WDCL registers go to write disabling status.
Writing "0" to the WRWD register during a write authorized state (WRWD="1") also returns to write disabling status.
At initial reset, the WRWD register is set to "0" (write is disabled).

EWD: NMI enable register (00FF53H•D6)

Controls non-maskable interrupt (NMI) generation by watchdog timer.

When "1" is written: NMI is valid
When "0" is written: NMI is invalid
Reading: Valid

When "0" is written to the EWD register, the watchdog timer interrupt signal is masked and NMI is not generated to the CPU. When the EWD register is set to "1", NMI is generated due to an overflow of the counter.
Writing to the EWD register is effective only when the WRWD register is set to "1".
The count operation is continued even when the EWD register is set to "0" if the clock is input. Therefore, when NMI is invalidated temporarily, reset the watchdog timer before changing back the EWD register to "1".
At initial reset, the EWD register is set to "1" (NMI is valid).

WDCL: Input clock selection register (00FF53H•D5)

Selects the input clock for the watchdog timer.

When "1" is written: f_{OSC3} / 16
When "0" is written: f_{OSC1} / 16
Reading: Valid

When "1" is written to the WDCL register, f_{OSC3} / 16 clock is input to the watchdog timer as the count clock. When "0" is written, f_{OSC1} / 16 clock is input. When f_{OSC3} / 16 clock is used, the watchdog timer stops if the OSC3 oscillation circuit stops (including SLEEP). In this case, the counter value at stop is maintained.
Writing to the WDCL register is effective only when the WRWD register is set to "1".
At initial reset, the WDCL register is set to "0" (f_{OSC1} / 16).

WDRST: Watchdog timer reset (00FF53H•D0)

Resets the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Always "0"

By writing "1" to WDRST, the watchdog timer is reset and restarts immediately after. When "0" is written, no operation results.
WDRST is dedicated for writing, and is always "0" for reading.

5.3.5 Programming notes

(1) When the watchdog timer NMI is authorized, it is necessary to reset the counter by software before an overflow is generated.

(2) At initial reset, the watchdog timer starts counting by inputting the f_{OSC1} / 16 clock and is set to generate NMI. When the watchdog timer is not used, write "0" to the EWD register before the first overflow is generated.

(3) The count operation is continued even when the EWD register is set to "0" if the clock is input. Therefore, when NMI is invalidated temporarily, reset the watchdog timer before changing back the EWD register to "1".

(4) The oscillation clock becomes unstable immediately after SLEEP is canceled. Therefore, reset the watchdog timer before shifting to SLEEP status and after SLEEP status is canceled so that an unnecessary NMI will not be generated.

5.4 Oscillation Circuit

5.4.1 Configuration of oscillation circuit

The S1C88408 has been designed as a twin clock system with two internal oscillation circuits (OSC1 and OSC3). The OSC1 oscillation circuit generates the 32.768 kHz (Typ.) operating clock, and the OSC3 oscillation circuit generates the high-speed clock for the CPU and the peripheral circuits (serial interface, programmable timer, LCD controller, etc.).
Figure 5.4.1.1 shows the configuration of the oscillation circuit.

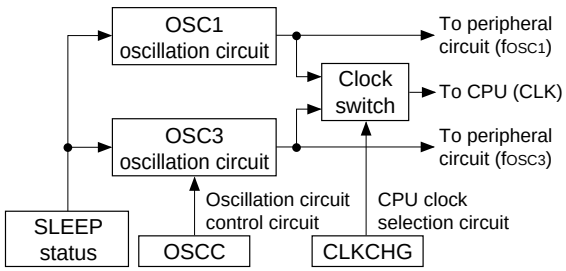


Fig. 5.4.1.1 Configuration of oscillation circuit

At initial reset, the OSC1 oscillation clock is selected for the CPU operating clock.
Turning the OSC3 oscillation circuit on / off and switching the system clock (OSC1↔OSC3) can be controlled by software. The OSC3 oscillation circuit is used when the CPU and the peripheral circuits require high-speed operation. When the CPU has to handle low-speed operation (e.g. clock control), stop the OSC3 oscillation and use OSC1 as the operating clock to reduce current consumption.

5.4.2 Mask option

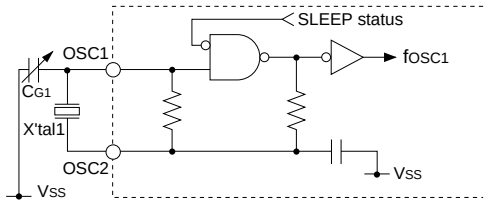
OSC1 oscillation circuit
- ☐ Crystal oscillation circuit
- ☐ CR oscillation circuit
- ☐ External clock input
- ☐ Crystal oscillation circuit (gate capacitor built-in)

OSC3 oscillation circuit
- ☐ Crystal oscillation circuit
- ☐ Ceramic oscillation circuit
- ☐ CR oscillation circuit
- ☐ External clock input

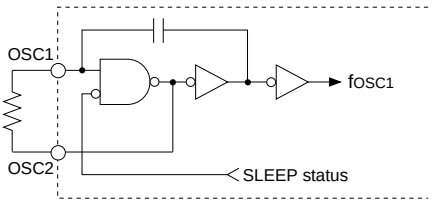
Either "Crystal oscillation", "CR oscillation", "Crystal oscillation (gate capacitor built-in)" or "External clock input" can be selected by mask option as a kind of OSC1 oscillation circuit.
Either "Crystal oscillation", "Ceramic oscillation", "CR oscillation" or "External clock input" can be selected as a kind of OSC3 oscillation circuit same as the OSC1.

5.4.3 OSC1 oscillation circuit

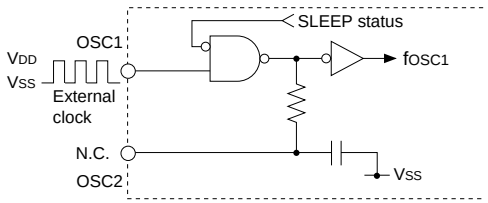
The OSC1 oscillation circuit generates the 32.768 kHz (Typ.) system clock. The OSC1 oscillation clock is used for the low-speed (low power) operation clock of the CPU. Furthermore, it is used as the source clock for the clock timer and watch-dog timer even when OSC3 is used as the system clock. The OSC1 oscillation circuit stops when the SLP instruction is executed.
Either "Crystal oscillation", "CR oscillation", "Crystal oscillation (gate capacitor built-in)" or "External clock input" can be selected by mask option as a kind of OSC1 oscillation circuit.
Figure 5.4.3.1 shows the structure of the OSC1 oscillation circuit.



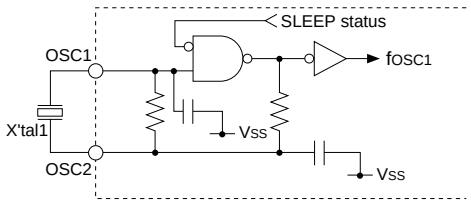
(1) Crystal oscillation circuit



(2) CR oscillation circuit



(3) External clock input



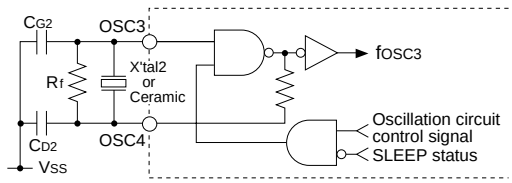
(4) Crystal oscillation circuit (gate capacitor built-in)

Fig. 5.4.3.1 OSC1 oscillation circuit

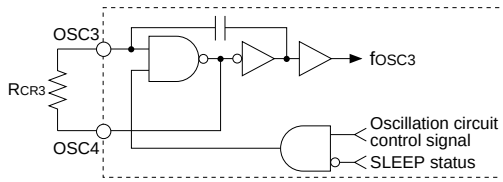
When crystal oscillation is selected, the crystal oscillation circuit can be configured simply by connecting a crystal oscillator X'tal1 (Typ. 32.768 kHz) between the OSC1 and OSC2 terminals and a trimmer capacitor C_{G1} (5–25pF) between the OSC1 terminal and V_{SS}.
For the C_{G1}, the built-in capacitor can also be selected by mask option.
When CR oscillation is selected, the CR oscillation circuit can be configured by connecting a resistor between the OSC1 and OSC2 terminals.
When external clock input is selected, open the OSC2 terminal and input a square wave clock to the OSC1 terminal.

5.4.4 OSC3 oscillation circuit

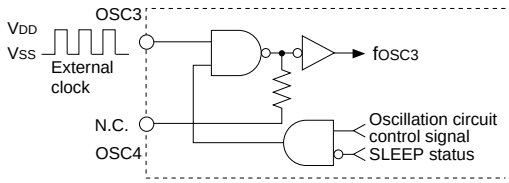
The OSC3 oscillation circuit generates the system clock for the CPU and peripheral circuits (serial interface, programmable timer, LCD controller, etc.). The OSC3 oscillation circuit stops when the SLP instruction is executed, or the OSCC register is set to "0".
Either "Crystal oscillation", "Ceramic oscillation", "CR oscillation" or "External clock input" can be selected by mask option as a kind of OSC3 oscillation circuit.
Figure 5.4.4.1 shows the structure of the OSC3 oscillation circuit.



(1) Crystal/Ceramic oscillation circuit



(2) CR oscillation circuit



(3) External clock input

Fig. 5.4.4.1 OSC3 oscillation circuit

When crystal / ceramic oscillation circuit is selected, the crystal or ceramic oscillation circuit is configured by connecting either a crystal oscillator (X'tal2) or a ceramic oscillator (Ceramic) and a feedback resistor (R_f) between the OSC3 and OSC4 terminals and two capacitors (C_{G2}, C_{D2}) between the OSC3 terminal and V_{SS}, and between the OSC4 terminal and V_{SS}, respectively.
When CR oscillation is selected, the CR oscillation circuit can be configured by connecting a resistor (R_{CR3}) between the OSC3 and OSC4 terminals.
When external clock input is selected, open the OSC4 terminal and input a square wave clock to the OSC3 terminal.
When the OSC3 oscillation circuit is not used, select external clock input by mask option, and pull down the OSC3 terminal to V_{SS}.

The maximum frequency of the clock, which can be generated by the OSC3 oscillation circuit or can be input to the OSC3 oscillation circuit, is limited depending on the supply voltage as shown in Table 5.4.4.1.

Table 5.4.4.1 Limit of OSC3 clock frequency depending on supply voltage

Operable voltage range (V_{DD})	Max. operable frequency
1.8 V–5.5 V	1.1 MHz
2.6 V–5.5 V	4.4 MHz
3.5 V–5.5 V	8.2 MHz

5.4.5 Switching of CPU clock and operating voltage V_{D1}

The OSC3 oscillation circuit can be turned on and off. It should be turned on when operating peripheral circuit (serial interface, programmable timer, LCD controller, etc.) that needs a high-speed clock. Further, the CPU operating clock can be switched from OSC1 to OSC3 to execute the program in high-speed.
In the S1C88408, the internal operating voltage V_{D1} can also be switched by software for stable operation in large supply voltage and operating frequency ranges and for saving power.

Switching operating voltage V_{D1}

When operating the OSC3 oscillation circuit, it is necessary to switch the internal operating voltage V_{D1} according to the oscillation frequency. Table 5.4.5.1 shows the relation between the supply voltage to be used, oscillation frequency and the internal operating voltage V_{D1} that should be set.

Table 5.4.5.1 Oscillation frequency and internal operating voltage V_{D1}

OSC3 oscillator	OSC3 frequency	Supply voltage	V_{D1} 1.6 V	V_{D1} 2.4 V	V_{D1} 3.2 V
OFF	*	1.8–5.5 V	○	△	△
ON	0.03–1.1 MHz	1.8–5.5 V	○	△	△
	0.03–4.4 MHz	2.6–5.5 V	×	○	△
	0.03–8.2 MHz	3.5–5.5 V	×	×	○

* Operation with OSC1 clock
○ Can be set
△ Can be set (However, it increases current consumption)
× Cannot be set

V_{D1} is switched with the V_{D1} level setting register VD1C.

Table 5.4.5.2 V_{D1} settings

VD1C1	VD1C0	Operating voltage V_{D1}
1	×	3.2 V
0	1	1.6 V
0	0	2.4 V

At initial reset, V_{D1} is set to 2.4 V (Typ.). V_{D1} should be switched to 1.6 V (Typ.) when using an OSC3 clock lower than 1.1 MHz or the OSC3 oscillation is stopped.

Note:
- *The V_{D1} level must be switched while the OSC3 oscillation circuit is off (before turning on and after turning off). Switching during operation may cause malfunction.*
- *The V_{D1} voltage required at least 5 msec of voltage stabilizing time after switching. Do not turn the OSC3 oscillation circuit on during this period.*
- *V_{D1} cannot be switched directly to a level that is two or three levels different from the current level. The middle level must be set between switching.*
  To switch from 1,6 (3.2) V to 3.2 (1.6) V:
  1.6 V → 2.4 V → 3.2 V
  1.6 V ← 2.4 V ← 3.2 V
  To switch from 2.4 (3.2) V to 3.2 (2.4) V:
  2.4 V → 3.2 V
  2.4 V ← 3.2 V
  A 5 msec interval is required for each switching step.

Turning the OSC3 oscillation circuit on and off

The OSC3 oscillation circuit can be turned on and off using the OSCC register. It is necessary to switch the V_{D1} voltage.
The switching procedure is as follows. The following procedures are described assuming the V_{D1} has been set to 1.6 V before turning the OSC3 oscillation on.

[OSC3 on sequence]

• OSC3 = 0.03 MHz–1.1 MHz

1. Write "1" to the OSCC register.
   (turning the OSC3 oscillation circuit on)
2. Wait at least 20 msec.

• OSC3 = 0.03 MHz–4.4 MHz

1. Write "00B" to the VD1C register. (V_{D1} = 2.4 V)
2. Wait at least 5 msec.
3. Write "1" to the OSCC register.
   (turning the OSC3 oscillation circuit on)
4. Wait at least 20 msec.

• OSC3 = 0.03 MHz–8.2 MHz

1. Write "00B" to the VD1C register. (V_{D1} = 2.4 V)
2. Wait at least 5 msec.
3. Write "10B" to the VD1C register. (V_{D1} = 3.2 V)
4. Wait at least 5 msec.
5. Write "1" to the OSCC register.
   (turning the OSC3 oscillation circuit on)
6. Wait at least 20 msec.

Note: • *The OSC3 oscillation circuit takes a maximum 20 msec for stabilizing oscillation after turning the OSC3 oscillation circuit on. Therefore, take an enough interval after the OSC3 oscillation goes on before starting control of the peripheral circuit, such as the programmable timer, serial interface and LCD controller, that uses the OSC3 oscillation circuit as the clock source. (The oscillation start time varies depending on the oscillator and external component to be used. Refer to Chapter 8, "ELECTRICAL CHARACTERISTICS", in which an example of oscillation start time is indicated.)*

• *Do not turn the OSC3 oscillation circuit on to reduce current consumption when the OSC3 clock is not necessary.*

[OSC3 off sequence]

• OSC3 = 0.03 MHz–1.1 MHz

1. Write "0" to the OSCC register. (turning the OSC3 oscillation circuit off)

• OSC3 = 0.03 MHz–4.4 MHz

1. Write "0" to the OSCC register. (turning the OSC3 oscillation circuit off)
2. Write "01B" to the VD1C register. (V_{D1} = 1.6 V)

• OSC3 = 0.03 MHz–8.2 MHz

1. Write "0" to the OSCC register. (turning the OSC3 oscillation circuit off)
2. Write "00B" to the VD1C register. (V_{D1} = 2.4 V)
3. Wait at least 5 msec.
4. Write "01B" to the VD1C register. (V_{D1} = 1.6 V)

Note: To prevent malfunction, before stopping the OSC3 oscillation, stop the operation of the peripheral circuits that use the OSC3 oscillation circuit as the clock source, such as programmable timer, serial interface and LCD controller.
Furthermore, when turning the OSC3 oscillation circuit off, make sure that the CPU operating clock is OSC1.

Switching the CPU operating clock from OSC1 to OSC3

When operating the CPU in high speed, the CPU operating clock should be switched from the OSC1 clock to the OSC3 clock using the CLKCHG register. The switching procedure is as follows:

1. Execute the OSC3 on sequence as described above.
2. Write "1" to the CLKCHG register. (OSC1 → OSC3)

Note: Be sure to wait 20 msec or more for oscillation stabilizing time between turning the OSC3 oscillation circuit on and switching the CPU operating clock.

Switching the CPU operating clock from OSC3 to OSC1

When the CPU has to handle low-speed operation (e.g. clock control), the OSC3 oscillation can be stopped and OSC1 can be used as the operating clock to reduce current consumption.
The switching procedure is as follows:

1. Write "0" to the CLKCHG register. (OSC3 → OSC1)
2. Execute the OSC3 off sequence described above.

Note: Use a separate instruction for switching the clock from OSC3 to OSC1 and turning the OSC3 oscillation off. Handling with one instruction may cause malfunction of the CPU.

5.4.6 I/O memory of oscillation circuit

Table 5.4.6.1 shows the control bits for the oscillation circuit.

Table 5.4.6.1 Oscillation circuit control bits

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF01	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	WT1	Wait state control WT1 WT0 Number of states 1 1 12(3 cycles) 1 0 8(2 cycles) 0 1 4(1 cycle) 0 0 No wait			0	R/W	
	D4	WT0				0	R/W	
	D3	CLKCHG	CPU operating clock switch	OSC3	OSC1	0	R/W	
	D2	OSCC	OSC3 oscillation ON/OFF control	On	Off	0	R/W	
	D1	VD1C1	V_{D1} output level setting VD1C1 VD1C0 V_{D1} (Typ.) 1 × 3.2 V 0 1 1.6 V 0 0 2.4 V			0	R/W	
	D0	VD1C0				0	R/W	

VD1C0, VD1C1: V_{D1} output level setting register (00FF01H• D0, D1)

Selects the V_{D1} level.

Table 5.4.6.2 V_{D1} settings

VD1C1	VD1C0	Operating voltage V_{D1}	OSC3 oscillation
1	×	3.2 V	ON (0.03–8.2 MHz)
0	1	1.6 V	ON (0.03–1.1 MHz) or OFF
0	0	2.4 V	ON (0.03–4.4 MHz)

The V_{D1} level should be switched according to the operation of the OSC3 oscillation circuit.

The OSC3 oscillation circuit must be off when switching the V_{D1} voltage.
V_{D1} cannot be switched directly to a level that is two or three levels different from the current level. The middle level must be set between switching.
To switch from 1,6 (3.2) V to 3.2 (1.6) V:

1.6 V → 2.4 V → 3.2 V
1.6 V ← 2.4 V ← 3.2 V

To switch from 2.4 (3.2) V to 3.2 (2.4) V:

2.4 V → 3.2 V
2.4 V ← 3.2 V

A 5 msec interval is required for each switching step.
At initial reset, the VD1C register is set to "0" (2.4 V, Typ.).

OSCC: OSC3 oscillation control register (00FF01H•D2)

Turns the OSC3 oscillation circuit on and off.

When "1" is written: OSC3 oscillation ON
When "0" is written: OSC3 oscillation OFF
Reading: Valid

When it is necessary to operate the CPU and peripheral circuits (serial interface, programmable timer, LCD controller, etc.) at high-speed, write "1" to the OSCC register. At other times, set it to "0" to reduce current consumption.
At initial reset, the OSCC register is set to "0" (OSC3 oscillation OFF).

CLKCHG: CPU operating clock switching register (00FF01H•D3)

Selects the operating clock for the CPU.

When "1" is written: OSC3 clock
When "0" is written: OSC1 clock
Reading: Valid

When the CPU operating clock is to be OSC3, write "1" to the CLKCHG register; for OSC1, write "0".
The OSC3 oscillation circuit takes a maximum 20 msec to stabilize oscillation after turning the OSC3 oscillation circuit on. Therefore, switching the system clock should be done after the stabilization time has passed.
At initial reset, the CLKCHG register is set to "0" (OSC1 clock).

5.4.7 Programming notes

(1) The V_{D1} level must be switched while the OSC3 oscillation circuit is off (before turning on and after turning off). Switching during operation may cause malfunction. Furthermore, the V_{D1} voltage required at least 5 msec of voltage stabilizing time after switching. Do not turn the OSC3 oscillation circuit on during this period.

(2) V_{D1} cannot be switched directly to a level that is two or three levels different from the current level. The middle level must be set between switching.
To switch from 1,6 (3.2) V to 3.2 (1.6) V:
1.6 V → 2.4 V → 3.2 V
1.6 V ← 2.4 V ← 3.2 V
To switch from 2.4 (3.2) V to 3.2 (2.4) V:
2.4 V → 3.2 V
2.4 V ← 3.2 V
A 5 msec interval is required for each switching step.

(3) To generate V_{D1} with specified voltage, the supply voltage must be higher than the specified voltage.
To prevent malfunction, make sure that the supply voltage is not lowered under the V_{D1} value to be set using the SVD circuit before switching V_{D1}. Do not switch V_{D1} to a voltage higher than the supply voltage if the supply voltage drops.

(4) The OSC3 oscillation circuit takes a maximum 20 msec for stabilizing oscillation after turning the OSC3 oscillation circuit on. Therefore, take an enough interval after the OSC3 oscillation goes on before starting control of the peripheral circuit, such as the programmable timer, serial interface and LCD controller, that uses the OSC3 oscillation circuit as the clock source. (The oscillation start time varies depending on the oscillator and external component to be used. Refer to Chapter 8, "ELECTRICAL CHARACTERISTICS", in which an example of oscillation start time is indicated.)

(5) Use a separate instruction for switching the clock from OSC3 to OSC1 and turning the OSC3 oscillation off. Handling with one instruction may cause malfunction of the CPU.

(6) To prevent malfunction, before stopping the OSC3 oscillation, stop the operation of the peripheral circuits that use the OSC3 oscillation circuit as the clock source, such as programmable timer, serial interface and LCD controller.

(7) Do not turn the OSC3 oscillation circuit on to reduce current consumption when the OSC3 clock is not necessary.

5.5 Prescaler and Clock Control Circuit for Peripheral Circuits

5.5.1 Configuration of prescaler

The S1C88408 has a prescaler that generates the clocks for the internal peripheral circuit by dividing the output clock of the OSC1 oscillation circuit and OSC3 oscillation circuit.
The division ratio of the prescaler can be selected individually for each peripheral circuit by software.
Furthermore, the clock control circuit is provided to control clock supply to each peripheral circuit.
The peripheral circuits which use the output clock are as follows:

- 16-bit programmable timer 0
- 16-bit programmable timer 1
- 8-bit programmable timer
- Clock output (FOUT1, FOUT3)

Figure 5.5.1.1 shows the configuration of the prescaler.
For control of each peripheral circuit, refer to respective section.

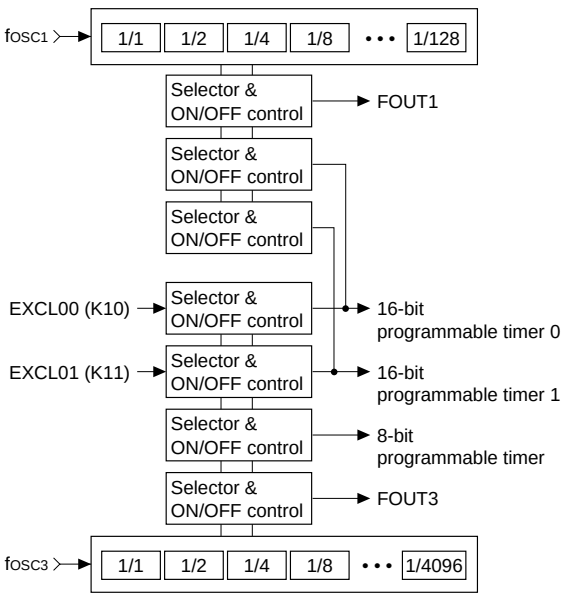


Fig. 5.5.1.1 Configuration of prescaler and clock control circuit

5.5.2 Setting of source clock

The prescaler uses the OSC1 clock and OSC3 clock as the source clocks.
The OSC1 prescaler always operates except for SLEEP status. When using an output clock from the OSC3 prescaler, it is necessary to turn the OSC3 oscillation circuit on.

Refer to Section 5.4.5, "Switching of CPU clock and operating voltage V_{D1}" for control of the OSC3 oscillation circuit and switching of the CPU operating clock.
At initial reset, the OSC3 oscillation circuit stops. The OSC3 oscillation circuit takes a maximum 20 msec for stabilizing oscillation after turning the OSC3 oscillation circuit on. Therefore, wait a long enough interval after the OSC3 oscillation goes on before turning the clock output of the OSC3 prescaler on. (The oscillation start time varies depending on the oscillator and external components to be used. Refer to Chapter 8, "ELECTRICAL CHARACTERISTICS", in which an example of oscillation start time is indicated.)

Among the peripheral circuits that use the clock output from the prescaler, the 16-bit programmable timer can select the clock source from either OSC1 or OSC3. Select the clock source before supplying the clock to the 16-bit programmable timer.

5.5.3 Prescaler division ratio selection and output control

The prescaler has division ratio selection registers and clock output control registers for the peripheral circuits, so the division ratio and the clock output for each circuit can be controlled individually.
The prescaler division ratio is selected by the division ratio selection register from 8 types set for each peripheral circuit. The dividing clock is output to the peripheral circuit by writing "1" to the clock output control register.
The following shows the division ratio selection register and the clock output control register for each peripheral circuit.

16-bit programmable timer 0

Table 5.5.3.1 Division ratio and control registers

16-bit programmable timer 0 (Clock source: OSC3)

Selection register			Division ratio	Output control
PST02	PST01	PST00		
1	1	1	fosc3/4096	PRPRT0 register "1": ON "0": OFF
1	1	0	fosc3/1024	
1	0	1	fosc3/256	
1	0	0	fosc3/128	
0	1	1	fosc3/64	
0	1	0	fosc3/32	
0	0	1	fosc3/8	
0	0	0	fosc3/2	

Table 5.5.3.2 Division ratio and control registers

16-bit programmable timer 0 (Clock source: OSC1)

Selection register			Division ratio	Output control
PST02	PST01	PST00		
1	1	1	fosc1/128	PRPRT0 register "1": ON "0": OFF
1	1	0	fosc1/64	
1	0	1	fosc1/32	
1	0	0	fosc1/16	
0	1	1	fosc1/8	
0	1	0	fosc1/4	
0	0	1	fosc1/2	
0	0	0	fosc1/1	

The source clock (OSC1, OSC3) is selected by the PRTF0 register.

16-bit programmable timer 1

Table 5.5.3.3 Division ratio and control registers

16-bit programmable timer 1 (Clock source: OSC3)

Selection register			Division ratio	Output control
PST12	PST11	PST10		
1	1	1	fosc3/4096	PRPRT1 register "1": ON "0": OFF
1	1	0	fosc3/1024	
1	0	1	fosc3/256	
1	0	0	fosc3/128	
0	1	1	fosc3/64	
0	1	0	fosc3/32	
0	0	1	fosc3/8	
0	0	0	fosc3/2	

Table 5.5.3.4 Division ratio and control registers

16-bit programmable timer 1 (Clock source: OSC1)

Selection register			Division ratio	Output control
PST12	PST11	PST10		
1	1	1	fosc1/128	PRPRT1 register "1": ON "0": OFF
1	1	0	fosc1/64	
1	0	1	fosc1/32	
1	0	0	fosc1/16	
0	1	1	fosc1/8	
0	1	0	fosc1/4	
0	0	1	fosc1/2	
0	0	0	fosc1/1	

The source clock (OSC1, OSC3) is selected by the PRTF1 register.

8-bit programmable timer

Table 5.5.3.5 Division ratio and control registers

8-bit programmable timer

Selection register			Division ratio	Output control
PST22	PST21	PST20		
1	1	1	fosc3/256	PRPRT2 register "1": ON "0": OFF
1	1	0	fosc3/128	
1	0	1	fosc3/64	
1	0	0	fosc3/32	
0	1	1	fosc3/16	
0	1	0	fosc3/8	
0	0	1	fosc3/4	
0	0	0	fosc3/2	

FOUT1/FOUT3 clock output

Table 5.5.3.6 Division ratio and control registers

FOUT1 clock

Selection register			Division ratio	Output control
PSF12	PSF11	PSF10		
1	1	1	fosc1/128	PRFO1 register "1": ON "0": OFF
1	1	0	fosc1/64	
1	0	1	fosc1/32	
1	0	0	fosc1/16	
0	1	1	fosc1/8	
0	1	0	fosc1/4	
0	0	1	fosc1/2	
0	0	0	fosc1/1	

Table 5.5.3.7 Division ratio and control registers

FOUT3 clock

Selection register			Division ratio	Output control
PSF32	PSF31	PSF30		
1	1	1	fosc3/128	PRFO3 register "1": ON "0": OFF
1	1	0	fosc3/64	
1	0	1	fosc3/32	
1	0	0	fosc3/16	
0	1	1	fosc3/8	
0	1	0	fosc3/4	
0	0	1	fosc3/2	
0	0	0	fosc3/1	

5.5.4 Control of external clock for event counter

The 16-bit programmable timer can operate as an event counter with the clock input from the EXCL00, EXCL01 (K10, K11) input terminals. These external clocks are controlled to supply the 16-bit programmable timer by the individual input control registers.
Table 5.5.4.1 shows the input terminals, the input control registers and the timers.

Table 5.5.4.1 Input control registers for an event counter clock

Input terminal	Input control register	Event counter
EXCL00 (K10)	PK10ON	Timer 0
EXCL01 (K11)	PK11ON	Timer 1

5.5.5 I/O memory of prescaler

Table 5.5.5.1 shows the control bits for the prescaler.

Table 5.5.5.1(a) Prescaler control bits

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF01	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	WT1	Wait state control WT1 WT0 Number of states 1 1 12(3 cycles) 1 0 8(2 cycles) 0 1 4(1 cycle) 0 0 No wait			0	R/W	
	D4	WT0				0	R/W	
	D3	CLKCHG	CPU operating clock switch	OSC3	OSC1	0	R/W	
	D2	OSCC	OSC3 oscillation ON/OFF control	On	Off	0	R/W	
	D1	VD1C1	V_{D1} output level setting VD1C1 VD1C0 V_{D1} (Typ.) 1 × 3.2 V 0 1 1.6 V 0 0 2.4 V			0	R/W	
	D0	VD1C0				0	R/W	
00FF10	D7	PRPRT1	16-bit programmable timer 1 clock control	On	Off	0	R/W	
	D6	PST12	16-bit programmable timer 1 division ratio PST12 PST11 PST10 (OSC3) (OSC1) 1 1 1 f_{OSC3} / 4096 f_{OSC1} / 128 1 1 0 f_{OSC3} / 1024 f_{OSC1} / 64 1 0 1 f_{OSC3} / 256 f_{OSC1} / 32 1 0 0 f_{OSC3} / 128 f_{OSC1} / 16 0 1 1 f_{OSC3} / 64 f_{OSC1} / 8 0 1 0 f_{OSC3} / 32 f_{OSC1} / 4 0 0 1 f_{OSC3} / 8 f_{OSC1} / 2 0 0 0 f_{OSC3} / 2 f_{OSC1} / 1			0	R/W	
	D5	PST11				0	R/W	
	D4	PST10				0	R/W	
	D3	PRPRT0	16-bit programmable timer 0 clock control	On	Off	0	R/W	
	D2	PST02	16-bit programmable timer 0 division ratio PST02 PST01 PST00 (OSC3) (OSC1) 1 1 1 f_{OSC3} / 4096 f_{OSC1} / 128 1 1 0 f_{OSC3} / 1024 f_{OSC1} / 64 1 0 1 f_{OSC3} / 256 f_{OSC1} / 32 1 0 0 f_{OSC3} / 128 f_{OSC1} / 16 0 1 1 f_{OSC3} / 64 f_{OSC1} / 8 0 1 0 f_{OSC3} / 32 f_{OSC1} / 4 0 0 1 f_{OSC3} / 8 f_{OSC1} / 2 0 0 0 f_{OSC3} / 2 f_{OSC1} / 1			0	R/W	
	D1	PST01				0	R/W	
	D0	PST00				0	R/W	
00FF11	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	PRPRT2	8-bit programmable timer clock control	On	Off	0	R/W	
	D2	PST22	8-bit programmable timer division ratio PST22 PST21 PST20 Division ratio 1 1 1 f_{OSC3} / 256 1 1 0 f_{OSC3} / 128 1 0 1 f_{OSC3} / 64 1 0 0 f_{OSC3} / 32 0 1 1 f_{OSC3} / 16 0 1 0 f_{OSC3} / 8 0 0 1 f_{OSC3} / 4 0 0 0 f_{OSC3} / 2			0	R/W	
	D1	PST21				0	R/W	
	D0	PST20				0	R/W	
00FF12	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	–	–	–	–	–	–	
	D1	PRTF1	16-bit programmable timer 1 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	
	D0	PRTF0	16-bit programmable timer 0 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	

Table 5.5.5.1(b) Prescaler control bits

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF14	D7	PRFO1	FOUT1 output control	On	Off	0	R/W	
	D6	PSF12	FOUT1 division ratio PSF12 PSF11 PSF10 Division ratio 1 1 1 fOSC1 / 128			0	R/W	
	D5	PSF11	1 1 0 fOSC1 / 64 1 0 1 fOSC1 / 32 1 0 0 fOSC1 / 16			0	R/W	
	D4	PSF10	0 1 1 fOSC1 / 8 0 1 0 fOSC1 / 4 0 0 1 fOSC1 / 2 0 0 0 fOSC1 / 1			0	R/W	
	D3	PRFO3	FOUT3 output control	On	Off	0	R/W	
	D2	PSF32	FOUT3 division ratio PSF32 PSF31 PSF30 Division ratio 1 1 1 fOSC3 / 128			0	R/W	
	D1	PSF31	1 1 0 fOSC3 / 64 1 0 1 fOSC3 / 32 1 0 0 fOSC3 / 16			0	R/W	
	D0	PSF30	0 1 1 fOSC3 / 8 0 1 0 fOSC3 / 4 0 0 1 fOSC3 / 2 0 0 0 fOSC3 / 1			0	R/W	
00FF15	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	–	–	–	–	–	–	
	D1	PK11ON	EXCL01 input clock ON/OFF control	On	Off	0	R/W	
	D0	PK10ON	EXCL00 input clock ON/OFF control	On	Off	0	R/W	

OSCC: OSC3 oscillation control register (00FF01H•D2)

Turns the OSC3 oscillation circuit on and off.

When "1" is written: OSC3 oscillation ON
When "0" is written: OSC3 oscillation OFF
Reading: Valid

When using the clock of which the clock source is OSC3, set the OSCC register to "1". Refer to Section 5.4, "Oscillation Circuit", for details of the oscillation control.
At initial reset, the OSCC register is set to "0" (OSC3 oscillation OFF).

PRTF0: 16-bit programmable timer 0 source clock selection register (00FF12H•D0)

Selects the source clock for the 16-bit programmable timer 0.

When "1" is written: fOSC1
When "0" is written: fOSC3
Reading: Valid

When "1" is written to the PRTF0 register, the OSC1 clock is selected as the source clock for the 16-bit programmable timer 0.
When "0" is written, the OSC3 clock is selected.
At initial reset, the PRTF0 register is set to "0" (fOSC3).

PST00–PST02: 16-bit programmable timer 0 division ratio selection register (00FF10H•D0–D2)

Selects the clock for the 16-bit programmable timer 0.
It can be selected from 8 types of division ratio shown in Table 5.5.5.1(a).
This register can also be read.
At initial reset, the PST0 register is set to "0".

PRPRT0: 16-bit programmable timer 0 clock control register (00FF10H•D3)

Controls the clock supply of the 16-bit programmable timer 0.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

By writing "1" to the PRPRT0 register, the clock that is selected with the PST0 register is output to the 16-bit programmable timer 0.
When "0" is written, the clock is not output.
At initial reset, the PRPRT0 register is set to "0" (OFF).

PK10ON: EXCL00 clock control register (00FF15H•D0)

Controls the event counter clock of the 16-bit programmable timer 0.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

By writing "1" to the PK10ON register, the EXCL00 (K10 input) clock is output to the 16-bit programmable timer 0.
When "0" is written, the clock is not output.
At initial reset, the PK10ON register is set to "0" (OFF).

PRTF1: 16-bit programmable timer 1 source clock selection register (00FF12H•D1)

Selects the source clock for the 16-bit programmable timer 1.

When "1" is written: f_{OSC1}
When "0" is written: f_{OSC3}
Reading: Valid

When "1" is written to the PRTF1 register, the OSC1 clock is selected as the source clock for the 16-bit programmable timer 1.
When "0" is written, the OSC3 clock is selected.
At initial reset, the PRTF1 register is set to "0" (f_{OSC3}).

PST10–PST12: 16-bit programmable timer 1 division ratio selection register (00FF10H•D4–D6)

Selects the clock for the 16-bit programmable timer 1.
It can be selected from 8 types of division ratio shown in Table 5.5.5.1(a).
This register can also be read.
At initial reset, the PST1 register is set to "0".

PRPRT1: 16-bit programmable timer 1 clock control register (00FF10H•D7)

Controls the clock supply of the 16-bit programmable timer 1.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

By writing "1" to the PRPRT1 register, the clock that is selected with the PST1 register is output to the 16-bit programmable timer 1.
When "0" is written, the clock is not output.
At initial reset, the PRPRT1 register is set to "0" (OFF).

PK11ON: EXCL01 clock control register (00FF15H•D1)

Controls the event counter clock of the 16-bit programmable timer 1.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

By writing "1" to the PK11ON register, the EXCL01 (K11 input) clock is output to the 16-bit programmable timer 1.
When "0" is written, the clock is not output.
At initial reset, the PK11ON register is set to "0" (OFF).

PST20–PST22: 8-bit programmable timer division ratio selection register (00FF11H•D0–D2)

Selects the clock for the 8-bit programmable timer.
It can be selected from 8 types of division ratio shown in Table 5.5.5.1(a).
This register can also be read.
At initial reset, the PST2 register is set to "0" (f_{OSC3} / 2).

PRPRT2: 8-bit programmable timer clock control register (00FF11H•D3)

Controls the clock supply of the 8-bit programmable timer.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

By writing "1" to the PRPRT2 register, the clock that is selected with the PST2 register is output to the 8-bit programmable timer.
When "0" is written, the clock is not output.
At initial reset, the PRPRT2 register is set to "0" (OFF).

PSF10–PSF12: FOUT1 division ratio selection register (00FF14H•D4–D6)

Selects the frequency for the FOUT1 clock.
It can be selected from 8 types of division ratio shown in Table 5.5.5.1(b).
This register can also be read.
At initial reset, the PSF1 register is set to "0" (f_{OSC1} / 1).

PRFO1: FOUT1 output control register (00FF14H•D7)

Controls the FOUT1 output.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

When "1" is written to the PRFO1 register, the FOUT1 (R41) terminal outputs the clock selected with the PSF1 register. However, the high-impedance control register HZR41 of the output port R41 must be set to "0" and the data register R41D must be set to "1".
When "0" is written, the clock is not output.
At initial reset, the PRFO1 register is set to "0" (OFF).

PSF30–PSF32: FOUT3 division ratio selection register (00FF14H•D0–D2)

Selects the frequency for the FOUT3 clock.
It can be selected from 8 types of division ratio shown in Table 5.5.5.1(b).
This register can also be read.
At initial reset, the PSF3 register is set to "0" (f_{OSC3} / 1).

PRFO3: FOUT3 output control register (00FF14H•D3)

Controls the FOUT3 output.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

When "1" is written to the PRFO3 register, the FOUT3 (R40) terminal outputs the clock selected with the PSF3 register. However, the high-impedance control register HZR40 of the output port R40 must be set to "0" and the data register R40D must be set to "1".
When "0" is written, the clock is not output.
At initial reset, the PRFO3 register is set to "0" (OFF).

5.5.6 Programming note

When using an output clock from the OSC3 prescaler, it is necessary to turn the OSC3 oscillation circuit on. Furthermore, the OSC3 oscillation circuit takes a maximum 20 msec for stabilizing oscillation after turning the OSC3 oscillation circuit on. Therefore, wait a long enough interval after the OSC3 oscillation goes on before turning the clock output of the OSC3 prescaler on. (The oscillation start time varies depending on the oscillator and external components to be used. Refer to Chapter 8, "ELECTRICAL CHARACTERISTICS", in which an example of oscillation start time is indicated.)

5.6 Input Ports (K ports)

5.6.1 Configuration of input ports

The S1C88408 has 12 bits of input ports built-in, and all the ports can be used as a general-purpose input port that has an interrupt function.

K0 port: K00–K07 8 bits
K1 port: K10–K13 4 bits

The K10 and K11 terminals serve both as the general-purpose input port terminal and the external clock (EXCL00, EXCL01) input terminal for the 16-bit programmable timer (event counter), and the input signal is common used. (Refer to Section 5.12, "16-bit Programmable Timer")
Figure 5.6.1.1 shows the structure of the input port.

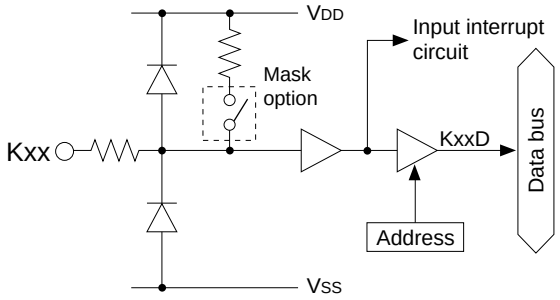


Fig. 5.6.1.1 Structure of input port

Each input port terminal is directly connected to the data bus via a three-state buffer. The input signal status can be read via the I/O memory as data.

5.6.2 Mask option

Input port pull-up resistors		
K00	☐ With resistor	☐ Gate direct
K01	☐ With resistor	☐ Gate direct
K02	☐ With resistor	☐ Gate direct
K03	☐ With resistor	☐ Gate direct
K04	☐ With resistor	☐ Gate direct
K05	☐ With resistor	☐ Gate direct
K06	☐ With resistor	☐ Gate direct
K07	☐ With resistor	☐ Gate direct
K10	☐ With resistor	☐ Gate direct
K11	☐ With resistor	☐ Gate direct
K12	☐ With resistor	☐ Gate direct
K13	☐ With resistor	☐ Gate direct

The input port has a built-in pull-up resistor, and it can be individually selected for use or not by the mask option.

The "With resistor" option is suitable for push switch and key matrix input.
When the input terminal is changed from a low level to a high level by the built-in pull-up resistor, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and load capacitance of the terminal. Hence, when reading the input port, it is necessary to wait an appropriate amount of time. Particular care must be taken of the key scan for the key matrix configuration. Make this waiting time the amount of time or more calculated by the following expression.

Waiting time = $R_{IN} \times (C_{IN} + C_L) \times 1.6$ [sec]
R_{IN}: Pull-up resistance Max. value
C_{IN}: Terminal capacitance Max. value
C_L: Load capacitance on the board

When "Gate direct" is selected, the pull-up resistor is disconnected and the port is suitable for slide switch input and interfacing with other LSIs. In this case, take care that a floating status does not occur in the input.
For unused input ports, select "With resistor" as the default setting.

5.6.3 Interrupt function

All the input ports provide the interrupt function. The input ports are divided into five systems: K0 (K00–K07), K10, K11, K12 and K13. The interrupt generation condition for each system can be set with software.

When the interrupt generation condition set for each terminal system is met, the interrupt factor flag (FK0, FK10, FK11, FK12 and FK13) corresponding to the terminal system is set to "1", and an interrupt is generated.

The interrupt can be prohibited by setting the interrupt enable register (EK0, EK10, EK11, EK12 and EK13) corresponding to each interrupt factor flag.

Furthermore, the priority level of the input interrupt for the CPU can be set at an optional level (0–3) using the interrupt priority registers PK0 and PK1 (two bits each) corresponding to two systems K0 and K1.

Refer to Section 5.18, "Interrupt and Standby Mode", for details of the interrupt control registers and operations subsequent to interrupt generation.

The exception processing vectors for each interrupt factor are set as follows:

K10 input interrupt: 000006H
K11 input interrupt: 000008H
K12 input interrupt: 00000AH
K13 input interrupt: 00000CH
K0 input interrupt: 00000EH

K0 input interrupt

Figure 5.6.3.1 shows the configuration of the K0 (K00–K07) input interrupt circuit.

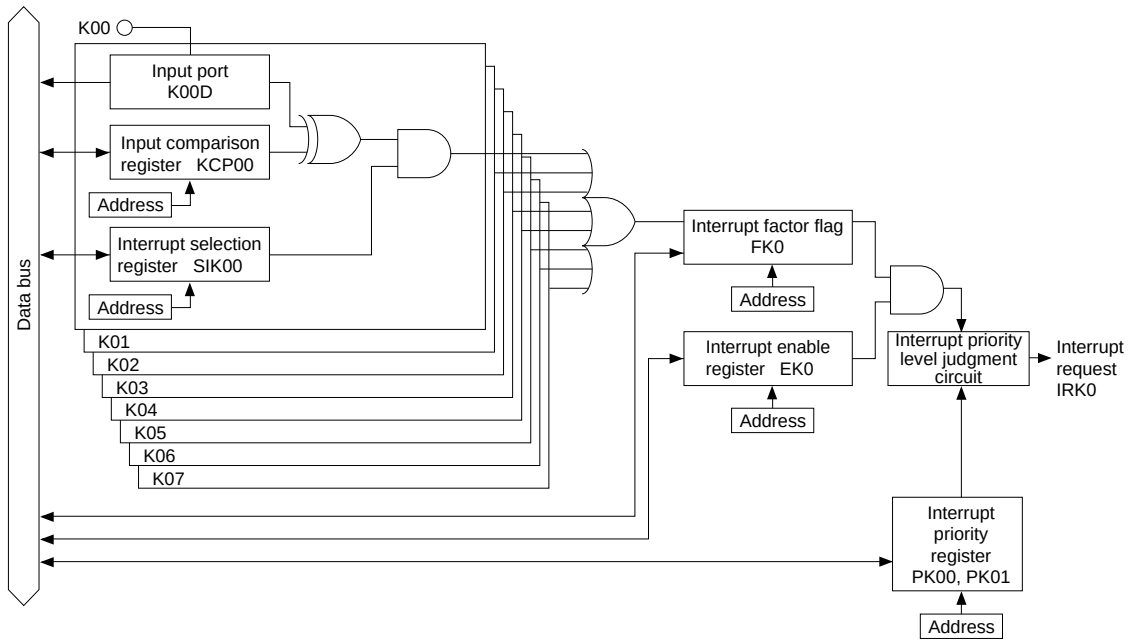


Fig. 5.6.3.1 Configuration of K0 input interrupt circuit

The interrupt selection register SIK0 and input comparison register KCP0 for the K0 port is used to set the interrupt generation condition.

Input port interrupt can be enabled or disabled by the setting of the interrupt selection registers SIK0. While the interrupt enable register EK0 masks the interrupt factor for the terminal system (8 bits), the interrupt selection register SIK0 masks in bit units.

The input comparison register KCP0 selects the interrupt generation timing that an interrupt is to be generated at the rising edge or the falling edge for each input.

When the status of the input terminals in which an interrupt has been enabled by the interrupt selection register SIK0 and the content of the input comparison register KCP0 change from a, matching to no matching, the interrupt factor flag FK0 is set to "1" and an interrupt is generated.
Figure 5.6.3.2 shows an example of interrupt generation in the K0 terminal system.

K00 interrupt is disabled by the interrupt selection register (SIK00), so that an interrupt does not occur at (2). At (3), K03 changes to "0"; the data of the terminals K01–K07 in which an interrupt is enabled no longer match the data of the input comparison registers KCP01–KCP07, so that interrupt occurs. As already explained, the condition for the interrupt to occur is the change in the port data and contents of the input comparison registers from matching to no matching. Hence, in (4), when the no matching status changes to another no matching status, an interrupt does not occur. Therefore, to generate the interrupt again after an interrupt is generated, it is necessary to return the input terminal status to the same content as the input comparison register KCP0 or re-set the input comparison register KCP0. Further, terminals that have been disabled for interrupt do not affect the conditions for interrupt generation.

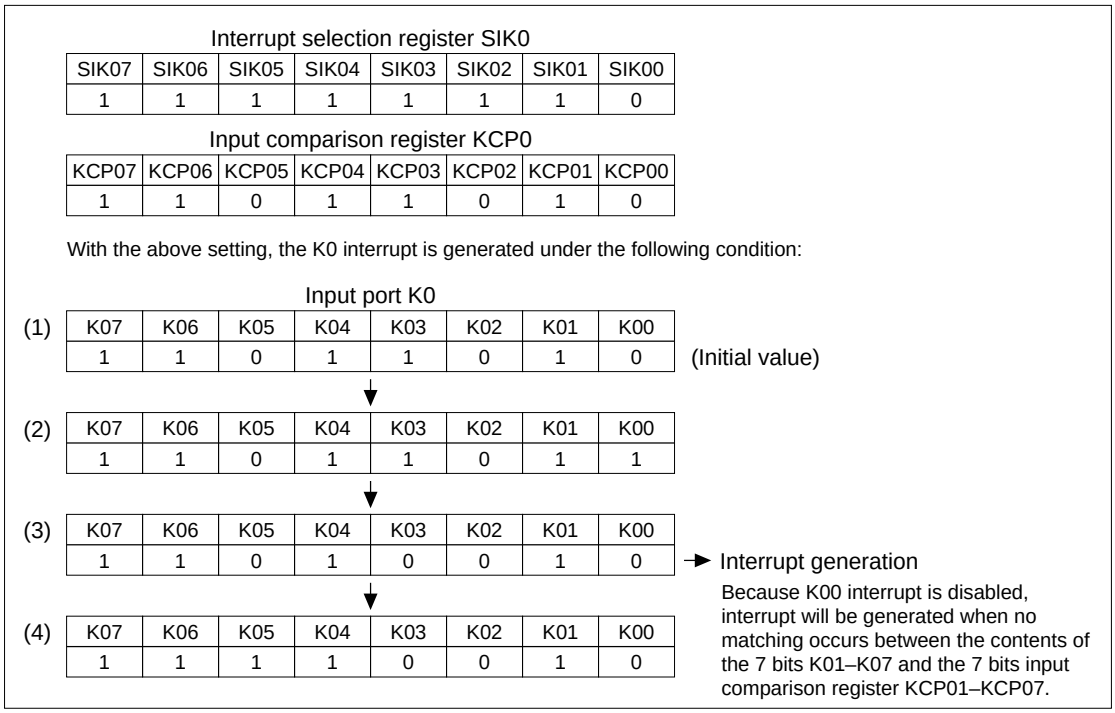


Fig. 5.6.3.2 Example of K0 (K00–K07) interrupt generation

K10–K13 input interrupt

Figure 5.6.3.3 shows the configuration of the K10–K13 input interrupt circuit.

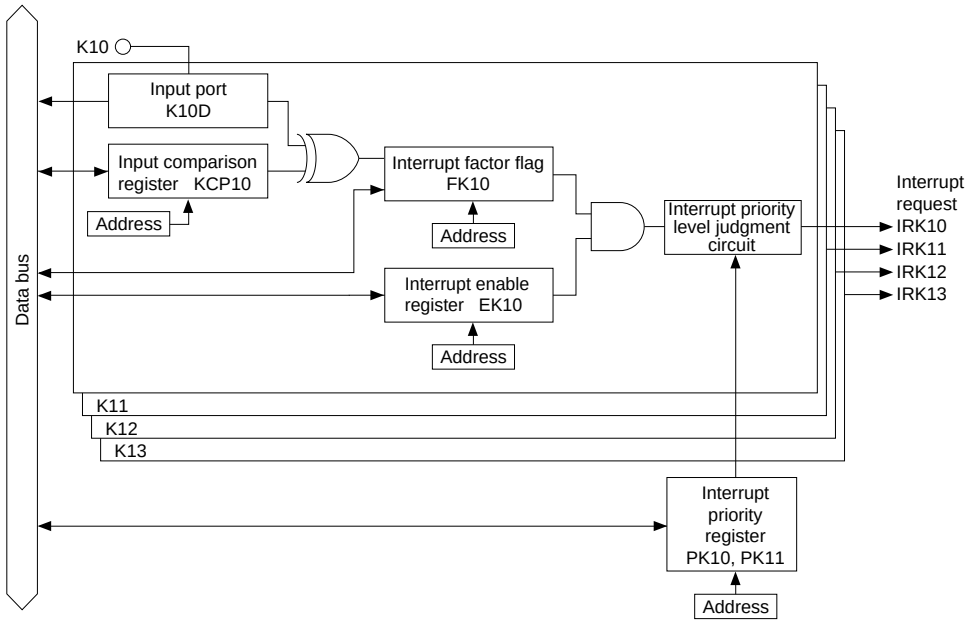


Fig. 5.6.3.3 Configuration of K10–K13 input interrupt circuit

Since the K10–K13 input ports can generate an interrupt by each bit, an interrupt selection register is not provided. The interrupts are enabled or disabled by the interrupt enable register EK1.
The input comparison register KCP1 selects the interrupt generation timing that an interrupt is to be generated at the rising edge or the falling edge for each input.

Each interrupt of the K10–K13 input ports is generated at the rising edge or the falling edge (depending on the setting of the input comparison register KCP1) when the interrupt has been enabled with the interrupt enable register EK1.

5.6.4 I/O memory of input ports

Table 5.6.4.1 shows the input port control bits.

Table 5.6.4.1 Input port control bits

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF20	D7	PK11	K10–K13	PK11 PK10		0	R/W	
	D6	PK10	interrupt priority register	PK01 PK00		0	R/W	
	D5	PK01	K00–K07	PTM11 PTM10	Priority	0	R/W	
	D4	PK00	interrupt priority register	PTM01 PTM00	level	0	R/W	
	D3	PTM11	16-bit programmable timer 1	1 1	Level 3	0	R/W	
	D2	PTM10	interrupt priority register	1 0	Level 2	0	R/W	
	D1	PTM01	16-bit programmable timer 0	0 1	Level 1	0	R/W	
	D0	PTM00	interrupt priority register	0 0	Level 0	0	R/W	
00FF23	D7	EK13	K13 interrupt enable register			0	R/W	
	D6	EK12	K12 interrupt enable register			0	R/W	
	D5	EK11	K11 interrupt enable register			0	R/W	
	D4	EK10	K10 interrupt enable register	Interrupt is enabled	Interrupt is disabled	0	R/W	
	D3	EK0	K00–K07 interrupt enable register			0	R/W	
	D2	–	–			–	–	"0" when being read
	D1	–	–			–	–	
	D0	–	–			–	–	
00FF27	D7	FK13	K13 interrupt factor flag	(R)	(R)	0	R/(W)	
	D6	FK12	K12 interrupt factor flag	Interrupt	Interrupt	0	R/(W)	
	D5	FK11	K11 interrupt factor flag	factor has	factor has not	0	R/(W)	
	D4	FK10	K10 interrupt factor flag	generated	generated	0	R/(W)	
	D3	FK0	K00–K07 interrupt factor flag			0	R/(W)	
	D2	–	–	(W)	(W)	–	–	"0" when being read
	D1	–	–	Reset	Invalid	–	–	
	D0	–	–			–	–	
00FFC0	D7	SIK07	K07 interrupt selection register			0	R/W	
	D6	SIK06	K06 interrupt selection register			0	R/W	
	D5	SIK05	K05 interrupt selection register			0	R/W	
	D4	SIK04	K04 interrupt selection register	Interrupt	Interrupt	0	R/W	
	D3	SIK03	K03 interrupt selection register	is enabled	is disabled	0	R/W	
	D2	SIK02	K02 interrupt selection register			0	R/W	
	D1	SIK01	K01 interrupt selection register			0	R/W	
	D0	SIK00	K00 interrupt selection register			0	R/W	
00FFC1	D7	KCP07	K07 input comparison register			1	R/W	
	D6	KCP06	K06 input comparison register			1	R/W	
	D5	KCP05	K05 input comparison register			1	R/W	
	D4	KCP04	K04 input comparison register	Falling edge	Rising edge	1	R/W	
	D3	KCP03	K03 input comparison register	generates	generates	1	R/W	
	D2	KCP02	K02 input comparison register	interrupt	interrupt	1	R/W	
	D1	KCP01	K01 input comparison register			1	R/W	
	D0	KCP00	K00 input comparison register			1	R/W	
00FFC2	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	KCP13	K13 input comparison register			1	R/W	
	D2	KCP12	K12 input comparison register	Falling edge	Rising edge	1	R/W	
	D1	KCP11	K11 input comparison register	generates	generates	1	R/W	
	D0	KCP10	K10 input comparison register	interrupt	interrupt	1	R/W	
00FFC3	D7	K07D	K07 input port data			–	R	
	D6	K06D	K06 input port data			–	R	
	D5	K05D	K05 input port data			–	R	
	D4	K04D	K04 input port data	High	Low	–	R	
	D3	K03D	K03 input port data			–	R	
	D2	K02D	K02 input port data			–	R	
	D1	K01D	K01 input port data			–	R	
	D0	K00D	K00 input port data			–	R	
00FFC4	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	K13D	K13 input port data			–	R	
	D2	K12D	K12 input port data	High	Low	–	R	
	D1	K11D	K11 input port data			–	R	
	D0	K10D	K10 input port data			–	R	

K00D–K07D: K0 input port data (00FFC3H)
K10D–K13D: K1 input port data (00FFC4H•D0–D3)

Input data of the input port terminals can be read out.

When "1" is read: HIGH level
When "0" is read: LOW level
Writing: Invalid

The terminal voltage of each of the input ports K00–K07 and K10–K13 can be directly read as either a "1" when the terminal is high (V_{DD}) level or a "0" when the terminal is low (V_{SS}) level.
These bits are dedicated for reading, so writing cannot be done.

SIK00–SIK07: K0 port interrupt selection register (00FFC0H)

Sets the interrupt generation condition (enables / disables interrupt) for the K0 input port.

When "1" is written: Interrupt is enabled
When "0" is written: Interrupt is disabled
Reading: Valid

SIK0 is the interrupt selection register corresponding to the input port K0. An interrupt of the port in which the SIK0 bit is set to "1" is enabled, and the others in which the SIK0 bit is set to "0" are disabled. Change of the input terminal in which the interrupt is disabled does not affect the interrupt generation.
At initial reset, the SIK0 register is set to "0" (interrupt is disabled).
The K10–K13 input port has no interrupt selection register because the port can generate interrupts in bit units.

KCP00–KCP07: K0 port input comparison register (00FFC1H)
KCP10–KCP13: K1 port input comparison register (00FFC2H•D0–D3)

Sets the interrupt generation condition (interrupt generation timing) for the K0 or K1 input port.

When "1" is written: Falling edge
When "0" is written: Rising edge
Reading: Valid

KCP is the input comparison register corresponding to each input port. An interrupt of the port in which the KCP bit is set to "1" is generated at the falling edge of the input and an interrupt in which the KCP bit is set to "0" is generated at the rising edge.
At initial reset, the KCP register is set to "1" (falling edge).

PK00, PK01: K0 input interrupt priority register (00FF20H•D4, D5)
PK10, PK11: K1 input interrupt priority register (00FF20H•D6, D7)

Sets the input interrupt priority level.
PK0 and PK1 are the interrupt priority registers corresponding to the K0, K1 input interrupts.
Table 5.6.4.2 shows the interrupt priority level which can be set by this register.

Table 5.6.4.2 Interrupt priority level settings

PK11 PK01	PK10 PK00	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, the PK register is set to "0" (level 0).

EK0: K0 input interrupt enable register (00FF23H•D3)
EK10–EK13: K1 input interrupt enable register (00FF23H•D4–D7)

Enables or disables the interrupt generation to the CPU.

When "1" is written: Interrupt is enabled
When "0" is written: Interrupt is disabled
Reading: Valid

EK0 is the interrupt enable register corresponding to eight bits of the K0 port and EK10–EK13 correspond to each bit of the K10–K13 ports.
An interrupt of the port in which the EK register is set to "1" is enabled, and the others in which the EK register is set to "0" are disabled.
At initial reset, the EK register is set to "0" (interrupt is disabled).

FK0: K0 input interrupt factor flag (00FF27H•D3)
FK10–FK13: K1 input interrupt factor flag (00FF27H•D4–D7)

Indicates the generation of input interrupt factor.

When "1" is read: Int. factor has generated
When "0" is read: Int. factor has not generated

When "1" is written: Factor flag is reset
When "0" is written: Invalid

FK0 is the interrupt factor flag corresponding to eight bits of the K0 port and FK10–FK13 correspond to each bit of the K10–K13 ports.
The interrupt factor flag is set to "1" when the interrupt generation condition is met.

At this point, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of the interrupt flags (I0 and I1), an interrupt is generated to the CPU.
Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag is set to "1" when the interrupt generation condition is met.
To accept the subsequent interrupt after an interrupt generation, it is necessary to re-set the interrupt flags (set the interrupt flag to a lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and to reset the interrupt factor flag. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, the FK flags are all reset to "0".

5.6.5 Programming note

When the input terminal is changed from a low level to a high level by the built-in pull-up resistor, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and load capacitance of the terminal. Hence, when reading the input port, it is necessary to wait an appropriate amount of time. Particular care must be taken of the key scan for the key matrix configuration. Make this waiting time the amount of time or more calculated by the following expression.

Waiting time = $R_{IN} \times (C_{IN} + C_L) \times 1.6$ [sec]

R_{IN}: Pull-up resistance Max. value
C_{IN}: Terminal capacitance Max. value
C_L: Load capacitance on the board

5.7 Output Ports (R ports)

5.7.1 Configuration of output ports

The S1C88408 has 30 bits of output ports.

R0 port: R00–R07 8 bits
R1 port: R10–R17 8 bits
R2 port: R20–R27 8 bits
R3 port: R30–R32 3 bits
R4 port: R40–R42 3 bits

Depending on the bus mode setting, the configuration of the output ports may vary as shown in the table below.

Table 5.7.1.1 Configuration of output ports

Terminal	Bus mode		
	Single chip	Expanded 64K	Expanded 4M
R00	Output port R00	Address A0	
R01	Output port R01	Address A1	
R02	Output port R02	Address A2	
R03	Output port R03	Address A3	
R04	Output port R04	Address A4	
R05	Output port R05	Address A5	
R06	Output port R06	Address A6	
R07	Output port R07	Address A7	
R10	Output port R10	Address A8	
R11	Output port R11	Address A9	
R12	Output port R12	Address A10	
R13	Output port R13	Address A11	
R14	Output port R14	Address A12	
R15	Output port R15	Address A13	
R16	Output port R16	Address A14	
R17	Output port R17	Address A15	
R20	Output port R20		Address A16
R21	Output port R21		Address A17
R22	Output port R22		Address A18
R23	Output port R23		Address A19
R24	Output port R24		Address A20
R25	Output port R25		Address A21
R26	Output port R26	$\overline{RD}$ signal	
R27	Output port R27	$\overline{WR}$ signal	
R30	Output port R30	Output port R30/$\overline{CE0}$ signal	
R31	Output port R31	Output port R31/$\overline{CE1}$ signal	
R32	Output port R32	Output port R32/$\overline{CE2}$ signal	
R40	Output port R40		
R41	Output port R41		
R42	Output port R42		

This section explains only the control of general-purpose output ports. Refer to Section 5.2, "System Controller and Bus Control", for the bus control. Figure 5.7.1.1 shows the structure of the output port.

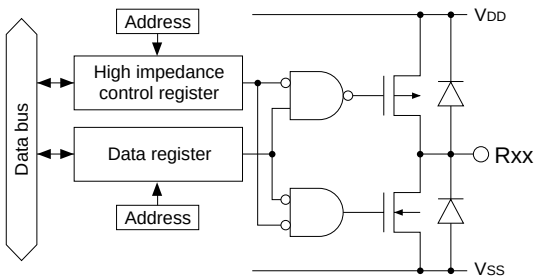


Fig. 5.7.1.1 Structure of output port

The data register and high impedance control register of the output port which is used for the bus function can be used as general purpose registers with the ability to read and write. They do not affect the bus signal output.

5.7.2 High impedance control

Each output port can be set in high impedance by software. Thus the output signal lines can be shared with other external devices.
By setting the bits of the high impedance control register to "1", the corresponding output ports go to a high impedance status. The output port in which the register is set to "0" becomes a complementary output.

5.7.3 DC output

As shown in Figure 5.7.1.1, when "1" is written to the output port data register, the output terminal goes high (V_{DD}) level and when "0" is written it goes low (V_{SS}) level.
The data written to the data register during high impedance status is output from the terminal when the output is switched to complementary.

5.7.4 Special output

The R40 to R42 terminals are shared with the special output terminals shown in Table 5.7.4.1.

Table 5.7.4.1 Special outputs

Output port	Special output
R40	Clock output : TOUT0/FOUT3
R41	Clock output : TOUT1/FOUT1
R42	Buzzer output : BZ

When using a special output, fix the high-impedance control register HZR4x of the port to "0" and the output data register R4xD to "1".
Refer to Section 5.9, "Clock Output", for the TOUT and FOUT outputs, and to Section 5.15, "Sound Generator", for the BZ output.

5.7.5 I/O memory of output ports

Table 5.7.5.1 shows the output port control bits.

Table 5.7.5.1(a) Output port control bits

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FFD0	D7	HZR07	R07 high impedance control register	High impedance	Complementary	1	R/W	
	D6	HZR06	R06 high impedance control register			1	R/W	
	D5	HZR05	R05 high impedance control register			1	R/W	
	D4	HZR04	R04 high impedance control register			1	R/W	
	D3	HZR03	R03 high impedance control register			1	R/W	
	D2	HZR02	R02 high impedance control register			1	R/W	
	D1	HZR01	R01 high impedance control register			1	R/W	
	D0	HZR00	R00 high impedance control register			1	R/W	
00FFD1	D7	HZR17	R17 high impedance control register	High impedance	Complementary	1	R/W	
	D6	HZR16	R16 high impedance control register			1	R/W	
	D5	HZR15	R15 high impedance control register			1	R/W	
	D4	HZR14	R14 high impedance control register			1	R/W	
	D3	HZR13	R13 high impedance control register			1	R/W	
	D2	HZR12	R12 high impedance control register			1	R/W	
	D1	HZR11	R11 high impedance control register			1	R/W	
	D0	HZR10	R10 high impedance control register			1	R/W	
00FFD2	D7	HZR27	R27 high impedance control register	High impedance	Complementary	1	R/W	
	D6	HZR26	R26 high impedance control register			1	R/W	
	D5	HZR25	R25 high impedance control register			1	R/W	
	D4	HZR24	R24 high impedance control register			1	R/W	
	D3	HZR23	R23 high impedance control register			1	R/W	
	D2	HZR22	R22 high impedance control register			1	R/W	
	D1	HZR21	R21 high impedance control register			1	R/W	
	D0	HZR20	R20 high impedance control register			1	R/W	
00FFD3	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	HZR32	R32 high impedance control register	High impedance	Complementary	1	R/W	
	D1	HZR31	R31 high impedance control register			1	R/W	
	D0	HZR30	R30 high impedance control register			1	R/W	
00FFD4	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	HZR42	R42 high impedance control register	High impedance	Complementary	1	R/W	
	D1	HZR41	R41 high impedance control register			1	R/W	
	D0	HZR40	R40 high impedance control register			1	R/W	
00FFD5	D7	R07D	R07 output port data register	High	Low	1	R/W	
	D6	R06D	R06 output port data register			1	R/W	
	D5	R05D	R05 output port data register			1	R/W	
	D4	R04D	R04 output port data register			1	R/W	
	D3	R03D	R03 output port data register			1	R/W	
	D2	R02D	R02 output port data register			1	R/W	
	D1	R01D	R01 output port data register			1	R/W	
	D0	R00D	R00 output port data register			1	R/W	
00FFD6	D7	R17D	R17 output port data register	High	Low	1	R/W	
	D6	R16D	R16 output port data register			1	R/W	
	D5	R15D	R15 output port data register			1	R/W	
	D4	R14D	R14 output port data register			1	R/W	
	D3	R13D	R13 output port data register			1	R/W	
	D2	R12D	R12 output port data register			1	R/W	
	D1	R11D	R11 output port data register			1	R/W	
	D0	R10D	R10 output port data register			1	R/W	

Table 5.7.5.1(b) Output port control bits

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FFD7	D7	R27D	R27 output port data register	High	Low	1	R/W	
	D6	R26D	R26 output port data register			1	R/W	
	D5	R25D	R25 output port data register			1	R/W	
	D4	R24D	R24 output port data register			1	R/W	
	D3	R23D	R23 output port data register			1	R/W	
	D2	R22D	R22 output port data register			1	R/W	
	D1	R21D	R21 output port data register			1	R/W	
	D0	R20D	R20 output port data register			1	R/W	
00FFD8	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	R32D	R32 output port data register	High	Low	1	R/W	
	D1	R31D	R31 output port data register			1	R/W	
	D0	R30D	R30 output port data register			1	R/W	
00FFD9	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	R42D	R42 output port data register	High	Low	1	R/W	
	D1	R41D	R41 output port data register			1	R/W	
	D0	R40D	R40 output port data register			1	R/W	

HZR00–HZR07: R0 port high impedance control register (00FFD0H)
HZR10–HZR17: R1 port high impedance control register (00FFD1H)
HZR20–HZR27: R2 port high impedance control register (00FFD2H)
HZR30–HZR32: R3 port high impedance control register (00FFD3H•D0–D2)
HZR40–HZR42: R4 port high impedance control register (00FFD4H•D0–D2)

Sets the output terminals into a high impedance state.

When "1" is written: High impedance
When "0" is written: Complementary
Reading: Valid

The HZR register is the high impedance control register corresponding to each output port.
When a HZR bit is set to "1", the corresponding output port terminal goes to a high impedance status and when "0" is set, it becomes a complementary output.
The high impedance control register of the output port which is used for bus function can be used as a general purpose register with the ability to read and write. It does not affect the bus signal output.
Among R40 to R42, the high-impedance control register of the port which is used for special output (TOUT/FOUT, BZ) should be fixed at "0".
At initial reset, the HZR register is set to "1" (high impedance).

R00D–R07D: R0 port output data register (00FFD5H)
R10D–R17D: R1 port output data register (00FFD6H)
R20D–R27D: R2 port output data register (00FFD7H)
R30D–R32D: R3 port output data register (00FFD8H•D0–D2)
R40D–R42D: R4 port output data register (00FFD9H•D0–D2)

Sets the data output from the output port terminal.

When "1" is written: HIGH level output
When "0" is written: LOW level output
Reading: Valid

RxxD is the data register for each output port.
When "1" is set, the corresponding output port terminal goes high (V_{DD}) level, and when "0" is set, it goes low (V_{SS}) level.
The data register of the output port which is used for the bus function can be used as general purpose register with the ability to read and write. It does not affect the bus signal output.
Among R40 to R42, the data register of the port which is used for special output (TOUT/FOUT, BZ) should be fixed at "1".
At initial reset, all the data bits are set to "1" (HIGH level output).

5.8 I/O Ports (P ports)

5.8.1 Configuration of I/O ports

The S1C88408 has 28 bits of I/O ports.

P0 port:	P00–P07	8 bits
P1 port:	P10–P17	8 bits
P2 port:	P20–P23	4 bits
P3 port:	P30–P37	8 bits

These ports can be switched between general-purpose I/O ports and input/output ports for the following functions by software.

- Data bus for external memory access
- Serial interface

This section explains control only when using these ports as general-purpose I/O ports. Refer to respective sections for other functions.
Figure 5.8.1.1 shows the structure of the I/O port.

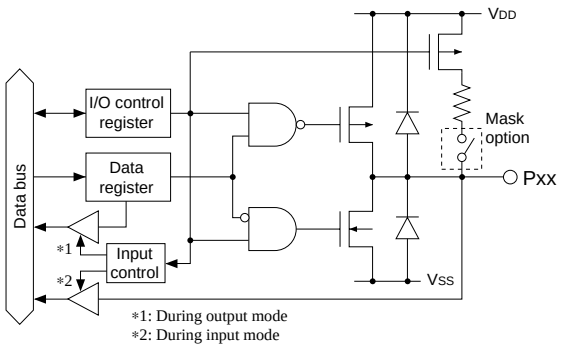


Fig. 5.8.1.1 Structure of I/O port

The port can be set individually in input mode or output mode when it is used as a general-purpose I/O port. This setting is done by writing data to the I/O control register (IOC).

5.8.2 Terminal configuration of I/O port and change of function

The I/O port terminals are shared with two or three functions. Therefore, the configuration of the terminals changes depending on the setting of each function. Since all the terminals are set for the I/O port at initial reset except for the MPU mode, switch them using software according to the functions to be used.
Table 5.8.2.1 lists the terminal functions.

When the expanded bus mode is set (P00–P07)

When a bus mode except for the single chip mode is set, P00–P07 functions as the data bus D0–D7. In this case, the data register P00D–P07D and the I/O control register IOC00–IOC07 can be used as a general-purpose register that does not affect the input/output for the data bus.
Refer to Section 5.2, "System Controller and Bus Control", for setting of bus mode.

When the serial interface is used (P10–P17)

The S1C88408 has a serial interface built-in. The serial interface uses the following terminals and unused terminals can be used as a general-purpose I/O ports.

Transfer mode	Terminals used for serial I/F (P10–P17)
Asynchronous	P10, P11 (or P14, P15)
Clock sync. slave	P10–P13 (or P14–P17)
Clock sync. master	P10–P12 (or P14–P16)
IrDA interface	P14, P15

The data register and the I/O control register of the port which is assigned to the serial interface can be used as a general-purpose register that does not affect the input/output.
Refer to Section 5.14, "Serial Interface", for setting of the serial interface.

Table 5.8.2.1 Terminal function list

Terminal	Standard function		I/O	Sub-function		I/O
P00	I/O port	P00	I/O	Data bus for external memory	D0	I/O
P01		P01	I/O	(Expanded mode)	D1	I/O
P02		P02	I/O		D2	I/O
P03		P03	I/O		D3	I/O
P04		P04	I/O		D4	I/O
P05		P05	I/O		D5	I/O
P06		P06	I/O		D6	I/O
P07		P07	I/O		D7	I/O
P10	I/O port	P10	I/O	Serial I/F data input	SIN	I
P11		P11	I/O	Serial I/F data output	SOUT	O
P12		P12	I/O	Serial I/F clock input/output	$\overline{\text{SCLK}}$	I/O
P13		P13	I/O	Serial I/F ready output	$\overline{\text{SRDY}}$	O
P14		P14	I/O	Serial I/F data input/IR input	SIN/IRI	I
P15		P15	I/O	Serial I/F data output/IR output	SOUT/IRO	O
P16		P16	I/O	Serial I/F clock input/output	$\overline{\text{SCLK}}$	I/O
P17		P17	I/O	Serial I/F ready output	$\overline{\text{SRDY}}$	O
P20	I/O port	P20	I/O	–	–	–
P21		P21	I/O	–	–	–
P22		P22	I/O	–	–	–
P23		P23	I/O	–	–	–
P30	I/O port	P30	I/O	–	–	–
P31		P31	I/O	–	–	–
P32		P32	I/O	–	–	–
P33		P33	I/O	–	–	–
P34		P34	I/O	–	–	–
P35		P35	I/O	–	–	–
P36		P36	I/O	–	–	–
P37		P37	I/O	–	–	–

5.8.3 Mask option

I/O port pull-up resistors

P00	☐ With resistor	☐ Gate direct
P01	☐ With resistor	☐ Gate direct
P02	☐ With resistor	☐ Gate direct
P03	☐ With resistor	☐ Gate direct
P04	☐ With resistor	☐ Gate direct
P05	☐ With resistor	☐ Gate direct
P06	☐ With resistor	☐ Gate direct
P07	☐ With resistor	☐ Gate direct
P10	☐ With resistor	☐ Gate direct
P11	☐ With resistor	☐ Gate direct
P12	☐ With resistor	☐ Gate direct
P13	☐ With resistor	☐ Gate direct
P14	☐ With resistor	☐ Gate direct
P15	☐ With resistor	☐ Gate direct
P16	☐ With resistor	☐ Gate direct
P17	☐ With resistor	☐ Gate direct
P20	☐ With resistor	☐ Gate direct
P21	☐ With resistor	☐ Gate direct
P22	☐ With resistor	☐ Gate direct
P23	☐ With resistor	☐ Gate direct
P30	☐ With resistor	☐ Gate direct
P31	☐ With resistor	☐ Gate direct
P32	☐ With resistor	☐ Gate direct
P33	☐ With resistor	☐ Gate direct
P34	☐ With resistor	☐ Gate direct
P35	☐ With resistor	☐ Gate direct
P36	☐ With resistor	☐ Gate direct
P37	☐ With resistor	☐ Gate direct

The I/O port has a built-in pull-up resistor that is activated during the input mode, and it can be individually selected for use or not by the mask option.
When "With resistor" is selected, the pull-up resistor of the port turns on during the input mode.
When the port terminal is changed from a low level to a high level by the built-in pull-up resistor, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and load capacitance of the terminal. So, when reading the I/O port, it is necessary to wait an appropriate amount of time. Make this waiting time the amount of time or more calculated by the following expression.

Waiting time = $R_{IN} \times (C_{IN} + C_L) \times 1.6$ [sec]

R_{IN}: Pull-up resistance Max. value
C_{IN}: Terminal capacitance Max. value
C_L: Load capacitance on the board

For unused I/O port, select "With resistor" default setting.

5.8.4 I/O control registers and I/O mode

The I/O port is set in the input mode or output mode by writing data to the corresponding I/O control register (IOC).
To set an I/O port to the input mode, write "0" to the I/O control register. The I/O port which is set in the input mode shifts to high impedance status and functions as an input port.
Reading during the input mode gets the input terminal status directly: the data being "1" when the terminal is at high (V_{DD}) level and "0" when it is at low (V_{SS}) level.
When "With resistor" is selected by mask option, the port terminal is pulled up during the input mode.

Data can be written to the data registers without affecting the terminal status even in the input mode.

To set an I/O port to the output mode, write "1" to the I/O control register. The I/O port which is set to output mode functions as an output port.
When the data register is set to "1", the port goes high (V_{DD}) level and when it is set to "0", the port goes low (V_{SS}) level.
Reading during the output mode gets the content of the data register.
At initial reset, the I/O control registers are set to "0" (I/O ports are set in the input mode).

5.8.5 I/O memory of I/O ports

Table 5.8.5.1 shows the I/O port control bits.

Table 5.8.5.1(a) I/O port control bits

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FFE0	D7	IOC07	P07 I/O control register	Output	Input	0	R/W	
	D6	IOC06	P06 I/O control register			0	R/W	
	D5	IOC05	P05 I/O control register			0	R/W	
	D4	IOC04	P04 I/O control register			0	R/W	
	D3	IOC03	P03 I/O control register			0	R/W	
	D2	IOC02	P02 I/O control register			0	R/W	
	D1	IOC01	P01 I/O control register			0	R/W	
	D0	IOC00	P00 I/O control register			0	R/W	
00FFE1	D7	IOC17	P17 I/O control register	Output	Input	0	R/W	
	D6	IOC16	P16 I/O control register			0	R/W	
	D5	IOC15	P15 I/O control register			0	R/W	
	D4	IOC14	P14 I/O control register			0	R/W	
	D3	IOC13	P13 I/O control register			0	R/W	
	D2	IOC12	P12 I/O control register			0	R/W	
	D1	IOC11	P11 I/O control register			0	R/W	
	D0	IOC10	P10 I/O control register			0	R/W	
00FFE2	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	IOC23	P23 I/O control register	Output	Input	0	R/W	
	D2	IOC22	P22 I/O control register			0	R/W	
	D1	IOC21	P21 I/O control register			0	R/W	
	D0	IOC20	P20 I/O control register			0	R/W	
00FFE3	D7	IOC37	P37 I/O control register	Output	Input	0	R/W	
	D6	IOC36	P36 I/O control register			0	R/W	
	D5	IOC35	P35 I/O control register			0	R/W	
	D4	IOC34	P34 I/O control register			0	R/W	
	D3	IOC33	P33 I/O control register			0	R/W	
	D2	IOC32	P32 I/O control register			0	R/W	
	D1	IOC31	P31 I/O control register			0	R/W	
	D0	IOC30	P30 I/O control register			0	R/W	

Table 5.8.5.1(b) I/O port control bits

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FFE4	D7	P07D	P07 I/O port data register	High	Low	1	R/W	
	D6	P06D	P06 I/O port data register			1	R/W	
	D5	P05D	P05 I/O port data register			1	R/W	
	D4	P04D	P04 I/O port data register			1	R/W	
	D3	P03D	P03 I/O port data register			1	R/W	
	D2	P02D	P02 I/O port data register			1	R/W	
	D1	P01D	P01 I/O port data register			1	R/W	
	D0	P00D	P00 I/O port data register			1	R/W	
00FFE5	D7	P17D	P17 I/O port data register	High	Low	1	R/W	
	D6	P16D	P16 I/O port data register			1	R/W	
	D5	P15D	P15 I/O port data register			1	R/W	
	D4	P14D	P14 I/O port data register			1	R/W	
	D3	P13D	P13 I/O port data register			1	R/W	
	D2	P12D	P12 I/O port data register			1	R/W	
	D1	P11D	P11 I/O port data register			1	R/W	
	D0	P10D	P10 I/O port data register			1	R/W	
00FFE6	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	P23D	P23 I/O port data register	High	Low	1	R/W	
	D2	P22D	P22 I/O port data register			1	R/W	
	D1	P21D	P21 I/O port data register			1	R/W	
	D0	P20D	P20 I/O port data register			1	R/W	
00FFE7	D7	P37D	P37 I/O port data register	High	Low	1	R/W	
	D6	P36D	P36 I/O port data register			1	R/W	
	D5	P35D	P35 I/O port data register			1	R/W	
	D4	P34D	P34 I/O port data register			1	R/W	
	D3	P33D	P33 I/O port data register			1	R/W	
	D2	P32D	P32 I/O port data register			1	R/W	
	D1	P31D	P31 I/O port data register			1	R/W	
	D0	P30D	P30 I/O port data register			1	R/W	

P00D–P07D: P0 port data register (00FFE4H)
P10D–P17D: P1 port data register (00FFE5H)
P20D–P23D: P2 port data register (00FFE6H•D0–D3)
P30D–P37D: P3 port data register (00FFE7H)

I/O port data can be read and output data can be set through these registers.

When writing:

When "1" is written: HIGH level
When "0" is written: LOW level

When the I/O port is set in the output mode, the written data is output from the I/O port terminal. When "1" is written as the port data, the port terminal goes high (V_{DD}) level, and when "0" is written, the terminal goes low (V_{SS}) level.
Port data can be written even in the input mode.

When reading:

When "1" is read: HIGH level ("1")
When "0" is read: LOW level ("0")

When the I/O port is in the input mode, the voltage level being input to the port terminal can be read. When the terminal voltage is high (V_{DD}) level, "1" is read, and "0" is read when it is low (V_{SS}) level.
In the output mode, the content of the data register is read.
At initial reset, the data bits are all set to "1" (HIGH level).

Refer to Section 5.8.2 for the data register of the ports set in a function other than I/O port.

IOC00–IOC07: P0 port I/O control register (00FFE0H)
IOC10–IOC17: P1 port I/O control register (00FFE1H)
IOC20–IOC23: P2 port I/O control register (00FFE2H•D0–D3)
IOC30–IOC37: P3 port I/O control register (00FFE3H)

Sets the I/O port to the input or output mode.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

The IOC register is the I/O control register corresponding to each I/O port individually.
When an IOC bit is set to "1", the corresponding I/O port enters the output mode. When it is set to "0", the port enters the input mode.
At initial reset, the IOC register is set to "0" (input mode).

Refer to Section 5.8.2 for the I/O control register of the ports set in a function other than I/O port.

5.8.6 Programming note

When the port terminal is changed from a low level to a high level by the built-in pull-up resistor, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and load capacitance of the terminal. So, when reading the I/O port, it is necessary to wait an appropriate amount of time. Make this waiting time the amount of time or more calculated by the following expression.

Waiting time = $R_{IN} \times (C_{IN} + C_L) \times 1.6$ [sec]

R_{IN}: Pull-up resistance Max. value
C_{IN}: Terminal capacitance Max. value
C_L: Load capacitance on the board

5.9 Clock Output

5.9.1 Configuration of clock output control circuit

The S1C88408 can output 4 kinds of clocks to external devices.
The kinds of clocks are as follows:

- OSC3 dividing clock (FOUT3)
- OSC1 dividing clock (FOUT1)
- The output clock of the 16-bit programmable timer 0 (TOUT0)
- The output clock of the 16-bit programmable timer 1 (TOUT1)

The output ports R40 and R41 are used for these outputs.
Figure 5.9.1.1 shows the configuration of the clock output control circuit.

The FOUT3 clock and TOUT0 clock cannot be output simultaneously, because they use the same port, similar to the FOUT1 clock and TOUT1 clock. The TOUT0 clock can be output when the 16-bit programmable timer operates in the 8-bit mode.

Refer to Section 5.12, "16-bit Programmable Timer", for the output clock of the 16-bit programmable timer.

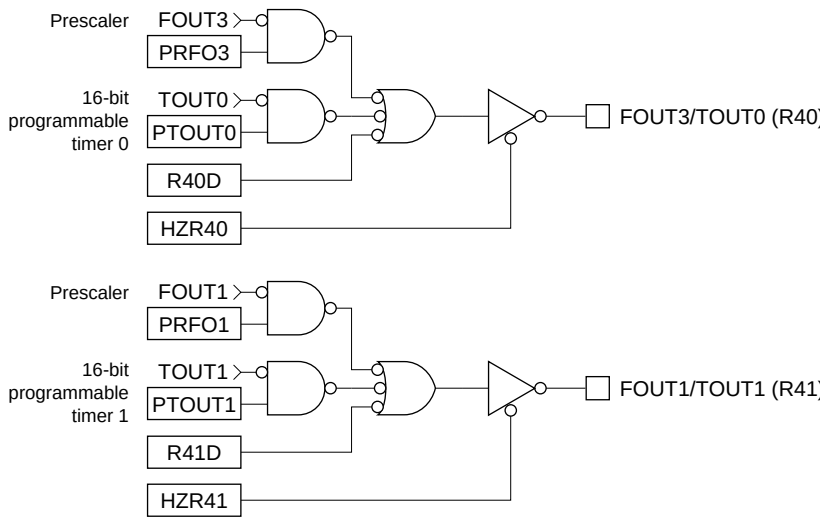


Fig. 5.9.1.1 Configuration of clock output control circuit

5.9.2 Clock output control

Table 5.9.2.1 shows the output control register of each clock.

To output the clock, fix the high-impedance control register of the output port to "0" and the output data register to "1". The output port terminal outputs the clock by writing "1" to the clock output control register in this status. The terminal goes high (V_{DD}) level when "0" is written.
Figure 5.9.2.1 shows the output waveform by this control.

The frequencies of the FOUT3 and FOUT1 clocks can be selected from eight types by setting the prescaler.

Note:
- *Be aware that the output is fixed at low (V_{SS}) level when the data register of the output port used for the clock output is set to "0".*
- *A hazard may occur on the output signal when the clock output control register is changed.*
- *Since the output clock becomes unstable when SLEEP mode is canceled, stop the output before shifting to SLEEP mode.*

Table 5.9.2.1 Clock output control registers

Clock	Output control register	Hi-Z control register	Data register
FOUT3	PRFO3 (00FF14H·D3)	HZR40 (00FFD4H·D0)	R40D (00FFD9H·D0)
FOUT1	PRFO1 (00FF14H·D7)	HZR41 (00FFD4H·D1)	R41D (00FFD9H·D1)
TOUT0	PTOUT0 (00FF30H·D3)	HZR40 (00FFD4H·D0)	R40D (00FFD9H·D0)
TOUT1	PTOUT1 (00FF31H·D3)	HZR41 (00FFD4H·D1)	R41D (00FFD9H·D1)

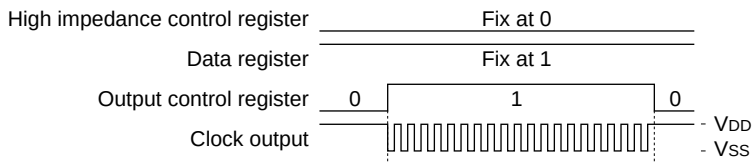


Fig. 5.9.2.1 Clock output waveform

5.9.3 I/O memory of clock output

Table 5.9.3.1 shows the clock output control bits.

Table 5.9.3.1 Clock output control bits

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF14	D7	PRFO1	FOUT1 output control	On	Off	0	R/W	
	D6	PSF12	FOUT1 division ratio			0	R/W	
			PSF12 PSF11 PSF10 Division ratio					
			1 1 1 f_{OSC1} / 128					
	D5	PSF11	1 1 0 f_{OSC1} / 64			0	R/W	
			1 0 1 f_{OSC1} / 32					
			1 0 0 f_{OSC1} / 16					
	D4	PSF10	0 1 1 f_{OSC1} / 8			0	R/W	
			0 1 0 f_{OSC1} / 4					
			0 0 1 f_{OSC1} / 2					
			0 0 0 f_{OSC1} / 1					
	D3	PRFO3	FOUT3 output control	On	Off	0	R/W	
	D2	PSF32	FOUT3 division ratio			0	R/W	
			PSF32 PSF31 PSF30 Division ratio					
			1 1 1 f_{OSC3} / 128					
	D1	PSF31	1 1 0 f_{OSC3} / 64			0	R/W	
			1 0 1 f_{OSC3} / 32					
			1 0 0 f_{OSC3} / 16					
	D0	PSF30	0 1 1 f_{OSC3} / 8			0	R/W	
			0 1 0 f_{OSC3} / 4					
			0 0 1 f_{OSC3} / 2					
			0 0 0 f_{OSC3} / 1					
00FF30	D7	MODE16	16-bit PTM 8-/16-bit mode selection	16-bit	8-bit × 2	0	R/W	
	D6	–	–	–	–	–	–	"0" when being read
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	PTOUT0	16-bit PTM0 clock output control	On	Off	0	R/W	
	D2	PTRUN0	16-bit PTM0 RUN/STOP control	Run	Stop	0	R/W	
	D1	PSET0	16-bit PTM0 preset	Preset	Invalid	0	W	"0" when being read
	D0	CKSEL0	16-bit PTM0 input clock selection	External clock	Internal clock	0	R/W	
00FF31	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	PTOUT1	16-bit PTM1 clock output control	On	Off	0	R/W	
	D2	PTRUN1	16-bit PTM1 RUN/STOP control	Run	Stop	0	R/W	
	D1	PSET1	16-bit PTM1 preset	Preset	Invalid	0	W	"0" when being read
	D0	CKSEL1	16-bit PTM1 input clock selection	External clock	Internal clock	0	R/W	
00FFD4	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	HZR42	R42 high impedance control register	High impedance	Comple-mentary	1	R/W	
	D1	HZR41	R41 high impedance control register			1	R/W	
	D0	HZR40	R40 high impedance control register			1	R/W	
00FFD9	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	R42D	R42 output port data register	High	Low	1	R/W	
	D1	R41D	R41 output port data register			1	R/W	
	D0	R40D	R40 output port data register			1	R/W	

HZR40, HZR41: R4 port high impedance control register (00FFD4H•D0, D1)

Sets the output terminals into a high impedance state.

When "1" is written: High impedance
When "0" is written: Complementary
Reading: Valid

The HZR40 and HZR41 registers are the high impedance control registers for the output ports R40 and R41 used for the clock output.
Fix data of the port used for the clock output at "0".
At initial reset, the HZR register is set to "1" (high impedance).

R40D, R41D: R4 port output data register (00FFD9H•D0, D1)

They are the data registers for the output ports R40, R41 used for the clock output.

When "1" is written: Clock output is possible
When "0" is written: LOW (V_{SS}) level is output
Reading: Valid

Fix data of the port used for the clock output at "1".
At initial reset, the data bits are all set to "1".

PSF10–PSF12: FOUT1 division ratio selection register (00FF14H•D4–D6)

Selects the frequency for the FOUT1 clock.
It can be selected from 8 types of division ratio shown in Table 5.9.3.1.
This register can also be read.
At initial reset, the PSF1 register is set to "0" (f_{OSC1} / 1).

PRFO1: FOUT1 output control register (00FF14H•D7)

Controls the FOUT1 output.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

When "1" is written to the PRFO1 register, the FOUT1 (R41) terminal outputs the clock selected with the PSF1 register. However, the high-impedance control register HZR41 of the output port R41 must be set to "0" and the data register R41D must be set to "1".
When "0" is written, the clock is not output.
At initial reset, the PRFO1 register is set to "0" (OFF).

PSF30–PSF32: FOUT3 division ratio selection register (00FF14H•D0–D2)

Selects the frequency for the FOUT3 clock.
It can be selected from 8 types of division ratio shown in Table 5.9.3.1.
This register can also be read.
At initial reset, the PSF3 register is set to "0" (f_{OSC3} / 1).

PRFO3: FOUT3 output control register (00FF14H•D3)

Controls the FOUT3 output.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

When "1" is written to the PRFO3 register, the FOUT3 (R40) terminal outputs the clock selected with the PSF3 register. However, the high-impedance control register HZR40 of the output port R40 must be set to "0" and the data register R40D must be set to "1". Furthermore, the OSC3 oscillation circuit must be used.
When "0" is written, the clock is not output.
At initial reset, the PRFO3 register is set to "0" (OFF).

PTOUT0: 16-bit programmable timer 0 clock output control register (00FF30H•D3)

Controls the output of the TOUT0 signal (16-bit programmable timer 0 clock).

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

The PTOUT0 register is the output control register for the TOUT0 signal. When "1" is written to this register, the TOUT0 signal is output from the TOUT0 (R40) terminal. When "0" is written, the terminal goes high (V_{DD}) level. However, the high-impedance control register HZR40 of the output port R40 must be set to "0" and the data register R40D must be set to "1".
The TOUT0 clock cannot be output simultaneously with the FOUT3 clock.
Refer to Section 5.12, "16-bit Programmable Timer", for setting of clock frequency.
At initial reset, the PTOUT0 register is set to "0" (OFF).

PTOUT1: 16-bit programmable timer 1 clock output control register (00FF31H•D3)

Controls the output of the TOUT1 signal (16-bit programmable timer 1 clock).

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

The PTOUT1 register is the output control register for the TOUT1 signal. When "1" is written to this register, the TOUT0 signal is output from the TOUT1 (R41) terminal. When "0" is written, the terminal goes high (V_{DD}) level. However, the high-impedance control register HZR41 of the output port R41 must be set to "0" and the data register R41D must be set to "1".
The TOUT1 clock cannot be output simultaneously with the FOUT1 clock.
Refer to Section 5.12, "16-bit Programmable Timer", for setting of clock frequency.
At initial reset, the PTOUT1 register is set to "0" (OFF).

5.9.4 Programming notes

(1) The FOUT3 clock and TOUT0 clock cannot be output simultaneously, because they use the same port, similar to the FOUT1 clock and TOUT1 clock.

(2) Be aware that the output is fixed at low (V_{SS}) level when the data register of the output port used for the clock output is set to "0".

(3) A hazard may occur on the output signal when the clock output control register is changed.

(4) Since the output clock becomes unstable when SLEEP mode is canceled, stop the output before shifting to SLEEP mode.

5.10 LCD Controller

5.10.1 Configuration of LCD controller

The S1C88408 has a built-in dot-matrix LCD controller and can drive a middle-scale LCD panel (eg., 240 × 100 dots, B&W) by connecting external common drivers (S1D16305 or S1D16700) and segment drivers (S1D16006 or S1D15700).

This LCD controller can drive 4-level gray scale LCD panels in addition to B&W (black and white) LCD panels. It also allows software to control scrolling display.
Figure 5.10.1.1 shows the configuration of the LCD controller and Figure 5.10.1.2 shows an example how to connect external LCD drivers.

The S1D16006 or S1D15700 are available for external segment drivers. Select the S1D16006 for cost down. The S1D15700 is better to reduce power.

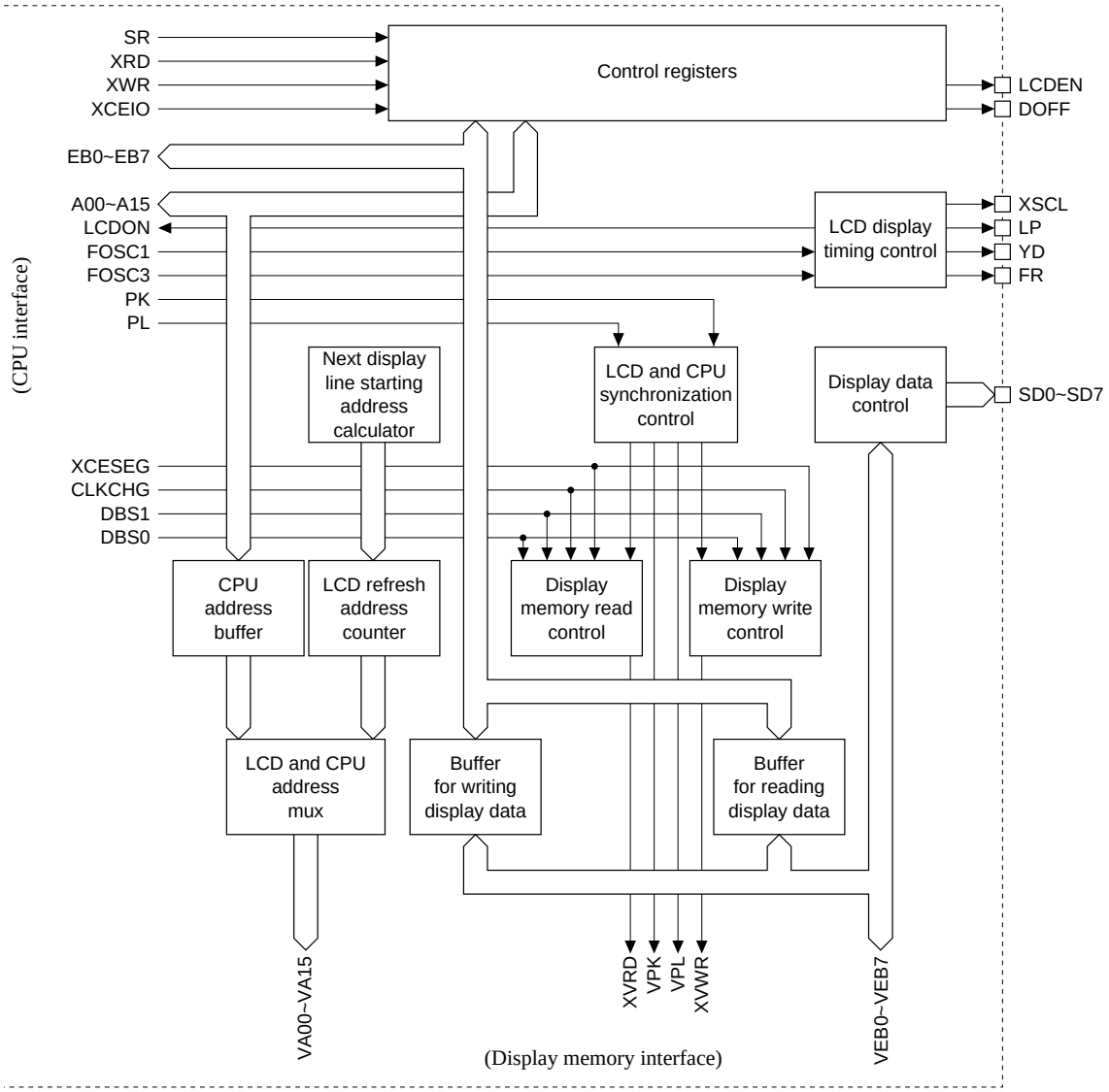


Fig. 5.10.1.1 Configuration of LCD controller

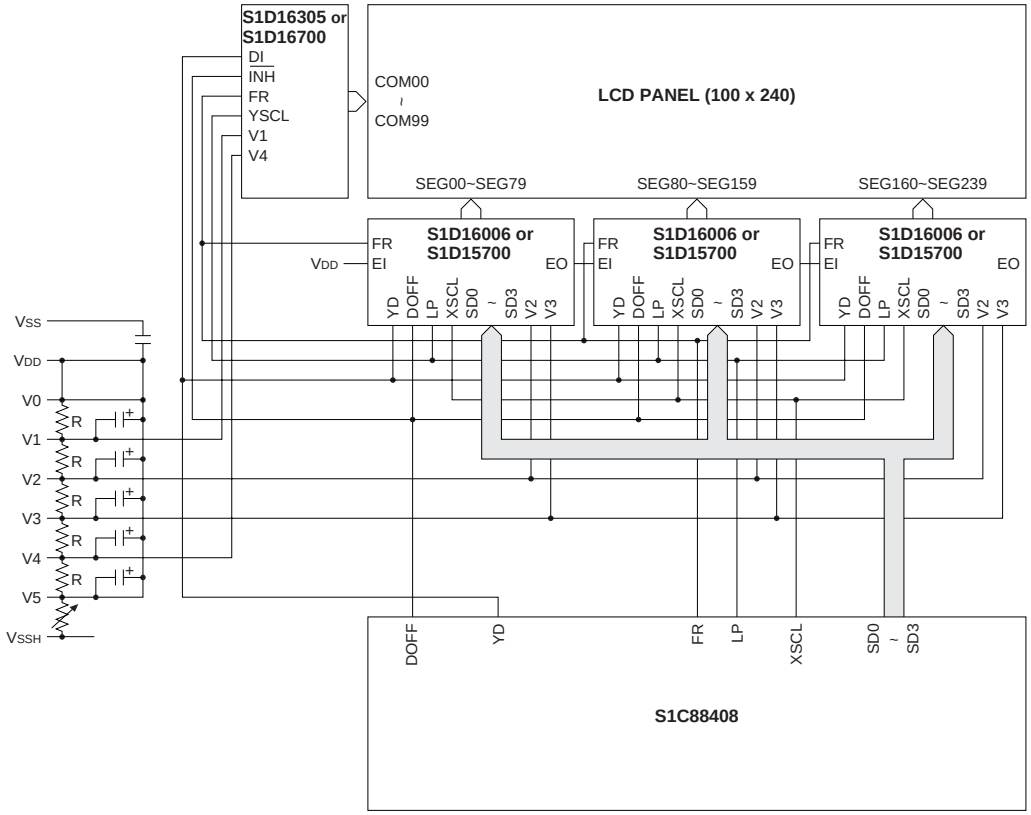


Fig. 5.10.1.2 Connection example of external LCD drivers

5.10.2 Output signals

This LCD controller outputs the following signals for controlling the S1D16305 (or S1D16700) common driver and the S1D16006 (or S1D15700) segment driver:

LCDEN

A LCD power control signal. It goes high level (V_{DD}) or low level (V_{SS}) according to the value set in the LCDEN register.

Note: When the LCD drive voltage is supplied to the LCD panel before supplying the power voltage (V_{DD}) to the S1C88408, the LCD panel may be damaged. To prevent this problem, design the circuit so that the LCD power is supplied to the LCD panel by switching the LCDEN signal to high level with the software. At initial reset, the LCDEN signal goes low level. This power control is also necessary when turning the S1C88408 off. Be sure to turn the LCD panel off before turning the S1C88408 off.

DOFF

A forced blank signal to turn the display off. Connect this signal to the $\overline{INH}$ terminal of the S1D16305 (or S1D16700) and the DOFF terminal of the S1D16006 (or S1D15700) and control the signal using the DISP register.

XSCL

A display data shift clock. Connect this signal to the XSCL terminal of the S1D16006 (or S1D15700).

LP

A display data latch pulse. Connect this signal to the YSCL terminal of the S1D16305 (or S1D16700) and the LP terminal of the S1D16006 (or S1D15700).

YD

A scan start pulse. Connect this signal to the DI terminal of the S1D16305 (or S1D16700) and the YD terminal of the S1D16006 (or S1D15700).

FR

A frame signal. Connect this signal to the FR terminals of the S1D16305 (or S1D16700) and S1D16006 (or S1D15700).

SD0–SD7

Display data signals. SD0 to SD3 are used in the 4-bit transfer mode. In the 8-bit transfer mode, SD0 to SD7 are all used.

5.10.3 Display control

To use the LCD controller, the following control procedures are necessary:

Setup of the LCD controller

(1) Selecting B&W or gray-scale mode

This LCD controller has two display mode: B&W (black and white) mode and 4-level gray scale mode. Select either one according to the LCD panel to be used. See Section 5.10.4, "B&W mode and gray-scale mode setting", for more information.

(2) Selecting the transfer data size

Select the size of data to be transferred to the segment drivers. 8-bit transfer and 4-bit transfer are available in this LCD controller. Select 4-bit transfer when using the S1D16006 or S1D15700. See Section 5.10.9, "Data transfer", for more information.

(3) Setting the LCD panel size and display start address

To correspond the display memory bits to the LCD panel dots one to one, it is necessary to set the LCD panel size in the LCD controller. Also a display start address should be set. See Section 5.10.6, "LCD panel", for more information.

(4) Setting the frame frequency

The frame frequency can be selected from 16 frequencies according to the LCD panel to be used. See Section 5.10.6, "LCD panel", for more information.

(5) Back light LCD panel

Since this LCD controller can reverse display by the REV register (REV = "1"), set in reverse display when using an LCD panel with a back light. The REV register can also be used to reverse display during normal display.

Turning display on and off

By writing "1" to the LCDEN register, the LCD controller turns on and starts outputting the signals to the external drivers. The content of the LCDEN register is output from the LCDEN terminal. Use the signal to control the LCD power supply.
When "0" is written to the LCDEN register, the LCD controller stops operating.

Note: The power of the LCD panel must be turned on/off while the LCDEN register is "1". Switching while the LCD controller is off (LCDEN = "0") may damage the LCD panel.

Besides the LCDEN register, the DISP register is provided for forced blanking function. When "1" is written to the DISP register, the LCD panel displays data in the display memory. When "0" is written, the display goes out. The control signals are output to the external drivers during forced blanking.

Data transfer control

The data transfer method can be selected according to the segment driver to be used. See Section 5.10.9, "Data transfer", for more information.
The data transfer uses the OSC3 clock. Therefore, turn the OSC3 oscillation on before writing "1" to the LCDEN register. Furthermore, wait 20 msec or more after turning the OSC3 oscillation on for stabilizing oscillation. Do not turn the OSC3 oscillation off during data transfer.

5.10.4 B&W and gray-scale mode setting

This LCD controller has two display mode: B&W (black and white) mode and 4-level gray scale mode. Select either one with the GRAY register according to the LCD panel to be used.
GRAY register = "0": B&W mode
GRAY register = "1": Gray-scale mode

In the B&W mode, the display memory bits correspond to the LCD panel dots one to one. When a memory bit is "0", the corresponding dot goes off and when the bit is"1", the dot goes on.

In the gray-scale mode, each two bits of the display memory corresponds to an LCD panel dot. When a display data is 00B, the corresponding dot goes off. As for the display data 01B, 10B and 11B, the intensity (gray-scale conversion code) can be specified using the GS1, GS2 and GS3 registers (8 bits each), respectively.
The specified gray-scale conversion code controls the 8 frame cycles for turning the dots on and off as shown in Figure 5.10.4.1.

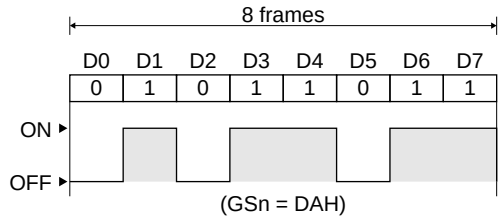


Fig. 5.10.4.1 Gray-scale conversion code

See LCD panel examples in Section 5.10.6 for correspondence between the display memory data and dots.

5.10.5 Display memory

The S1C88408 has a 3.75KB of RAM built-in and the display memory is allocated in the RAM. The display memory size can be selected from seven types listed in Table 5.10.5.1 by mask option.

Table 5.10.5.1 Display memory size

	Data memory	Display memory
1	1792 bytes 00F800H–00FEFFH	2048 bytes 00F000H–00F7FFH
2	1536 bytes 00F900H–00FEFFH	2304 bytes 00F000H–00F8FFH
3	1280 bytes 00FA00H–00FEFFH	2560 bytes 00F000H–00F9FFH
4	1024 bytes 00FB00H–00FEFFH	2816 bytes 00F000H–00FAFFH
5	768 bytes 00FC00H–00FEFFH	3072 bytes 00F000H–00FBFFH
6	512 bytes 00FD00H–00FEFFH	3328 bytes 00F000H–00FCFFH
7	256 bytes 00FE00H–00FEFFH	3584 bytes 00F000H–00FDFFH

Note: The display memory area configured by mask option may be used as data memory. However, the stack area cannot be assigned there.

The required display memory size is calculated by the following expressions according to the LCD panel size:

B&W LCD panel:

Memory size = (number of horizontal dots / 8) × Number of vertical dots

Gray-scale panel:

Memory size = (number of horizontal dots / 4) × Number of vertical dots

When using the vertical scroll function or virtual screen function, the display memory size should be increased for the scroll area or virtual area. Use the LCD panel examples in Sections 5.10.6 to 5.10.8 as reference for deciding the memory size.

5.10.6 LCD panel

FR frequency

The FR (frame) signal is generated by dividing the OSC1 clock. The dividing ratio can be selected using the CKCN and POINT5 registers. Select one according to the LCD panel to be used so that it is not out of the permissible range.

Table 5.10.6.1 FR frequency setting

CKCN2	CKCN1	CKCN0	POINT5	FR frequency
0	0	0	0	fosc1/(SLT+1)
0	0	0	1	fosc1/1.5/(SLT+1)
0	0	1	0	fosc1/2/(SLT+1)
0	0	1	1	fosc1/2.5/(SLT+1)
0	1	0	0	fosc1/3/(SLT+1)
0	1	0	1	fosc1/3.5/(SLT+1)
0	1	1	0	fosc1/4/(SLT+1)
0	1	1	1	fosc1/4.5/(SLT+1)
1	0	0	0	fosc1/5/(SLT+1)
1	0	0	1	fosc1/5.5/(SLT+1)
1	0	1	0	fosc1/6/(SLT+1)
1	0	1	1	fosc1/6.5/(SLT+1)
1	1	0	0	fosc1/7/(SLT+1)
1	1	0	1	fosc1/7.5/(SLT+1)
1	1	1	0	fosc1/8/(SLT+1)
1	1	1	1	fosc1/8.5/(SLT+1)

Setting the panel size

To correspond the display memory bits to the LCD panel dots one to one, it is necessary to set the LCD panel size in the LCD controller. The following registers should be used for this setting.

LBC6–LBC0: Sets the number of bytes for one line of display data.
Specify [Number of horizontal dots / 8] in the B&W mode or [Number of horizontal dots / 4] in the gray-scale mode.

SLT7–SLT0: Sets the number of lines (number of vertical dots) of the LCD panel.

SAD15–SAD0: Sets the display start address in the display memory.

LCD panel examples

(1) 240 × 100 dot B&W panel

Display memory setting

3072 byte memory size is selected by mask option (00F000H–00FBFFH)
In the B&W mode, the display memory bits correspond to the LCD panel dots one to one.

Register settings

LBC register: 1EH (240 / 8 = 30 bytes)
SLT register: 64H (100 dots)
SAD register: F000H

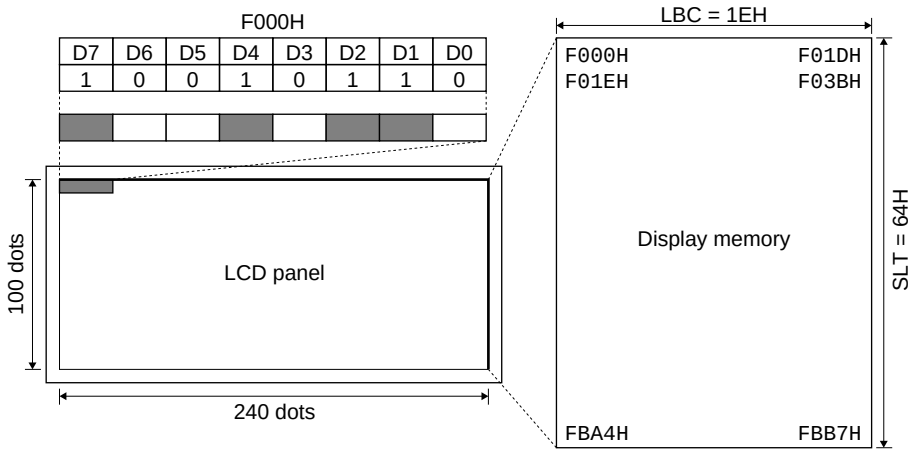


Fig. 5.10.6.1 Correspondence between LCD panel and display memory

(2) 160 × 80 dot gray-scale panel

Display memory setting

3328 byte memory size is selected by mask option (00F000H–00FCFFH)
In the gray-scale mode, each two bits of the display memory corresponds to an LCD panel dot.

Register settings

LBC register: 28H (160 / 4 = 40 bytes)
SLT register: 50H (80 dots)
SAD register: F000H

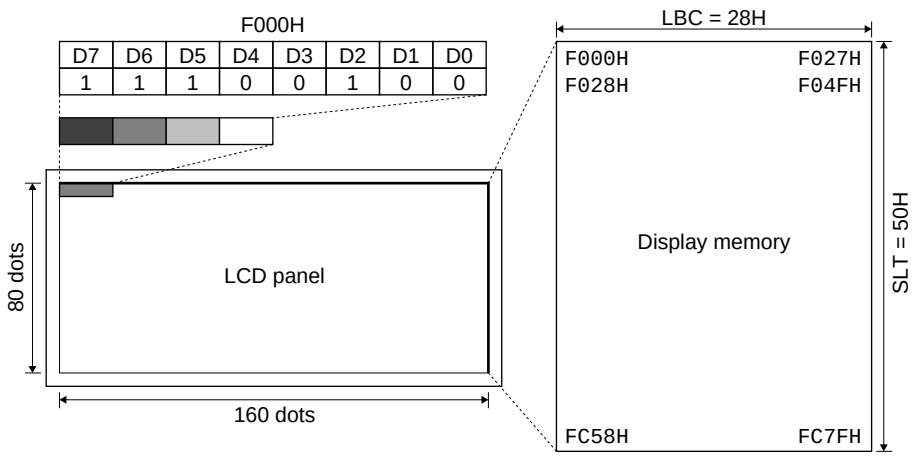


Fig. 5.10.6.2 Correspondence between LCD panel and display memory

The above examples are basic settings. See Sections 5.10.7 and 5.10.8 for examples when using the vertical scroll and virtual memory functions.

5.10.7 Vertical scroll function

Since the display start address is specified by the SAD register, vertical scroll can be done by increasing / decreasing the address by one line at a step.

Note: When using the vertical scroll function, it is necessary to reserve the display memory for the scroll area in addition to the memory for the LCD panel size.
Do not specify a display start address that cannot entirely display one screen (as exceeding the last display memory address in the middle of the LCD panel).

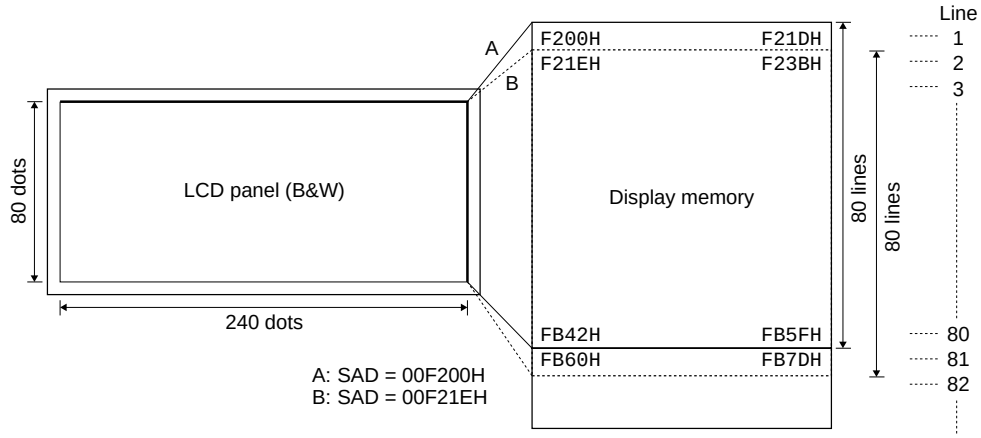


Fig. 5.10.7.1 Vertical scroll

5.10.8 Virtual screen function

In normal display, the beginning address of a line follows the end address of the previous line. In this LCD controller, the interval between the addresses can be specified using the APADJ register in byte units. This function can configure a virtual screen larger than the actual display size as shown in Figure 5.10.8.1. By controlling the display start address with the SAD register, the screen can be scrolled horizontally in byte units (B&W: 8-dot units, gray-scale: 4-dot units) or any part of the virtual screen can be displayed.

Furthermore, when a virtual screen with a two page size is assigned, the page can simply be switched.

Note: When using the virtual screen function, enough display memory must be reserved for the screen size.
Do not specify a display start address that cannot entirely display one screen (as exceeding the last display memory address in the middle of the LCD panel).

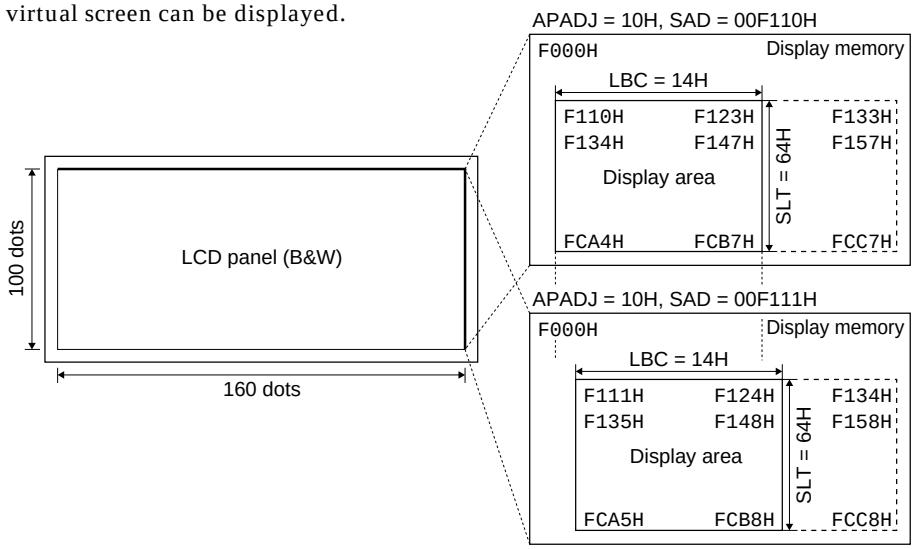


Fig. 5.10.8.1 Virtual screen function

5.10.9 Data transfer

Transfer data size

The transfer data size can be set to either 8 bits or 4 bits using the BITNO register.
4-bit data transfer only is available for the S1D16006 and S1D15700 drivers.

(1) 4-bit data transfer (BITNO = "0")

In 4-bit data transfer, data is sent as shown in Figure 5.10.9.1.

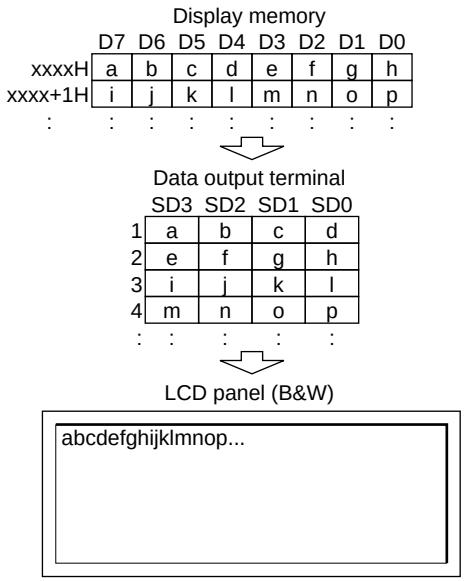


Fig. 5.10.9.1 4-bit data transfer

(2) 8-bit data transfer (BITNO = "1")

In 8-bit data transfer, data is sent as shown in Figure 5.10.9.2.

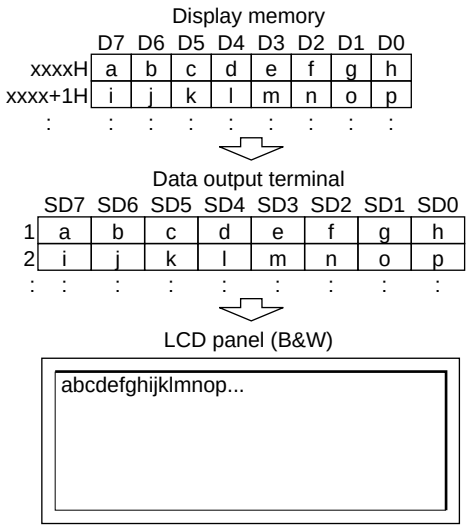


Fig. 5.10.9.2 8-bit data transfer

Data transfer method

The LCD controller has three data transfer modes for sending data to the segment drivers.

(1) Continuous data refresh mode

This mode is available for both the S1D16006 and S1D15700 segment drivers. The S1D16006 and the gray-scale display can be controlled only in this mode.
The continuous data refresh mode is set by writing "1" to the S1606 register. It is also set at initial reset.
In this mode, the display memory data is continuously sent to the segment driver in every frames while the LCDEN register is "1".
Figures 5.10.9.3 to 5.10.9.5 show the timing charts in the continuous data refresh mode.

(2) One-shot transfer mode (software control)

This mode is available only for the S1D15700 segment driver and only in the B&W mode. The S1D16006 and the gray-scale display cannot use this mode.
To set the one-shot transfer mode, write "0" to the S1606 and S1570A registers.
When "1" is written to the LCDEN register, the LCD controller outputs only the FR, LP and YD signals for a self-refresh of the S1D15700.
When updating the display, rewrite the display memory then write "1" to the S1570O register. The LCD controller outputs one-frame data in the frame cycle immediately after the writing. After that, the LCD controller outputs the FR, LP and YD signals only.
This mode is best to reduce current consumption in the three transfer mode because data is transferred only when it is necessary.
Figure 5.10.9.6 shows the timing chart in the one-shot transfer mode.

The S1570O register, which is used for a trigger of the one-shot transfer, can be read as a status. After "1" is written to the S1570O register, the register maintains "1" until the data transfer has completed to indicate that the data transfer circuit is in busy status. A new data transfer cannot be started during this period (writing "1" to the S1570O register is ignored).
Further this mode can generate an interrupt at the end of a data transfer (see the next section). When updating the display, check to see if the data transfer is possible using these functions.

(3) Hardware auto-transfer mode

This mode is available only for the S1D15700 segment driver and only in the B&W mode. The S1D16006 and the gray-scale display cannot use this mode.

To set the hardware auto-transfer mode, write "0" to the S1606 register and write "1" to the S1570A register.

When "1" is written to the LCDEN register, the LCD controller outputs only the FR, LP and YD signals for a self-refresh of the S1D15700.

When data is written to the display memory, the LCD controller outputs one-frame data in the frame cycle immediately after the writing. After that, the LCD controller outputs the FR, LP and YD signals only.

This mode does not need other software controls because data is automatically transferred by only writing display data.

This mode can reduce current consumption better than the continuous data refresh mode. However, display data is transferred even if data is written in the scroll area or virtual screen that are out of the display range. To avoid such a transfer or to write display data separately from display update, use the one-shot transfer with software control.

Figure 5.10.9.7 shows the timing chart in the hardware auto-transfer mode.

The data transfer status in this mode can be read from the S1570AS register. The S1570AS register maintains "1" during data transfer to indicate that the data transfer circuit is in busy status. It goes to "0" while the segment drivers are in self-refresh operation (the data transfer circuit is in standby status).

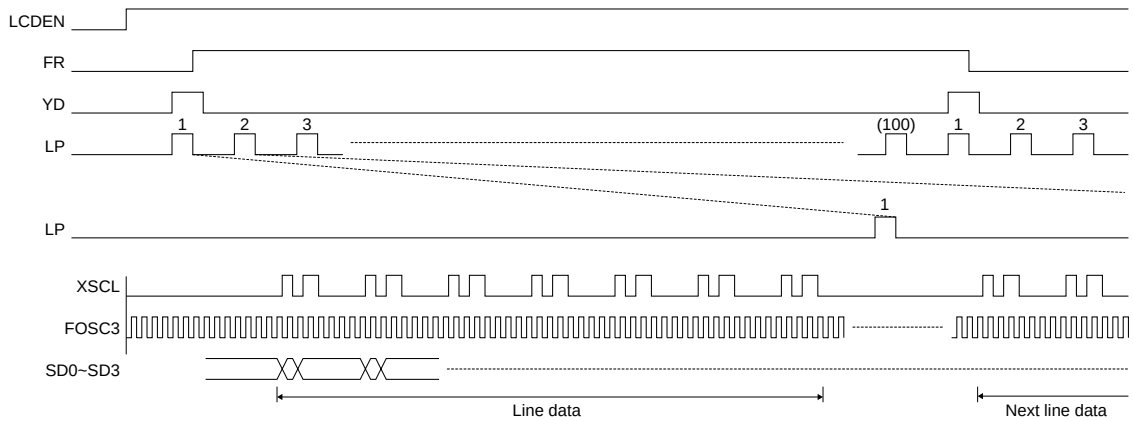


Fig. 5.10.9.3 Data transfer in continuous data refresh mode (B&W, 4-bit transfer)

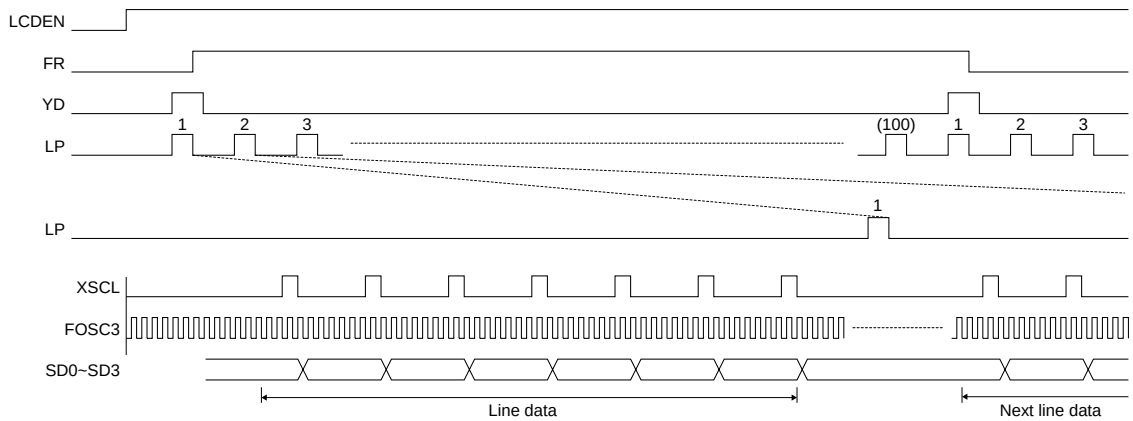


Fig. 5.10.9.4 Data transfer in continuous data refresh mode (gray-scale, 4-bit transfer)

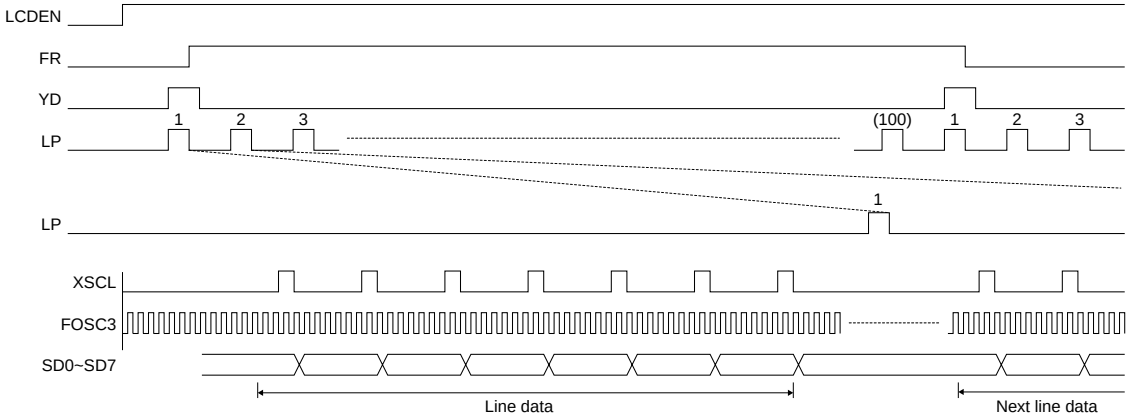


Fig. 5.10.9.5 Data transfer in continuous data refresh mode (B&W, 8-bit transfer)

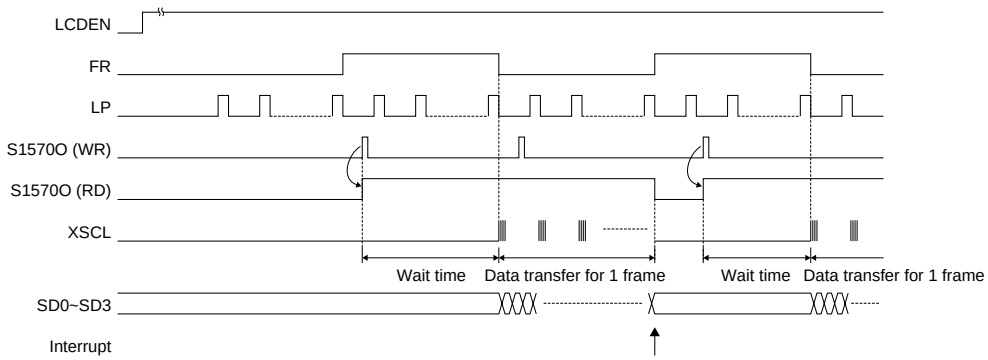


Fig. 5.10.9.6 Data transfer in one-shot transfer mode

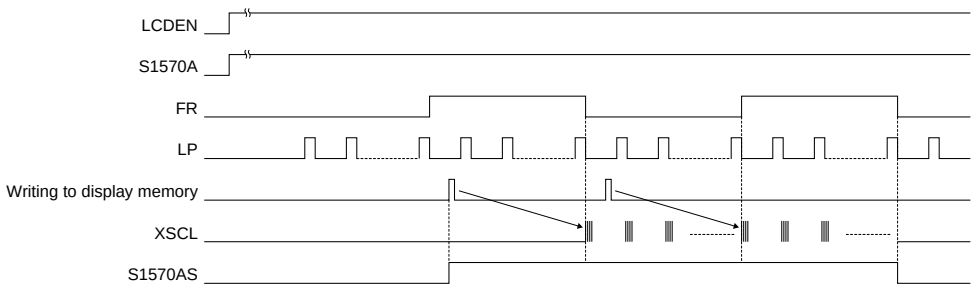


Fig. 5.10.9.7 Data transfer in hardware auto-transfer mode

5.10.10 Interrupt function

The LCD controller can generate an interrupt when a software one-shot data transfer or a hardware auto transfer has completed.
Figure 5.10.10.1 shows the configuration of the LCD controller interrupt circuit.

When a one-shot data transfer has completed, the interrupt factor flag FLCD is set to "1" and an interrupt is generated. The interrupt can be disabled using the interrupt enable register ELCD corresponding to the interrupt factor flag. See Figure 5.10.9.6 for the interrupt timing.

In addition, a priority level of the LCD controller interrupt for the CPU can be optionally set at levels 0 to 3 by the interrupt priority register PLCD.
For details on the above mentioned interrupt control registers and the operation following an interrupt generation, see Section 5.18, "Interrupt and Standby Mode".
The exception processing vector address of the interrupt factor is set as below.

LCD controller interrupt: 000024H

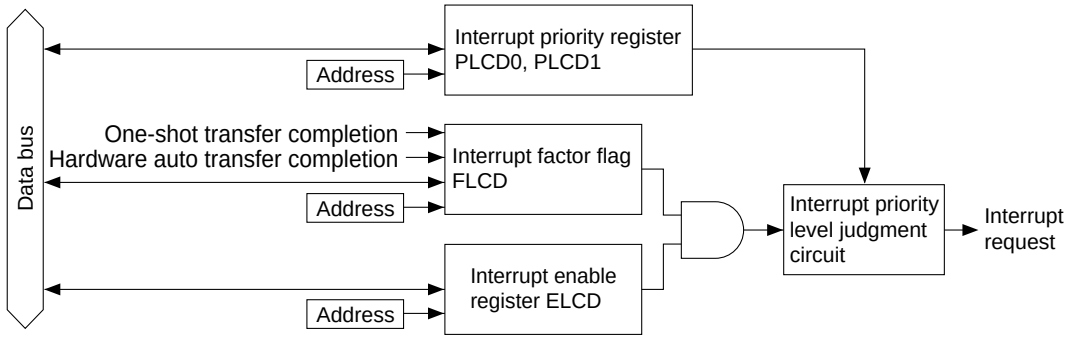


Fig. 5.10.10.1 Configuration of LCD interrupt circuit

5.10.11 I/O memory of LCD controller

Table 5.10.11.1 shows the control bits of the LCD controller.

Table 5.10.11.1(a) LCD controller control bits

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF60	D7	DISP	Display On/Off control	On	Off	0	R/W	
	D6	REV	Normal/Inverse display control	Inverse	Normal	0	R/W	
	D5	CKCN2	Scanning line frequency selection			0	R/W	
	D4	CKCN1				0	R/W	
	D3	CKCN0				0	R/W	
	D2	POINT5				0	R/W	
	D1	GRAY	Gray/B&W mode selection	Gray	B&W	0	R/W	
	D0	BITNO	8-bit/4-bit transfer selection	8 bits	4 bits	0	R/W	
00FF61	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	S1570AS	Hardware auto-transfer status	Busy	Standby	0	R	
	D3	LCDEN	LCD power On/Off control	On	Off	0	R/W	
	D2	S1570A	Hardware auto-transfer control	On	Off	0	R/W	
	D1	S1570O	One-shot transfer trigger/status	Busy	Standby	0	R	
				Trigger	Invalid	0	W	
	D0	S1606	Continuous refresh transfer control	On	Off	1	R/W	
00FF62	D7	–	–	–	–	–	–	"0" when being read
	D6	LBC6	Number of bytes per display line	D6(MSB)		0	R/W	
	D5	LBC5		D5		0	R/W	
	D4	LBC4		D4		0	R/W	
	D3	LBC3		D3	High	0	R/W	
	D2	LBC2		D2		0	R/W	
	D1	LBC1		D1		0	R/W	
	D0	LBC0		D0(LSB)		0	R/W	
00FF63	D7	SAD7	Display start address (lower 8 bits)	D7		0	R/W	
	D6	SAD6		D6		0	R/W	
	D5	SAD5		D5		0	R/W	
	D4	SAD4		D4		0	R/W	
	D3	SAD3		D3	High	0	R/W	
	D2	SAD2		D2		0	R/W	
	D1	SAD1		D1		0	R/W	
	D0	SAD0		D0		0	R/W	
00FF64	D7	SAD15	Display start address (upper 8 bits)	D15		0	R/W	
	D6	SAD14		D14		0	R/W	
	D5	SAD13		D13		0	R/W	
	D4	SAD12		D12		0	R/W	
	D3	SAD11		D11	High	0	R/W	
	D2	SAD10		D10		0	R/W	
	D1	SAD9		D9		0	R/W	
	D0	SAD8		D8		0	R/W	
00FF65	D7	SLT7	Total display lines	D7		0	R/W	
	D6	SLT6		D6		0	R/W	
	D5	SLT5		D5		0	R/W	
	D4	SLT4		D4		0	R/W	
	D3	SLT3		D3	High	0	R/W	
	D2	SLT2		D2		0	R/W	
	D1	SLT1		D1		0	R/W	
	D0	SLT0		D0		0	R/W	

Scanning line frequency selection

CKCN2	CKCN1	CKCN0	POINT5	Frequency
0	0	0	0	f_{OSC1}
0	0	0	1	f_{OSC1} / 1.5
0	0	1	0	f_{OSC1} / 2
0	0	1	1	f_{OSC1} / 2.5
0	1	0	0	f_{OSC1} / 3
0	1	0	1	f_{OSC1} / 3.5
0	1	1	0	f_{OSC1} / 4
0	1	1	1	f_{OSC1} / 4.5
1	0	0	0	f_{OSC1} / 5
1	0	0	1	f_{OSC1} / 5.5
1	0	1	0	f_{OSC1} / 6
1	0	1	1	f_{OSC1} / 6.5
1	1	0	0	f_{OSC1} / 7
1	1	0	1	f_{OSC1} / 7.5
1	1	1	0	f_{OSC1} / 8
1	1	1	1	f_{OSC1} / 8.5

Table 5.10.11.1(b) LCD controller control bits

Address	Bit	Name	Function		1	0	Init	R/W	Comment
00FF66	D7	–	–		–	–	–	–	"0" when being read
	D6	–	–		–	–	–	–	
	D5	–	–		–	–	–	–	
	D4	–	–		–	–	–	–	
	D3	–	–		–	–	–	–	
	D2	–	–		–	–	–	–	
	D1	–	–		–	–	–	–	
	D0	SLT8	Total display lines (MSB)		High	Low	0	R/W	
00FF67	D7	APADJ7	Address pitch adjustment	D7	High	Low	0	R/W	
	D6	APADJ6		D6			0	R/W	
	D5	APADJ5		D5			0	R/W	
	D4	APADJ4		D4			0	R/W	
	D3	APADJ3		D3			0	R/W	
	D2	APADJ2		D2			0	R/W	
	D1	APADJ1		D1			0	R/W	
	D0	APADJ0		D0			0	R/W	
00FF68	D7	GS17	Gray scale (0,1) conversion code	D7	High	Low	0	R/W	
	D6	GS16		D6			0	R/W	
	D5	GS15		D5			0	R/W	
	D4	GS14		D4			0	R/W	
	D3	GS13		D3			0	R/W	
	D2	GS12		D2			0	R/W	
	D1	GS11		D1			0	R/W	
	D0	GS10		D0			0	R/W	
00FF69	D7	GS27	Gray scale (1,0) conversion code	D7	High	Low	0	R/W	
	D6	GS26		D6			0	R/W	
	D5	GS25		D5			0	R/W	
	D4	GS24		D4			0	R/W	
	D3	GS23		D3			0	R/W	
	D2	GS22		D2			0	R/W	
	D1	GS21		D1			0	R/W	
	D0	GS20		D0			0	R/W	
00FF6A	D7	GS37	Gray scale (1,1) conversion code	D7	High	Low	0	R/W	
	D6	GS36		D6			0	R/W	
	D5	GS35		D5			0	R/W	
	D4	GS34		D4			0	R/W	
	D3	GS33		D3			0	R/W	
	D2	GS32		D2			0	R/W	
	D1	GS31		D1			0	R/W	
	D0	GS30		D0			0	R/W	
00FF21	D7	PTM21	8-bit programmable timer		PTM21 PTM20		0	R/W	
	D6	PTM20	interrupt priority register		PSI1 PSI0		0	R/W	
	D5	PSI1	Serial interface		PCTM1 PCTM0	Priority	0	R/W	
	D4	PSI0	interrupt priority register		PLCD1 PLCD0	level	0	R/W	
	D3	PCTM1	Clock timer		1 1	Level 3	0	R/W	
	D2	PCTM0	interrupt priority register		1 0	Level 2	0	R/W	
	D1	PLCD1	LCD controller		0 1	Level 1	0	R/W	
	D0	PLCD0	interrupt priority register		0 0	Level 0	0	R/W	
00FF25	D7	ET60S	Clock timer 60 S interrupt enable register		Interrupt is enabled	Interrupt is disabled	0	R/W	
	D6	ECTM1	Clock timer 1 Hz interrupt enable register				0	R/W	
	D5	ECTM2	Clock timer 2 Hz interrupt enable register				0	R/W	
	D4	ECTM8	Clock timer 8 Hz interrupt enable register				0	R/W	
	D3	ECTM32	Clock timer 32 Hz interrupt enable register				0	R/W	
	D2	ELCD	LCD controller interrupt enable register				0	R/W	
	D1	–	–				–	–	"0" when being read
	D0	–	–				–	–	
00FF29	D7	FT60S	Clock timer 60 S interrupt factor flag		(R) Interrupt factor has generated	(R) Interrupt factor has not generated	0	R/(W)	
	D6	FCTM1	Clock timer 1 Hz interrupt factor flag				0	R/(W)	
	D5	FCTM2	Clock timer 2 Hz interrupt factor flag				0	R/(W)	
	D4	FCTM8	Clock timer 8 Hz interrupt factor flag				0	R/(W)	
	D3	FCTM32	Clock timer 32 Hz interrupt factor flag				0	R/(W)	
	D2	FLCD	LCD controller interrupt factor flag		(W) Reset	(W) Invalid	0	R/(W)	
	D1	–	–				–	–	"0" when being read
	D0	–	–				–	–	

DISP: Display ON/OFF control register (00FF60H•D7)

Turns the display on and off.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

When "1" is written to the DISP register, the DOFF terminal goes low and when "0" is written, the DOFF terminal goes high.
This signal controls the external driver to turn the display on and off.
At initial reset, the DISP register is set to "0" (OFF).

REV: Normal/reverse display control register (00FF60H•D6)

Controls reverse display.

When "1" is written: Reverse display
When "0" is written: Normal display
Reading: Valid

When "1" is written to the REV register, the display reverses and when "0" is written, it returns to the normal. When using an LCD panel with a back light, the setting reverses.
At initial reset, the REV register is set to "0" (normal).

POINT5, CKCN0–CKCN2: Scanning line frequency selection register (00FF60H•D2–D5)

Selects a scanning line frequency from 16 types as shown in Table 5.10.11.2.

Table 5.10.11.2 Selection of scanning line frequency

CKCN2	CKCN1	CKCN0	POINT5	Frequency
0	0	0	0	fOSC1
0	0	0	1	fOSC1/1.5
0	0	1	0	fOSC1/2
0	0	1	1	fOSC1/2.5
0	1	0	0	fOSC1/3
0	1	0	1	fOSC1/3.5
0	1	1	0	fOSC1/4
0	1	1	1	fOSC1/4.5
1	0	0	0	fOSC1/5
1	0	0	1	fOSC1/5.5
1	0	1	0	fOSC1/6
1	0	1	1	fOSC1/6.5
1	1	0	0	fOSC1/7
1	1	0	1	fOSC1/7.5
1	1	1	0	fOSC1/8
1	1	1	1	fOSC1/8.5

The frame frequency is set as "scanning frequency / (SLT+1)".
At initial reset, these registers are set to "0" (fOSC1).

GRAY: Gray-scale/B&W mode selection register (00FF60H•D1)

Selects the gray-scale mode or B&W mode.

When "1" is written: Gray-scale mode
When "0" is written: B&W mode
Reading: Valid

When "1" is written to the GRAY register, the gray-scale mode is set and it displays a dot with 2 bits of the display memory.
When "0" is written, the B&W mode is set and each bit of the display memory corresponds to a dot on the LCD panel one to one.
At initial reset, the GRAY register is set to "0" (B&W mode).

BITNO: 8-bit/4-bit transfer selection register (00FF60H•D0)

Set the transfer data size.

When "1" is written: 8 bits
When "0" is written: 4 bits
Reading: Valid

BITNO sets the size of data to be transferred to the segment drivers. When "1" is written to the BITNO register, 8-bit transfer is set and when "0" is written, 4-bit transfer is set. The 4-bit transfer uses the data output terminals SD0 to SD3 only.
When using S1606 or S1570 as the segment driver, fix this register at "0".
When the gray-scale mode is selected, 4-bit transfer only is available regardless of the BITNO register setting.
At initial reset, the BITNO register is set to "0" (4 bits).

LCDEN: LCD power control register (00FF61H•D3)

Controls the power of the LCD controller.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

When "1" is written to the LCDEN register, the power of the LCD controller turns on and when "0" is written, it turns off.
The LCDEN terminal goes high while the LCDEN register is "1" and goes low while the register is "0". Use this signal for controlling the power of the LCD panel so that the LCD panel does not turn on while the LCDEN is "0".
At initial reset, the LCDEN register is set to "0" (OFF).

S1606: Continuous refresh transfer selection register (00FF61H•D0)

Sets the continuous refresh transfer mode.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

When "1" is written to the S1606 register, the continuous refresh transfer mode is set. In this mode, the display data is transferred to the segment drivers while the LCDEN register is "1". When using the S1606 segment driver and / or in gray-scale mode, fix this register at "1". When using other transfer mode, fix this register at "0".
At initial reset, the S1606 register is set to "1" (ON).

S1570O: One-shot transfer trigger/status (00FF61H•D1)

Starts one-shot transfer and indicates the transfer status.

When "1" is written: Trigger
When "0" is written: Invalid

When "1" is read: Busy
When "0" is read: Standby

By writing "1" to S1570O after rewriting the display memory, the LCD controller sends the display data to the segment drivers to update the display. Writing "0" and writing "1" during data transfer are invalid.
S1570O also indicates the status of the data transfer circuit when reading. It goes "1" during data transfer and goes "0" in standby status.
S1570O cannot be used for transferring data when using the S1606 segment driver and / or in gray-scale mode.
At initial reset, S1570O is set to "0" (standby).

S1570A: Hardware auto-transfer control register (00FF61H•D2)

Sets the hardware auto-transfer mode.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

When "1" is written to the S1570A register, the hardware auto-transfer mode is set. In this mode, the hardware automatically sends the display data to the segment drivers by writing data to the display memory while the LCDEN register is "1".
When using other transfer modes, fix this register at "0". This transfer mode cannot be selected when using the S1606 segment driver and / or in gray-scale mode.
At initial reset, the S1570A register is set to "0" (OFF).

S1570AS: Hardware auto-transfer status (00FF61H•D4)

Indicates the hardware auto-transfer status.

When "1" is read: Busy
When "0" is read: Standby
Writing: Invalid

S1570AS indicates the status of the data transfer circuit; it goes "1" during hardware auto-transfer and "0" in standby status.
S1570AS is a read only bit, so writing is invalid.
At initial reset, S1570AS is set to "0" (standby).

LBC0–LBC6: Horizontal LCD panel size setting register (00FF62H•D0–D6)

The display line size should be specified as the number of bytes with this register.
Specify [Number of dots / 8] in the B&W mode or [Number of dots / 4] in the gray-scale mode.
At initial reset, the LBC register is set to "00H".

SLT0–SLT8: Vertical LCD panel size setting register (00FF65H, 00FF66H•D0)

Number of display lines (vertical dot number) should be specified with this register.
At initial reset, the SLT register is set to "000H".

SAD0–SAD15: Display start address setting register (00FF63H, 00FF64H)

Specifies the display memory address that contains the data to be displayed at the first dot of the LCD panel.
By changing this address successively, the screen scrolls.
At initial reset, the SAD register is set to "0000H".

APADJ0–APADJ7: Address pitch adjustment register (00FF67H)

Specifies the address pitch between lines as number of bytes.
After a line has been displayed, the specified number of addresses in the display memory are skipped and the next line begins from the following address.
At initial reset, the APADJ register is set to "00H".

GS10–GS17: Gray-scale (0, 1) conversion code setting register (00FF68H)
GS20–GS27: Gray-scale (1, 0) conversion code setting register (00FF69H)
GS30–GS37: Gray-scale (1, 1) conversion code setting register (00FF6AH)

Sets the gray-scale conversion code.

When "1" is written: Dot goes ON
When "0" is written: Dot goes OFF
Reading: Valid

The GS1, GS2 and GS3 registers correspond to gray levels 01B, 10B and 11B, respectively.
Each register specifies a display pattern for eight frame cycles, thus the intensity of each gray level can be set. D0 to D7 in the register control dots on (1) and off (0) in each frame cycle.
At initial reset, the GS register is set to "00H" (OFF).

PLCD0, PLCD1: LCD controller interrupt priority register (00FF21H•D0, D1)

Sets the priority level of the LCD controller interrupt.
Table 5.10.11.3 shows the interrupt priority level which can be set by the PLCD register.

Table 5.10.11.3 Interrupt priority level settings

PLCD1	PLCD0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, the PLCD register is set to "0" (level 0).

ELCD: LCD controller interrupt enable register (00FF25H•D2)

Enables or disables the LCD controller interrupt generation to the CPU.

When "1" is written: Interrupt is enabled
When "0" is written: Interrupt is disabled
Reading: Valid

The ELCD register is the interrupt enable register corresponding to the LCD controller interrupt factor. When this register is set to "1", the interrupt is enabled, and when it is set to "0", the interrupt is disabled.
At initial reset, the ELCD register is set to "0" (interrupt is disabled).

FLCD: LCD controller interrupt factor flag (00FF29H•D2)

Indicates the generation of LCD controller interrupt factor.

When "1" is read: Int. factor has generated
When "0" is read: Int. factor has not generated

When "1" is written: Factor flag is reset
When "0" is written: Invalid

FLCD is the interrupt factor flag corresponding to the LCD controller interrupt. It is set to "1" when a software one-shot data transfer or a hardware auto transfer has completed.
At this point, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of the interrupt flags (I0 and I1), an interrupt is generated to the CPU.
Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag is set to "1" when the interrupt generation condition is met.
To accept the subsequent interrupt after an interrupt generation, it is necessary to reset the interrupt flag (set the interrupt flag to a lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and to reset the interrupt factor flag. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, the FLCD flag is reset to "0".

5.10.12 Programming notes

(1) Do not write "0" to the LCDEN register while the LCD panel is ON. The LCD panel may be damaged.

(2) Only the 4-bit continuous data refresh mode is available in the gray-scale mode. Do not use 8-bit data transfer or another transfer mode.

(3) The data transfer uses the OSC3 clock. Therefore, turn the OSC3 oscillation on before writing "1" to the LCDEN register. Furthermore, wait 20 msec or more after turning the OSC3 oscillation on for stabilizing oscillation. In the one-shot transfer mode or hardware auto-transfer mode, do not turn the OSC3 oscillation off before finishing data transfer. When the segment driver is in self-refresh status, the OSC3 oscillation can be stopped to reduce current consumption.

(4) When setting the CPU in SLEEP status, be sure to turn the LCD panel power off and stop operation of the LCD controller.

5.11 Clock Timer

5.11.1 Configuration of clock timer

The S1C88408 has a built-in clock timer that uses the OSC1 oscillation circuit as the clock source.
The clock timer is composed of an 8-bit binary counter that inputs a 256 Hz clock divided from f_{OSC1} and a 7-bit BCD counter for counting up to 60 seconds. The 128–1 Hz and 0–60 second counter data can be read by software. The 60-second counter can preset data.
Ordinarily, this clock timer is used for various timing functions such as clocks.
Figure 5.11.1.1 shows the configuration of the clock timer.

5.11.2 Interrupt function

The clock timer can generate an interrupt by each of the 32 Hz, 8 Hz, 2 Hz and 1 Hz signals or when the 60-second counter overflows.
Figure 5.11.2.1 shows the configuration of the clock timer interrupt circuit.

The interrupt factor flags FCTM32, FCTM8, FCTM2 and FCTM1 are set to "1" at the falling edge of the 32 Hz, 8 Hz, 2 Hz and 1 Hz signals, respectively. At that point, the interrupt is generated. When the 60-second counter overflows, FT60S is set to "1" to generate the 60S interrupt.
The interrupt can also be prohibited by setting the interrupt enable registers ECTM32, ECTM8, ECTM2, ECTM1 and ET60S corresponding to the interrupt factor flags.
Furthermore, the priority level of the input interrupt for the CPU can be set in an optional level (0–3) using the interrupt priority register PCTM (two bits).

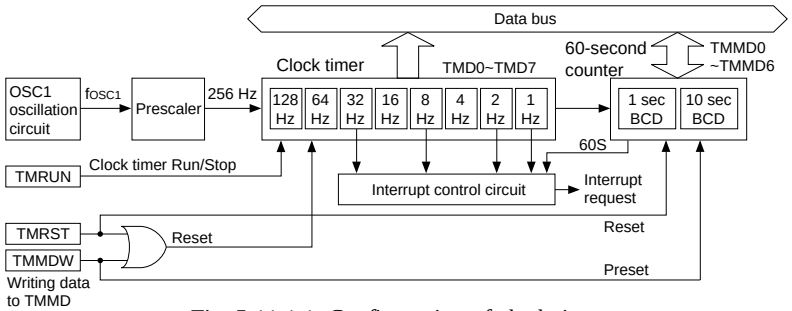


Fig. 5.11.1.1 Configuration of clock timer

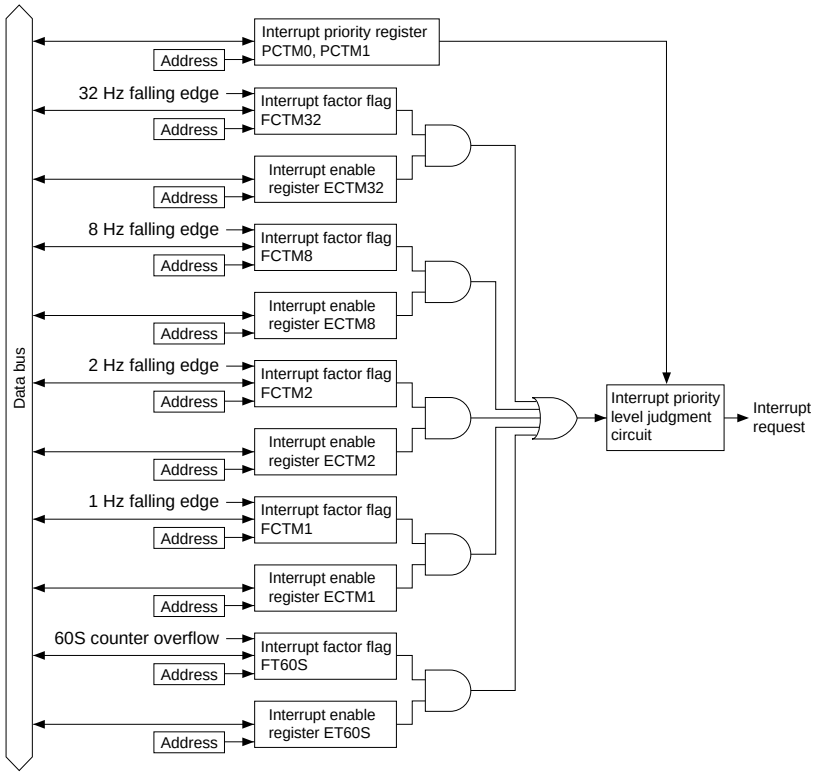


Fig. 5.11.2.1 Configuration of clock timer interrupt circuit

Refer to Section 5.18, "Interrupt and Standby Mode", for details of the interrupt control registers and operations subsequent to interrupt generation.

The exception processing vector address for the clock timer interrupt is set to 000028H.

Figures 5.11.2.2 and 5.11.2.3 show the timing chart for the clock timer.

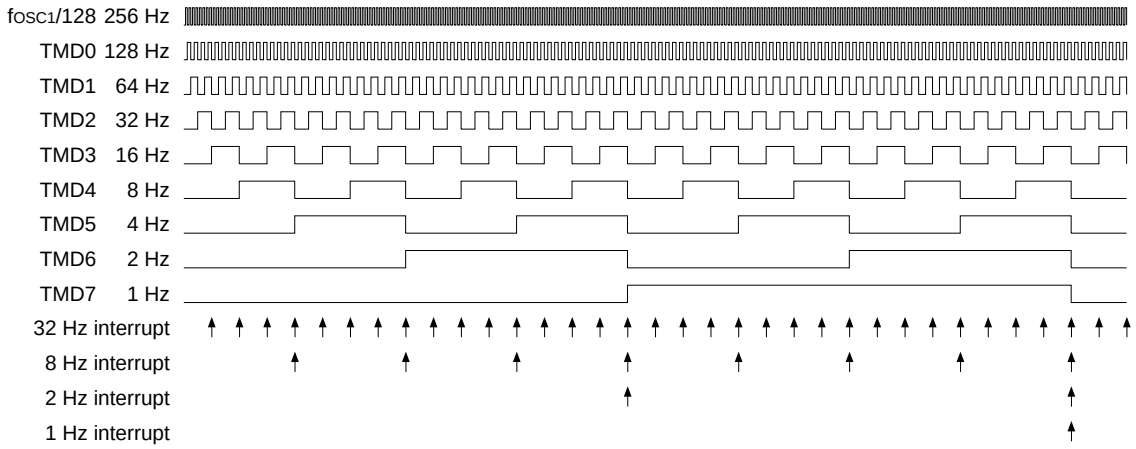


Fig. 5.11.2.2 Timing chart of clock timer (128 Hz–1 Hz)

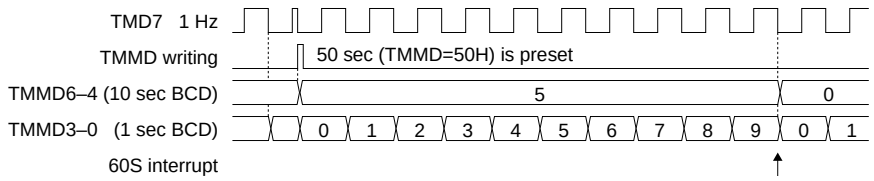


Fig. 5.11.2.3 Timing chart of clock timer (60-second counter)

5.11.3 I/O memory of clock timer

Table 5.11.3.1 shows the clock timer control bits.

Table 5.11.3.1 Clock timer control bits

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF21	D7	PTM21	8-bit programmable timer	PTM21	PTM20	0	R/W	
	D6	PTM20	interrupt priority register	PSI1	PSI0	0	R/W	
	D5	PSI1	Serial interface	PCTM1	PCTM0	Priority	0	R/W	
	D4	PSI0	interrupt priority register	PLCD1	PLCD0	level	0	R/W	
	D3	PCTM1	Clock timer	1	1	Level 3	0	R/W	
	D2	PCTM0	interrupt priority register	1	0	Level 2	0	R/W	
	D1	PLCD1	LCD controller	0	1	Level 1	0	R/W	
	D0	PLCD0	interrupt priority register	0	0	Level 0	0	R/W	
00FF25	D7	ET60S	Clock timer 60 S interrupt enable register	Interrupt is enabled	Interrupt is disabled	0	R/W	
	D6	ECTM1	Clock timer 1 Hz interrupt enable register			0	R/W	
	D5	ECTM2	Clock timer 2 Hz interrupt enable register			0	R/W	
	D4	ECTM8	Clock timer 8 Hz interrupt enable register			0	R/W	
	D3	ECTM32	Clock timer 32 Hz interrupt enable register			0	R/W	
	D2	ELCD	LCD controller interrupt enable register			0	R/W	
	D1	–	–			–	–	"0" when being read
	D0	–	–			–	–	
00FF29	D7	FT60S	Clock timer 60 S interrupt factor flag	(R)	(R)	0	R/(W)	
	D6	FCTM1	Clock timer 1 Hz interrupt factor flag	Interrupt	Interrupt	0	R/(W)	
	D5	FCTM2	Clock timer 2 Hz interrupt factor flag	factor has	factor has not	0	R/(W)	
	D4	FCTM8	Clock timer 8 Hz interrupt factor flag	generated	generated	0	R/(W)	
	D3	FCTM32	Clock timer 32 Hz interrupt factor flag			0	R/(W)	
	D2	FLCD	LCD controller interrupt factor flag	(W)	(W)	0	R/(W)	
	D1	–	–	Reset	Invalid	–	–	"0" when being read
	D0	–	–			–	–	
00FF50	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	–	–	–	–	–	–	
	D1	TMRST	Clock timer reset	Reset	Invalid	–	W	
	D0	TMRUN	Clock timer RUN/STOP	Run	Stop	0	R/W	
00FF51	D7	TMD7	Clock timer data 1 Hz	High	Low	0	R	
	D6	TMD6	Clock timer data 2 Hz			0	R	
	D5	TMD5	Clock timer data 4 Hz			0	R	
	D4	TMD4	Clock timer data 8 Hz			0	R	
	D3	TMD3	Clock timer data 16 Hz			0	R	
	D2	TMD2	Clock timer data 32 Hz			0	R	
	D1	TMD1	Clock timer data 64 Hz			0	R	
	D0	TMD0	Clock timer data 128 Hz			0	R	
00FF52	D7	–	–	–	–	–	–	"0" when being read
	D6	TMMD6	Clock timer data 10 sec (BCD)			0	R/W	
	D5	TMMD5				0	R/W	
	D4	TMMD4				0	R/W	
	D3	TMMD3	Clock timer data 1 sec (BCD)			0	R/W	
	D2	TMMD2				0	R/W	
	D1	TMMD1				0	R/W	
	D0	TMMD0				0	R/W	

TMD0–TMD7: Clock timer data (00FF51H)

The clock timer data (128 Hz–1 Hz) can be read. Correspondence between TMD bit and frequency is as follows:

TMD0: 128 Hz	TMD4: 8 Hz
TMD1: 64 Hz	TMD5: 4 Hz
TMD2: 32 Hz	TMD6: 2 Hz
TMD3: 16 Hz	TMD7: 1 Hz

Since TMD is read only, the writing operation is invalid.
At initial reset, the timer data is set to "00H".

TMMD0–TMMD6: 60-second counter data (00FF52H•D0–D6)

The 60-second counter data can be read. Correspondence between TMMD bit and data is as follows:

TMMD6–TMMD4: 10 sec BCD data
TMMD3–TMMD0: 1 sec BCD data

When data is written to the TMMD register, it is preset to the 60-second counter. At the same time, the timer for 128 Hz to 1 Hz is also reset.
The counter is preset only when data is written to the TMMD register. The register does not maintain the preset data and returns to 0-second when the counter overflows.
To prevent the counter from abnormal operation, do not preset data without a range of 0 to 59 (BCD).
At initial reset, the counter data is set to "0".

TMRST: Clock timer reset (00FF50H•D1)

Resets the clock timer.

When "1" is written: Clock timer reset
When "0" is written: No operation
Reading: Always "0"

The clock timer TMD and the 60S counter TMMD are reset by writing "1" to TMRST. When the clock timer is reset in RUN status, it restarts immediately after resetting. In the case of STOP status, the reset data "00H" is maintained.
No operation results when "0" is written to TMRST. TMRST is write only, and so it is always "0" at reading.

TMRUN: Clock timer RUN/STOP control register (00FF50H•D0)

Controls RUN / STOP of the clock timer.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The clock timer starts counting by writing "1" to the TMRUN register and stops by writing "0".
In STOP status, the count data is maintained until the timer is reset or is set in the next RUN status. Also, when STOP status changes to RUN status, the data that was maintained can be used for resuming the count.
At initial reset, the TMRUN register is set to "0" (STOP).

PCTM0, PCTM1: Clock timer interrupt priority register (00FF21H•D2, D3)

Sets the priority level of the clock timer interrupt. The PCTM register is the interrupt priority register corresponding to the clock timer interrupt.
Table 5.11.3.2 shows the interrupt priority level which can be set by this register.

Table 5.11.3.2 Interrupt priority level settings

PCTM1	PCTM0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, the PCTM register is set to "0" (level 0).

ECTM32: Clock timer 32 Hz interrupt enable register (00FF25H•D3)
ECTM8: Clock timer 8 Hz interrupt enable register (00FF25H•D4)
ECTM2: Clock timer 2 Hz interrupt enable register (00FF25H•D5)
ECTM1: Clock timer 1 Hz interrupt enable register (00FF25H•D6)
ET60S: Clock timer 60S interrupt enable register (00FF25H•D7)

Enables or disables the interrupt generation to the CPU.

When "1" is written: Interrupt is enabled
When "0" is written: Interrupt is disabled
Reading: Valid

ECTM32, ECTM8, ECTM2, ECTM1 and ET60S are the interrupt enable registers corresponding to 32 Hz, 8 Hz, 2 Hz, 1 Hz and 60S interrupt factors. Interrupt of the frequency in which the ECTM register is set to "1" is enabled, and the others in which the ECTM register is set to "0" are disabled.
At initial reset, the interrupt enable registers are all set to "0" (interrupt is disabled).

FCTM32: Clock timer 32 Hz interrupt factor flag (00FF29H•D3)
FCTM8: Clock timer 8 Hz interrupt factor flag (00FF29H•D4)
FCTM2: Clock timer 2 Hz interrupt factor flag (00FF29H•D5)
FCTM1: Clock timer 1 Hz interrupt factor flag (00FF29H•D6)
FT60S: Clock timer 60S interrupt factor flag (00FF29H•D7)

Indicates the generation of clock timer interrupt factor.

When "1" is read: Int. factor has generated
When "0" is read: Int. factor has not generated

When "1" is written: Factor flag is reset
When "0" is written: Invalid

FCTM32, FCTM8, FCTM2 and FCTM1 are the interrupt factor flags corresponding to the 32 Hz, 8 Hz, 2 Hz and 1 Hz interrupt, and are set to "1" at the falling edge of the respective signals. FT60S is the interrupt factor flag corresponding to the 60S interrupt and is set to "1" due to an overflow of the 60-second counter.
At this point, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of the interrupt flags (I0 and I1), an interrupt is generated to the CPU.
Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag is set to "1" when the interrupt generation condition is met.
To accept the subsequent interrupt after an interrupt generation, it is necessary to re-set the interrupt flags (set the interrupt flag to a lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and to reset the interrupt factor flag. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, the interrupt factor flags are all reset to "0".

5.11.4 Programming notes

(1) The clock timer actually entqzs into RUN or STOP status at the falling edge of the 256 Hz signal after writing to the TMRUN register. Consequently, when "0" is written to TMRUN, the timer stops after counting once more (+1). TMRUN is read as "1" until the timer actually stops.
Figure 5.11.4.1 shows the timing chart at the RUN / STOP control.

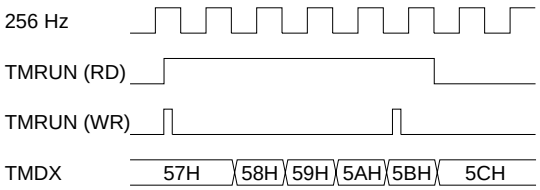


Fig. 5.11.4.1 Timing chart at RUN/STOP control

(2) The 60-second counter is preset only when data is written to the TMMD register. The register does not maintain the preset data and returns to 0-second when the counter overflows.
To prevent the counter from abnormal operation, do not preset data without a range of 0 to 59 (BCD).

5.12 16-bit Programmable Timer

5.12.1 Configuration of 16-bit programmable timer

The S1C88408 has a 16-bit programmable timer built-in. The timer consists of a 16-bit presettable down counter, and can be used as 16-bit × 1 channel or 8-bit × 2 channels of programmable timer. Furthermore, they function as event counters using the input port terminal.
Figure 5.12.1.1 shows the configuration of the 16-bit programmable timer.

Two 8-bit down counters, two reload data registers (RDR0, RDR1) and the compare data registers (CDR0, CDR1) corresponding to each down counter are arranged in the 16-bit programmable timer.
The reload data register is used to set an initial value to the down counter.
The compare data register stores data for comparison with the content of the down counter.
By setting these registers, a TOUT signal is generated, and it can be output to external devices.

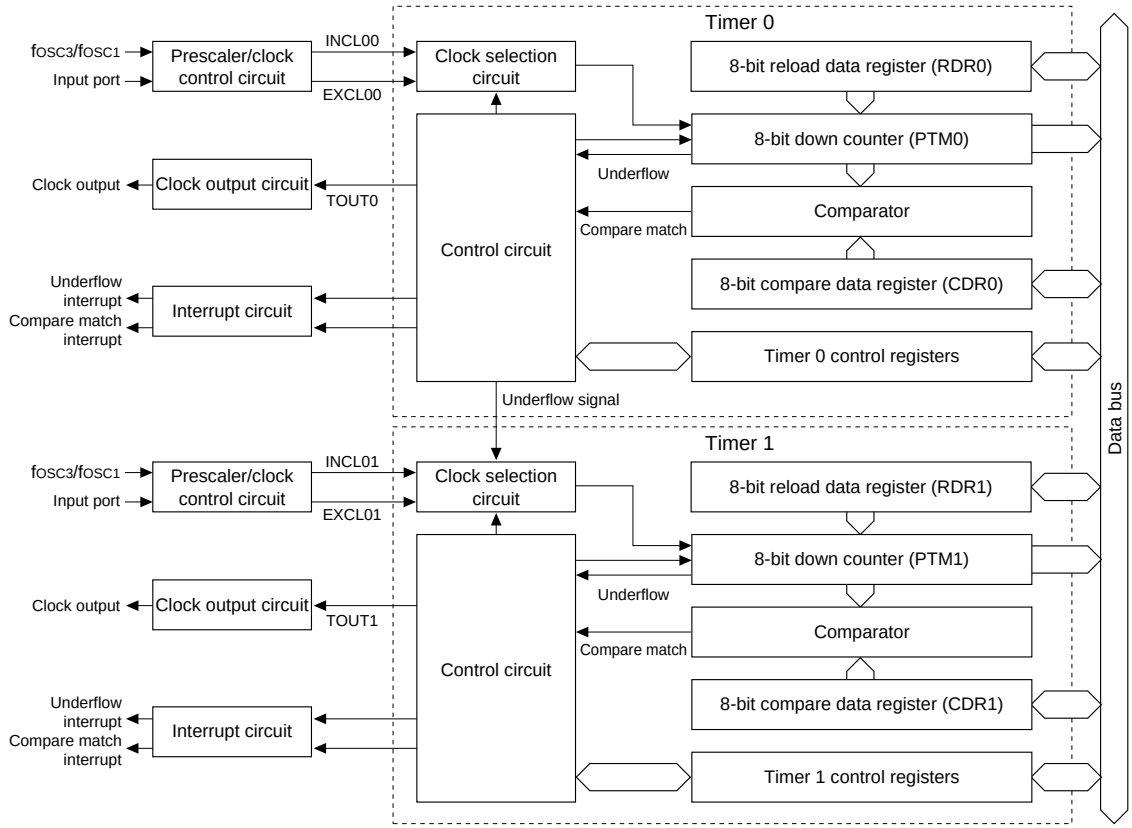


Fig. 5.12.1.1 Configuration of 16-bit programmable timer

5.12.2 Operation mode

The 16-bit programmable timer can be used as two channels of 8-bit timers or one channel of 16-bit timer. Two kinds of operation modes are provided corresponding to this configuration, and it can be selected by the 8-/16-bit mode selection register MODE16.

MODE16 register = "0": 8-bit mode
(8 bits × 2 channels)
MODE16 register = "1": 16-bit mode
(16 bits × 1 channel)

In the 8-bit mode, Timer 0 and Timer 1 can be controlled individually.
In the 16-bit mode, the underflow signal of Timer 0 is used as the input clock of Timer 1 so that the down counters operate as a 16-bit counter.
The timer in the 16-bit mode is controlled with the control registers for Timer 0 except for the clock output.

Figure 5.12.2.1 shows the timer configuration depending on the operation mode and Table 5.12.2.1 shows the configuration of the control registers.

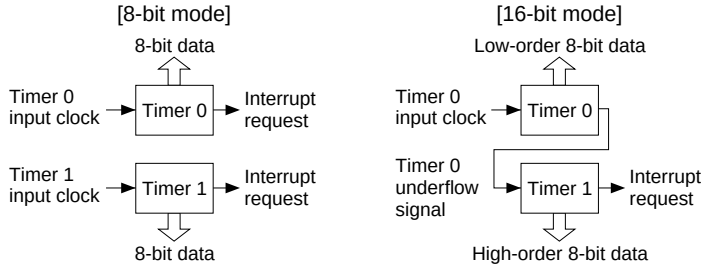


Fig. 5.12.2.1 Counter configuration in 8- and 16-bit mode

Table 5.12.2.1(a) Control registers in 8-bit mode

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF30	D7	MODE16	16-bit PTM 8-/16-bit mode selection	16-bit	8-bit × 2	0	R/W	
	D6	–	–	–	–	–	–	"0" when being read
	D5	–	–	–	–	–	–	"0" when being read
	D4	–	–	–	–	–	–	"0" when being read
	D3	PTOUT0	16-bit PTM0 clock output control	On	Off	0	R/W	
	D2	PTRUN0	16-bit PTM0 RUN/STOP control	Run	Stop	0	R/W	
	D1	PSET0	16-bit PTM0 preset	Preset	Invalid	0	W	"0" when being read
	D0	CKSEL0	16-bit PTM0 input clock selection	External clock	Internal clock	0	R/W	
00FF31	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	"0" when being read
	D5	–	–	–	–	–	–	"0" when being read
	D4	–	–	–	–	–	–	"0" when being read
	D3	PTOUT1	16-bit PTM1 clock output control	On	Off	0	R/W	
	D2	PTRUN1	16-bit PTM1 RUN/STOP control	Run	Stop	0	R/W	
	D1	PSET1	16-bit PTM1 preset	Preset	Invalid	0	W	"0" when being read
	D0	CKSEL1	16-bit PTM1 input clock selection	External clock	Internal clock	0	R/W	

Table 5.12.2.1(b) Control registers in 16-bit mode

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF30	D7	MODE16	16-bit PTM 8-/16-bit mode selection	16-bit	8-bit × 2	0	R/W	
	D6	–	–	–	–	–	–	"0" when being read
	D5	–	–	–	–	–	–	"0" when being read
	D4	–	–	–	–	–	–	"0" when being read
	D3	PTOUT0	Invalid (fixed at "0")	Invalid	Fixed at "0"	0	R/W	
	D2	PTRUN0	16-bit PTM RUN/STOP control	Run	Stop	0	R/W	
	D1	PSET0	16-bit PTM preset	Preset	Invalid	0	W	"0" when being read
	D0	CKSEL0	16-bit PTM input clock selection	External clock	Internal clock	0	R/W	
00FF31	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	"0" when being read
	D5	–	–	–	–	–	–	"0" when being read
	D4	–	–	–	–	–	–	"0" when being read
	D3	PTOUT1	16-bit PTM clock output control	On	Off	0	R/W	
	D2	PTRUN1	Invalid (fixed at "0")	Invalid	Fixed at "0"	0	R/W	
	D1	PSET1	Invalid (fixed at "0")	Invalid	Fixed at "0"	0	W	"0" when being read
	D0	CKSEL1	Invalid (fixed at "0")	Invalid	Fixed at "0"	0	R/W	

5.12.3 Setting of input clock

The clock to be input to the counter can be selected from either the internal clock or external clock by the input clock selection register (CKSEL) provided for each timer. The internal clock is an output of the prescaler. The external clock is used for the event counter function. A signal from the input port is used as the count clock.
Table 5.12.3.1 shows the input clock selection register and input clock of each timer.

Table 5.12.3.1 Input clock selection

Timer	Register setting	Input clock
Timer 0	CKSEL0 = "0"	INCL00 (Prescaler)
	CKSEL0 = "1"	EXCL00 (K10 input)
Timer 1	CKSEL1 = "0"	INCL01 (Prescaler)
	CKSEL1 = "1"	EXCL01 (K11 input)

When the internal clock is used, the clock frequency is set by selecting a source clock and a division ratio of the prescaler.
When the external clock is selected, a signal from the input port is directly input to the programmable timer.
However, it is necessary to control the output from the clock control circuit and to input the internal clock and external clock to the timers.
Refer to Section 5.5, "Prescaler and Clock Control Circuit for Peripheral Circuits", for selection of the division ratio and clock output control.

When the 16-bit mode is selected, the programmable timer operates with the clock input to Timer 0, and Timer 1 inputs the Timer 0 underflow signal as the clock. Therefore, the setting of Timer 1 input clock is invalid.

5.12.4 Operation and control of timer

Reload data register and setting of initial value

The reload data register (RDR) is used to set an initial value of the down counter.
In the 8-bit mode, it is used as two 8-bit registers RDR0 (Timer 0) and RDR1 (Timer 1) separate for each timer.
In the 16-bit mode, the RDR0 register is handled as low-order 8 bits of reload data, and the RDR1 register is as high-order 8 bits.

The reload data register can be read and written, and both the RDR0 and RDR1 registers are set to FFH at initial reset.

Data written in this register is loaded into the down counter, and a down counting starts from the value.
The preset to down counter is done in the following two cases:

1) When software presets

The software preset can be done using the preset control bits PSET0 (Timer 0) and PSET1 (Timer 1). When the preset control bit is set to "1", the content of the reload data register is loaded into the down counter at that point.
In the 16-bit mode, a 16-bit reload data is loaded all at one time by setting PSET0. In this case, writing to PSET1 is invalid.

2) When down counter has underflowed during a count

Since the down counter presets the reload data by the underflow, the underflow period is decided according to the value set in the reload data register. This underflow generates an interrupt, and controls the clock (TOUT signal) output.

Compare data register

The programmable timer has a built-in data comparator so that count data can be compared with an optional value. The compare data register (CDR) is used to set the value to be compared.
In the 8-bit mode, it is used as two 8-bit registers CDR0 (Timer 0) and CDR1 (Timer 1) separate for each timer.
In the 16-bit mode, the CDR0 register is handled as low-order 8 bits of compare data, and the CDR1 register is as high-order 8 bits.

The compare data register can be read and written, and both the CDR0 and CDR1 registers are set to 00H at initial reset.

The programmable timer compares count data with the compare data register (CDR), and generates a compare match signal when they become the same value. This compare match signal generates an interrupt, and controls the clock (TOUT signal) output.

Timer operation

Timer 0 and Timer 1 are equipped with PTRUN0 (Timer 0) and PTRUN1 (Timer 1) registers which control the RUN / STOP of the timer. The programmable timer starts down counting by writing "1" to the PTRUN register. However, it is necessary to control the input clock and to preset the reload data before starting a count.

When "0" is written to PTRUN register, clock input is prohibited, and the count stops.
This RUN / STOP control does not affect data in the counter. The data in the counter is maintained during count deactivation, so it is possible to resume counting from the data.

In the 8-bit mode, the channels can be controlled individually by the PTRUN0 register and the PTRUN1 register.
In the 16-bit mode, the PTRUN0 register controls both channels as a 16-bit timer. In this case, control of the PTRUN1 register is invalid.

The buffers PTM0 (Timer 0) and PTM1 (Timer 1) are attached to the counter, and reading is possible in optional timing.

When the counter agrees with the data set in the compare data register during down counting, the timer generates a compare match interrupt.
And, when the counter underflows, an underflow interrupt is generated, and the initial value set in the reload data register is loaded to the counter.
The interrupt generated does not stop the down counting.
After an underflow interrupt is generated, the counter continues counting from the initial value reloaded.

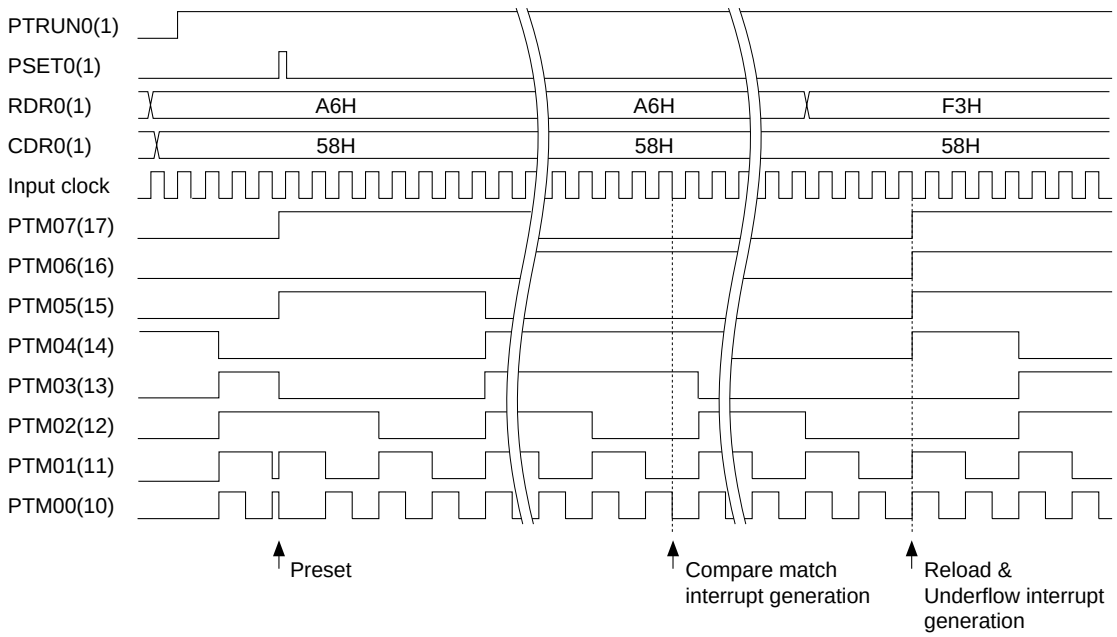


Fig. 5.12.4.1 Basic operation timing of counter (an example of 8-bit mode)

5.12.5 Interrupt function

The 16-bit programmable timer can generate an interrupt with the compare match signal and underflow signal of each timer.
Figure 5.12.5.1 shows the configuration of the 16-bit programmable timer interrupt circuit.

The compare match signal and underflow signal of each timer set the corresponding interrupt factor flag to "1". At that point, the interrupt is generated. The interrupt can also be prohibited by setting the interrupt enable register to correspond with the interrupt factor flag.
Furthermore, the priority level of the interrupt for the CPU can be set to an optional level (0–3) using the interrupt priority register.

Table 5.12.5.1 shows the interrupt factor flags, interrupt enable registers and interrupt priority registers corresponding to the interrupt factors.

In the 8-bit mode, the compare match interrupt factor flag and underflow interrupt factor flag are individually set to "1" by the timers.
In the 16-bit mode, the interrupt factor flags of Timer 1 are set to "1" by the compare match and underflow of 16 bits.

Refer to Section 5.18, "Interrupt and Standby Mode", for details of the interrupt control registers and operations subsequent to interrupt generation.

The exception processing vector addresses for the 16-bit programmable timer interrupt are set as follows:

Timer 0 underflow interrupt:	000010H
Timer 0 compare match interrupt:	000012H
Timer 1 underflow interrupt:	000014H
Timer 1 compare match interrupt:	000016H

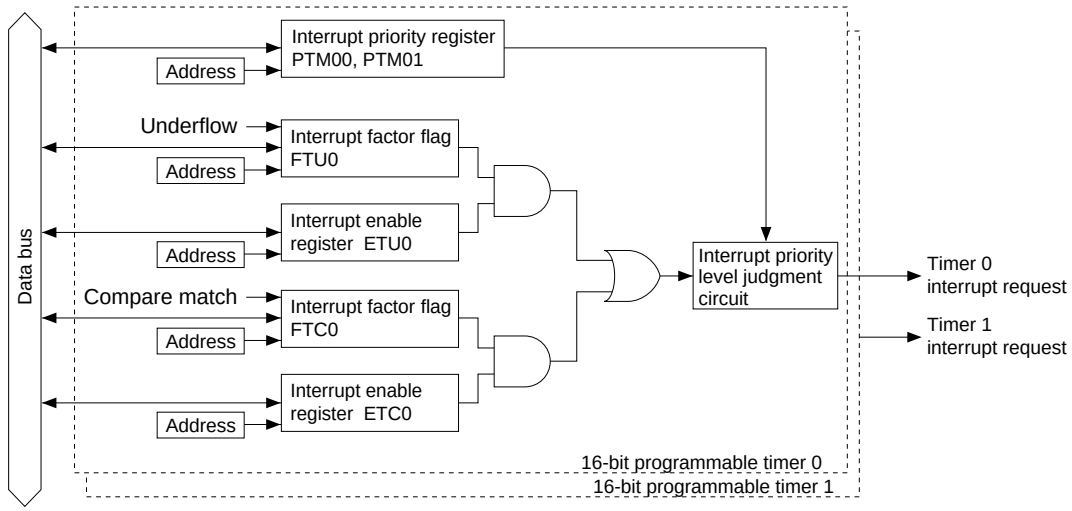


Fig. 5.12.5.1 Configuration of 16-bit programmable timer interrupt circuit

Table 5.12.5.1 Interrupt control registers

Interrupt factor		Interrupt factor flag		Interrupt enable register		Interrupt priority register	
		Name	Address·Dx	Name	Address·Dx	Name	Address·Dx
16-bit programmable timer 0	Counter underflow	FTU0	00FF28H·D3	ETU0	00FF24H·D3	PTM00	00FF20H·D0
	Compare match between counter and compare data register CDR0	FTC0	00FF28H·D4	ETC0	00FF24H·D4	PTM01	00FF20H·D1
16-bit programmable timer 1	Counter underflow	FTU1	00FF28H·D5	ETU1	00FF24H·D5	PTM10	00FF20H·D2
	Compare match between counter and compare data register CDR1	FTC1	00FF28H·D6	ETC1	00FF24H·D6	PTM11	00FF20H·D3

5.12.6 Setting of TOUT output

The 16-bit programmable timer can generate TOUT signals with the underflow and compare match signals of Timer 0 and Timer 1. The TOUT signal generated in the 16-bit programmable timer can be output from the output port terminal shown in Table 5.12.6.1 so that a programmable clock can be supplied for external devices.

Table 5.12.6.1 TOUT output terminal

Timer	Output clock name	Output terminal
Timer 0	TOUT0	R40
Timer 1	TOUT1	R41

The TOUT signal rises at the falling edge of the underflow signal and falls at the falling edge of the compare match signal. Therefore, it is possible to change the frequency and duty ratio of the TOUT signal by setting the reload data register (RDR) and compare data register (CDR). However, it needs a condition setting: RDR>CDR, CDR≠ 0.
In the case of RDR≤CDR, TOUT signal is fixed at "1".

The TOUT output can be controlled by the TOUT output control register of each timer (Timer 0: PTOUT0, Timer 1: PTOUT1).
In the 16-bit mode, the output is controlled by the control register PTOUT1 for Timer 1. The clock is output from Timer 1.

Figure 5.12.6.1 shows the output waveform of TOUT signal.

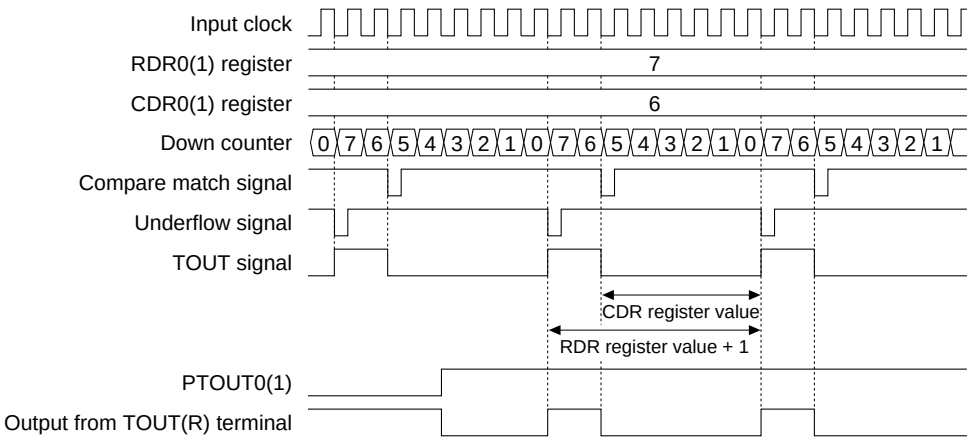


Fig. 5.12.6.1 Output waveform of TOUT signal

Refer to Section 5.9, "Clock Output", for output control of TOUT signal to the outside.

5.12.7 I/O memory of 16-bit programmable timer

Table 5.12.7.1 shows the 16-bit programmable timer control bits.

Table 5.12.7.1(a) 16-bit programmable timer control bits

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF10	D7	PRPRT1	16-bit programmable timer 1 clock control	On	Off	0	R/W	
	D6	PST12	16-bit programmable timer 1 division ratio PST12 PST11 PST10 (OSC3) (OSC1) 1 1 1 fOSC3 / 4096 fOSC1 / 128			0	R/W	
	D5	PST11	1 1 0 fOSC3 / 1024 fOSC1 / 64 1 0 1 fOSC3 / 256 fOSC1 / 32 1 0 0 fOSC3 / 128 fOSC1 / 16			0	R/W	
	D4	PST10	0 1 1 fOSC3 / 64 fOSC1 / 8 0 1 0 fOSC3 / 32 fOSC1 / 4 0 0 1 fOSC3 / 8 fOSC1 / 2 0 0 0 fOSC3 / 2 fOSC1 / 1			0	R/W	
	D3	PRPRT0	16-bit programmable timer 0 clock control	On	Off	0	R/W	
	D2	PST02	16-bit programmable timer 0 division ratio PST02 PST01 PST00 (OSC3) (OSC1) 1 1 1 fOSC3 / 4096 fOSC1 / 128			0	R/W	
	D1	PST01	1 1 0 fOSC3 / 1024 fOSC1 / 64 1 0 1 fOSC3 / 256 fOSC1 / 32 1 0 0 fOSC3 / 128 fOSC1 / 16			0	R/W	
	D0	PST00	0 1 1 fOSC3 / 64 fOSC1 / 8 0 1 0 fOSC3 / 32 fOSC1 / 4 0 0 1 fOSC3 / 8 fOSC1 / 2 0 0 0 fOSC3 / 2 fOSC1 / 1			0	R/W	
00FF12	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	–	–	–	–	–	–	
	D1	PRTF1	16-bit programmable timer 1 source clock selection	fOSC1	fOSC3	0	R/W	
	D0	PRTF0	16-bit programmable timer 0 source clock selection	fOSC1	fOSC3	0	R/W	
00FF15	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	–	–	–	–	–	–	
	D1	PK11ON	EXCL01 input clock ON/OFF control	On	Off	0	R/W	
	D0	PK10ON	EXCL00 input clock ON/OFF control	On	Off	0	R/W	
00FF20	D7	PK11	K10–K13	PK11 PK10		0	R/W	
	D6	PK10	interrupt priority register	PK01 PK00		0	R/W	
	D5	PK01	K00–K07	PTM11 PTM10	Priority	0	R/W	
	D4	PK00	interrupt priority register	PTM01 PTM00	level	0	R/W	
	D3	PTM11	16-bit programmable timer 1	1 1	Level 3	0	R/W	
	D2	PTM10	interrupt priority register	1 0	Level 2	0	R/W	
	D1	PTM01	16-bit programmable timer 0	0 1	Level 1	0	R/W	
	D0	PTM00	interrupt priority register	0 0	Level 0	0	R/W	
00FF24	D7	ETU2	8-bit programmable timer underflow interrupt enable register	Interrupt is enabled	Interrupt is disabled	0	R/W	
	D6	ETC1	16-bit programmable timer 1 compare match interrupt enable register			0	R/W	
	D5	ETU1	16-bit programmable timer 1 underflow interrupt enable register			0	R/W	
	D4	ETC0	16-bit programmable timer 0 compare match interrupt enable register			0	R/W	
	D3	ETU0	16-bit programmable timer 0 underflow interrupt enable register			0	R/W	
	D2	ESTX	Serial interface transmit completion interrupt enable register			0	R/W	
	D1	ESRX	Serial interface receive completion interrupt enable register			0	R/W	
	D0	ESERR	Serial interface receive error interrupt enable register			0	R/W	

Table 5.12.7.1(b) 16-bit programmable timer control bits

Address	Bit	Name	Function		1	0	Init	R/W	Comment
00FF28	D7	FTU2	8-bit programmable timer underflow interrupt factor flag		(R) Interrupt factor has generated / (W) Reset	(R) Interrupt factor has not generated / (W) Invalid	0	R/(W)	
	D6	FTC1	16-bit programmable timer 1 compare match interrupt factor flag				0	R/(W)	
	D5	FTU1	16-bit programmable timer 1 underflow interrupt factor flag				0	R/(W)	
	D4	FTC0	16-bit programmable timer 0 compare match interrupt factor flag				0	R/(W)	
	D3	FTU0	16-bit programmable timer 0 underflow interrupt factor flag				0	R/(W)	
	D2	FSTX	Serial interface transmit completion interrupt factor flag				0	R/(W)	
	D1	FSRX	Serial interface receive completion interrupt factor flag				0	R/(W)	
	D0	FSERR	Serial interface receive error interrupt factor flag				0	R/(W)	
00FF30	D7	MODE16	16-bit PTM 8-/16-bit mode selection		16-bit	8-bit × 2	0	R/W	
	D6	–	–		–	–	–	–	"0" when being read
	D5	–	–		–	–	–	–	
	D4	–	–		–	–	–	–	
	D3	PTOUT0	16-bit PTM0 clock output control		On	Off	0	R/W	
	D2	PTRUN0	16-bit PTM0 RUN/STOP control		Run	Stop	0	R/W	
	D1	PSET0	16-bit PTM0 preset		Preset	Invalid	0	W	"0" when being read
	D0	CKSEL0	16-bit PTM0 input clock selection		External clock	Internal clock	0	R/W	
00FF31	D7	–	–		–	–	–	–	"0" when being read
	D6	–	–		–	–	–	–	
	D5	–	–		–	–	–	–	
	D4	–	–		–	–	–	–	
	D3	PTOUT1	16-bit PTM1 clock output control		On	Off	0	R/W	
	D2	PTRUN1	16-bit PTM1 RUN/STOP control		Run	Stop	0	R/W	
	D1	PSET1	16-bit PTM1 preset		Preset	Invalid	0	W	"0" when being read
	D0	CKSEL1	16-bit PTM1 input clock selection		External clock	Internal clock	0	R/W	
00FF32	D7	RDR07	16-bit programmable timer 0 reload data register	D7(MSB)			1	R/W	Low-order 8 bits data in 16-bit mode
	D6	RDR06		D6			1	R/W	
	D5	RDR05		D5			1	R/W	
	D4	RDR04		D4			1	R/W	
	D3	RDR03		D3			1	R/W	
	D2	RDR02		D2			1	R/W	
	D1	RDR01		D1			1	R/W	
	D0	RDR00		D0(LSB)			1	R/W	
00FF33	D7	RDR17	16-bit programmable timer 1 reload data register	D7(MSB)			1	R/W	High-order 8 bits data in 16-bit mode
	D6	RDR16		D6			1	R/W	
	D5	RDR15		D5			1	R/W	
	D4	RDR14		D4			1	R/W	
	D3	RDR13		D3			1	R/W	
	D2	RDR12		D2			1	R/W	
	D1	RDR11		D1			1	R/W	
	D0	RDR10		D0(LSB)			1	R/W	
00FF34	D7	CDR07	16-bit programmable timer 0 compare data register	D7(MSB)			0	R/W	Low-order 8 bits data in 16-bit mode
	D6	CDR06		D6			0	R/W	
	D5	CDR05		D5			0	R/W	
	D4	CDR04		D4			0	R/W	
	D3	CDR03		D3			0	R/W	
	D2	CDR02		D2			0	R/W	
	D1	CDR01		D1			0	R/W	
	D0	CDR00		D0(LSB)			0	R/W	
00FF35	D7	CDR17	16-bit programmable timer 1 compare data register	D7(MSB)			0	R/W	High-order 8 bits data in 16-bit mode
	D6	CDR16		D6			0	R/W	
	D5	CDR15		D5			0	R/W	
	D4	CDR14		D4			0	R/W	
	D3	CDR13		D3			0	R/W	
	D2	CDR12		D2			0	R/W	
	D1	CDR11		D1			0	R/W	
	D0	CDR10		D0(LSB)			0	R/W	

Table 5.12.7.1(c) 16-bit programmable timer control bits

Address	Bit	Name	Function		1	0	Init	R/W	Comment
00FF36	D7	PTM07	16-bit programmable timer 0	D7(MSB)			1	R	Low-order 8 bits data
	D6	PTM06	data register	D6			1	R	in 16-bit mode
	D5	PTM05		D5			1	R	
	D4	PTM04		D4			1	R	
	D3	PTM03		D3			1	R	
	D2	PTM02		D2			1	R	
	D1	PTM01		D1			1	R	
	D0	PTM00		D0(LSB)			1	R	
00FF37	D7	PTM17	16-bit programmable timer 1	D7(MSB)			1	R	High-order 8 bits data
	D6	PTM16	data register	D6			1	R	in 16-bit mode
	D5	PTM15		D5			1	R	
	D4	PTM14		D4			1	R	
	D3	PTM13		D3			1	R	
	D2	PTM12		D2			1	R	
	D1	PTM11		D1			1	R	
	D0	PTM10		D0(LSB)			1	R	
00FFD4	D7	–	–		–	–	–	–	"0" when being read
	D6	–	–		–	–	–	–	
	D5	–	–		–	–	–	–	
	D4	–	–		–	–	–	–	
	D3	–	–		–	–	–	–	
	D2	HZR42	R42 high impedance control register		High impedance	Comple-mentary	1	R/W	
	D1	HZR41	R41 high impedance control register				1	R/W	
	D0	HZR40	R40 high impedance control register				1	R/W	
00FFD9	D7	–	–		–	–	–	–	"0" when being read
	D6	–	–		–	–	–	–	
	D5	–	–		–	–	–	–	
	D4	–	–		–	–	–	–	
	D3	–	–		–	–	–	–	
	D2	R42D	R42 output port data register		High	Low	1	R/W	
	D1	R41D	R41 output port data register				1	R/W	
	D0	R40D	R40 output port data register				1	R/W	

MODE16: 8-/16-bit mode selection register (00FF30H•D7)

Selects either the 8-bit or 16-bit mode.

When "1" is written: 16 bits × 1 channel
When "0" is written: 8 bits × 2 channels
Reading: Valid

Select whether Timer 0 and Timer 1 are used as 2 channels independent 8-bit timers or as 1 channel combined 16-bit timer. When "0" is written to the MODE16 register, 8-bit × 2 channels is selected and when "1" is written, 16-bit × 1 channel is selected. At initial reset, the MODE16 register is set to "0" (8-bit × 2 channels).

CKSEL0: Timer 0 input clock selection register (00FF30H•D0)
CKSEL1: Timer 1 input clock selection register (00FF31H•D0)

Selects the input clock for each timer.

When "1" is written: External clock
When "0" is written: Internal clock
Reading: Valid

The clock to be input to each timer is selected from either the external clock (input signal of input port) or the internal clock (prescaler output clock).

When "0" is written to the CKSEL0 register, the internal clock (prescaler output INCL00) is selected as the input clock for Timer 0. When "1" is written, the external clock (K10 input EXCL00) is selected and the timer functions as an event counter.
Same as above, when "0" is written to the CKSEL1 register, the internal clock (prescaler output INCL01) is selected as the input clock for Timer 1. When "1" is written, the external clock (K11 input EXCL01) is selected.
In the 16-bit mode, the setting of the CKSEL1 register is invalid.
At initial reset, the CKSEL register is set to "0" (internal clock).

PRTF0: 16-bit programmable timer 0 source clock selection register (00FF12H•D0)

Selects the source clock for the 16-bit programmable timer 0.

When "1" is written: f_{OSC1}
When "0" is written: f_{OSC3}
Reading: Valid

When "1" is written to the PRTF0 register, the OSC1 clock is selected as the source clock for the 16-bit programmable timer 0.
When "0" is written, the OSC3 clock is selected.
At initial reset, the PRTF0 register is set to "0" (f_{OSC3}).

PRTF1: 16-bit programmable timer 1 source clock selection register (00FF12H•D1)

Selects the source clock for the 16-bit programmable timer 1.

When "1" is written: f_{OSC1}
When "0" is written: f_{OSC3}
Reading: Valid

When "1" is written to the PRTF1 register, the OSC1 clock is selected as the source clock for the 16-bit programmable timer 1.
When "0" is written, the OSC3 clock is selected.
At initial reset, the PRTF1 register is set to "0" (f_{OSC3}).

PST00–PST02: 16-bit programmable timer 0 division ratio selection register (00FF10H•D0–D2)

Selects the clock for the 16-bit programmable timer 0.
It can be selected from 8 types of division ratio shown in Table 5.12.7.1(a).
This register can also be read.
At initial reset, the PST0 register is set to "0".

PST10–PST12: 16-bit programmable timer 1 division ratio selection register (00FF10H•D4–D6)

Selects the clock for the 16-bit programmable timer 1.
It can be selected from 8 types of division ratio shown in Table 5.12.7.1(a).
This register can also be read.
At initial reset, the PST1 register is set to "0".

PRPRT0: 16-bit programmable timer 0 clock control register (00FF10H•D3)

Controls the clock supply of the 16-bit programmable timer 0.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

By writing "1" to the PRPRT0 register, the clock that is selected with the PST0 register is output to the 16-bit programmable timer 0.
When "0" is written, the clock is not output.
At initial reset, the PRPRT0 register is set to "0" (OFF).

PRPRT1: 16-bit programmable timer 1 clock control register (00FF10H•D7)

Controls the clock supply of the 16-bit programmable timer 1.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

By writing "1" to the PRPRT1 register, the clock that is selected with the PST1 register is output to the 16-bit programmable timer 1.
When "0" is written, the clock is not output.
At initial reset, the PRPRT1 register is set to "0" (OFF).

PK10ON: EXCL00 clock control register (00FF15H•D0)

Controls the event counter clock of the 16-bit programmable timer 0.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

By writing "1" to the PK10ON register, the EXCL00 (K10 input) clock is output to the 16-bit programmable timer 0.
When "0" is written, the clock is not output.
At initial reset, the PK10ON register is set to "0" (OFF).

PK11ON: EXCL01 clock control register (00FF15H•D1)

Controls the event counter clock of the 16-bit programmable timer 1.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

By writing "1" to the PK11ON register, the EXCL01 (K11 input) clock is output to the 16-bit programmable timer 1.
When "0" is written, the clock is not output.
At initial reset, the PK11ON register is set to "0" (OFF).

RDR00–RDR07: Timer 0 reload data register (00FF32H)
RDR10–RDR17: Timer 1 reload data register (00FF33H)

Sets the initial value for the counter of each timer. Each counter loads the reload data set in this register and counts using it as the initial value. The reload data set in this register is loaded into the counter when "1" is written to PSET0 or PSET1, or when a counter underflow occurs.
This register can be read.
At initial reset, the RDR register is set to "FFH".

CDR00–CDR07: Timer 0 compare data register (00FF34H)
CDR10–CDR17: Timer 1 compare data register (00FF35H)

Sets the compare data for each timer.
The timer compares the data set in this register with the corresponding counter data, and outputs the compare match signals when they are the same. The compare match signal controls the interrupt and the TOUT output waveform.
This register can be read.
At initial reset, the CDR register is set to "00H".

PTM00–PTM07: Timer 0 counter data (00FF36H)
PTM10–PTM17: Timer 1 counter data (00FF37H)

The counter data of each timer can be read.
Data can be read at any given time. However, in the 16-bit mode, reading PTM0 does not latch the timer 1 counter data in PTM1. To avoid generating a borrow from timer 0 to timer 1, read the counter data after stopping the timer by writing "0" to PTRUN0.
PTM0 and PTM1 can only be read, so writing operation is invalid.
At initial reset, PTM is set to "FFH".

PSET0: Timer 0 preset (00FF30H•D1)
PSET1: Timer 1 preset (00FF31H•D1)

Presets the reload data to the counter.

When "1" is written: Preset
When "0" is written: Invalid
Reading: Always "0"

Writing "1" to PSET0 presets the reload data in the RDR0 register to the counter of Timer 0. When the counter of Timer 0 is in RUN status, the counter restarts immediately after presetting.
In the case of STOP status, the counter maintains the preset data.
No operation results when "0" is written.
Same as above, PSET1 presets the reload data in the RDR1 register to the counter of Timer 1.
In the 16-bit mode, writing "1" to PSET1 is invalid because 16-bit data is preset by PSET0 only.
This bit is only for writing, and it is always "0" during reading.

PTRUN0: Timer 0 RUN/STOP control register (00FF30H•D2)
PTRUN1: Timer 1 RUN/STOP control register (00FF31H•D2)

Controls the RUN / STOP of the counter.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The counter of Timer 0 starts down-counting by writing "1" to the PTRUN0 register and stops by writing "0".
In STOP status, the counter data is maintained until it is preset or the counter restarts. When STOP status changes to RUN status, the counter resumes counting from the data maintained.
Same as above, the PTRUN1 register controls the counter of Timer 1.
In the 16-bit mode, both channels are controlled with the PTRUN0 register, and the PTRUN1 register is fixed at "0".
At initial reset, the PTRUN register is set to "0" (STOP).

PTOUT0: Timer 0 clock output control register (00FF30H•D3)
PTOUT1: Timer 1 clock output control register (00FF31H•D3)

Controls the output of the TOUT signal.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

The PTOUT0 is the output control register for the TOUT0 signal (Timer 0 output clock). When "1" is written to this register, the TOUT0 signal is output from the R40 terminal. When "0" is written, the terminal goes high (V_{DD}) level. However, the high-impedance control register HZR40 of the output port R40 must be set to "0" and the data register R40D must be set to "1".
The TOUT0 clock cannot be output simultaneously with the FOUT3 clock.
The PTOUT1 is the output control register for the TOUT1 signal (Timer 1 output clock). When "1" is written to this register, the TOUT1 signal is output from the R41 terminal. When "0" is written, the terminal goes high (V_{DD}) level. However, the high-impedance control register HZR41 of the output port R41 must be set to "0" and the data register R41D must be set to "1".
The TOUT1 clock cannot be output simultaneously with the FOUT1 clock.
At initial reset, the PTOUT register is set to "0" (OFF).

HZR40, HZR41: R4 port high impedance control register (00FFD4H•D0, D1)

Sets the output terminals into a high impedance state.

When "1" is written: High impedance
When "0" is written: Complementary
Reading: Valid

The HZR40 and HZR41 registers are the high impedance control registers for the output ports R40 and R41 used for the clock output.
Fix data of the port used for the TOUT output at "0".
At initial reset, the HZR register is set to "1" (high impedance).

R40D, R41D: R4 port output data register (00FFD9H•D0, D1)

They are the data registers for the output ports R40, R41 used for the clock output.

When "1" is written: Clock output is possible
When "0" is written: LOW (V_{SS}) level is output
Reading: Valid

Fix data of the port used for the TOUT output at "1".
At initial reset, the data bits are all set to "1".

PTM00, PTM01: Timer 0 interrupt priority register (00FF20H•D0, D1)
PTM10, PTM11: Timer 1 interrupt priority register (00FF20H•D2, D3)

Sets the priority level of the 16-bit programmable timer interrupt.
The PTM register is the interrupt priority register corresponding to each timer interrupt.
Table 5.12.7.2 shows the interrupt priority level which can be set by this register.

Table 5.12.7.2 Interrupt priority level settings

PTM11 PTM01	PTM10 PTM00	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, the PTM register is set to "0" (level 0).

ETU0: Timer 0 underflow interrupt enable register (00FF24H•D3)
ETU1: Timer 1 underflow interrupt enable register (00FF24H•D5)

Enables or disables the underflow interrupt generation to the CPU.

When "1" is written: Interrupt is enabled
When "0" is written: Interrupt is disabled
Reading: Valid

The ETU register is the interrupt enable register corresponding to the underflow interrupt factor of each timer.
Interrupt in which the ETU register is set to "1" is enabled, and the others in which the ETU register is set to "0" are disabled.
In the 16-bit mode, the setting of the ETU0 is invalid.
At initial reset, the ETU register is set to "0" (interrupt is disabled).

ETC0: Timer 0 compare match interrupt enable register (00FF24H•D4)
ETC1: Timer 1 compare match interrupt enable register (00FF24H•D6)

Enables or disables the compare match interrupt generation to the CPU.

When "1" is written: Interrupt is enabled
When "0" is written: Interrupt is disabled
Reading: Valid

The ETC register is the interrupt enable register corresponding to the compare match interrupt factor of each timer.
Interrupt in which the ETC register is set to "1" is enabled, and the others in which the ETC register is set to "0" are disabled.
In the 16-bit mode, the setting of the ETC0 is invalid.
At initial reset, the ETC register is set to "0" (interrupt is disabled).

FTU0: Timer 0 underflow interrupt factor flag (00FF28H•D3)
FTU1: Timer 1 underflow interrupt factor flag (00FF28H•D5)

Indicates the generation of underflow interrupt factor.

When "1" is read: Int. factor has generated
When "0" is read: Int. factor has not generated

When "1" is written: Factor flag is reset
When "0" is written: Invalid

FTU is the interrupt factor flag corresponding to interrupt of each timer, and is set to "1" due to the counter underflow.
At this point, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of the interrupt flags (I0 and I1), an interrupt is generated to the CPU.
Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag is set to "1" when the interrupt generation condition is met.
To accept the subsequent interrupt after an interrupt generation, it is necessary to re-set the interrupt flags (set the interrupt flag to a lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and to reset the interrupt factor flag. The interrupt factor flag is reset to "0" by writing "1".
In the 16-bit mode, the interrupt factor flag FTU0 is not set to "1" and Timer 0 interrupt is not generated. In this mode, the interrupt factor flag FTU1 is set to "1" by the underflow of the 16-bit counter.
At initial reset, the FTU flag is reset to "0".

FTC0: Timer 0 compare match interrupt factor flag (00FF28H•D4)
FTC1: Timer 1 compare match interrupt factor flag (00FF28H•D6)

Indicates the generation of compare match interrupt factor.

When "1" is read: Int. factor has generated
When "0" is read: Int. factor has not generated

When "1" is written: Factor flag is reset
When "0" is written: Invalid

FTC is the interrupt factor flag corresponding to interrupt of each timer, and is set to "1" due to the compare match signal.
At this point, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of the interrupt flags (I0 and I1), an interrupt is generated to the CPU.
Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag is set to "1" when the interrupt generation condition is met.
To accept the subsequent interrupt after an interrupt generation, it is necessary to re-set the interrupt flags (set the interrupt flag to a lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and to reset the interrupt factor flag. The interrupt factor flag is reset to "0" by writing "1".
In the 16-bit mode, the interrupt factor flag FTC0 is not set to "1" and Timer 0 interrupt is not generated. In this mode, the interrupt factor flag FTC1 is set to "1" by the compare match of the 16-bit counter.
At initial reset, the FTC flag is reset to "0".

5.12.8 Programming notes

(1) The 16-bit programmable timer actually enters into RUN or STOP status at the falling edge of the input clock after writing to the PTRUN0(1) register. Consequently, when "0" is written to PTRUN0(1), the timer stops after counting once more (+1). PTRUN0(1) is read as "1" until the timer actually stops.
Figure 5.12.8.1 shows the timing chart at the RUN / STOP control.

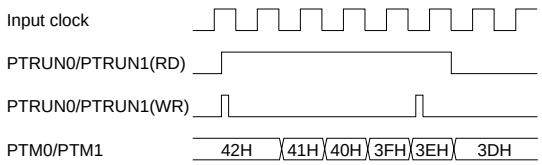


Fig. 5.12.8.1 Timing chart at RUN/STOP control

(2) When the SLP instruction is executed while the 16-bit programmable timer is running (PTRUN0(1) = "1"), the timer stops counting during SLEEP status. When SLEEP status is canceled, the timer starts counting. However, the operation becomes unstable immediately after SLEEP status is canceled. Therefore, when shifting to SLEEP status, stop the 16-bit programmable timer (PTRUN0(1) = "0") prior to executing the SLP instruction.
Same as above, the TOUT signal output should be disabled (PTOUT0(1) = "0") so that an unstable clock is not output to the clock output port terminal.

(3) In the 16-bit mode, reading PTM0 does not latch the timer 1 counter data in PTM1. To avoid generating a borrow from timer 0 to timer 1, read the counter data after stopping the timer by writing "0" to PTRUN0.

5.13 8-bit Programmable Timer

5.13.1 Configuration of 8-bit programmable timer

The S1C88408 has a built-in 8-bit programmable timer. The timer consists of an 8-bit presettable down counter, and can be used as 8 bits × 1 channel of programmable timer.
Figure 5.13.1.1 shows the configuration of the 8-bit programmable timer.

The serial interface uses the underflow signal of the 8-bit programmable timer as the synchronous clock, so programmable setting of the transfer rate is possible.

5.13.2 Setting of input clock

The prescaler supplies the clocks to the timer. The prescaler generates the clocks for the timer by dividing the source clock supplied from the OSC3 oscillation circuit.

Note: The prescaler, which supplies the clock to the 8-bit programmable timer, can operate only when the OSC3 oscillation has been set to ON. Be aware that the 8-bit programmable timer does not operate when the OSC3 oscillation circuit has been turned off.

Division ratio of the prescaler can be individually selected by software.
The division ratio can be selected from eight kinds using the prescaler division ratio selection register PST2.
Further, it is necessary to control the prescaler output using the clock control register PRPRT2.
Refer to Section 5.5, "Prescaler and Clock Control Circuit for Peripheral Circuits", or Section 5.13.6, "I/O memory of 8-bit programmable timer", for setting of the division ratio.

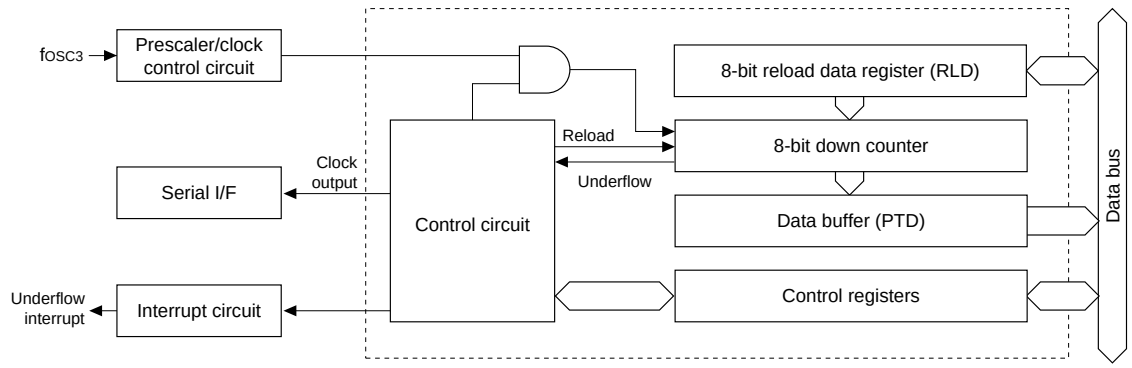


Fig. 5.13.1.1 Configuration of 8-bit programmable timer

5.13.3 Operation and control of timer

Reload data register and setting of initial value

The reload data register RLD is used to set the initial value of the down counter.
The reload data register can be read and written, and is set to FFH at initial reset.

Data written in this register is loaded into the down counter, and down counting starts from the value. A preset to down counter is done in the following two cases:

1) ***When software presets***
   The software preset can be done using the preset control bit PSET. When the preset control bit is set to "1", the content of the reload data register is loaded into the down counter at that point.

2) ***When down counter has underflowed during a count***
   Since the down counter presets the reload data by the underflow, the underflow period is decided according to the value set in the reload data register. This underflow generates an interrupt, and controls the clock output to the serial interface.

Timer operation

The 8-bit programmable timer is equipped with the register PRUN which control the RUN / STOP of the timer. The programmable timer starts down counting by writing "1" to the PRUN register. However, it is necessary to control the input clock and to preset the reload data before starting a count.
When "0" is written to the PRUN register, clock input is prohibited, and the count stops.
This RUN / STOP control does not affect data in the counter. The data in the counter is maintained during count deactivation, so it is possible to resume counting from the data.

The counter data can be read via the buffer PTD in optional timing.

When the counter underflows, an underflow interrupt is generated, and the initial value set in the reload data register is loaded to the counter. This underflow signal controls supplying the clock to the serial interface.

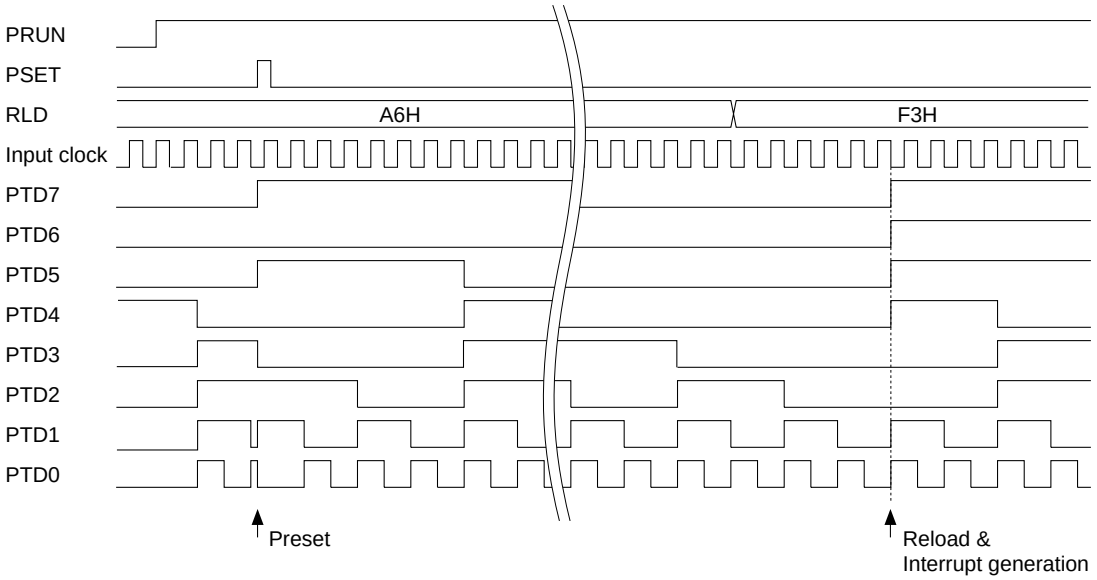


Fig. 5.13.3.1 Operation timing of counter

5.13.4 Interrupt function

The 8-bit programmable timer can generate an interrupt by the underflow signal of the counter. Figure 5.13.4.1 shows the configuration of the 8-bit programmable timer interrupt circuit.

The underflow signal of the timer sets the interrupt factor flag FTU2 to "1". At that point, the interrupt is generated. The interrupt can also be prohibited by setting the interrupt enable register ETU2.

Furthermore, the priority level of the interrupt for the CPU can be set to an optional level (0–3) using the interrupt priority register PTM2.
Refer to Section 5.18, "Interrupt and Standby Mode", for details of the interrupt control registers and operations subsequent to interrupt generation.

The exception processing vector address for the 8-bit programmable timer interrupt is set as follows:

8-bit programmable timer interrupt: 000018H

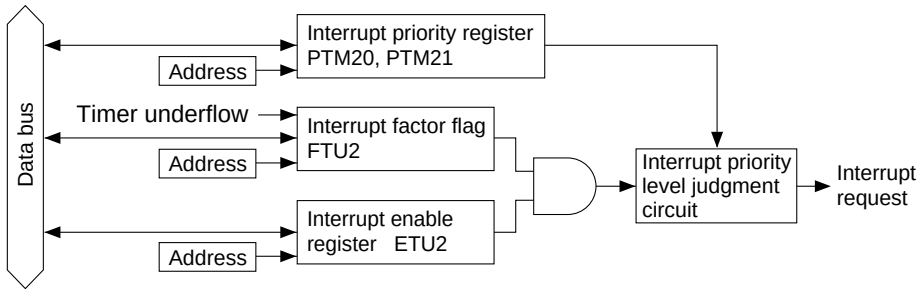


Fig. 5.13.4.1 Configuration of 8-bit programmable timer interrupt circuit

5.13.5 Transfer rate setting for serial interface

The 8-bit programmable timer can supply the clock, generated by dividing the underflow of the counter in 1/2, to the serial interface. The clock output control register PTOUT controls the clock output from the 8-bit programmable timer.
Figure 5.13.5.1 shows the output waveform of the clock.

The transfer rate of the serial interface is decided by the clock output from the prescaler and the value set in the reload register.
The output clock is divided by 16 in the serial interface. Therefore, the setting value of the reload data register according to the transfer rate can be calculated with the expression below.

$RLD = f_{OSC3} * dr / (32 * bps) - 1$

RLD: Setting value of the reload register
f_{OSC3}: OSC3 oscillation frequency
bps: Transfer rate
dr: Prescaler division ratio (1/2 to 1/256)

(00H can be set to RLD)

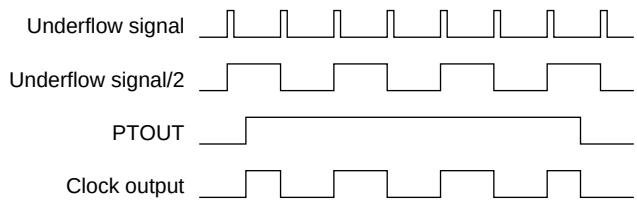


Fig. 5.13.5.1 Clock output waveform

5.13.6 I/O memory of 8-bit programmable timer

Table 5.13.6.1 shows the 8-bit programmable timer control bits.

Table 5.13.6.1(a) 8-bit programmable timer control bits

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF11	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	PRPRT2	8-bit programmable timer clock control	On	Off	0	R/W	
	D2	PST22	8-bit programmable timer division ratio PST22 PST21 PST20 Division ratio 1 1 1 fOSC3 / 256			0	R/W	
	D1	PST21	1 1 0 fOSC3 / 128 1 0 1 fOSC3 / 64 1 0 0 fOSC3 / 32 0 1 1 fOSC3 / 16			0	R/W	
	D0	PST20	0 1 0 fOSC3 / 8 0 0 1 fOSC3 / 4 0 0 0 fOSC3 / 2			0	R/W	
00FF21	D7	PTM21	8-bit programmable timer	PTM21 PTM20		0	R/W	
	D6	PTM20	interrupt priority register	PSI1 PSI0		0	R/W	
	D5	PSI1	Serial interface	PCTM1 PCTM0	Priority	0	R/W	
	D4	PSI0	interrupt priority register	PLCD1 PLCD0	level	0	R/W	
	D3	PCTM1	Clock timer	1 1	Level 3	0	R/W	
	D2	PCTM0	interrupt priority register	1 0	Level 2	0	R/W	
	D1	PLCD1	LCD controller	0 1	Level 1	0	R/W	
	D0	PLCD0	interrupt priority register	0 0	Level 0	0	R/W	
00FF24	D7	ETU2	8-bit programmable timer underflow interrupt enable register	Interrupt is enabled	Interrupt is disabled	0	R/W	
	D6	ETC1	16-bit programmable timer 1 compare match interrupt enable register			0	R/W	
	D5	ETU1	16-bit programmable timer 1 underflow interrupt enable register			0	R/W	
	D4	ETC0	16-bit programmable timer 0 compare match interrupt enable register			0	R/W	
	D3	ETU0	16-bit programmable timer 0 underflow interrupt enable register			0	R/W	
	D2	ESTX	Serial interface transmit completion interrupt enable register			0	R/W	
	D1	ESRX	Serial interface receive completion interrupt enable register			0	R/W	
	D0	ESERR	Serial interface receive error interrupt enable register			0	R/W	
00FF28	D7	FTU2	8-bit programmable timer underflow interrupt factor flag	(R) Interrupt factor has generated (W) Reset	(R) Interrupt factor has not generated (W) Invalid	0	R/(W)	
	D6	FTC1	16-bit programmable timer 1 compare match interrupt factor flag			0	R/(W)	
	D5	FTU1	16-bit programmable timer 1 underflow interrupt factor flag			0	R/(W)	
	D4	FTC0	16-bit programmable timer 0 compare match interrupt factor flag			0	R/(W)	
	D3	FTU0	16-bit programmable timer 0 underflow interrupt factor flag			0	R/(W)	
	D2	FSTX	Serial interface transmit completion interrupt factor flag			0	R/(W)	
	D1	FSRX	Serial interface receive completion interrupt factor flag			0	R/(W)	
	D0	FSERR	Serial interface receive error interrupt factor flag			0	R/(W)	

Table 5.13.6.1(b) 8-bit programmable timer control bits

Address	Bit	Name	Function		1	0	Init	R/W	Comment
00FF38	D7	–	–		–	–	–	–	"0" when being read
	D6	–	–		–	–	–	–	
	D5	–	–		–	–	–	–	
	D4	–	–		–	–	–	–	
	D3	–	–		–	–	–	–	
	D2	PTOUT	8-bit programmable timer clock output control		On	Off	0	R/W	
	D1	PSET	8-bit programmable timer preset		Preset	Invalid	–	W	"0" when being read
	D0	PRUN	8-bit programmable timer RUN/STOP control		Run	Stop	0	R/W	
00FF39	D7	RLD7	8-bit programmable timer	D7(MSB)			1	R/W	
	D6	RLD6	reload data register	D6			1	R/W	
	D5	RLD5		D5			1	R/W	
	D4	RLD4		D4			1	R/W	
	D3	RLD3		D3			1	R/W	
	D2	RLD2		D2			1	R/W	
	D1	RLD1		D1			1	R/W	
	D0	RLD0		D0(LSB)			1	R/W	
00FF3A	D7	PTD7	8-bit programmable timer	D7(MSB)			1	R	
	D6	PTD6	data register	D6			1	R	
	D5	PTD5		D5			1	R	
	D4	PTD4		D4			1	R	
	D3	PTD3		D3			1	R	
	D2	PTD2		D2			1	R	
	D1	PTD1		D1			1	R	
	D0	PTD0		D0(LSB)			1	R	

PST20–PST22: 8-bit programmable timer division ratio selection register (00FF11H•D0–D2)

Selects the clock for the 8-bit programmable timer. It can be selected from 8 types of division ratio shown in Table 5.13.6.1(a).
This register can also be read.
At initial reset, the PST2 register is set to "0" (f_{OSC3}/2).

PRPRT2: 8-bit programmable timer clock control register (00FF11H•D3)

Controls the clock supply of the 8-bit programmable timer.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

By writing "1" to the PRPRT2 register, the clock that is selected with the PST2 register is output to the 8-bit programmable timer. However, the OSC3 oscillation circuit must be used.
When "0" is written, the clock is not output.
At initial reset, the PRPRT2 register is set to "0" (OFF).

RLD0–RLD7: Reload data register (00FF39H)

Sets the initial value for the counter.
The counter loads the reload data set in this register and counts using it as the initial value.
The reload data set in this register is loaded into the counter when "1" is written to PSET, or when a counter underflow occurs.
This register can be read.
At initial reset, the RLD register is set to "FFH".

PTD0–PTD7: Counter data (00FF3AH)

The counter data of the 8-bit programmable timer can be read.
PTD is a buffer to maintain the count data during reading, and the data can be read in optional timing.
At initial reset, PTD is set to "FFH".

PSET: Preset (00FF38H•D1)

Presets the reload data to the counter.

When "1" is written: Preset
When "0" is written: Invalid
Reading: Always "0"

Writing "1" to PSET presets the reload data in the RLD register to the counter. When the counter is in RUN status, the counter restarts immediately after presetting.

In the case of STOP status, the counter maintains the preset data.
No operation results when "0" is written.
This bit is valid only for writing, and it is always "0" during reading.

PRUN: RUN/STOP control register (00FF38H•D0)

Controls the RUN / STOP of the counter.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The counter starts down-counting by writing "1" to the PRUN register and stops by writing "0".
In STOP status, the counter data is maintained until it is preset or the counter restarts. When STOP status changes to RUN status, the counter resumes counting from the data maintained.
At initial reset, the PRUN register is set to "0" (STOP).

PTOUT: Clock output control register (00FF38H•D2)

Controls the clock output to the serial interface.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

The PTOUT register is the output control register. When "1" is written to this register, the clock (underflow ∗ 1/2) that is generated by the 8-bit programmable timer is output to the serial interface.
When "0" is written, the clock is not output to the serial interface.
At initial reset, the PTOUT register is set to "0" (OFF).

PTM20, PTM21: Interrupt priority register (00FF21H•D6, D7)

Sets the priority level of the 8-bit programmable timer interrupt.
Table 5.13.6.2 shows the interrupt priority level which can be set by this register.

Table 5.13.6.2 Interrupt priority level settings

PTM21	PTM20	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, the PTM2 register is set to "0" (level 0).

ETU2: Underflow interrupt enable register (00FF24H•D7)

Enables or disables the underflow interrupt generation to the CPU.

When "1" is written: Interrupt is enabled
When "0" is written: Interrupt is disabled
Reading: Valid

The ETU2 register is the interrupt enable register corresponding to the interrupt factor of the 8-bit programmable timer.
Interrupt in which the ETU2 register is set to "1" is enabled, and the others in which the ETU2 register is set to "0" are disabled.
At initial reset, the ETU2 register is set to "0" (interrupt is disabled).

FTU2: Underflow interrupt factor flag (00FF28H•D7)

Indicates the generation of underflow interrupt factor.

When "1" is read: Int. factor has generated
When "0" is read: Int. factor has not generated

When "1" is written: Factor flag is reset
When "0" is written: Invalid

FTU2 is the interrupt factor flag corresponding to the 8-bit programmable timer interrupt, and is set to "1" due to the counter underflow.
At this point, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of the interrupt flags (I0 and I1), an interrupt is generated to the CPU.
Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag is set to "1" when the interrupt generation condition is met.
To accept the subsequent interrupt after an interrupt generation, it is necessary to re-set the interrupt flags (set the interrupt flag to a lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and to reset the interrupt factor flag. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, the FTU2 flag is reset to "0".

5.13.7 Programming notes

(1) The 8-bit programmable timer actually enters into RUN or STOP status at the falling edge of the input clock after writing to the PRUN register. Consequently, when "0" is written to PRUN, the timer stops after counting once more (+1). PRUN is read as "1" until the timer actually stops.
Figure 5.13.7.1 shows the timing chart of the RUN / STOP control.

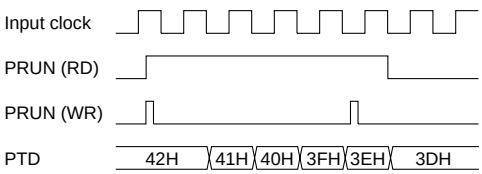


Fig. 5.13.7.1 Timing chart at RUN/STOP control

(2) When the SLP instruction is executed while the 8-bit programmable timer is running (PRUN = "1"), the timer stops counting during SLEEP status. When SLEEP status is canceled, the timer starts counting. However, the operation becomes unstable immediately after SLEEP status is canceled. Therefore, when shifting to SLEEP status, stop the 8-bit programmable timer (PRUN = "0") prior to executing the SLP instruction.

(3) The prescaler, which supplies the clock to the 8-bit programmable timer, can operate only when the OSC3 oscillation has been set to ON. Be aware that the 8-bit programmable timer does not operate when the OSC3 oscillation circuit has been turned off.

5.14 Serial Interface

5.14.1 Configuration of serial interface

The S1C88408 has a serial interface built-in. The following shows the features.

- 8-bit clock synchronous system / 8(7)-bit asynchronous system (full duplex) are switchable
- Two systems of input / output terminals (P10–P13, P14–P17) are selectable
- Data bit length, stop bit length and parity bit are selectable with software for the asynchronous system
- IrDA interface compatible

Figure 5.14.1.1 shows the configuration of the serial interface.

The input / output port of the serial interface is shared with an I / O port, and it is set in the I / O port at initial reset. Therefore, when using the serial interface, enable the serial interface by writing "1" to the serial interface enable register (ESIF).

The serial interface in which the ESIF register is "0" cannot be used.

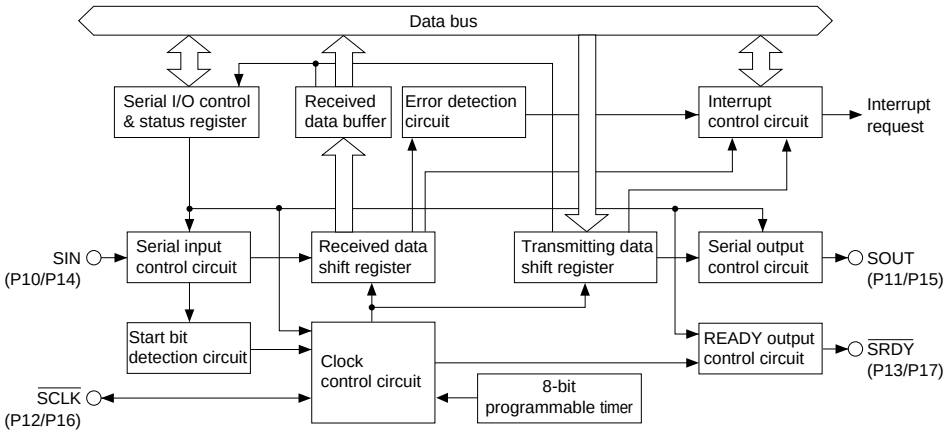


Fig. 5.14.1.1 Configuration of serial interface

5.14.2 Transfer mode and input/output terminals

In this serial interface, the transfer mode can be selected by software.

Transfer mode summary

Clock synchronous transfer is the formula that transfers 8-bit data by synchronizing each bit to a clock common to transmitter and receiver.

Asynchronous transfer is the formula that transfers the serial converted data in which a start bit is added to the front and a stop bit is added to the rear. In this formula, it is not necessary to use the same synchronous clock for transmitter and receiver. Data transfer is done by synchronizing the start / stop bit attached in front and rear of each data. The asynchronous interface has separate transmit and receive shift registers and is designed to permit full duplex transmission to be done simultaneously for transmitting and receiving.

Four transfer modes shown below are available in this interface.

(1) Clock synchronous master mode

In this mode, clock synchronous 8-bit serial data transfer can be done. This serial interface becomes the master and uses the internal clock as the synchronous clock for the built-in shift register.
The synchronous clock is output from the $\overline{\text{SCLK}}$ terminal and can control the external serial I / O device (the slave side).
Figure 5.14.2.1 shows a connection example of input / output terminals in clock synchronous master mode.

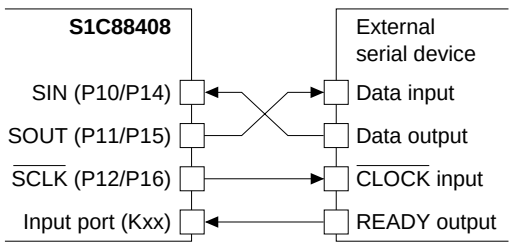


Fig. 5.14.2.1 Connection example of clock synchronous master mode

(2) Clock synchronous slave mode

In this mode, clock synchronous 8-bit serial data transfer can be done. This serial interface becomes the slave and uses the synchronous clock supplied externally (the master side).
The synchronous clock is input from the $\overline{\text{SCLK}}$ terminal and is used in this serial interface.
Further, this mode can output the $\overline{\text{SRDY}}$ signal that indicates transmit / receive ready status from the $\overline{\text{SRDY}}$ terminal.
Figure 5.14.2.2 shows a connection example of input / output terminals in clock synchronous slave mode.

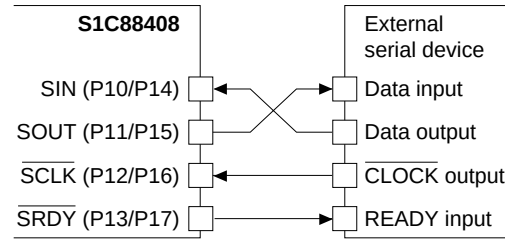


Fig. 5.14.2.2 Connection example of clock synchronous slave mode

(3) 7-bit asynchronous mode

In this mode, start stop synchronous transfer can be done. Data length is 7 bits. It is possible to select a stop bit length, addition of a parity bit and even / odd parity.
Further, this mode works only with the internal clock.
Figure 5.14.2.3 shows a connection example of input / output terminals in asynchronous mode.

(4) 8-bit asynchronous mode

In this mode, start stop synchronous transfer can be done. Data length is 8 bits. It is possible to select a stop bit length, addition of a parity bit and even / odd parity.
Further, this mode works only with the internal clock.
Figure 5.14.2.3 shows a connection example of input / output terminals in asynchronous mode.

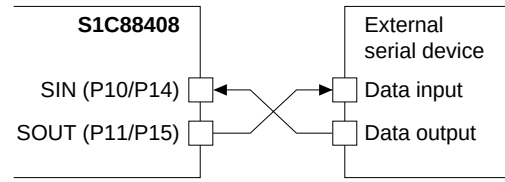


Fig. 5.14.2.3 Connection example of clock asynchronous mode

Setting of serial interface

(1) Transfer mode

The transfer mode is set with the SMD register (2 bits) as shown in Table 5.14.2.1.

Table 5.14.2.1 Transfer mode

SMD1	SMD0	Mode
1	1	8-bit asynchronous
1	0	7-bit asynchronous
0	1	Clock synchronous slave
0	0	Clock synchronous master

It is set to the clock synchronous master mode at initial reset.
In the clock synchronous mode, start / stop bit and parity bit cannot be added.
The clock synchronous slave mode outputs the $\overline{SRDY}$ signal showing transmit / receive ready status from the $\overline{SRDY}$ terminal.

When using the IR interface, set the 7-bit asynchronous mode or 8-bit asynchronous mode.

The input / output terminals of the serial interface can be assigned to P10–P13 or P14–P17. Select either one using the SIOSEL register.

Table 5.14.2.2 Input/output terminals

Terminal	SIOSEL="0"	SIOSEL="1"
SIN	P10	P14
SOUT	P11	P15
$\overline{SCLK}$	P12	P16
$\overline{SRDY}$	P13	P17

(ESIF="1")

It is set to P10–P13 at initial reset.
When using the IR interface, select P14–P17.
The ports which are not used in the serial interface can be used as the I / O port.

Input / output configuration of the four lines differs depending on the transfer mode. Table 5.14.2.3 shows the terminal configuration of each mode.

The clock synchronous slave mode uses all four lines.

The clock synchronous master mode does not use $\overline{SRDY}$, so P13 (P17) can be used as the I / O port.

The asynchronous mode does not use $\overline{SCLK}$ and $\overline{SRDY}$, so P12 and P13 (P16 and P17) can be used as the I / O port.

The I / O control registers and data registers of the I / O port which is used with the serial interface can be used as a general-purpose register.

(2) Data format of clock synchronous transfer

In the clock synchronous mode, data format is stationary as follows:

Data length: 8 bits
Start bit: none
Stop bit: none
Parity bit: none

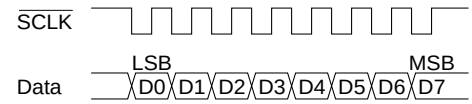


Fig. 5.14.2.4 Clock synchronous transfer data format

(3) Data format of asynchronous transfer

The data format of asynchronous transfer is as follows:

Data length: 7 bits or 8 bits
(decided by transfer mode selection)
Start bit: 1 bit stationary
Stop bit: 1 bit or 2 bits
Parity bit: even parity, odd parity or none

The stop bit can be set with the STPB register, and the parity bit can be set with the EPR register and the PMD register shown in Table 5.14.2.4.

Table 5.14.2.4 Setting of stop bit and parity bit

STPB	EPR	PMD	Setting	
			Stop bit	Parity bit
1	1	1	2 bits	Odd
		0	2 bits	Even
	0	–	2 bits	None
0	1	1	1 bit	Odd
		0	1 bit	Even
	0	–	1 bit	None

At initial reset, they are set in 1 stop bit and no parity.

Table 5.14.2.3 Terminal setting for each transfer mode

Mode	SIN	SOUT	$\overline{SCLK}$	$\overline{SRDY}$
8-bit asynchronous	Data input	Data output	P12/P16	P13/P17
7-bit asynchronous	Data input	Data output	P12/P16	P13/P17
Clock synchronous slave	Data input	Data output	Clock input	Ready output
Clock synchronous master	Data input	Data output	Clock output	P13/P17

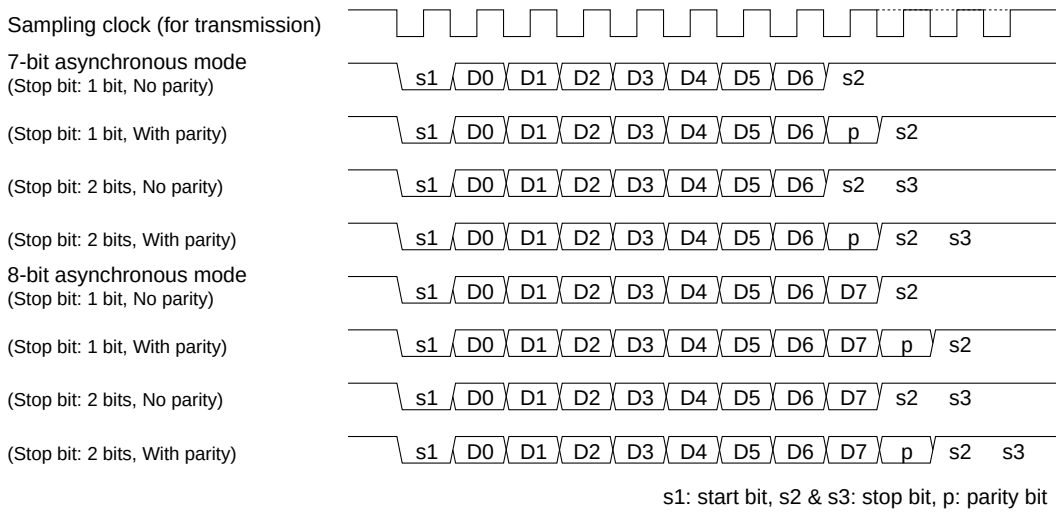


Fig. 5.14.2.5 Asynchronous transfer data format

5.14.3 Mask option

The input/output terminals of the serial interface are shared with the I/O port terminals. Therefore, the terminal specification of the serial interface is decided by setting the I/O port mask option.

I/O port pull-up resistor		
P10 (SIN)	☐ With resistor	☐ Gate direct
P12 ($\overline{\text{SCLK}}$)	☐ With resistor	☐ Gate direct
P14 (SIN)	☐ With resistor	☐ Gate direct
P16 ($\overline{\text{SCLK}}$)	☐ With resistor	☐ Gate direct

Note: The configuration of the ports which are used for the serial interface input differs depending on the transfer mode setting.

The I/O port has a built-in pull-up resistor that is activated during the input mode, and it can be individually selected for use or not by the mask option. This mask option (pull-up resistor) is effective for the input lines of the serial interface.

When "Gate direct" is selected, take care that a floating status does not occur in the input terminal.

5.14.4 Clock source

The clock source of the serial interface is the 8-bit programmable timer.

When using the internal clock, it is necessary to output the clock from the 8-bit programmable timer beforehand.
Refer to Section 5.13, "8-bit Programmable Timer", for control of the 8-bit programmable timer.
Be aware that the serial interface does not operate when the OSC3 oscillation circuit has been turned off, because in this case the 8-bit programmable timer does not operate.

Synchronous clock in clock synchronous mode

The clock synchronous master mode divides the output clock of the 8-bit programmable timer in 1/16, and uses it as the synchronous clock $\overline{\text{SCLK}}$.

The clock synchronous slave mode uses an external clock input from the $\overline{\text{SCLK}}$ terminal. In this mode, it is not necessary to control the 8-bit programmable timer.

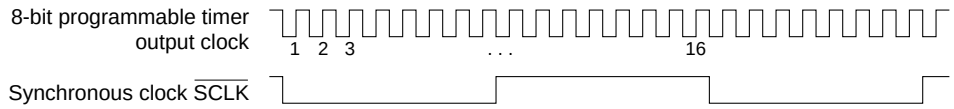


Fig. 5.14.4.1 Synchronous clock $\overline{SCLK}$

Sampling clock of asynchronous mode

The asynchronous system in this interface generates a sampling clock on the basis of the output clock of the 8-bit programmable timer.
However, it is necessary that the 8-bits programmable timer has output a clock of 16 times the baud rate.

(1) At receiving

As shown in Figure 5.14.4.2, duty of the internal sampling clock is not 50 %. The sampling clock changes from "1" to "0" with the second input clock after recognizing a start bit, and returns to "1" with the eighth clock so that sampling will be done at the middle of each bit data received. This sampling waveform is continuously output until sampling of the stop bit has completed. Each bit data is sampled at the rising edge of the sampling clock. When the stop bit is sampled, the sampling signal is fixed at "1" until the next start bit is detected.
If the serial input is not "0" at the time of start bit sampling with the eighth input clock because the baud rate set in this interface is different from the transmitter or noise is input to the SIN terminal, the following data sampling is stopped and the interface shifts into standby status for the next start bit detection.

(2) At transmission

In transmission, the serial interface generates a clock for transmission by dividing the output clock of the 8-bit programmable timer in 1/16 and outputs each bit in synchronization with the clock.

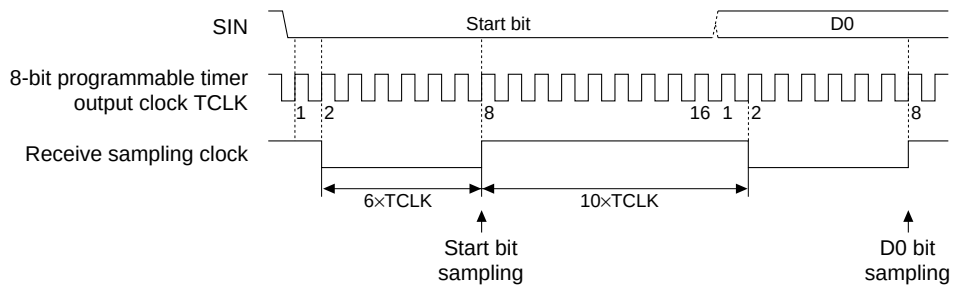


Fig. 5.14.4.2 Sampling clock for receiving in asynchronous system

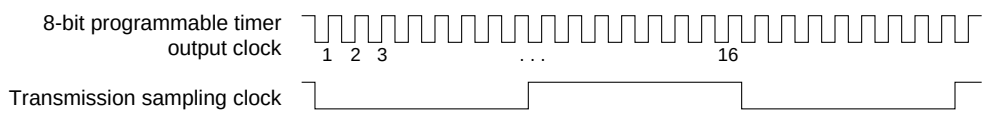


Fig. 5.14.4.3 Sampling clock for sending in asynchronous system

5.14.5 Control procedure to transmit/receive

This section explains the control registers used to transmit and receive.

Shift register and receive data buffer

The serial interface is equipped with a shift register for serial / parallel conversion.

Transmit data written in the transmit / receive data register TRXD is converted to serial data through the shift register and is output from the SOUT terminal.

Besides the shift register, the receiver is equipped with a receive data buffer.
At the time of receiving, data input from the SIN terminal is converted to parallel data through the shift register and loaded into the receive data buffer. However, the buffering function cannot be used in the clock synchronous mode. Therefore, it is necessary to read the received data before starting the next data receiving.

Transmission enable register and transmission control bit

The transmission enable register TXEN and the transmission control bit TXTRG are used to control transmissions.
The transmission enable register TXEN enables and disables transmission. Writing "1" to this register enables transmission. In this status, clock input of the shift register is authorized, and the transmitter shifts into transmit standby status. In the clock synchronous mode, the synchronous clock input and output of the $\overline{\text{SCLK}}$ terminal is authorized, too.

The transmission control bit TXTRG is used as a trigger for starting transmissions.
To start a transmission, write "1" to TXTRG after a preparation to transmit has been completed by writing transmit data to the transmit / receive data register TRXD.
When the transmission is completed, an interrupt is generated when the interrupt has been enabled. After the interrupt is generated, the next transmit data can be written.

TXTRG can also be read as a status. It goes "1" during transmission and goes "0" during standby (stopped) status.

Refer to Section 5.14.9, "Timing charts", for timing of transmission.

Note: Do not set interface conditions, such as transfer mode, when the TXEN register is "1" (transmission authorize status). Setting except for transmission control must be done after writing "0" to the TXEN register.

Receiving enable register and receiving control bit

The receiving enable register RXEN and receiving control bit RXTRG are used to control receiving.
The receiving enable register RXEN enables and disables receiving. Writing "1" to this register enables receiving. In this status, clock input of the shift register is authorized, and the receiver shifts into receive standby status. In the clock synchronous mode, the synchronous clock input and output of the $\overline{\text{SCLK}}$ terminal is authorized, too. When serial data is sent from the transmitter in this status, the data is loaded in the shift register. When receiving has completed, an interrupt is generated when the interrupt has been enabled.

The operation of the receiving control bit RXTRG is slightly different depending on whether the clock synchronous mode or the asynchronous mode is being used.

In the clock synchronous mode, RXTRG is used as a trigger to start receiving.
When received data has been read and the preparation for the next data receiving is completed, write "1" in RXTRG to start receiving. (In the slave mode, the $\overline{\text{SRDY}}$ signal goes "0" when "1" is written to RXTRG.)
In the asynchronous mode, RXTRG is used to prepare for the next data receiving. After reading the received data from the receive data buffer, write "1" in RXTRG to signify that the receive data buffer is empty. If "1" is not written in RXTRG, the overrun error flag OER will be set to "1" when the next receiving is completed. (An overrun error will be generated when the next receiving is completed between reading the previously received data and the writing of "1" to RXTRG.)

RXTRG can also be read as a status. It goes "1" during receiving and goes "0" during standby (stopped) status. This function is the same in either the clock synchronous mode or the asynchronous mode.

Refer to Section 5.14.9, "Timing charts", for timing of receiving.

Note: Do not set interface conditions, such as transfer mode, when the RXEN register is "1" (receiving authorize status). Setting except for receiving control must be done after writing "0" to the RXEN register.

5.14.6 Receive error

During receiving the following three kinds of errors can be detected by an interrupt.

Parity error

When the EPR register has been set to "1" (with parity), a parity check is executing during receiving (except for the clock synchronous mode).
The parity check is done when data received in the shift register is transferred to the receive data buffer. It checks matching with the receive data and the setting of the PMD register (odd parity or even parity). If they are not matched, it is recognized as a parity error and the parity error flag PER and the error interrupt factor flag FSERR are set to "1". An error interrupt is generated at this point when the interrupt has been enabled.
The PER flag is reset to "0" by writing "1".
The received data is transferred to the receive data buffer even when a parity error has generated, and the receiving operation also continues. However, the received data cannot be assured.

Framing error

When the serial interface receives a stop bit as "0", it judges that the synchronization is deviated and generates a framing error.
When a framing error is generated, the framing error flag FER and the error interrupt factor flag FSERR are set to "1". An error interrupt is generated at this point when the interrupt has been enabled.
The FER flag is reset to "0" by writing "1".
The received data is transferred to the receive data buffer even when a framing error has generated, and the receiving operation also continues.
However, even when the following data receiving does not generate a framing error, the data cannot be assured.

Overrun error

In the asynchronous mode, an overrun error occurs when the next data is received before writing "1" to RXTRG.
In the clock synchronous slave mode, an overrun error occurs when the next data is received before reading the received data.
When an overrun error is generated, the overrun error flag OER and the error interrupt factor flag FSERR are set to "1". An error interrupt is generated at this point when the interrupt has been enabled.
The OER flag is reset to "0" by writing "1".
The received data is transferred to the receive data buffer even when an overrun error has generated, and the receiving operation also continues.
Furthermore, when the received data is transferred to the receive data buffer at the same time "1" is written to RXTRG in the asynchronous mode, it is recognized as an overrun error.

5.14.7 Interrupt function

The serial interface can generate the following three interrupts.

- Transmit completion interrupt
- Receive completion interrupt
- Receive error interrupt

The interrupt factor flag that indicates an interrupt factor generation and the interrupt enable register that enables and disables the interrupt are provided for each interrupt factor.

Furthermore, the priority level of the interrupt for the CPU can be set to an optional level (0–3) using the interrupt priority register.
Table 5.14.7.1 shows the interrupt control registers.

Refer to Section 5.18 "Interrupt and Standby Mode", for details of the interrupt control registers and operations subsequent to interrupt generation.
Figure 5.14.7.1 shows the configuration of the serial interface interrupt circuit.

Table 5.14.7.1 Interrupt control registers

Interrupt factor	Interrupt factor flag		Interrupt enable register		Interrupt priority register	
	Name	Address·Dx	Name	Address·Dx	Name	Address·Dx
Receive error	FSERR	00FF28H·D0	ESERR	00FF24H·D0	PSI0	00FF21H·D4
Receive completion	FSRX	00FF28H·D1	ESRX	00FF24H·D1	PSI1	00FF21H·D5
Transmit completion	FSTX	00FF28H·D2	ESTX	00FF24H·D2		

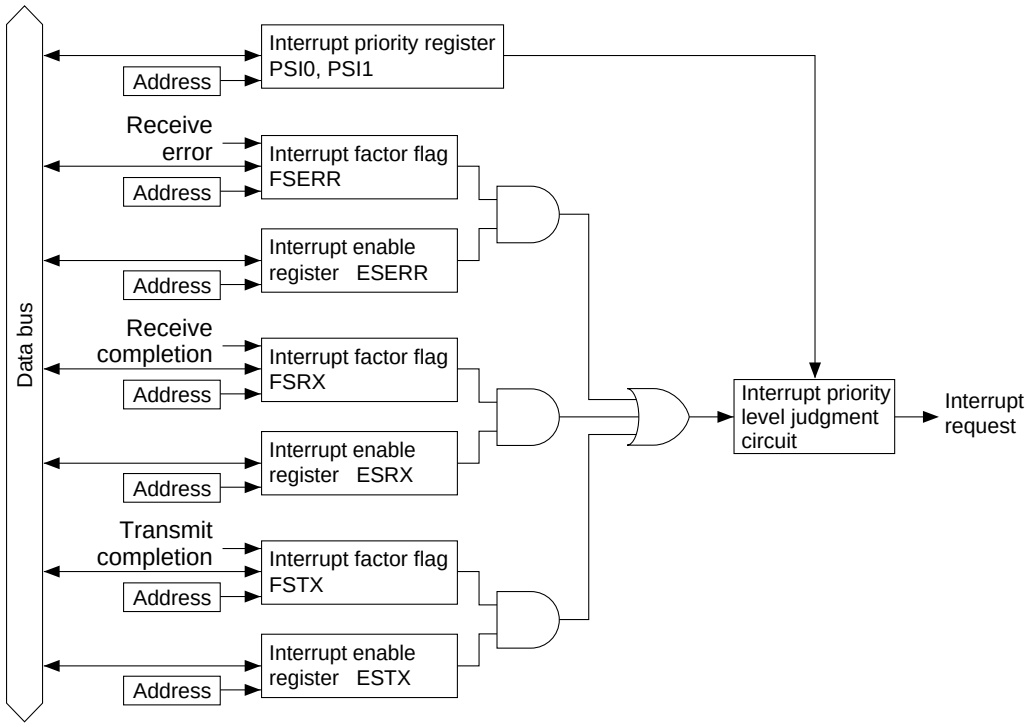


Fig. 5.14.7.1 Configuration of serial interface interrupt circuit

Transmit completion interrupt

This interrupt factor occurs when the transmission of the data written in the shift register has completed, and sets the interrupt factor flag FSTX to "1". It generates an interrupt to the CPU when the interrupt enable register ESTX has been set to "1" and the interrupt priority register PSI has been set to a higher level than the setting of the interrupt flag (I0, I1).
When the interrupt is disabled by setting the ESTX register to "0", interrupt does not occur to the CPU. However, even in this case the FSTX flag is set to "1".
The interrupt factor flag FSTX is reset to "0" by writing "1".

After the interrupt factor occurs, it is possible to write the next transmission data and to start the transmission (writing "1" to TXTRG).
The exception processing vector addresses for the transmit completion interrupt are set as follows:

Transmit completion interrupt: 00001EH

Receive completion interrupt

This interrupt factor occurs when the data received into the shift register is transferred to the receive data buffer after receiving is completed, and sets the interrupt factor flag FSRX to "1". It generates an interrupt to the CPU when the interrupt enable register ESRX has been set to "1" and the interrupt priority register PSI has been set to a higher level than the setting of the interrupt flag (I0, I1).
When the interrupt is disabled by setting the ESRX register to "0", interrupt does not occur to the CPU. However, even in this case the FSRX flag is set to "1".
The interrupt factor flag FSRX is reset to "0" by writing "1".

After the interrupt factor occurs, it is possible to read the received data.
The interrupt factor flag FSRX is set to "1" even when a parity error or a framing error has occurred.
The exception processing vector addresses for the receive completion interrupt are set as follows:

Receive completion interrupt: 00001CH

Receive error interrupt

This interrupt factor occurs when a parity error , a framing error or an overrun error is detected during receiving, and sets the interrupt factor flag FSERR to "1" at the same point of the receive completion interrupt generation. It generates an interrupt to the CPU when the interrupt enable register ESERR has been set to "1" and the interrupt priority register PSI has been set to a higher level than the setting of the interrupt flag (I0, I1).
When the interrupt is disabled by setting the ESERR register to "0", interrupt does not occur to the CPU. However, even in this case the FSERR flag is set to "1".
The interrupt factor flag FSERR is reset to "0" by writing "1".

Since all three kinds of errors result in the same interrupt factor, the error generated should be distinguished using the error flags PER (parity error), OER (overrun error) and FER (framing error).

The exception processing vector addresses for the receive error interrupt are set as follows:

Receive error interrupt: 00001AH

Note: When a parity error or a framing error occurs, both the receive error interrupt factor flag FSERR and the receive completion interrupt factor flag FSRX are simultaneously set to "1". However, since the receive error interrupt has priority over the receive completion interrupt, the receive error interrupt process is executed first. Therefore, it is necessary to reset the FSRX flag in the receive error handling routine. When a receive error interrupt occurs due to an overrun, receive completion interrupt does not occur.

5.14.8 IR (Infrared-ray) interface

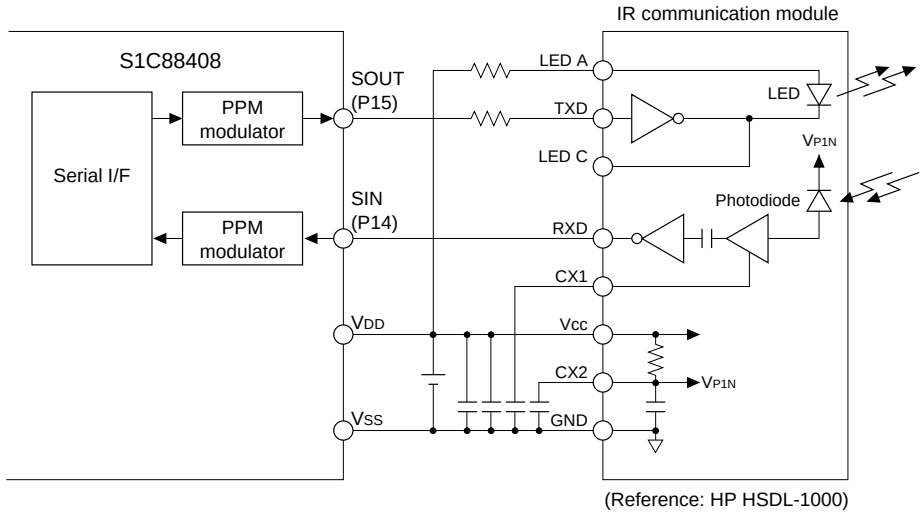


Fig. 5.14.8.1 Configuration example of IR interface

The serial interface has a built-in PPM modulator. Thus a circuit for infrared-ray communication based on IrDA (Infrared Data Association) standard can be configured by adding a simple external circuit.

Setting of IR interface

The PPM modulator is only available when the P14–P17 terminals are selected and the asynchronous mode is set.

When using the IR interface, change the function of the serial interface using the IRST register. (See Table 5.14.8.1.)

At initial reset, the serial interface is set as general interface.

When IR interface function is set, the serial interface can reverse the logic polarity of the input / output signal according to the infrared-ray communication module to be connected to the outside. It is negative logic usually. Reverse the logic when inputting and outputting positive logic signal.

The logic of the SIN input and SOUT output can be individually set by the IRIL register and the IRTL register. (See Tables 5.14.8.2 and 5.14.8.3.)

At initial reset, both the IRIL register and IRTL register are set to "0" (logic not reversed).

Table 5.14.8.1 Setting of IR interface

IRST1	IRST0	Setting
1	1	Reserved (do not set)
1	0	IR interface is used
0	1	Reserved (do not set)
0	0	IR interface is not used (normal interface is set)

Table 5.14.8.2 Input logic of IR interface

IRIL	Setting
1	SIN input logic is reversed (HIGH active)
0	SIN input logic is not reversed (LOW active)

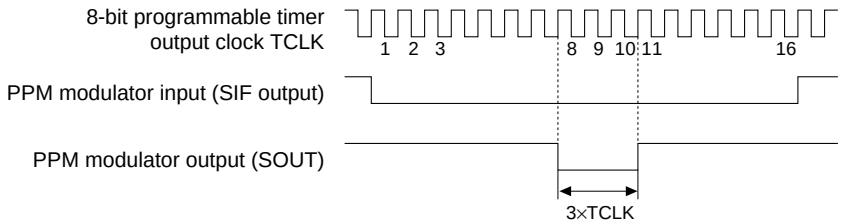
Table 5.14.8.3 Output logic of IR interface

IRTL	Setting
1	SOUT output logic is reversed (HIGH active)
0	SOUT output logic is not reversed (LOW active)

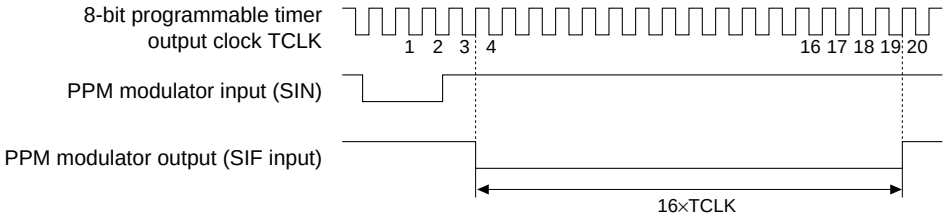
Control of IR interface

The PPM modulator converts input/output signals so that an IR pulse width becomes 3/16 of the pulse width asynchronous input/output signal.

The control procedure of data transfer is the same as in case of the asynchronous mode. Refer to Section 5.14.5 "Control procedure to transmit/receive".



(1) During transmission



(2) During receiving

Fig. 5.14.8.2 Input/output signal

5.14.9 Timing charts

The following shows the transmit / receive timing chart for each transfer mode.

Clock synchronous master mode

This mode uses a clock generated by dividing the 8-bit programmable timer output in 1 / 16 as the synchronous clock $\overline{\text{SCLK}}$. (See Figure 5.14.4.1.)

(1) Transmission timing in clock synchronous master mode

Figure 5.14.9.1 shows the transmission timing in clock synchronous master mode.
By writing "1" to the TXTRG bit, the synchronous clock is output from the $\overline{\text{SCLK}}$ terminal. Each bit of transmission data is output from the SOUT terminal at the falling edge of the synchronous clock. When the last bit is output, a transmit completion interrupt is generated at the rising edge of the synchronous clock.

Note: Do not write data to TXTRG, RXTRG and the TRXD register during transmission (while reading of TXTRG is "1").

(2) Receiving timing in clock synchronous master mode

Figure 5.14.9.2 shows the receiving timing in clock synchronous master mode.
By writing "1" to the RXTRG bit, the synchronous clock is output from the $\overline{\text{SCLK}}$ terminal. The status of the SIN terminal is input at each rising edge of the synchronous clock. When the last bit is input, a receive completion interrupt is generated simultaneously. After the interrupt is generated, the received data can be read from the TRXD register.

Note: Do not write data to TXTRG, RXTRG and the TRXD register during receiving (while reading of RXTRG is "1").

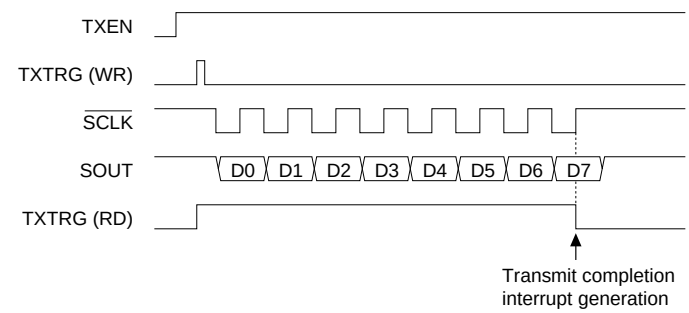


Fig. 5.14.9.1 Transmission timing (clock synchronous master mode)

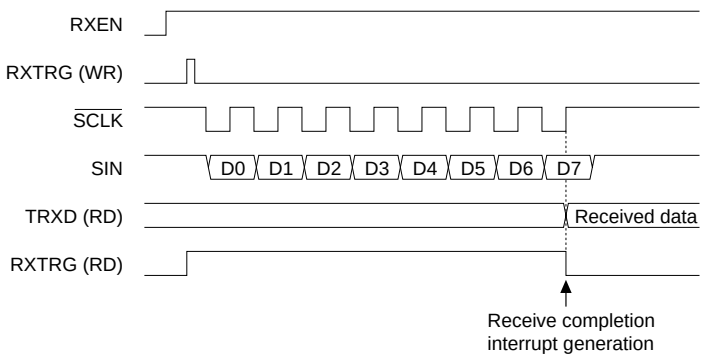


Fig. 5.14.9.2 Receiving timing (clock synchronous master mode)

Clock synchronous slave mode

This mode uses a clock input from the $\overline{SCLK}$ terminal (output from the master device) as the synchronous clock $\overline{SCLK}$.

(1) Transmission timing in clock synchronous slave mode

Figure 5.14.9.3 shows the transmission timing in clock synchronous slave mode.
After writing "1" to the TXTRG bit each bit of transmission data is output from the SOUT terminal at the falling edge of the synchronous clock input from the $\overline{SCLK}$ terminal. When the last bit is output, a transmit completion interrupt is generated at the rising edge of the synchronous clock.

Note: Do not write data to TXTRG, RXTRG and the TRXD register during transmission (while reading of TXTRG is "1").

(2) Receiving timing in clock synchronous slave mode

Figure 5.14.9.4 shows the receiving timing in clock synchronous slave mode.
After writing "1" to the RXTRG bit, the status of the SIN terminal is input at each rising edge of the synchronous clock input from the $\overline{SCLK}$ terminal. When the last bit is input, a receive completion interrupt is generated simultaneously. After the interrupt is generated, the received data can be read from the TRXD register.
When a parity error or a framing error (stop bit = "0") occurs, the error interrupt is generated at the same time as the receive completion interrupt. An overrun error occurs when the next data is received before reading the previous received data. In this case, the interrupt generation timing is the same as other interrupts.

Note: Do not write data to TXTRG, RXTRG and the TRXD register during receiving (while reading of RXTRG is "1").

(3) Transmit/receive ready ($\overline{SRDY}$) signal

When the serial interface is used in the clock synchronous slave mode, it can output the $\overline{SRDY}$ signal that indicates whether the serial interface is ready to transmit / receive or not. The $\overline{SRDY}$ signal is output from the $\overline{SRDY}$ terminal as "0" (low level) when the serial interface is in ready status (ready to transmit / receive) and as "1" (high level) when it is in busy status (during transmission / receiving). The $\overline{SRDY}$ signal changes from "1" to "0" immediately after writing "1" to TXTRG or RXTRG, and returns from "0" to "1" when the first synchronous clock is input (at rising edge). (See Figure 5.14.9.3, Figure 5.14.9.4.)

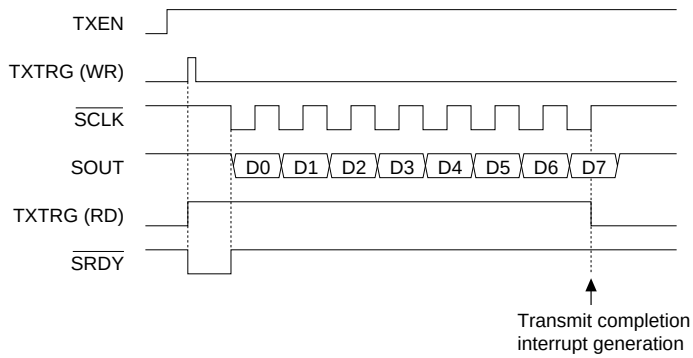


Fig. 5.14.9.3 Transmission timing (clock synchronous slave mode)

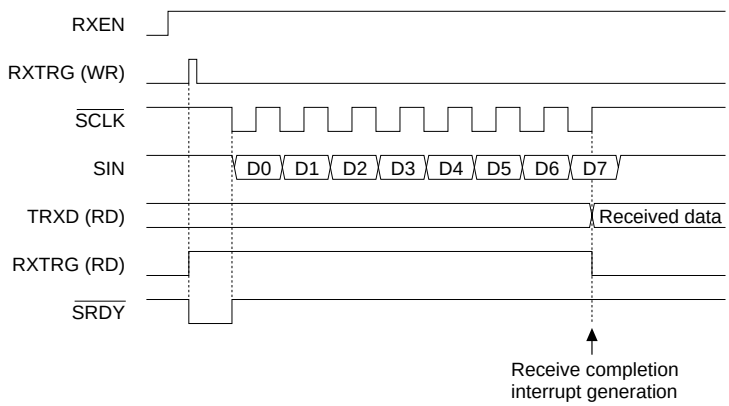


Fig. 5.14.9.4 Receiving timing (clock synchronous slave mode)

Asynchronous mode

(1) Transmission timing in asynchronous mode

Figure 5.14.9.5 shows the transmission timing of the 8-bit asynchronous mode (stop bit = 2 bits, with parity).

After writing "1" to the TXTRG bit, each bit of transmission data is output from the SOUT terminal at the falling edge of the sampling clock generated internally. When the last bit is output, a transmit completion interrupt is generated at the rising edge of the clock. The sampling clock is generated by dividing the 8-bit programmable timer output in 1/16. (See Figure 5.14.4.3.)

(2) Receiving timing in asynchronous mode

Figure 5.14.9.6 shows the receiving timing of the 8-bit asynchronous mode (stop bit = 1 bit, with parity).

When a start bit is input from the SIN terminal, a sampling clock for data receiving is generated (see Figure 4.14.4.2). The status of the SIN terminal is input at each rising edge of the sampling clock. When the last stop bit is input, a receive completion interrupt is generated simultaneously. After the interrupt is generated, the received data can be read from the TRXD register. When a parity error or a framing error (stop bit = "0") occurs, the error interrupt is generated at the same time as the receive completion interrupt.

When receiving data in the asynchronous mode, it is necessary to write "1" to the RXTRG bit after reading received data. An internal signal OERCS checks overrun error. It goes "1" at the end of every data receiving (immediately after inputting the stop bit), and goes "0" by writing "1" to the RXTRG bit. An overrun error occurs if the OERCS signal has not returned to "0" when the stop bit is input. In this case, the error interrupt is generated at the same time as the receive completion interrupt. When the received data is transferred to the receive data buffer at the same time "1" is written to RXTRG, it is recognized as an overrun error. Pay attention to the write timing.

Note: When a parity error or a framing error occurs, both the receive error interrupt factor flag FSERR and the receive completion interrupt factor flag FSRX are simultaneously set to "1". However, since the receive error interrupt has priority over the receive completion interrupt, the receive error interrupt process is executed first. Therefore, it is necessary to reset the FSRX flag in the receive error handling routine. When a receive error interrupt occurs due to an overrun, receive completion interrupt does not occur.

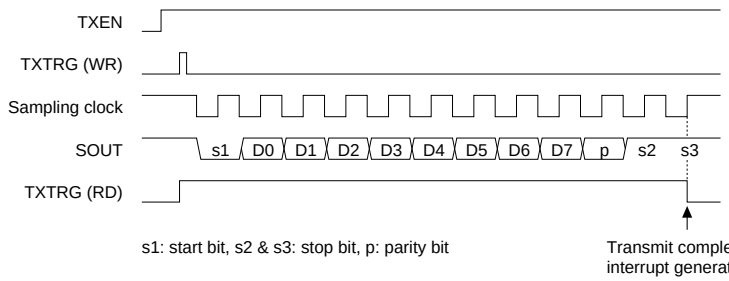


Fig. 5.14.9.5 Transmission timing (8-bit asynchronous mode, stop bit = 2 bits, with parity)

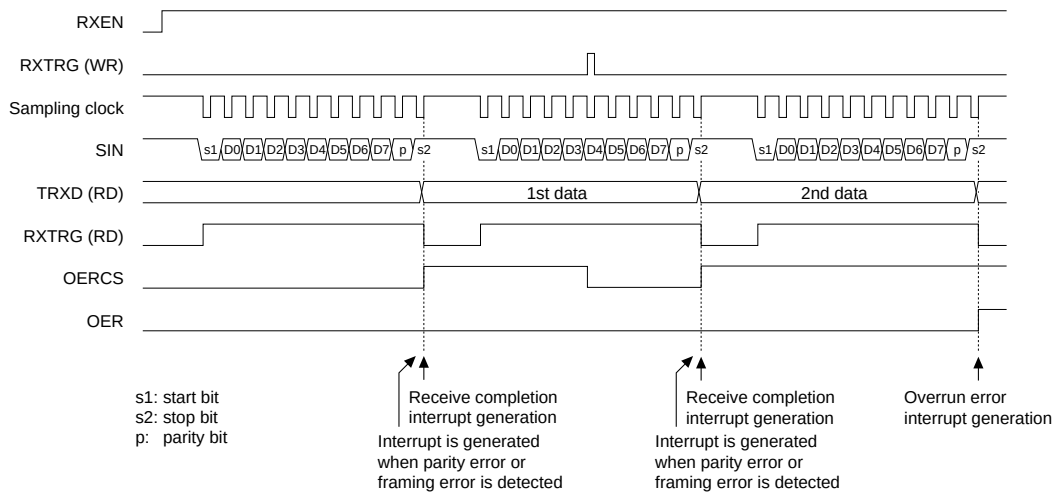


Fig. 5.14.9.6 Receiving timing (8-bit asynchronous mode, stop bit = 1 bit, with parity)

5.14.10 I/O memory of serial interface

Table 5.14.10.1 shows the serial interface control bits.

Table 5.14.10.1(a) Serial interface control bits

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF21	D7	PTM21	8-bit programmable timer	PTM21 PTM20		0	R/W	
	D6	PTM20	interrupt priority register	PSI1 PSI0		0	R/W	
	D5	PSI1	Serial interface	PCTM1 PCTM0	Priority	0	R/W	
	D4	PSI0	interrupt priority register	PLCD1 PLCD0	level	0	R/W	
	D3	PCTM1	Clock timer	1 1	Level 3	0	R/W	
	D2	PCTM0	interrupt priority register	1 0	Level 2	0	R/W	
	D1	PLCD1	LCD controller	0 1	Level 1	0	R/W	
	D0	PLCD0	interrupt priority register	0 0	Level 0	0	R/W	
00FF24	D7	ETU2	8-bit programmable timer underflow interrupt enable register	Interrupt is enabled	Interrupt is disabled	0	R/W	
	D6	ETC1	16-bit programmable timer 1 compare match interrupt enable register			0	R/W	
	D5	ETU1	16-bit programmable timer 1 underflow interrupt enable register			0	R/W	
	D4	ETC0	16-bit programmable timer 0 compare match interrupt enable register			0	R/W	
	D3	ETU0	16-bit programmable timer 0 underflow interrupt enable register			0	R/W	
	D2	ESTX	Serial interface transmit completion interrupt enable register			0	R/W	
	D1	ESRX	Serial interface receive completion interrupt enable register			0	R/W	
	D0	ESERR	Serial interface receive error interrupt enable register			0	R/W	
00FF28	D7	FTU2	8-bit programmable timer underflow interrupt factor flag	(R) Interrupt factor has generated	(R) Interrupt factor has not generated	0	R/(W)	
	D6	FTC1	16-bit programmable timer 1 compare match interrupt factor flag			0	R/(W)	
	D5	FTU1	16-bit programmable timer 1 underflow interrupt factor flag			0	R/(W)	
	D4	FTC0	16-bit programmable timer 0 compare match interrupt factor flag			0	R/(W)	
	D3	FTU0	16-bit programmable timer 0 underflow interrupt factor flag	(W) Reset	(W) Invalid	0	R/(W)	
	D2	FSTX	Serial interface transmit completion interrupt factor flag			0	R/(W)	
	D1	FSRX	Serial interface receive completion interrupt factor flag			0	R/(W)	
	D0	FSERR	Serial interface receive error interrupt factor flag			0	R/(W)	
00FF38	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	PTOUT	8-bit programmable timer clock output control	On	Off	0	R/W	
	D1	PSET	8-bit programmable timer preset	Preset	Invalid	–	W	"0" when being read
	D0	PRUN	8-bit programmable timer RUN/STOP control	Run	Stop	0	R/W	
00FF40	D7	SIOSEL	Serial I/F terminal selection	P14–P17	P10–P13	0	R/W	
	D6	EPR	Serial I/F parity enable	With parity	No parity	0	R/W	
	D5	PMD	Serial I/F parity mode selection	Odd	Even	0	R/W	
	D4	STPB	Serial I/F stop bit selection	2 bits	1 bit	0	R/W	
	D3	–	–	–	–	–	–	"0" when being read
	D2	SMD1	Serial I/F mode selection SMD1 SMD0 Mode 1 1 8-bit asynchronous			0	R/W	
	D1	SMD0	1 0 7-bit asynchronous 0 1 Clock synchronous slave 0 0 Clock synchronous master			0	R/W	
	D0	ESIF	Serial I/F enable	Serial I/F	I/O port	0	R/W	

Table 5.14.10.1(b) Serial interface control bits

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF41	D7	–	–	–	–	–	–	"0" when being read
	D6	FER	Serial I/F framing error flag	Error / Reset (0)	No error / Invalid	0	R / W	
	D5	PER	Serial I/F parity error flag	Error / Reset (0)	No error / Invalid	0	R / W	
	D4	OER	Serial I/F overrun error flag	Error / Reset (0)	No error / Invalid	0	R / W	
	D3	RXTRG	Serial I/F receive trigger/status	Run / Trigger	Stop / Invalid	0	R / W	
	D2	RXEN	Serial I/F receive enable	Enable	Disable	0	R/W	
	D1	TXTRG	Serial I/F transmit trigger/status	Run / Trigger	Stop / Invalid	0	R / W	
	D0	TXEN	Serial I/F transmit enable	Enable	Disable	0	R/W	
00FF42	D7	TRXD7	Serial I/F transmit/receive data register D7(MSB)	High	Low	×	R/W	TRXD7 is invalid in 7-bit asynchronous mode
	D6	TRXD6	D6			×	R/W	
	D5	TRXD5	D5			×	R/W	
	D4	TRXD4	D4			×	R/W	
	D3	TRXD3	D3			×	R/W	
	D2	TRXD2	D2			×	R/W	
	D1	TRXD1	D1			×	R/W	
	D0	TRXD0	D0(LSB)			×	R/W	
00FF43	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	IRTL	IrDA interface output logic inversion	Inverse	Normal	0	R/W	
	D2	IRIL	IrDA interface input logic inversion	Inverse	Normal	0	R/W	
	D1	IRST1	IrDA interface setting			0	R/W	Valid only when SIOSEL = "1" in asynchronous mode
	D0	IRST0	IRST1 / IRST0 / Setting: 1 / 1 / Reserved (do not set); 1 / 0 / IrDA interface; 0 / 1 / Reserved (do not set); 0 / 0 / Normal interface			0	R/W	

ESIF: Serial interface enable register (00FF40H•D0)

Sets the input/output terminals for serial interface.

When "1" is written: Serial I/F I/O terminal
When "0" is written: I/O port terminal
Reading: Valid

The ESIF register is the serial interface enable register. When "1" is written to the register, specified I/O port terminals are set to the terminals for the serial interface. Refer to Section 5.14.2, "Transfer mode and input/output terminals", for the terminal configurations.
When "0" is written, they become the I/O port terminals.
At initial reset, the ESIF register is set to "0" (I/O port terminal).

PTOUT: 8-bit programmable timer clock output control register (00FF38H•D2)

Controls the clock output to the serial interface.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

The PTOUT register is the output control register of the 8-bit programmable timer. When "1" is written to this register, the clock (underflow ∗ 1/2) that is generated by the 8-bit programmable timer is output to the serial interface.
When "0" is written, the clock is not output to the serial interface.
Refer to Section 5.13, "8-bit Programmable Timer", for control of the 8-bit programmable timer.
At initial reset, the PTOUT register is set to "0" (OFF).

SIOSEL: Terminal selection register (00FF40H•D7)

Selects the terminals to be used for the serial interface input/output.

When "1" is written: P14–P17
When "0" is written: P10–P13
Reading: Valid

When "1" is written to the SIOSEL register, the input/output terminals of the serial interface are assigned to P14–P17. When "0" is written, they are assigned to P10–P13. However, the terminals which are actually used within four the terminals are decided by the transfer mode setting (SMD register).
When using IR interface, be sure to set the SIOSEL register to "1" (P14–P17).
At initial reset, the SIOSEL register is set to "0" (P10–P13).

SMD0, SMD1: Mode selection register (00FF40H•D1, D2)

Sets the transfer mode as shown in Table 5.14.10.2.

Table 5.14.10.2 Transfer mode settings

SMD1	SMD0	Mode
1	1	8-bit asynchronous
1	0	7-bit asynchronous
0	1	Clock synchronous slave
0	0	Clock synchronous master

The SMD register can also be read.
When using IR interface, be sure to set in the asynchronous mode.
At initial reset, the SMD register is set to "0" (clock synchronous master mode).

STPB: Stop bit selection register (00FF40H•D4)

Selects the stop bit length asynchronous transfer.

When "1" is written: 2 bits
When "0" is written: 1 bit
Reading: Valid

The STPB register is the stop bit selection register that is valid only for asynchronous transfer. When "1" is written to the register, the stop bit length is set in 2 bits. When "0" is written, it is set in 1 bit.
The start bit length is fixed at 1 bit.
The start/stop bit cannot be added for clock synchronous transfer. Therefore, the setting of the STPB register is invalid.
At initial reset, the STPB register is set to "0" (1 bit).

EPR: Parity enable register (00FF40H•D6)

Selects the parity function.

When "1" is written: With parity
When "0" is written: No parity
Reading: Valid

The EPR register is the parity enable register. By setting this register, parity check for received data and addition of a parity bit to transmission data can be enabled. When "1" is written to the register, the most significant bit of received data is regarded as a parity bit and a parity check is executed and a parity bit is added to transmission data. When "0" is written, neither a parity check nor adding a parity bit is done.
This setting is valid only in the asynchronous mode. It is invalid in the clock synchronous mode.
At initial reset, the EPR register is set to "0" (no parity).

PMD: Parity mode selection register (00FF40H•D5)

Selects odd parity or even parity.

When "1" is written: Odd parity
When "0" is written: Even parity
Reading: Valid

The PMD register is the parity mode selection register. When "1" is written to the register, odd parity is selected. When "0" is written, even parity is selected. The parity check and addition of a parity bit are valid only when "1" has been written to the EPR register. When "0" has been written to the EPR register, parity setting by the PMD register is invalid.
At initial reset, the PMD register is set to "0" (even parity).

TXEN: Transmission enable register (00FF41H•D0)

Sets the serial interface to the transmission authorize status.

When "1" is written: Transmission is enabled
When "0" is written: Transmission is disabled
Reading: Valid

The TXEN register is the transmission enable register. When "1" is written to the register, the serial interface shifts to a transmission authorize status. When "0" is written, it shifts to a transmission disabling status.
Set the TXEN register to "0" when setting the transfer mode.
At initial reset, the TXEN register is set to "0" (transmission is disabled).

TXTRG: Transmission trigger/status (00FF41H•D1)

This bit is used as the transmission start trigger and the operation status indicator (transmission / stop status).

When "1" is read: During transmission
When "0" is read: During stop

When "1" is written: Transmission trigger
When "0" is written: Invalid

TXTRG is the transmission control bits (trigger / status). Transmission starts when "1" is written to TXTRG after writing the transmission data.
TXTRG can be read as the status. When it is "1", it indicates transmission, and "0" indicates stoppage.
At initial reset, TXTRG is set to "0" (during stop).

RXEN: Receiving enable register (00FF41H•D2)

Sets the serial interface to the receiving authorize status.

When "1" is written: Receiving is enabled
When "0" is written: Receiving is disabled
Reading: Valid

The RXEN register is the receiving enable register. When "1" is written to the register, the serial interface shifts to a receiving authorize status. When "0" is written, it shifts to a receiving disabling status.
Set the RXEN register to "0" when setting the transfer mode.
At initial reset, the RXEN is set to "0" (receiving is disabled).

RXTRG: Receiving trigger/status (00FF41H•D3)

This bit is used as the receiving start trigger, ready to receive and the operation status indicator (receiving / stop status).

When "1" is read: During receiving
When "0" is read: During stop

When "1" is written: Receiving trigger / Ready to receive
When "0" is written: Invalid

RXTRG is the receiving control bits (trigger / status).

In the clock synchronous mode, RXTRG is used as a trigger to start receiving.
When received data has been read and the preparation for the next data receiving is completed, write "1" in RXTRG to start receiving.

In the asynchronous mode, RXTRG is used to prepare for the next data receiving. After reading the received data from the receive data buffer, write "1" in RXTRG to signify that the receive data buffer is empty. If "1" is not written in RXTRG, the overrun error flag OER will be set to "1" when the next receiving is completed. (An overrun error will be generated when the next receiving is completed between reading the previous received data and the writing of "1" to RXTRG.)

RXTRG can also be read as a status. When it is "1", it indicates receiving, and "0" indicates stoppage. This function is the same in both the clock synchronous mode and the asynchronous mode.
At initial reset, RXTRG is set to "0" (during stop).

TRXD0–TRXD7: Transmit/receive data register (00FF42H)

The TRXD register is the transmit / receive data register for the serial interface.

During transmission

Write a transmission data to this register.

When "1" is written: HIGH level
When "0" is written: LOW level

Write the transmitting data prior to start transmission.
When transmitting data continuously, following data should be written after the transmit completion interrupt occurs.
In the 7-bit asynchronous mode, TRXD7 is invalid.
The data written in this register is converted into serial data, and output from the SOUT terminal as the bit set to "1" is a high (V_{DD}) level and the bit set to "0" is a low (V_{SS}) level.

During receiving

Received data can be read from this register.

When "1" is read: HIGH level
When "0" is read: LOW level

The data in the receive data buffer can be read. Received data should be read after the receive completion interrupt occurs.
In the asynchronous mode, the received data can be read even while the next data is being received because the receive data buffer is provided separately from the shift register. (The buffer function is not used in the clock synchronous mode.)

In the 7-bit asynchronous mode, TRXD7 is always read as "0".
The serial data input from the SIN terminal is loaded into this buffer after converting into parallel data as the bit of a high (V_{DD}) level is "1" and the bit of a low (V_{SS}) level is "1".
At initial reset, the content of the TRXD register is undefined.

OER: Overrun error flag (00FF41H•D4)

Indicates the occurrence of an overrun error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

OER is the error flag that indicates the occurrence of an overrun error. The flag goes "1" when an overrun error occurs.
In the asynchronous mode, an overrun error occurs when the next data is received prior to writing "1" to RXTRG.
In the clock synchronous slave mode, an overrun error occurs when the next data is received prior to reading the received data.
In the clock synchronous master mode, overrun error does not occur.
The OER flag is reset to "0" by writing "1".
At initial reset and when the RXEN register is "0", the OER flag is set to "0" (no error).

PER: Parity error flag (00FF41H•D5)

Indicates the occurrence of a parity error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

PER is the error flag that indicates the occurrence of a parity error. The flag goes "1" when a parity error occurs.
The PER flag is reset to "0" by writing "1".
At initial reset and when the RXEN register is "0", the PER flag is set to "0" (no error).

FER: Framing error flag (00FF41H•D6)

Indicates the occurrence of a framing error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

FER is the error flag that indicates the occurrence of a framing error. The flag goes "1" when a framing error occurs.
Framing error occurs when a stop bit is received as "0".
The FER flag is reset to "0" by writing "1".
At initial reset and when the RXEN register is "0", the FER flag is set to "0" (no error).

PSI0, PSI1: Interrupt priority register (00FF21H•D4, D5)

Sets the priority level of the serial interface interrupt.
The PSI register is the interrupt priority register corresponding to the serial interface interrupt.
Table 5.14.10.3 shows the interrupt priority level which can be set by this register.

Table 5.14.10.3 Interrupt priority level settings

PSI1	PSI0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, the PSI register is set to "0" (level 0).

ESERR, ESRX, ESTX: Interrupt enable register (00FF24H•D0, D1, D2)

Enables or disables the serial interface interrupt generation to the CPU.

When "1" is written: Interrupt is enabled
When "0" is written: Interrupt is disabled
Reading: Valid

The ESERR, ESRX and ESTX registers are interrupt enable registers corresponding to the receive error, receive completion and transmit completion interrupt factors, respectively.
Interrupt in which the interrupt enable register is set to "1" is enabled, and the others in which the register is set to "0" are disabled.
At initial reset, the interrupt enable registers are all set to "0" (interrupt is disabled).

FSERR, FSRX, FSTX: Interrupt factor flag (00FF28H•D0, D1, D2)

Indicates the generation of the serial interface interrupt factor.

When "1" is read: Int. factor has generated
When "0" is read: Int. factor has not generated

When "1" is written: Factor flag is reset
When "0" is written: Invalid

The FSERR, FSRX and FSTX flags are interrupt factor flags corresponding to the receive error, receive completion and transmit completion interrupts, respectively. They are set to "1" by a generation of each factor.
Transmit completion interrupt factor is generated when a transmission of the shift register data is completed.
Receive completion interrupt factor is generated when the received data is transferred to the receive data buffer.
Receive error interrupt factor is generated when a parity error, framing error or overrun error has been detected during data receiving.
At this point, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of the interrupt flags (I0 and I1), an interrupt is generated to the CPU.
Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag is set to "1" when the interrupt generation condition is met.
To accept the subsequent interrupt after an interrupt generation, it is necessary to re-set the interrupt flags (set the interrupt flag to a lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and to reset the interrupt factor flag. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, the interrupt factor flags are all reset to "0".

5.14.11 Programming notes

(1) Setting of the serial interface mode must be done in the transmission / receiving disabling status (TXEN = RXEN = "0").

(2) Do not perform double trigger (writing "1") to TXTRG (RXTRG) during transmission (receiving). Furthermore, do not execute the SLP instruction. (When executing the SLP instruction, set TXEN and RXEN to "0".)

(3) Transmission and receiving cannot be done simultaneously in the clock synchronous mode because the clock line ($\overline{SCLK}$) is shared with transmit and receive operation. Therefore, do not write "1" to RXTRG (TXTRG) when TXTRG (RXTRG) is "1".

(4) When a parity error or a framing error occurs, both the receive error interrupt factor flag FSERR and the receive completion interrupt factor flag FSRX are simultaneously set to "1". However, since the receive error interrupt has priority over the receive completion interrupt, the receive error interrupt process is executed first. Therefore, it is necessary to reset the FSRX flag in the receive error handling routine.
When a receive error interrupt occurs due to an overrun, receive completion interrupt does not occur.

5.15 Sound Generator

5.15.1 Configuration of sound generator

The S1C88408 has a built-in sound generator for generating BZ (buzzer) signal.
BZ signals generated from the sound generator can be output from the R42 output port terminal.
Aside permitting the respective setting of the buzzer signal frequency and sound level (duty adjustment) to 8 stages, it permits the adding of a digital envelope by means of duty ratio control. It also has a one-shot output function for outputting key operated sounds.
Figure 5.15.1.1 shows the configuration of the sound generator.

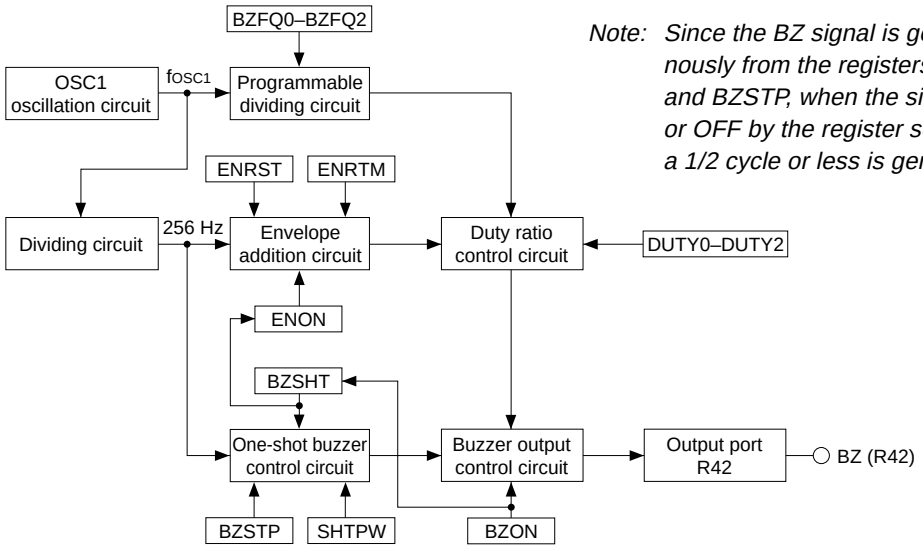


Fig. 5.15.1.1 Configuration of sound generator

5.15.2 Control of buzzer output

BZ signal can be output from the R42 output port terminal.
The configuration of the output port R42 is shown in Figure 5.15.2.1.

The output control for the BZ signal generated by the sound generator is done by the buzzer output control register BZON, one-shot buzzer trigger bit BZSHT and one-shot buzzer forced stop bit BZSTP. When "1" is set to BZON or BZSHT, the BZ signal is output from the R42 output port terminal and when "0" is set to BZON or "1" is set to BZSTP, the high (V_{DD}) level is output. At this time, "1" must always be set for the output data register R42D.
Figure 5.15.2.2 shows the output waveform of the BZ signal.

Note: Since the BZ signal is generated asynchronously from the registers BZON, BZSHT and BZSTP, when the signal is turned ON or OFF by the register settings, a hazard of a 1/2 cycle or less is generated.

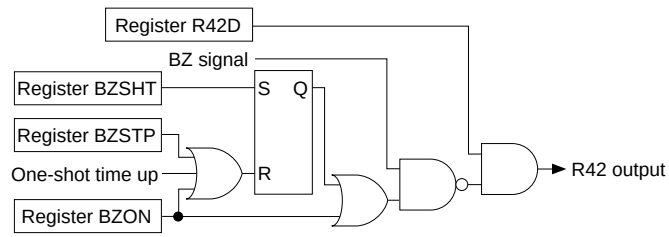


Fig. 5.15.2.1 Configuration of R42

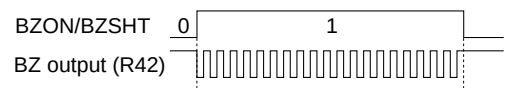


Fig. 5.15.2.2 Output waveform of BZ signal

5.15.3 Setting of buzzer frequency and sound level

The BZ signal is a divided signal using the OSC1 oscillation circuit (32.768 kHz) as the clock source and 8 frequencies can be selected. This selection is done by the buzzer frequency selection register BZFQ0–BZFQ2. The setting value and buzzer frequency correspondence is shown in Table 5.15.3.1.

By selecting the duty ratio of the BZ signal from among 8 types, the buzzer sound level can be adjusted. This selection is made in the duty ratio selection register DUTY0–DUTY2. The setting value and duty ratio correspondence is shown in Table 5.15.3.2.

Table 5.15.3.1 Buzzer signal frequency settings

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

Table 5.15.3.2 Duty ratio settings

Level	DUTY2	DUTY1	DUTY0	Duty ratio by buzzer frequencies (Hz)			
				4096.0	3276.8	2730.7	2340.6
				2048.0	1638.4	1365.3	1170.3
Level 1 (Max)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (Min)	1	1	1	1/16	1/20	5/24	5/28

Duty ratio refers to the ratio of pulse width to the pulse cycle; given that HIGH level output time is TH, and low level output time is TL the BZ signal becomes TL / (TH+TL).
When DUTY0–DUTY2 have all been set to "0", the duty ratio becomes maximum and the sound level also becomes maximum. Conversely, when DUTY0–DUTY2 have all been set to "1", the duty ratio becomes minimum and the sound level also becomes minimum.

Note that the duty ratio setting differ depending on frequency. See Table 5.15.3.2.

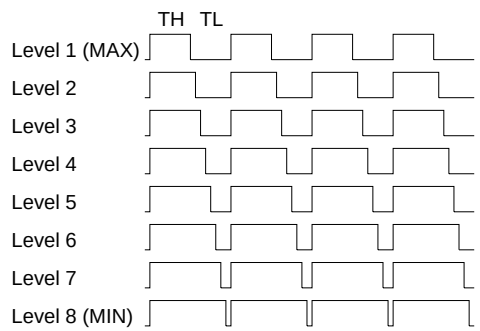


Fig. 5.15.3.1 Duty ratio of buzzer signal waveform

Note: When using the digital envelope, the DUTY0–DUTY2 setting becomes invalid.

5.15.4 Digital envelope

A digital envelope with duty control can be added to the BZ signal.
The envelope can be realized by staged changing of the same duty ratio as detailed in Table 5.15.3.2 in the preceding section from level 1 (maximum) to level 8 (minimum).
The addition of an envelope to the buzzer signal can be done by writing "1" to the envelope control register ENON. When "0" is written, the duty ratio is set at the level selected in DUTY0–DUTY2.
By writing "1" to ENON and turning the buzzer output ON (writing "1" to BZON), a BZ signal with a level 1 duty ratio is output, and then the duty ratio can be attenuated in stages to level 8. The attenuated envelope can be returned to level 1 by writing "1" to the envelope reset bit ENRST. When attenuated to level 8, the duty level remains at level 8 until the buzzer output is turned OFF (writing "0" to BZON) or writing "1" to ENRST.
The stage changing time for the envelope level can be selected either 125 msec or 62.5 msec by the envelope attenuation time selection register ENRTM.
Figure 5.15.4.1 shows the timing chart of the digital envelope.

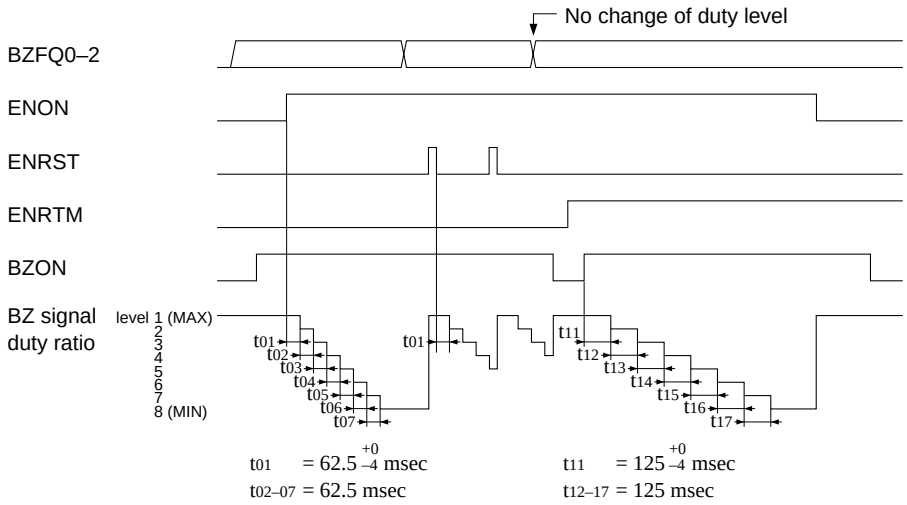


Fig. 5.15.4.1 Timing chart of digital envelope

5.15.5 One-shot output

The sound generator has a built-in one-shot output function for outputting a short duration buzzer signal for key operation sounds and similar effects. Either 125 msec or 31.25 msec can be selected by the one-shot buzzer duration selection register SHTPW for buzzer signal output time.
The output control of the one-shot buzzer is done by writing "1" to the one-shot buzzer trigger BZSHT, then the BZ signal is output in synchronization with the internal 256 Hz signal from the R42 output port terminal. Thereafter, when the set time has elapsed, the BZ signal in synchronization with the 256 Hz signal automatically goes OFF in the same manner.
The BZSHT can be read to determine status. When BZSHT is "1", it indicates a BUSY status (during one-shot output) and when BZSHT is "0", it indicates a READY status (during stop).
When you want to turn the BZ signal OFF prior to the elapse of the set time, the BZ signal can be immediately stopped (goes OFF in asynchonization with 256 Hz signal) by writing "1" to the one-shot forced stop bit BZSTP.

Since the one-shot output has a short duration, an envelope cannot be added. (When "1" is written to BZSHT, ENON is automatically reset to "0".) Consequently, only the frequency and sound level can be set for one-shot output.

The control for the one-shot output is invalid during normal buzzer output.

Figure 5.15.5.1 shows the timing chart of the one-shot output.

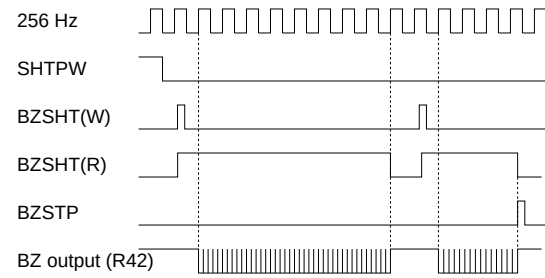


Fig. 5.15.5.1 Timing chart of one-shot output

5.15.6 I/O memory of sound generator

Table 5.15.6.1 shows the sound generator control bits.

Table 5.15.6.1 Sound generator control bits

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF54	D7	–	–	–	–	–	–	"0" when being read
	D6	BZSTP	One-shot buzzer forcibly stop	Forcibly stop	No operation	–	W	
	D5	BZSHT	One-shot buzzer trigger/status	Busy	Ready	0	R	
				Trigger	No operation	0	W	
	D4	SHTPW	One-shot buzzer duration width selection	125 msec	31.25 msec	0	R/W	
	D3	ENRTM	Envelope attenuation time	1 sec	0.5 sec	0	R/W	
	D2	ENRST	Envelope reset	Reset	No operation	–	W	"0" when being read
	D1	ENON	Envelope On/Off control	On	Off	0	R/W	∗1
	D0	BZON	Buzzer output control	On	Off	0	R/W	
00FF55	D7	–	–	–	–	–	–	"0" when being read
	D6	DUTY2	Buzzer signal duty ratio selection			0	R/W	
	D5	DUTY1				0	R/W	
	D4	DUTY0				0	R/W	
	D3	–	–	–	–	–	–	"0" when being read
	D2	BZFQ2	Buzzer frequency selection			0	R/W	
	D1	BZFQ1				0	R/W	
	D0	BZFQ0				0	R/W	

DUTY2–1 / Buzzer frequency (Hz)

2	1	0	4096.0 2048.8	3276.8 1638.4	2730.7 1365.3	2340.6 1170.3
0	0	0	8/16	8/20	12/24	12/28
0	0	1	7/16	7/20	11/24	11/28
0	1	0	6/16	6/20	10/24	10/28
0	1	1	5/16	5/20	9/24	9/28
1	0	0	4/16	4/20	8/24	8/28
1	0	1	3/16	3/20	7/24	7/28
1	1	0	2/16	2/20	6/24	6/28
1	1	1	1/16	1/20	5/24	5/28

Buzzer frequency selection

BZFQ2	BZFQ1	BZFQ0	Frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

∗1 ENON is reset to "0" during one-shot output.

BZON: Buzzer output control register (00FF54H•D0)

Controls the BZ signal output.

When "1" is written: BZ signal output
When "0" is written: HIGH level (DC) output
Reading: Valid

BZON is the output control register for BZ signal. When "1" is set, the BZ signal is output from the output port terminal R42 and when "0" is set, high (V_{DD}) level is output. At this time, the high-impedance control register of the output port R42 must be set to "0" and the data register must be set to "1".

At initial reset, BZON is set to "0" (high level output).

BZFQ0–BZFQ2: Buzzer frequency selection register (00FF55H•D0–D2)

Selects the BZ signal frequency.

Table 5.15.6.2 Buzzer frequency settings

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

The buzzer frequency can be selected from among the above 8 types that have divided the OSC1 clock.

At initial reset, the BZFQ register is set to "0" (4096.0 Hz).

DUTY0–DUTY2: Duty ratio selection register (00FF55H•D4–D6)

Selects the duty ratio of the BZ signal.

Table 5.15.6.3 Duty ratio settings

Level	DUTY2	DUTY1	DUTY0	Duty ratio by buzzer frequencies (Hz)			
				4096.0 2048.0	3276.8 1638.4	2730.7 1365.3	2340.6 1170.3
Level 1 (Max)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (Min)	1	1	1	1/16	1/20	5/24	5/28

The buzzer sound level can be adjusted by selecting the duty ratio from among the above 8 types. However, when the envelope has been set to ON (ENON = "1"), this setting becomes invalid.
At initial reset, the DUTY register is set to "0" (level 1).

ENRST: Envelope reset (00FF54H•D2)

Resets the envelope.

When "1" is written: Reset
When "0" is written: No operation
Reading: Always "0"

The envelope is reset by writing "1" to ENRST and the duty ratio returns to level 1 (maximum). Writing "0" to ENRST and writing "1" when an envelope has not been added become invalid. Since ENRST is exclusively for writing, it always becomes "0" during reading.

ENON: Envelope ON/OFF control register (00FF54H•D1)

Controls the addition of an envelope to the BZ signal.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

By writing "1" to ENON, an envelope can be added to BZ signal output. When "0" is written, an envelope is not added and the BZ signal is fixed at the duty ratio selected in DUTY0–DUTY2.
At initial reset and when "1" is written to BZSHT, the ENON register is set to "0" (OFF).

ENRTM: Envelope attenuation time selection register (00FF54H•D3)

Selects the envelope attenuation time that is added to the BZ signal.

When "1" is written: 1.0 sec
(125 msec × 7 = 875 msec)
When "0" is written: 0.5 sec
(62.5 msec × 7 = 437.5 msec)
Reading: Valid

The attenuation time of the digital envelope is determined by the time for changing the duty ratio.
The duty ratio is changed in 125 msec (8 Hz) units when "1" is written to ENRTM and in 62.5 msec (16 Hz) units, when "0" is written.
This setting becomes invalid when an envelope has been set to OFF (ENON = "0").
At initial reset, the ENRTM register is set to "0" (0.5 sec).

SHTPW: One-shot buzzer output duration width selection register (00FF54H•D4)

Selects the output duration width of the one-shot buzzer.

When "1" is written: 125 msec
When "0" is written: 31.25 msec
Reading: Valid

The one-shot buzzer output duration width is set to 125 msec when "1" is written to SHTPW and 31.25 msec, when "0" is written.
At initial reset, the SHTPW register is set to "0" (31.25 msec).

BZSHT: One-shot buzzer trigger/status (00FF54H•D5)

Controls the one-shot buzzer output.

When "1" is written: Trigger
When "0" is written: No operation

When "1" is read: Busy
When "0" is read: Ready

Writing "1" into BZSHT causes the one-shot output circuit to operate and the BZ signal to be output. The buzzer output is automatically turned OFF after the time set by SHTPW has elapsed. At this time, the high-impedance control register of the output port R42 must be set to "0" and the data register must be "1".
The one-shot output is only valid when the normal buzzer output is OFF (BZON = "0") status. The trigger is invalid during ON (BZON = "1") status.
When a re-trigger is assigned during a one-shot output, the one-shot output time set with SHTPW is measured again from that point. (time extension)
The operation status of the one-shot output circuit can be confirmed by reading BZSHT, when the one-shot output is ON (busy), BZSHT is read as "1" and when the output is OFF (ready), it is read as "0".
At initial reset, BZSHT is set to "0" (ready).

BZSTP: One-shot buzzer forcibly stop (00FF54H•D6)

Forcibly stops the one-shot buzzer output.

When "1" is written: Forcibly stop
When "0" is written: No operation
Reading: Constantly "0"

By writing "1" into BZSTP, the one-shot buzzer output can be stopped prior to the elapsing of the time set with SHTPW.
Writing "0" is invalid and writing "1" except during one-shot output is also invalid.
When "1" is written to BZSHT and BZSTP simultaneously, BZSTP takes precedence and one-shot output becomes stop status.
Since BZSTP is for writing only, during readout it is constantly set to "0".

5.15.7 Programming notes

(1) Since the BZ signal is generated asynchronously from the register BZON, when the signal is turned ON or OFF by the register setting, a hazard of a 1/2 cycle or less is generated.

(2) The SLP instruction has executed when the BZ signal is in the enable status (BZON = "1" or BZSHT = "1"), an unstable clock is output from the R42 output port terminal at the time of return from the SLEEP status. Consequently, when shifting to the SLEEP status, you should set the BZ signal to the disable status (BZON = BZSHT = "0") prior to executing the SLP instruction.

(3) The one-shot output is only valid when the normal buzzer output is OFF (BZON = "0") status. The trigger is invalid during ON (BZON = "1") status.

5.16 SVD (Supply Voltage Detection) Circuit

5.16.1 Configuration of SVD circuit

The S1C88408 has a built-in SVD (supply voltage detection) circuit, so that the software can find when the source voltage lowers. Turning the SVD circuit ON / OFF and the SVD criteria voltage setting can be done with software.
Figure 5.16.1.1 shows the configuration of the SVD circuit.

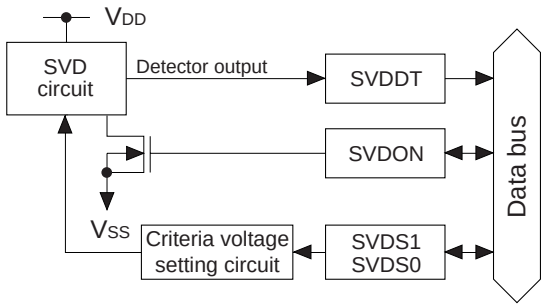


Fig. 5.16.1.1 Configuration of SVD circuit

5.16.2 SVD operation

The SVD circuit compares the criteria voltage set by software and the supply voltage (V_{DD}–V_{SS}) and sets its results into the SVDDT latch. By reading the data of this SVDDT latch, it can be determined by means of software whether the supply voltage is normal or has dropped.

The criteria voltage can be set for the 3 types shown in Table 5.16.2.1 by the SVD register.

Table 5.16.2.1 Criteria voltage setting

SVD1	SVD0	Criteria voltage
1	×	3.4 V
0	1	2.8 V
0	0	1.9 V

When the SVDON register is set to "1", source voltage detection by the SVD circuit is executed. As soon as the SVDON register is reset to "0", the result is loaded to the SVDDT latch and the SVD circuit goes OFF.
To obtain a stable detection result, the SVD circuit must be ON for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 100 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

The SVD operation increases current consumption, so turn the SVD circuit off when voltage detection is unnecessary or executing the SLP instruction.

5.16.3 I/O memory of SVD circuit

Table 5.16.3.1 shows the control bits for the SVD circuit.

Table 5.16.3.1 SVD circuit control bits

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF56	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	SVD1	SVD criteria voltage setting SVD1 SVD0 Voltage (V) 1 × 3.4 V 0 1 2.8 V 0 0 1.9 V			0	R/W	
	D2	SVD0				0	R/W	
	D1	SVDDT	SVD data	Low	Normal	0	R	
	D0	SCDON	SVD On/Off control	On	Off	0	R/W	

SVD0, SVD1: SVD criteria voltage setting register (FF56H•D2, D3)

Criteria voltage for SVD is set as shown in Table 5.16.3.1.
At initial reset, this SVD register is set to "0" (1.9 V).

SVDON: SVD control (ON/OFF) register (FF56H•D0)

Turns the SVD circuit ON and OFF.

When "1" is written: SVD circuit ON
When "0" is written: SVD circuit OFF
Reading: Valid

When the SVDON register is set to "1", a source voltage detection is executed by the SVD circuit. As soon as SVDON is reset to "0", the result is loaded to the SVDDT latch. To obtain a stable detection result, the SVD circuit must be ON for at least l00 µsec.
At initial reset, this SVD register is set to "0" (Off).

SVDDT: SVD data (FF56H•D1)

This is the result of supply voltage detection.

When "0" is read: Supply voltage (V_{DD}–V_{SS}) ≥ Criteria voltage
When "1" is read: Supply voltage (V_{DD}–V_{SS}) < Criteria voltage
Writing: Invalid

The result of supply voltage detection at time of SVDON is set to "0" can be read from this latch.
At initial reset, SVDDT is set to "0" (Normal).

5.16.4 Programming notes

(1) To obtain a stable detection result, the SVD circuit must be ON for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 100 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

(2) The SVD operation increases current consumption, so turn the SVD circuit off when voltage detection is unnecessary or executing the SLP instruction.

5.17 Address Match Jump

5.17.1 Outline of function

The S1C88408 has the address match jump function that issues a vector jump when the CPU fetches the operation code at the specified address in the internal ROM. This function is useful to patch the program in the internal ROM for bug measures and adding functions.

5.17.2 Match address set and vector jump

Up to four addresses can be set to issue vector jumps. It should be done by writing the addresses to the four sets of match address registers.

Note: The address match jump function can be used in the MCU mode because it uses accessing to the internal ROM. In the MPU mode, this function cannot be used.
Also design the system in the expanded mode to allow adding the branch destination routines in the future.
The jump address must be a logical address in the internal ROM area, and the address must contain the first operation code of an instruction. Be aware that the program will run away when an address that contains the second operation code or an operand is set.

Table 5.17.2.1 shows the match address registers and the predefined vector addresses.

Table 5.17.2.1 Match address register and vector address

Set	Match address set register	Vector
0	MA0A00–MA0A07 (00FF70H) MA0A08–MA0A15 (00FF71H)	2A
1	MA1A00–MA1A07 (00FF70H) MA1A08–MA1A15 (00FF71H)	2C
2	MA2A00–MA2A07 (00FF70H) MA2A08–MA2A15 (00FF71H)	2E
3	MA3A00–MA3A07 (00FF70H) MA3A08–MA3A15 (00FF71H)	30

When a match address register is set to 0000H (default), an address match jump of the set will not be issued.
However a jump vector should be written in each vector address if address match jump is not be used in development stage, because it may be necessary in the future.
Since the vector must be a logical address, jumping to another bank cannot be done.

When the CPU fetches the operation code in an address (one of four sets), it executes the "JP [kk]" instruction (kk is the vector address of each set).
Figure 5.17.2.1 shows the timing chart for address match jump.

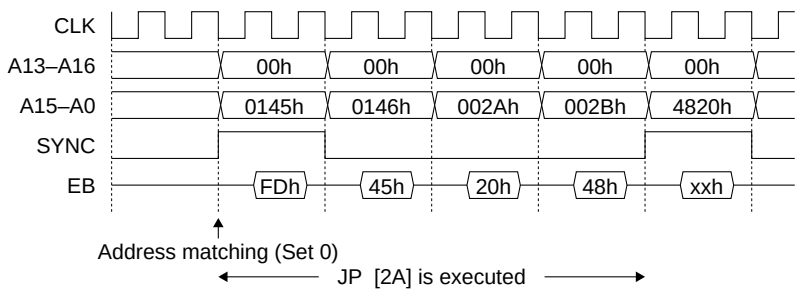


Fig. 5.17.2.1 Timing chart for address match jump

5.17.3 I/O memory of address match jump

Table 5.17.3.1 shows the control bits of the address match jump function.

Table 5.17.3.1 Address match jump control bits

Address	Bit	Name	Function		1	0	Init	R/W	Comment
00FF70	D7	MA0A07	Match address set 0	A07	High	Low	0	R/W	Address match jump 0
	D6	MA0A06	Address (Lower 8 bits)	A06			0	R/W	does not occur when
	D5	MA0A05		A05			0	R/W	FF71 and FF70 are set
	D4	MA0A04		A04			0	R/W	to 0000H.
	D3	MA0A03		A03			0	R/W	
	D2	MA0A02		A02			0	R/W	
	D1	MA0A01		A01			0	R/W	
	D0	MA0A00		A00			0	R/W	
00FF71	D7	MA0A15	Match address set 0	A15	High	Low	0	R/W	Address match jump 0
	D6	MA0A14	Address (Upper 8 bits)	A14			0	R/W	does not occur when
	D5	MA0A13		A13			0	R/W	FF71 and FF70 are set
	D4	MA0A12		A12			0	R/W	to 0000H.
	D3	MA0A11		A11			0	R/W	
	D2	MA0A10		A10			0	R/W	
	D1	MA0A09		A09			0	R/W	
	D0	MA0A08		A08			0	R/W	
00FF72	D7	MA1A07	Match address set 1	A07	High	Low	0	R/W	Address match jump 1
	D6	MA1A06	Address (Lower 8 bits)	A06			0	R/W	does not occur when
	D5	MA1A05		A05			0	R/W	FF73 and FF72 are set
	D4	MA1A04		A04			0	R/W	to 0000H.
	D3	MA1A03		A03			0	R/W	
	D2	MA1A02		A02			0	R/W	
	D1	MA1A01		A01			0	R/W	
	D0	MA1A00		A00			0	R/W	
00FF73	D7	MA1A15	Match address set 1	A15	High	Low	0	R/W	Address match jump 1
	D6	MA1A14	Address (Upper 8 bits)	A14			0	R/W	does not occur when
	D5	MA1A13		A13			0	R/W	FF73 and FF72 are set
	D4	MA1A12		A12			0	R/W	to 0000H.
	D3	MA1A11		A11			0	R/W	
	D2	MA1A10		A10			0	R/W	
	D1	MA1A09		A09			0	R/W	
	D0	MA1A08		A08			0	R/W	
00FF74	D7	MA2A07	Match address set 2	A07	High	Low	0	R/W	Address match jump 2
	D6	MA2A06	Address (Lower 8 bits)	A06			0	R/W	does not occur when
	D5	MA2A05		A05			0	R/W	FF75 and FF74 are set
	D4	MA2A04		A04			0	R/W	to 0000H.
	D3	MA2A03		A03			0	R/W	
	D2	MA2A02		A02			0	R/W	
	D1	MA2A01		A01			0	R/W	
	D0	MA2A00		A00			0	R/W	
00FF75	D7	MA2A15	Match address set 2	A15	High	Low	0	R/W	Address match jump 2
	D6	MA2A14	Address (Upper 8 bits)	A14			0	R/W	does not occur when
	D5	MA2A13		A13			0	R/W	FF75 and FF74 are set
	D4	MA2A12		A12			0	R/W	to 0000H.
	D3	MA2A11		A11			0	R/W	
	D2	MA2A10		A10			0	R/W	
	D1	MA2A09		A09			0	R/W	
	D0	MA2A08		A08			0	R/W	
00FF76	D7	MA3A07	Match address set 3	A07	High	Low	0	R/W	Address match jump 3
	D6	MA3A06	Address (Lower 8 bits)	A06			0	R/W	does not occur when
	D5	MA3A05		A05			0	R/W	FF77 and FF76 are set
	D4	MA3A04		A04			0	R/W	to 0000H.
	D3	MA3A03		A03			0	R/W	
	D2	MA3A02		A02			0	R/W	
	D1	MA3A01		A01			0	R/W	
	D0	MA3A00		A00			0	R/W	
00FF77	D7	MA3A15	Match address set 3	A15	High	Low	0	R/W	Address match jump 3
	D6	MA3A14	Address (Upper 8 bits)	A14			0	R/W	does not occur when
	D5	MA3A13		A13			0	R/W	FF77 and FF76 are set
	D4	MA3A12		A12			0	R/W	to 0000H.
	D3	MA3A11		A11			0	R/W	
	D2	MA3A10		A10			0	R/W	
	D1	MA3A09		A09			0	R/W	
	D0	MA3A08		A08			0	R/W	

MA0A00–MA0A15: Match address register for set 0 (00FF70H, 00FF71H)
MA1A00–MA1A15: Match address register for set 1 (00FF72H, 00FF73H)
MA2A00–MA2A15: Match address register for set 2 (00FF74H, 00FF75H)
MA3A00–MA3A15: Match address register for set 3 (00FF76H, 00FF77H)

Specifies the address that issues address match jump. When the CPU fetches the operation code in the specified address, an address match jump (JP [kk]) is issued. The vector addresses of the four sets are as follows:
Set 0: 2A
Set 1: 2C
Set 2: 2E
Set 3: 30

The jump address must be a logical address in the internal ROM area, and the address must contain the first operation code of an instruction.
The register for an unused set should be fixed at 0000H.
At initial reset, these registers are set to "0000H".

5.17.4 Programming note

The jump address must be a logical address in the internal ROM area, and the address must contain the first operation code of an instruction. Be aware that the program will run away when an address that contains the second operation code or an operand is set.

5.18 Interrupt and Standby Mode

5.18.1 Types of interrupts

The S1C88408 allows one line of non-maskable interrupt, and 8 systems (19 types) of hardware interrupts.

Non-maskable interrupts (NMI)

- Watchdog timer interrupt (1 type)

NMI is the interrupt that cannot be masked with software. It is accepted prior to all hardware interrupts. However, the watchdog timer can be set by software so that it does not generate NMI. Refer to Section 5.3, "Watchdog Timer", for the control of the watchdog timer.

NMI is exceptionally masked at initial reset and it is not input to the CPU in order to prevent malfunction caused by an NMI generation before setting the system configuration. The masking is released when data is written to the addresses 00FF00H and 00FF01H in the I/O memory.

Hardware interrupts

External interrupts

- K00–K07 input interrupt (1 type)
- K10–K13 input interrupt (4 types)

Internal interrupts

- 16-bit programmable timer 0 interrupt (2 types)
- 16-bit programmable timer 1 interrupt (2 types)
- 8-bit programmable timer interrupt (1 type)
- Serial interface interrupt (3 types)
- LCD controller interrupt (1 type)
- Clock timer interrupt (5 types)

An interrupt factor flag that indicates a generation of the interrupt factor and an interrupt enable register to enable/disable the interrupt request have been provided for each interrupt. By using those, interrupt generation can be controlled by each factor.
In addition, an interrupt priority register has been provided for each system of interrupts and the priority of interrupt processing can be set to 3 levels in each system.
Figure 5.18.1.1 shows the configuration of the interrupt circuit.

Refer to the explanations of the respective peripheral circuits for details of each interrupt.

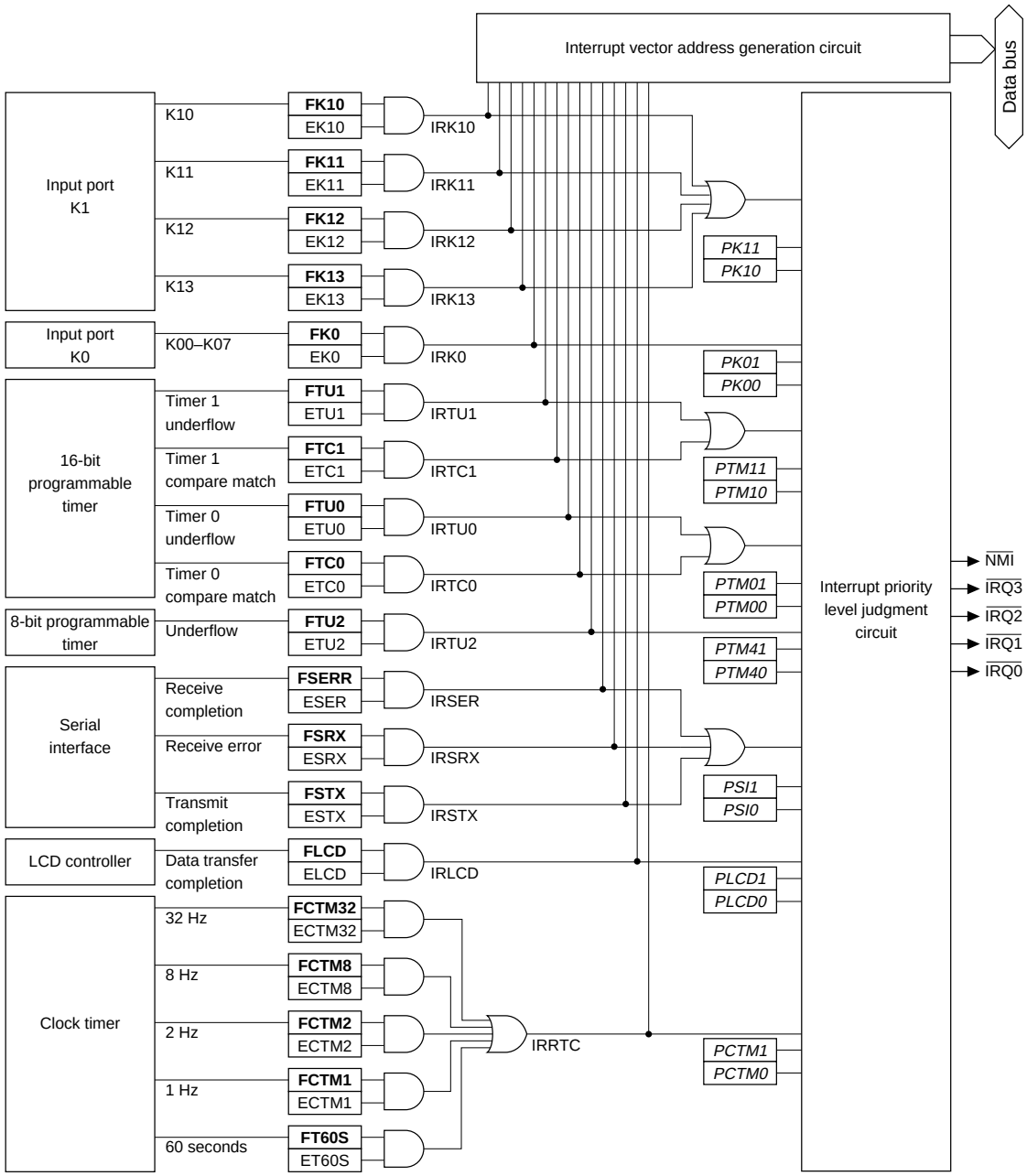


Fig. 5.18.1.1 Configuration of interrupt circuit

5.18.2 Standby mode

The S1C88408 has two standby modes, HALT mode and SLEEP mode, for saving power. The following explains each standby mode.

HALT mode

The S1C88408 enters into HALT mode by executing the HALT instruction.
In HALT mode, the peripheral circuits operate but the CPU stops operating. Thus, saving power can be realized.
HALT mode is canceled by initial reset or an optional interrupt request, and the CPU resumes program execution from the exception processing routine.
Refer to the "S1C88 Core CPU Manual" for HALT status and reactivating sequence.

SLEEP mode

The S1C88408 enters into SLEEP mode by executing the SLP instruction.
In SLEEP mode, the CPU and the oscillation circuits (OSC1 and OSC3) stop operating. Consequently, a greater power saving than HALT mode can be realized.
SLEEP status is canceled by initial reset, NMI or an input interrupt from the input port. The oscillation circuit, that has stopped by shifting to SLEEP mode, resumes oscillating when SLEEP mode is canceled. The CPU resumes program execution from the exception processing routine.

5.18.3 Interrupt generation conditions

For all interrupts (8 systems, 19 types) except for NMI, interrupt factor flags that indicate the generation of the interrupt factors are provided. They are set to "1" when the corresponding interrupt factor is generated.
In addition, interrupt enable registers corresponding to the interrupt factor flags are provided. Writing "1" to the interrupt enable register enables the interrupt to the CPU, and writing "0" disables the interrupt.
The CPU controls interrupt requests with the interrupt priority level. The priority level of each interrupt can be set with the interrupt priority registers, and the CPU accepts only the interrupts which have a level higher than the setting of the interrupt flags (I0 and I1).
Therefore, it is necessary to meet the following three conditions so that the CPU accepts the interrupt.

(1) The interrupt factor flag has been set to "1" by generation of an interrupt factor.

(2) The interrupt enable register corresponding to the interrupt factor has been set to "1".

(3) The interrupt priority register corresponding to the interrupt factor has been set to a priority level higher than the interrupt flag (I0 and I1) setting.

The CPU samples interrupt requests in the first opcode fetch cycle for every instruction, and shifts to exception processing when the above mentioned conditions have been met.
Refer to the "S1C88 Core CPU Manual" for the exception processing sequence.

Table 5.18.3.1 shows the interrupt factors, interrupt enable registers and interrupt priority registers corresponding to the interrupt factors.

Table 5.18.3.1 Interrupt factors and control registers

Interrupt factor		Interrupt factor flag		Interrupt enable register		Interrupt priority register	
		Name	Address·Dx	Name	Address·Dx	Name	Address·Dx
Input port K1	No match between K10 input and input comparison register KCP10	FK10	00FF27H·D4	EK10	00FF23H·D4	PK10 PK11	00FF20H·D6 00FF20H·D7
	No match between K11 input and input comparison register KCP11	FK11	00FF27H·D5	EK11	00FF23H·D5		
	No match between K12 input and input comparison register KCP12	FK12	00FF27H·D6	EK12	00FF23H·D6		
	No match between K13 input and input comparison register KCP13	FK13	00FF27H·D7	EK13	00FF23H·D7		
Input port K0	No match between K0 input (8 bits) and input comparison register KCP0	FK0	00FF27H·D3	EK0	00FF23H·D3	PK00 PK01	00FF20H·D4 00FF20H·D5
16-bit programmable timer	Timer 0 underflow	FTU0	00FF28H·D3	ETU0	00FF24H·D3	PTM00 PTM01	00FF20H·D0 00FF20H·D1
	Compare match between timer 0 and compare data register CDR0	FTC0	00FF28H·D4	ETC0	00FF24H·D4		
	Timer 1 underflow	FTU1	00FF28H·D5	ETU1	00FF24H·D5	PTM10 PTM11	00FF20H·D2 00FF20H·D3
	Compare match between timer 1 and compare data register CDR1	FTC1	00FF28H·D6	ETC1	00FF24H·D6		
8-bit programmable timer	Counter underflow	FTU2	00FF28H·D7	ETU2	00FF24H·D7	PTM20 PTM21	00FF21H·D6 00FF21H·D7
Serial I/F	Receive error	FSERR	00FF28H·D0	ESERR	00FF24H·D0	PSI0 PSI1	00FF21H·D4 00FF21H·D5
	Receive completion	FSRX	00FF28H·D1	ESRX	00FF24H·D1		
	Transmit completion	FSTX	00FF28H·D2	ESTX	00FF24H·D2		
LCD controller	Data transfer completion	FLCD	00FF29H·D2	ELCD	00FF25H·D2	PLCD0 PLCD1	00FF21H·D0 00FF21H·D1
Clock timer	Falling edge of 32 Hz signal	FCTM32	00FF29H·D3	ECTM32	00FF25H·D3	PCTM0 PCTM1	00FF21H·D2 00FF21H·D3
	Falling edge of 8 Hz signal	FCTM8	00FF29H·D4	ECTM8	00FF25H·D4		
	Falling edge of 2 Hz signal	FCTM2	00FF29H·D5	ECTM2	00FF25H·D5		
	Falling edge of 1 Hz signal	FCTM1	00FF29H·D6	ECTM1	00FF25H·D6		
	60S counter overflow	FT60S	00FF29H·D7	ET60S	00FF25H·D7		

5.18.4 Interrupt factor flag

The interrupt factor flag is set to "1" when the corresponding interrupt factor generates.
By reading the interrupt factor flag, it is possible to confirm the interrupt factor that has been generated.
Interrupt factor flag that has been set to "1" is reset to "0" by writing "1".
At initial reset, all the interrupt factor flags are reset to "0".

Note: When the RETE instruction is executed without resetting the interrupt factor flag after an interrupt has been generated, the same interrupt is generated again. Therefore, the interrupt factor flag must be reset (writing "1") in the interrupt handler routine.

5.18.5 Interrupt enable register

The interrupt enable registers corresponding to all interrupt factor flags are provided to enable / disable the interrupt requests to the CPU.
When "1" is written to the interrupt enable register, the interrupt request is enabled and when "0" is written, it is disabled. This register can also be read, thus making it possible to confirm the setting status.
At initial reset, all the interrupt enable registers are set to "0" and all the interrupts except for NMI are disabled.

5.18.6 Interrupt priority register and interrupt priority level

Each interrupt system provides the interrupt priority register shown in Table 5.18.3.1. By using the interrupt priority register, the priority of each interrupt can be changed so that the CPU can process interrupt in order of priority. Consequently, it is possible to make a multiple interrupt system that meets the demand of the application.

The priority level of each interrupt system can be optionally set to four levels (0 to 3) by the interrupt priority register. However, when two or more systems are set to the same priority level, they are processed according to the default priority level.

Table 5.18.6.1 Setting of interrupt priority level

P*1	P*0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, all the interrupt priority registers are set to "0" and all interrupts are set to level 0. Furthermore, the priorities inside of each system have been previously decided and they cannot be changed.

The CPU can mask each interrupt by setting the interrupt flags (I0 and I1). The relation between the interrupt priority level of each system and interrupt flags is shown in Table 5.18.6.2. The CPU accepts only interrupts set in a higher level than the interrupt flag setting.
The priority level of NMI (watchdog timer) is set in level 4, so it is always accepted regardless of the interrupt flag setting.

Table 5.18.6.2 Interrupt mask setting for CPU

I1	I0	Acceptable interrupt
1	1	Level 4 ($\overline{NMI}$)
1	0	Level 4, Level 3 ($\overline{IRQ3}$)
0	1	Level 4, Level 3, Level 2 ($\overline{IRQ2}$)
0	0	Level 4, Level 3, Level 2, Level 1 ($\overline{IRQ1}$)

After an interrupt is accepted, the interrupt flags are changed to the same level of the interrupt accepted as shown in Table 5.18.6.3 in order to mask interrupt requests with the same priority level or less. However, it is set to level 3 after an NMI is accepted.

Table 5.18.6.3 Interrupt flags after acceptance of interrupt

Accepted interrupt priority level	I1	I0
Level 4 ($\overline{NMI}$)	1	1
Level 3 ($\overline{IRQ3}$)	1	1
Level 2 ($\overline{IRQ2}$)	1	0
Level 1 ($\overline{IRQ1}$)	0	1

The interrupt flags changed are returned to the previous value at return from the interrupt handler routine.
Multiple interrupts up to 3 levels can be controlled by only setting the interrupt priority registers.
Multiple interrupts exceeding 3 levels can be realized by rewriting the interrupt flags and interrupt enable register in the interrupt handler routine.

Note: Be aware if the interrupt flags are rewritten (set to lower priority) prior to resetting the interrupt factor flag after an interrupt is generated, the same interrupt will be generated again.

5.18.7 Exception processing vectors

When the CPU accepts an interrupt request, it starts exception processing immediately after completing the instruction being executed. The CPU executes the following sequence as an exception processing for branching the program.

(1) In the minimum mode, the program counter (PC) and system condition flag (SC) are saved in the stack. In the maximum mode, the code bank register (CB), PC and SC are saved.

(2) The branch destination address is read from the exception processing vector corresponding to each exception processing (interrupt) factor and is set in the PC.

Exception processing vector is a 2-byte data to address the top of each exception (interrupt) handler routine. The vector addresses correspond to the exception processing factors as shown in Table 5.18.7.1.

Note: An exception processing vector is fixed at 2 bytes, so it cannot specify a branch destination bank address. Therefore, to branch from two or more banks to a common exception handler routine, the top portion of the exception handler routine must be described within the common area (000000H–007FFFH).

Table 5.18.7.1 Vector address and exception processing vector

Vector address	Symbol	Exception processing factor		Priority
000000H	RESET	Reset		High ↑
000002H	ZDIV	Zero division		
000004H	NMI	NMI (Watchdog timer)		
000006H	IRK10	Input port K1	K10 input interrupt	
000008H	IRK11		K11 input interrup	
00000AH	IRK12		K12 input interrup	
00000CH	IRK13		K13 input interrup	
00000EH	IRK0	Input port K0	K00–K07 input interrup	
000010H	IRTU0	16-bit programmable timer 0	Underflow interrupt	
000012H	IRTC0		Compare match interrupt	
000014H	IRTU1	16-bit programmable timer 1	Underflow interrupt	
000016H	IRTC1		Compare match interrupt	
000018H	IRTU2	8-bit programmable timer	Underflow interrupt	
00001AH	IRSER	Serial interface	Receive error interrupt	
00001CH	IRSRX		Receive completion interrupt	
00001EH	IRSTX		Receive error interrupt	
000024H	IRLCD	LCD controller	Data transfer completion interrupt	↓
000028H	IRRTC	Clock timer	32Hz/8Hz/2Hz/1Hz/60S interrupt	Low
000032H	–	System reserved (cannot be used)		No Priority rating
000034H ↓ 0000FEH	–	Software interrupt		

5.18.8 I/O memory of interrupt

Table 5.18.8.1 shows the interrupt control bits.

Table 5.18.8.1(a) Interrupt control bits

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF20	D7	PK11	K10–K13	PK11	PK10	0	R/W	
	D6	PK10	interrupt priority register	PK01	PK00	0	R/W	
	D5	PK01	K00–K07	PTM11	PTM10	0	R/W	
	D4	PK00	interrupt priority register	PTM01	PTM00	0	R/W	
	D3	PTM11	16-bit programmable timer 1	1	1	0	R/W	
	D2	PTM10	interrupt priority register	1	0	0	R/W	
	D1	PTM01	16-bit programmable timer 0	0	1	0	R/W	
	D0	PTM00	interrupt priority register	0	0	0	R/W	
00FF21	D7	PTM21	8-bit programmable timer	PTM21	PTM20	0	R/W	
	D6	PTM20	interrupt priority register	PSI1	PSI0	0	R/W	
	D5	PSI1	Serial interface	PCTM1	PCTM0	0	R/W	
	D4	PSI0	interrupt priority register	PLCD1	PLCD0	0	R/W	
	D3	PCTM1	Clock timer	1	1	0	R/W	
	D2	PCTM0	interrupt priority register	1	0	0	R/W	
	D1	PLCD1	LCD controller	0	1	0	R/W	
	D0	PLCD0	interrupt priority register	0	0	0	R/W	
00FF23	D7	EK13	K13 interrupt enable register			0	R/W	
	D6	EK12	K12 interrupt enable register			0	R/W	
	D5	EK11	K11 interrupt enable register			0	R/W	
	D4	EK10	K10 interrupt enable register	Interrupt is	Interrupt is	0	R/W	
	D3	EK0	K00–K07 interrupt enable register	enabled	disabled	0	R/W	
	D2	–	–			–	–	"0" when being read
	D1	–	–			–	–	
	D0	–	–			–	–	
00FF24	D7	ETU2	8-bit programmable timer underflow interrupt enable register			0	R/W	
	D6	ETC1	16-bit programmable timer 1 compare match interrupt enable register			0	R/W	
	D5	ETU1	16-bit programmable timer 1 underflow interrupt enable register			0	R/W	
	D4	ETC0	16-bit programmable timer 0 compare match interrupt enable register	Interrupt is	Interrupt is	0	R/W	
	D3	ETU0	16-bit programmable timer 0 underflow interrupt enable register	enabled	disabled	0	R/W	
	D2	ESTX	Serial interface transmit completion interrupt enable register			0	R/W	
	D1	ESRX	Serial interface receive completion interrupt enable register			0	R/W	
	D0	ESERR	Serial interface receive error interrupt enable register			0	R/W	
00FF25	D7	ET60S	Clock timer 60 S interrupt enable register			0	R/W	
	D6	ECTM1	Clock timer 1 Hz interrupt enable register			0	R/W	
	D5	ECTM2	Clock timer 2 Hz interrupt enable register			0	R/W	
	D4	ECTM8	Clock timer 8 Hz interrupt enable register	Interrupt is	Interrupt is	0	R/W	
	D3	ECTM32	Clock timer 32 Hz interrupt enable register	enabled	disabled	0	R/W	
	D2	ELCD	LCD controller interrupt enable register			0	R/W	
	D1	–	–			–	–	"0" when being read
	D0	–	–			–	–	
00FF27	D7	FK13	K13 interrupt factor flag	(R)	(R)	0	R/(W)	
	D6	FK12	K12 interrupt factor flag	Interrupt	Interrupt	0	R/(W)	
	D5	FK11	K11 interrupt factor flag	factor has	factor has not	0	R/(W)	
	D4	FK10	K10 interrupt factor flag	generated	generated	0	R/(W)	
	D3	FK0	K00–K07 interrupt factor flag			0	R/(W)	
	D2	–	–	(W)	(W)	–	–	"0" when being read
	D1	–	–	Reset	Invalid	–	–	
	D0	–	–			–	–	

Table 5.18.8.1(b) Interrupt control bits

Address	Bit	Name	Function	1	0	Init	R/W	Comment
00FF28	D7	FTU2	8-bit programmable timer underflow interrupt factor flag	(R) Interrupt factor has generated / (W) Reset	(R) Interrupt factor has not generated / (W) Invalid	0	R/(W)	
	D6	FTC1	16-bit programmable timer 1 compare match interrupt factor flag			0	R/(W)	
	D5	FTU1	16-bit programmable timer 1 underflow interrupt factor flag			0	R/(W)	
	D4	FTC0	16-bit programmable timer 0 compare match interrupt factor flag			0	R/(W)	
	D3	FTU0	16-bit programmable timer 0 underflow interrupt factor flag			0	R/(W)	
	D2	FSTX	Serial interface transmit completion interrupt factor flag			0	R/(W)	
	D1	FSRX	Serial interface receive completion interrupt factor flag			0	R/(W)	
	D0	FSERR	Serial interface receive error interrupt factor flag			0	R/(W)	
00FF29	D7	FT60S	Clock timer 60 S interrupt factor flag	(R) Interrupt factor has generated / (W) Reset	(R) Interrupt factor has not generated / (W) Invalid	0	R/(W)	
	D6	FCTM1	Clock timer 1 Hz interrupt factor flag			0	R/(W)	
	D5	FCTM2	Clock timer 2 Hz interrupt factor flag			0	R/(W)	
	D4	FCTM8	Clock timer 8 Hz interrupt factor flag			0	R/(W)	
	D3	FCTM32	Clock timer 32 Hz interrupt factor flag			0	R/(W)	
	D2	FLCD	LCD controller interrupt factor flag			0	R/(W)	
	D1	–	–			–	–	"0" when being read
	D0	–	–			–	–	
00FF53	D7	WRWD	EWD, WDCL write enable	Write enable	Write disable	0	R/W	∗1
	D6	EWD	Watchdog timer NMI enable	NMI enable	NMI disable	1	R/W	∗1
	D5	WDCL	Watchdog timer input clock selection	f_{OSC3}/16	f_{OSC1}/16	0	R/W	∗1
	D4	–	–	–	–	–	–	"0" when being read
	D3	–	–	–	–	–	–	
	D2	–	–	–	–	–	–	
	D1	–	–	–	–	–	–	
	D0	WDRST	Watchdog timer reset	Reset	Invalid	–	W	
00FFC0	D7	SIK07	K07 interrupt selection register	Interrupt is enabled	Interrupt is disabled	0	R/W	
	D6	SIK06	K06 interrupt selection register			0	R/W	
	D5	SIK05	K05 interrupt selection register			0	R/W	
	D4	SIK04	K04 interrupt selection register			0	R/W	
	D3	SIK03	K03 interrupt selection register			0	R/W	
	D2	SIK02	K02 interrupt selection register			0	R/W	
	D1	SIK01	K01 interrupt selection register			0	R/W	
	D0	SIK00	K00 interrupt selection register			0	R/W	
00FFC1	D7	KCP07	K07 input comparison register	Falling edge generates interrupt	Rising edge generates interrupt	1	R/W	
	D6	KCP06	K06 input comparison register			1	R/W	
	D5	KCP05	K05 input comparison register			1	R/W	
	D4	KCP04	K04 input comparison register			1	R/W	
	D3	KCP03	K03 input comparison register			1	R/W	
	D2	KCP02	K02 input comparison register			1	R/W	
	D1	KCP01	K01 input comparison register			1	R/W	
	D0	KCP00	K00 input comparison register			1	R/W	
00FFC2	D7	–	–	–	–	–	–	"0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	KCP13	K13 input comparison register	Falling edge generates interrupt	Rising edge generates interrupt	1	R/W	
	D2	KCP12	K12 input comparison register			1	R/W	
	D1	KCP11	K11 input comparison register			1	R/W	
	D0	KCP10	K10 input comparison register			1	R/W	

∗1 Writing to EWD or WDCL is valid after "1" is written to WRWD. WRWD is automatically returns to "0" after writing to EWD or WDCL.

Refer to the explanations on the respective peripheral circuits for the setting contents and control for each bit.

5.18.9 Programming notes

(1) When the RETE instruction is executed without resetting the interrupt factor flag after an interrupt has been generated, the same interrupt is generated again. Therefore, the interrupt factor flag must be reset (writing "1") in the interrupt handler routine.

(2) Be aware if the interrupt flags (I0, I1) are rewritten (set to lower priority) prior to resetting the interrupt factor flag after an interrupt is generated, the same interrupt will be generated again.

(3) An exception processing vector is fixed at 2 bytes, so it cannot specify a branch destination bank address. Therefore, to branch from two or more banks to a common exception handler routine, the top portion of the exception handler routine must be described within the common area (000000H–007FFFH).

CHAPTER 6 SUMMARY OF NOTES

6.1 Notes for Low Current Consumption

The S1C88408 can turn circuits, which consume a large amount of power, ON or OFF by the control registers.
These control registers lower the current consumption through programs that operate the circuits at the minimum levels. Table 6.1.1 shows the circuits and the control registers (instructions).
Refer to Chapter 8, "ELECTRICAL CHARACTERISTICS" for the current consumption.

Table 6.1.1 Circuits and control registers

Circuit	Control register/instruction	Status at initial reset
CPU	HALT and SLP instructions	Operating
Oscillation circuit	CLKCHG, OSCC	OSC1 clock (CLKCHG="0") OSC3 oscillation OFF (OSCC="0")
Operating voltage V_{D1}	VD1C	2.4 V (VD1C="00B")
SVD circuit	SVDON	OFF status (SVDON="0")

6.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

System controller and bus control

After initial reset, all the interrupts including NMI are masked until the appropriate values are written to the I/O memory addresses "00FF00H" and "00FF01H" to prevent malfunctions that may occur before setting the system configuration. Therefore, write data to the addresses in the initial routine even though the initial settings are used. Furthermore, set the stack pointer SP prior to writing so that interrupt processing will operate normally.

Watchdog timer

(1) When the watchdog timer NMI is authorized, it is necessary to reset the counter by software before an overflow is generated.

(2) At initial reset, the watchdog timer starts counting by inputting the f_{OSC1}/16 clock and is set to generate NMI. When the watchdog timer is not used, write "0" to the EWD register before the first overflow is generated.

(3) The count operation is continued even when the EWD register is set to "0" if the clock is input. Therefore, when NMI is invalidated temporarily, reset the watchdog timer before changing back the EWD register to "1".

(4) The oscillation clock becomes unstable immediately after SLEEP is canceled. Therefore, reset the watchdog timer before shifting to SLEEP status and after SLEEP status is canceled so that an unnecessary NMI will not be generated.

Oscillation circuit

(1) The V_{D1} level must be switched while the OSC3 oscillation circuit is off (before turning on and after turning off). Switching during operation may cause malfunction.
Furthermore, the V_{D1} voltage required at least 5 msec of voltage stabilizing time after switching. Do not turn the OSC3 oscillation circuit on during this period.

(2) V_{D1} cannot be switched directly to a level that is two or three levels different from the current level. The middle level must be set between the switching.
To switch from 1,6 (3.2) V to 3.2 (1.6) V:
1.6 V → 2.4 V → 3.2 V
1.6 V ← 2.4 V ← 3.2 V
To switch from 2.4 (3.2) V to 3.2 (2.4) V:
2.4 V → 3.2 V
2.4 V ← 3.2 V
A 5 msec interval is required for each switching steps.

(3) To generate V_{D1} with specified voltage, the supply voltage must be higher than the specified voltage.
To prevent malfunction, make sure that the supply voltage is not lowered under the V_{D1} value to be set using the SVD circuit before switching V_{D1}. Do not switch V_{D1} to a voltage higher than the supply voltage if the supply voltage drops.

(4) The OSC3 oscillation circuit takes a maximum 20 msec for stabilizing oscillation after turning the OSC3 oscillation circuit on. Therefore, take an enough interval after the OSC3 oscillation goes on before starting control of the peripheral circuit, such as the programmable timer, serial interface and LCD controller, that uses the OSC3 oscillation circuit as the clock source. (The oscillation start time varies depending on the oscillator and external component to be used. Refer to Chapter 8, "ELECTRICAL CHARACTERISTICS", in which an example of oscillation start time is indicated.)

(5) Use a separate instruction for switching the clock from OSC3 to OSC1 and turning the OSC3 oscillation off. Handling with one instruction may cause malfunction of the CPU.

(6) To prevent malfunction, before stopping the OSC3 oscillation, stop the operation of the peripheral circuits that use the OSC3 oscillation circuit as the clock source, such as programmable timer, serial interface and LCD controller.

(7) Do not turn the OSC3 oscillation circuit on to reduce current consumption when the OSC3 clock is not necessary.

Prescaler

When using an output clock from the OSC3 prescaler, it is necessary to turn the OSC3 oscillation circuit on. Furthermore, the OSC3 oscillation circuit takes a maximum 20 msec for stabilizing oscillation after turning the OSC3 oscillation circuit on. Therefore, wait a long enough interval after the OSC3 oscillation goes on before turning the clock output of the OSC3 prescaler on. (The oscillation start time varies depending on the oscillator and external components to be used. Refer to Chapter 8, "ELECTRICAL CHARACTERISTICS", in which an example of oscillation start time is indicated.)

Input port (K port)
I/O port (P port)

When the input terminal is changed from a low level to a high level by the built-in pull-up resistor, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and load capacitance of the terminal. Hence, when reading the input port, it is necessary to wait an appropriate amount of time. Particular care must be taken of the key scan for the key matrix configuration. Make this waiting time the amount of time or more calculated by the following expression.

Waiting time = $R_{IN} \times (C_{IN} + C_L) \times 1.6$ [sec]

R_{IN}: Pull-up resistance Max. value
C_{IN}: Terminal capacitance Max. value
C_L: Load capacitance on the board

Clock output

(1) The FOUT3 clock and TOUT0 clock cannot be output simultaneously, because they use the same port, similar to the FOUT1 clock and TOUT1 clock.

(2) Be aware that the output is fixed at low (V_{SS}) level when the data register of the output port used for the clock output is set to "0".

(3) A hazard may occur on the output signal when the clock output control register is changed.

(4) Since the output clock becomes unstable when SLEEP mode is canceled, stop the output before shifting to SLEEP mode.

LCD controller

(1) Do not write "0" to the LCDEN register while the LCD panel is ON. The LCD panel may be damaged.

(2) Only the 4-bit continuous data refresh mode is available in the gray-scale mode. Do not use 8-bit data transfer or another transfer mode.

(3) The data transfer uses the OSC3 clock. Therefore, turn the OSC3 oscillation on before writing "1" to the LCDEN register. Furthermore, wait 20 msec or more after turning the OSC3 oscillation on for stabilizing oscillation. In the one-shot transfer mode or hardware auto-transfer mode, do not turn the OSC3 oscillation off before finishing data transfer. When the segment driver is in self-refresh status, the OSC3 oscillation can be stopped to reduce current consumption.

(4) When setting the CPU in SLEEP status, be sure to turn the LCD panel power off and stop operation of the LCD controller.

Clock timer

(1) The clock timer actually entqzs into RUN or STOP status at the falling edge of the 256 Hz signal after writing to the TMRUN register. Consequently, when "0" is written to TMRUN, the timer stops after counting once more (+1). TMRUN is read as "1" until the timer actually stops.
Figure 6.2.1 shows the timing chart at the RUN / STOP control.

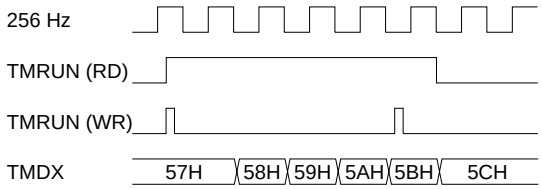


Fig. 6.2.1 Timing chart at RUN/STOP control

(2) The 60-second counter is preset only when data is written to the TMMD register. The register does not maintain the preset data and returns to 0-second when the counter overflows.
To prevent the counter from abnormal operation, do not preset data without a range of 0 to 59 (BCD).

16-bit programmable timer

(1) The 16-bit programmable timer actually enters into RUN or STOP status at the falling edge of the input clock after writing to the PTRUN0(1) register. Consequently, when "0" is written to PTRUN0(1), the timer stops after counting once more (+1). PTRUN0(1) is read as "1" until the timer actually stops.
Figure 6.2.2 shows the timing chart at the RUN / STOP control.

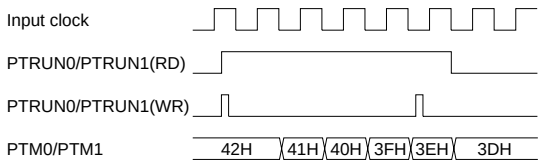


Fig. 6.2.2 Timing chart at RUN/STOP control

(2) When the SLP instruction is executed while the 16-bit programmable timer is running (PTRUN0(1) = "1"), the timer stops counting during SLEEP status. When SLEEP status is canceled, the timer starts counting. However, the operation becomes unstable immediately after SLEEP status is canceled. Therefore, when shifting to SLEEP status, stop the 16-bit programmable timer (PTRUN0(1) = "0") prior to executing the SLP instruction. Same as above, the TOUT signal output should be disabled (PTOUT0(1) = "0") so that an unstable clock is not output to the clock output port terminal.

(3) In the 16-bit mode, reading PTM0 does not latch the timer 1 counter data in PTM1. To avoid generating a borrow from timer 0 to timer 1, read the counter data after stopping the timer by writing "0" to PTRUN0.

8-bit programmable timer

(1) The 8-bit programmable timer actually enters into RUN or STOP status at the falling edge of the input clock after writing to the PRUN register. Consequently, when "0" is written to PRUN, the timer stops after counting once more (+1). PRUN is read as "1" until the timer actually stops.
Figure 6.2.3 shows the timing chart of the RUN / STOP control.

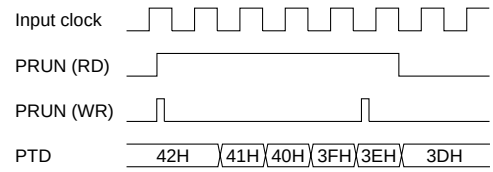


Fig. 6.2.3 Timing chart at RUN/STOP control

(2) When the SLP instruction is executed while the 8-bit programmable timer is running (PRUN = "1"), the timer stops counting during SLEEP status. When SLEEP status is canceled, the timer starts counting. However, the operation becomes unstable immediately after SLEEP status is canceled. Therefore, when shifting to SLEEP status, stop the 8-bit programmable timer (PRUN = "0") prior to executing the SLP instruction.

(3) The prescaler, which supplies the clock to the 8-bit programmable timer, can operate only when the OSC3 oscillation has been set to ON. Be aware that the 8-bit programmable timer does not operate when the OSC3 oscillation circuit has been turned off.

Serial interface

(1) Setting of the serial interface mode must be done in the transmission / receiving disabling status (TXEN = RXEN = "0").

(2) Do not perform double trigger (writing "1") to TXTRG (RXTRG) during transmission (receiving). Furthermore, do not execute the SLP instruction. (When executing the SLP instruction, set TXEN and RXEN to "0".)

(3) Transmission and receiving cannot be done simultaneously in the clock synchronous mode because the clock line ($\overline{SCLK}$) is shared with transmit and receive operation. Therefore, do not write "1" to RXTRG (TXTRG) when TXTRG (RXTRG) is "1".

(4) When a parity error or a framing error occurs, both the receive error interrupt factor flag FSERR and the receive completion interrupt factor flag FSRX are simultaneously set to "1". However, since the receive error interrupt has priority over the receive completion interrupt, the receive error interrupt process is executed first. Therefore, it is necessary to reset the FSRX flag in the receive error handling routine. When a receive error interrupt occurs due to an overrun, receive completion interrupt does not occur.

Sound generator

(1) Since the BZ signal is generated asynchronously from the register BZON, when the signal is turned ON or OFF by the register setting, a hazard of a 1/2 cycle or less is generated.

(2) The SLP instruction has executed when the BZ signal is in the enable status (BZON = "1" or BZSHT = "1"), an unstable clock is output from the R42 output port terminal at the time of return from the SLEEP status. Consequently, when shifting to the SLEEP status, you should set the BZ signal to the disable status (BZON = BZSHT = "0") prior to executing the SLP instruction.

(3) The one-shot output is only valid when the normal buzzer output is OFF (BZON = "0") status. The trigger is invalid during ON (BZON = "1") status.

SVD circuit

(1) To obtain a stable detection result, the SVD circuit must be ON for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 100 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

(2) The SVD operation increases current consumption, so turn the SVD circuit off when voltage detection is unnecessary or executing the SLP instruction.

Address match jump

The jump address must be a logical address in the internal ROM area, and the address must contain the first operation code of an instruction. Be aware that the program will run away when an address that contains the second operation code or an operand is set.

Interrupt

(1) When the RETE instruction is executed without resetting the interrupt factor flag after an interrupt has been generated, the same interrupt is generated again. Therefore, the interrupt factor flag must be reset (writing "1") in the interrupt handler routine.

(2) Be aware if the interrupt flags (I0, I1) are rewritten (set to lower priority) prior to resetting the interrupt factor flag after an interrupt is generated, the same interrupt will be generated again.

(3) An exception processing vector is fixed at 2 bytes, so it cannot specify a branch destination bank address. Therefore, to branch from two or more banks to a common exception handler routine, the top portion of the exception handler routine must be described within the common area (000000H–007FFFH).

6.3 Precautions on Mounting

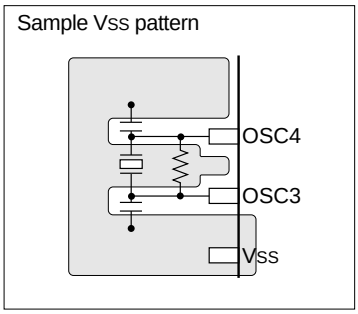
<Oscillation Circuit>

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.).
  In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.

- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC1, OSC2, OSC3, OSC4 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.

  (2) As shown in the right hand figure, make a VSS pattern as large as possible at circumscription of the OSC1, OSC2, OSC3, OSC4 terminals and the components connected to these terminals.
  Furthermore, do not use this VSS pattern for any purpose other than the oscillation system.



  (3) When supplying an external clock to the OSC1 (OSC3) terminal, the clock source should be connected to the OSC1 (OSC3) terminal in the shortest line.
  Furthermore, do not connect anything else to the OSC2 (OSC4) terminal.

- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC3 and VDD, please keep enough distance between OSC3 and VDD or other signals on the board pattern.

<Reset Circuit>

- The power-on reset signal which is input to the $\overline{\text{RESET}}$ terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
  Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product.
  When the built-in pull-up resistor is added to the $\overline{\text{RESET}}$ terminal by mask option, take into consideration dispersion of the resistance for setting the constant.

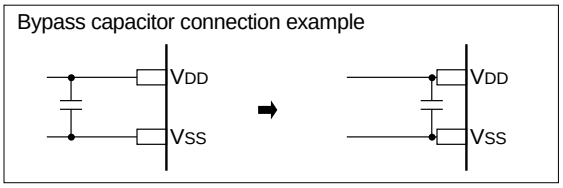
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the $\overline{\text{RESET}}$ terminal in the shortest line.

<Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

(1) The power supply should be connected to the VDD and VSS terminals with patterns as short and large as possible.

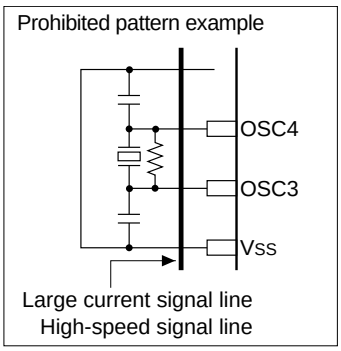
(2) When connecting between the VDD and VSS terminals with a bypass capacitor, the terminals should be connected as short as possible.



<Arrangement of Signal Lines>

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit.

- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction.
  Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit.



<Precautions for Visible Radiation (when bare chip is mounted)>

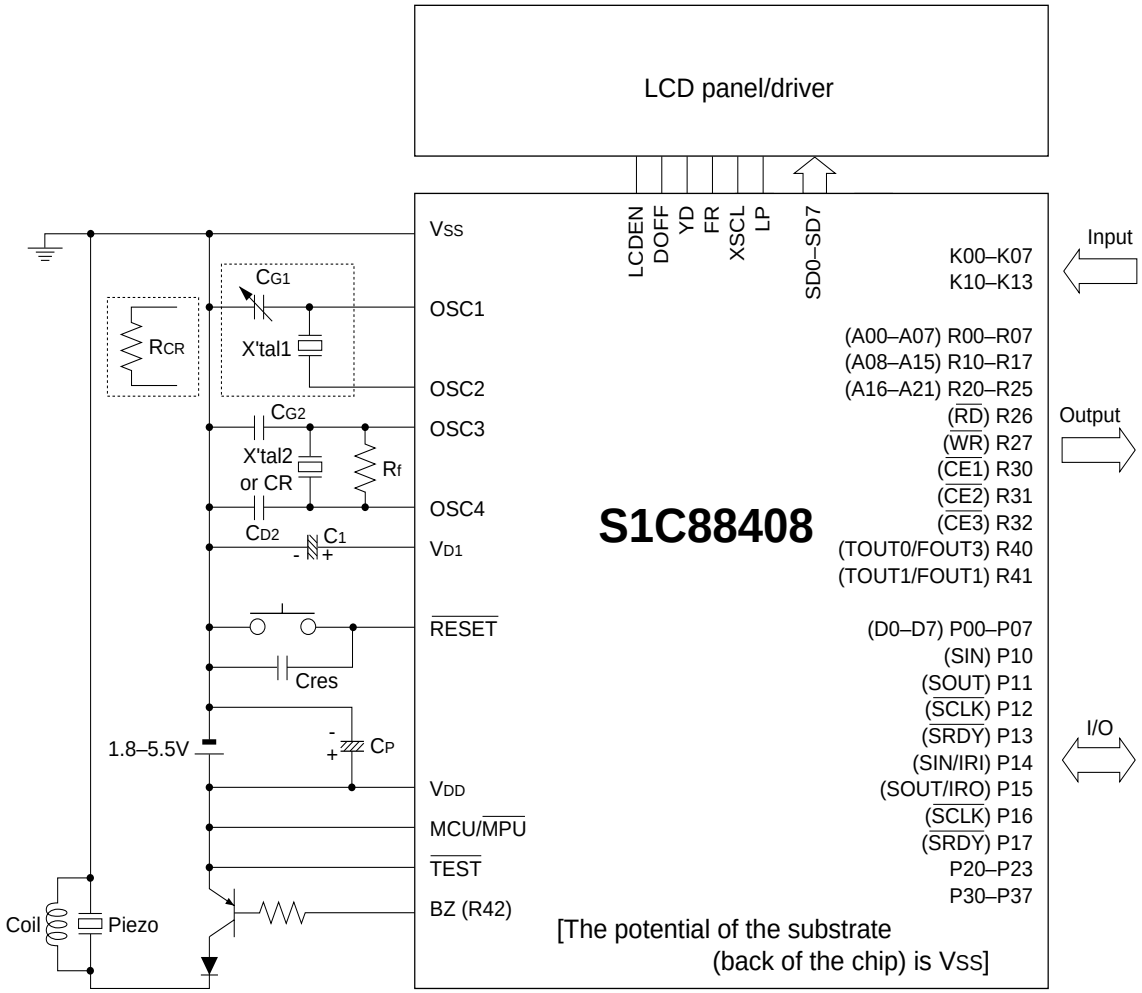
- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

(1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

(2) The inspection process of the product needs an environment that shields the IC from visible radiation.

(3) As well as the face of the IC, shield the back and side too.

CHAPTER 7 BASIC EXTERNAL WIRING DIAGRAM



Recommended values for external parts

Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768 kHz, CI(Max.) = 35 kΩ
R_{CR}	Resistor for CR oscillation	1.8 Ω
X'tal2	Crystal oscillator	4, 6, 8 MHz
CR	Ceramic oscillator	4, 6, 8 MHz
R_f	Feedback resistor	1 MΩ
C_{G1}	Trimmer capacitor	5–25 pF
C_{G2}	Gate capacitor	15 pF
C_{D2}	Drain capacitor	15 pF
C_1	Capacitor between V_{SS} and V_{D1}	0.1 µF
C_P	Capacitor for power supply	3.3 µF
Cres	Capacitor for $\overline{\text{RESET}}$ terminal	0.47 µF

CHAPTER 8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Rating

(V_{SS}=0 V)

Item	Symbol	Condition	Rated value	Unit	Note
Supply voltage	V_{DD}		-0.3 to +0.7	V	
Input voltage	V_I		-0.3 to V_{DD}+0.3	V	
Output voltage	V_O		-0.3 to V_{DD}+0.3	V	
High-level output current	I_{OH}	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Low-level output current	I_{OL}	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Operating temperature	T_{opr}		-20 to +70	°C	
Storage temperature	T_{stg}		-65 to +150	°C	
Permissible disspation	P_D	Ta=25°C	200	mW	1

Note) 1. In case of plastic package.

8.2 Recommended Operating Conditions

(V_{SS}=0 V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Supply voltage	V_{DD}		1.8		5.5	V	
Clock frequency	f_{OSC1}	V_{DD}=1.8 to 5.5 V	30.000	32.768	50.000	kHz	1
	f_{OSC3}	V_{DD}=1.8 to 5.5 V	0.03		1.1	MHz	1
		V_{DD}=2.6 to 5.5 V	0.03		4.4	MHz	1
		V_{DD}=3.5 to 5.5 V	0.03		8.2	MHz	1
Operating temperature	T_{opr}		-20		+70	°C	
Capacitor between V_{SS} and V_{D1}	C_1			0.1		µF	

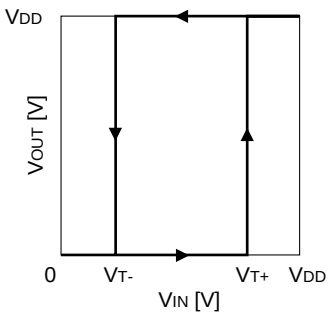
Note) 1. When an external clock is input from the OSC1 terminal by setting the mask option, do not connect anything to the OSC2 terminal. When an external clock is input from the OSC3 terminal, do not connect anything to the OSC4 terminal.

8.3 DC Characteristics

Unless otherwise specified: V_{DD}=1.8 to 5.5 V, V_{SS}=0 V, Ta=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
High-level input voltage	V_{IH1}	Pxx, MCU/$\overline{MPU}$, Kxx	0.8V_{DD}		V_{DD}	V	
Low-level input voltage	V_{IL1}	Pxx, MCU/$\overline{MPU}$, Kxx	0		0.2V_{DD}	V	
High-level input voltage	V_{IH2}	OSC1, OSC3, V_{D1} = 1.6V	1.3		V_{DD}	V	1,3
		OSC1, OSC3, V_{D1} = 2.4V	1.8		V_{DD}	V	1,4
		OSC1, OSC3, V_{D1} = 3.2V	2.4		V_{DD}	V	1,5
Low-level input voltage	V_{IL2}	OSC1, OSC3, V_{D1} = 1.6V	0		0.3	V	1,3
		OSC1, OSC3, V_{D1} = 2.4V	0		0.6	V	1,4
		OSC1, OSC3, V_{D1} = 3.2V	0		0.8	V	1,5
High-level schmitt trigger input voltage	V_{T+}	$\overline{RESET}$	0.5V_{DD}		0.9V_{DD}	V	
Low-level schmitt trigger input voltage	V_{T-}	$\overline{RESET}$	0.1V_{DD}		0.5V_{DD}	V	
Schmitt trigger hysteresis voltage	V_{HS}	$\overline{RESET}$ $V_{HS}=V_{T+}-V_{T-}$	0.2			V	
High-level output current	I_{OH}	Pxx, Rxx, $V_{OH}=V_{DD}$-0.2 V	-0.5			mA	6
Low-level output current	I_{OL}	Pxx, Rxx, V_{OL}=0.2 V			0.5	mA	6
Input leak current	I_{LI1}	Kxx, Pxx, MCU/$\overline{MPU}$, $\overline{RESET}$	-1		1	µA	
Input leak current	I_{LI2}	OSC1, OSC3	-1		1	µA	1
Output leak current	I_{LO}	Pxx, Rxx	-1		1	µA	
Input pull-up resistance	R_{IN}	Kxx, Pxx, MCU/$\overline{MPU}$, $\overline{RESET}$	100		500	kΩ	2
Input terminal capacitance	C_{IN}	Kxx, Pxx V_{IN}=0 V, ϕ=1 MHz, Ta=25°C			15	pF	

Note) 1. When external clock is selected by mask option.
2. When pull-up resistor is added by mask option.
3. Low-power mode (VD1C1 = "0", VD1C0 = "1")
4. Normal mode (VD1C1 = "0", VD1C0 = "0")
5. High-speed mode 1 (VD1C1 = "1", VD1C0 = ×)
6. Characteristics when only one terminal is driven. If two or more terminals are driven simultaneously, the characteristics had happen to reduced because the V_{OH} and V_{OL} voltages drop due to the parasitic resistance on the power line in the IC.



8.4 Analog Circuit Characteristics and Current Consumption

Unless otherwise specified: V_{DD}=1.8 to 5.5 V, V_{SS}=0 V, Ta=25°C, OSC1=32.768 kHz crystal oscillation, OSC3=external clock input

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SVD voltage	V_{SVD}	SVD1="1", SVD0=×	3.05	3.4	3.75	V	
		SVD1="0", SVD0="1"	2.55	2.8	3.05	V	
		SVD1="0", SVD0="0"	1.7	1.9	2.1	V	
SVD circuit response time	t_{SVD}				100	µs	
Power current	I_{DD1}	In SLEEP status		0.45	1.0	µA	1
Low-power mode	I_{DD2}	In HALT status		1.8	5.0	µA	2
VD1C1="0", VD1C0="1"	I_{DD3}	CPU is in operating (32.768 kHz)		9.0	20.0	µA	3
	I_{DD4}	CPU is in operating (1 MHz)		0.3	0.5	mA	4
Power current	I_{DD1}	In SLEEP status		0.55	1.5	µA	1
Normal mode	I_{DD2}	In HALT status		3.0	7.0	µA	2
VD1C1="0", VD1C0="0"	I_{DD3}	CPU is in operating (32.768 kHz)		14.0	25.0	µA	3
	I_{DD4}	CPU is in operating (1 MHz)		0.45	0.7	mA	4
Power current	I_{DD1}	In SLEEP status		0.65	2.0	µA	1
High-speed mode 1	I_{DD2}	In HALT status		5.0	12.0	µA	2
VD1C1="1", VD1C0=×	I_{DD3}	CPU is in operating (32.768 kHz)		21.0	35.0	µA	3
	I_{DD4}	CPU is in operating (1 MHz)		0.65	1.0	mA	4
SVD circuit current	I_{SVDN}	V_{DD}=5.0 V		7	15	µA	5
OSC1 CR oscillation current	I_{CR1}	R_{CR}=1.5 MΩ, normal mode		20	50	µA	6

Note) 1. OSC1: Stop OSC3: Stop CPU, ROM, RAM: Stop Clock Timer: Stop SVD: Off Others: Stop
2. OSC1: On OSC3: Stop CPU, ROM, RAM: Stop Clock Timer: Run SVD: Off Others: Stop
3. OSC1: On OSC3: Stop CPU, ROM, RAM: Run Clock Timer: Run SVD: Off Others: Stop
4. OSC1: On OSC3: On CPU, ROM, RAM: Run Clock Timer: Run SVD: Off Others: Stop
5. OSC1: On OSC3: Stop CPU, ROM, RAM: Stop Clock Timer: Run SVD: On Others: Stop
6. When the OSC1 CR oscillation circuit is selected by mask option.

8.5 AC Characteristics

8.5.1 External memory access

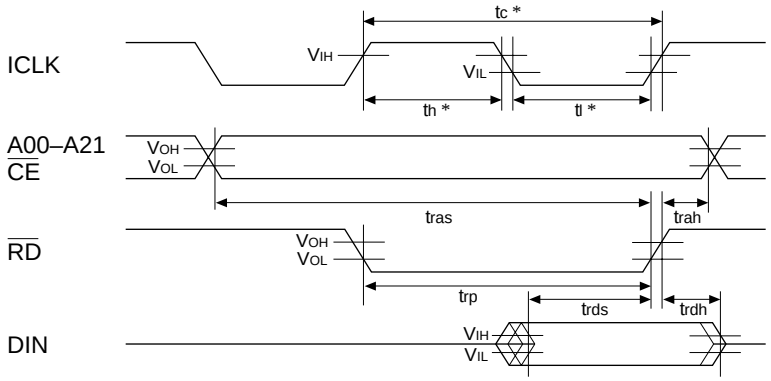
Read cycle

Unless otherwise specified: V_{DD}=5.5 V, V_{SS}=0 V, f_{OSC1}=32.768 kHz, f_{OSC3}=1.0 MHz, Ta=-20 to 70°C, C_L=100 pF, V_{IH}=0.8V_{DD}, V_{IL}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Address set-up time in read cycle	tras	V_{DD}=1.8 to 5.5 V	tc+tl-200+n*tc/2	–	–	ns	1
Address hold time in read cycle	trah	V_{D1}=1.6 V	th-160	–	–	ns	
Read signal pulse width	trp		tc-40+n*tc/2	–	–	ns	1
Data input set-up time in read cycle	trds		600	–	–	ns	
Data input hold time in read cycle	trdh		0	–	–	ns	
Address set-up time in read cycle	tras	V_{DD}=2.6 to 5.5 V	tc+tl-100+n*tc/2	–	–	ns	1
Address hold time in read cycle	trah	V_{D1}=2.4 V	th-80	–	–	ns	
Read signal pulse width	trp		tc-20+n*tc/2	–	–	ns	1
Data input set-up time in read cycle	trds		300	–	–	ns	
Data input hold time in read cycle	trdh		0	–	–	ns	
Address set-up time in read cycle	tras	V_{DD}=3.5 to 5.5 V	tc+tl-50+n*tc/2	–	–	ns	1
Address hold time in read cycle	trah	V_{D1}=3.2 V	th-40	–	–	ns	
Read signal pulse width	trp		tc-10+n*tc/2	–	–	ns	1
Data input set-up time in read cycle	trds		150	–	–	ns	
Data input hold time in read cycle	trdh		0	–	–	ns	

tc=input clock cycle time, th=input clock H pulse width, tl=input clock L pulse width

Note) 1. Substitute the number of states for wait insertion in n.



* In the case of crystal or ceramic oscillation: th=0.5tc±0.05tc, tl=tc-th
In the case of CR oscillation: th=0.5tc±0.10tc, tl=tc-th
(1/tc: oscillation frequency)

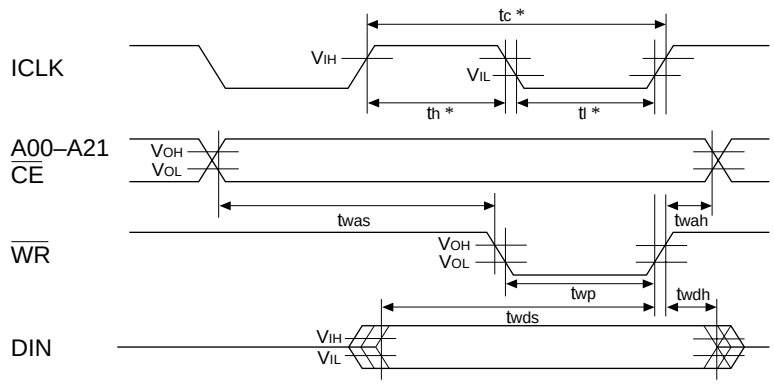
Write cycle

Unless otherwise specified: V_{DD}=5.5 V, V_{SS}=0 V, f_{OSC1}=32.768 kHz, f_{OSC3}=1.0 MHz, Ta=-20 to 70°C, C_L=100 pF,
V_{IH}=0.8V_{DD}, V_{IL}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Address set-up time in write cycle	twas	V_{DD}=1.8 to 5.5 V	tc-360	–	–	ns	
Address hold time in write cycle	twah	V_{D1}=1.6 V	th-160	–	–	ns	
Write signal pulse width	twp		tl-80+n*tc/2	–	–	ns	1
Data output set-up time in write cycle	twds		tc-360+n*tc/2	–	–	ns	1
Data output hold time in write cycle	twdh		th-160	–	th+160	ns	
Address set-up time in write cycle	twas	V_{DD}=2.6 to 5.5 V	tc-180	–	–	ns	
Address hold time in write cycle	twah	V_{D1}=2.4 V	th-80	–	–	ns	
Write signal pulse width	twp		tl-40+n*tc/2	–	–	ns	1
Data output set-up time in write cycle	twds		tc-180+n*tc/2	–	–	ns	1
Data output hold time in write cycle	twdh		th-160	–	th+160	ns	
Address set-up time in write cycle	twas	V_{DD}=3.5 to 5.5 V	tc-90	–	–	ns	
Address hold time in write cycle	twah	V_{D1}=3.2 V	th-40	–	–	ns	
Write signal pulse width	twp		tl-20+n*tc/2	–	–	ns	1
Data output set-up time in write cycle	twds		tc-90+n*tc/2	–	–	ns	1
Data output hold time in write cycle	twdh		th-160	–	th+160	ns	

tc=input clock cycle time, th=input clock H pulse width, tl=input clock L pulse width

Note) 1. Substitute the number of states for wait insertion in n.



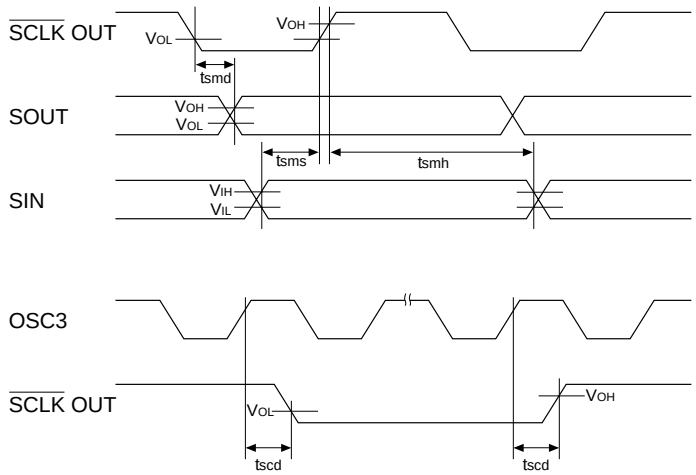
∗ In the case of crystal or ceramic oscillation: th=0.5tc±0.05tc, tl=tc-th
In the case of CR oscillation: th=0.5tc±0.10tc, tl=tc-th
(1/tc: oscillation frequency)

8.5.2 Serial interface

Clock synchronous master mode

Unless otherwise specified: V_{DD}=5.5 V, V_{SS}=0 V, f_{OSC1}=32.768 kHz, f_{OSC3}=100 kHz, Ta=-20 to 70°C, C_L=100 pF, V_{IH}=0.8V_{DD}, V_{IL}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

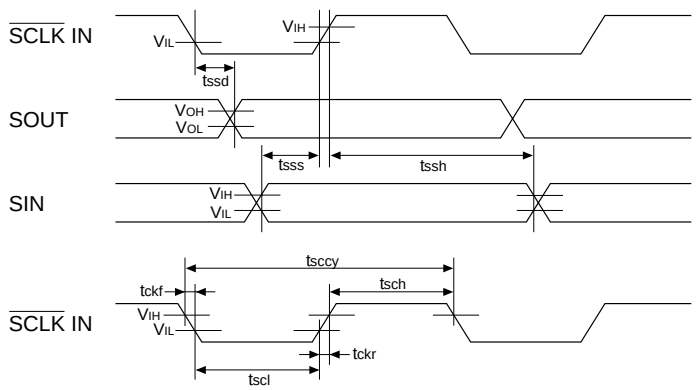
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmit data output delay time	tsmd	V_{DD}=1.8 to 5.5 V	–	–	400	ns	
Receive data input set-up time	tsms	V_{D1}=1.6 V	1000	–	–	ns	
Receive data input hold time	tsmh		400	–	–	ns	
Transmit data output delay time	tsmd	V_{DD}=2.6 to 5.5 V	–	–	200	ns	
Receive data input set-up time	tsms	V_{D1}=2.4 V	500	–	–	ns	
Receive data input hold time	tsmh		200	–	–	ns	
Transmit data output delay time	tsmd	V_{DD}=3.5 to 5.5 V	–	–	100	ns	
Receive data input set-up time	tsms	V_{D1}=3.2 V	250	–	–	ns	
Receive data input hold time	tsmh		100	–	–	ns	



Clock synchronous slave mode

Unless otherwise specified: V_{DD}=5.5 V, V_{SS}=0 V, f_{OSC1}=32.768 kHz, f_{OSC3}=100 kHz, Ta=-20 to 70°C, C_L=100 pF, V_{IH}=0.8V_{DD}, V_{IL}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmit data output delay time	tssd	V_{DD}=1.8 to 5.5 V	–	–	1000	ns	
Receive data input set-up time	tsss	V_{D1}=1.6 V	400	–	–	ns	
Receive data input hold time	tssh	SCKIN=100 kHz	400	–	–	ns	
Transmit data output delay time	tssd	V_{DD}=2.6 to 5.5 V	–	–	500	ns	
Receive data input set-up time	tsss	V_{D1}=2.4 V	200	–	–	ns	
Receive data input hold time	tssh	SCKIN=100 kHz	200	–	–	ns	
Transmit data output delay time	tssd	V_{DD}=3.5 to 5.5 V	–	–	250	ns	
Receive data input set-up time	tsss	V_{D1}=3.2 V	100	–	–	ns	
Receive data input hold time	tssh	SCKIN=100 kHz	100	–	–	ns	



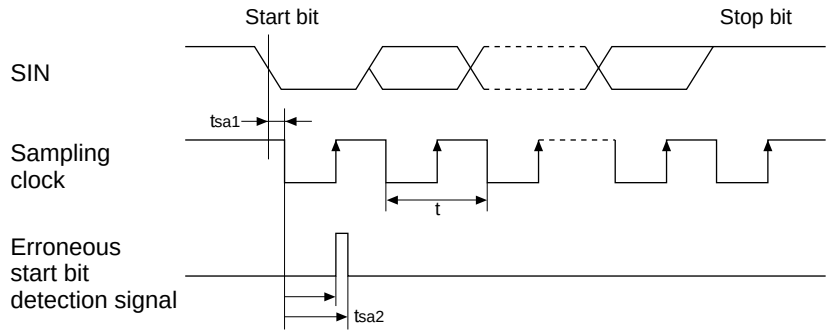
Asynchronous mode

Unless otherwise specified: V_{DD}=1.8 to 5.5 V, V_{SS}=0 V, Ta=-20 to 70°C, V_{IH}=0.7V_{DD}, V_{IL}=0.3V_{DD}, V_{OH}=0.7V_{DD}, V_{OL}=0.3V_{DD}

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Start bit detection error time	t_{sa1}		0	–	t/16	s	1
Erroneous start bit detection range time	t_{sa2}		8t/16	–	9t/16	s	2

Note) 1. Start bit detection error time is a logical delay time from inputting a start bit until the internal sampling starts operating. (AC time is not included.)

2. Erroneous start bit detection range time is a logical time from starting sampling clock (detecting a start bit) until the start bit is detected again whether a low level (start bit) has still been input. When a high level is detected, the start bit detection circuit is reset and goes into a start bit waiting status. (AC time is not included.)

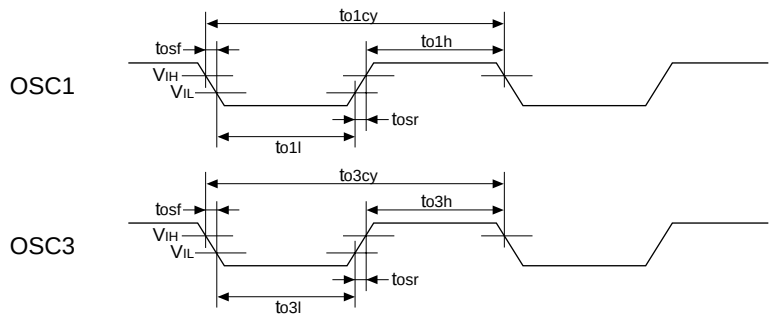


8.5.3 Input clock

OSC1, OSC3 external clock

Unless otherwise specified: V_{SS}=0 V, Ta=-20 to 70°C

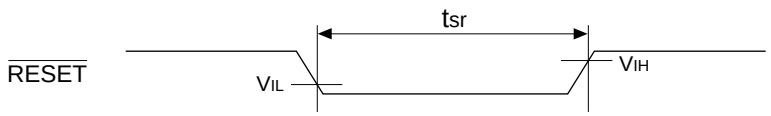
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
OSC1 input clock time	Cycle time	to1cy	V_{DD}=1.8 to 5.5 V	20	–	32	µs	
	"H" pulse width	to1h	V_{D1}=1.6 V	10	–	16	µs	
	"L" pulse width	to1l	V_{IH}=1.3 V	10	–	16	µs	
OSC3 input clock time	Cycle time	to3cy	V_{IL}=0.3 V	1000	–	32000	ns	
	"H" pulse width	to3h		500	–	16000	ns	
	"L" pulse width	to3l		500	–	16000	ns	
Input clock rising time		tosr		–	–	25	ns	
Input clock falling time		tosf		–	–	25	ns	
OSC1 input clock time	Cycle time	to1cy	V_{DD}=2.6 to 5.5 V	20	–	32	µs	
	"H" pulse width	to1h	V_{D1}=2.4 V	10	–	16	µs	
	"L" pulse width	to1l	V_{IH}=1.8 V	10	–	16	µs	
OSC3 input clock time	Cycle time	to3cy	V_{IL}=0.6 V	240	–	32000	ns	
	"H" pulse width	to3h		120	–	16000	ns	
	"L" pulse width	to3l		120	–	16000	ns	
Input clock rising time		tosr		–	–	25	ns	
Input clock falling time		tosf		–	–	25	ns	
OSC1 input clock time	Cycle time	to1cy	V_{DD}=3.5 to 5.5 V	20	–	32	µs	
	"H" pulse width	to1h	V_{D1}=3.2 V	10	–	16	µs	
	"L" pulse width	to1l	V_{IH}=2.4 V	10	–	16	µs	
OSC3 input clock time	Cycle time	to3cy	V_{IL}=0.8 V	155	–	32000	ns	
	"H" pulse width	to3h		77.5	–	16000	ns	
	"L" pulse width	to3l		77.5	–	16000	ns	
Input clock rising time		tosr		–	–	25	ns	
Input clock falling time		tosf		–	–	25	ns	



$\overline{\text{RESET}}$ input clock

Unless otherwise specified: V_{DD}=1.8 to 5.5 V, V_{SS}=0 V, Ta=-20 to 70°C, V_{IH}=0.5V_{DD}, V_{IL}=0.1V_{DD}

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
$\overline{\text{RESET}}$ pulse width	tsr		100	–	–	µs	

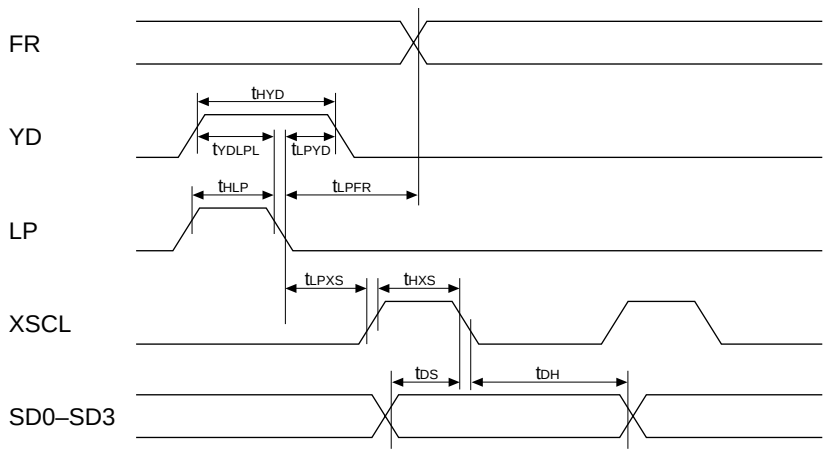


8.5.4 LCD controller

Unless otherwise specified: V_{DD}=5.5 V, V_{SS}=0 V, f_{OSC1}=32.768 kHz, f_{OSC3}=2.0 MHz, Ta=-20 to 70°C, C_L=100 pF, V_{IH}=0.8V_{DD}, V_{IL}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
XSCL H-level pulse width (B&W, 4 bits)	tHXS(1)	V_{DD}=1.8 to 5.5 V	tc-360	–	–	ns	
XSCL H-level pulse width (gray, 4 bits)	tHXS(2)	V_{D1}=1.6 V	tc-tl-360	–	–	ns	
LP falling edge to XSCL rising edge	tLPXS		6*tc-360	–	–	ns	
LCD data setup time	tDS		tc-360	–	–	ns	
LCD data hold time	tDH		tc-360	–	–	ns	
YD H-level pulse width	tHYD		tc(f_{OSC1})-3	–	–	µs	
LP H-level pulse width	tHLP		tl(f_{OSC1})-1.5	–	–	µs	
YD setup time	tYDLPL		tl(f_{OSC1})-1.5	–	–	µs	
YD hold time	tLPYD		th(f_{OSC1})-1.5	–	–	µs	
FR change from LP falling edge	tLPFR		-300	–	300	ns	
XSCL H-level pulse width (B&W, 4 bits)	tHXS(1)	V_{DD}=2.6 to 5.5 V	tc-180	–	–	ns	
XSCL H-level pulse width (gray, 4 bits)	tHXS(2)	V_{D1}=2.4 V	tc-tl-180	–	–	ns	
LP falling edge to XSCL rising edge	tLPXS		6*tc-180	–	–	ns	
LCD data setup time	tDS		tc-180	–	–	ns	
LCD data hold time	tDH		tc-180	–	–	ns	
YD H-level pulse width	tHYD		tc(f_{OSC1})-3	–	–	µs	
LP H-level pulse width	tHLP		tl(f_{OSC1})-1.5	–	–	µs	
YD setup time	tYDLPL		tl(f_{OSC1})-1.5	–	–	µs	
YD hold time	tLPYD		th(f_{OSC1})-1.5	–	–	µs	
FR change from LP falling edge	tLPFR		-200	–	200	ns	
XSCL H-level pulse width (B&W, 4 bits)	tHXS(1)	V_{DD}=3.5 to 5.5 V	tc-90	–	–	ns	
XSCL H-level pulse width (gray, 4 bits)	tHXS(2)	V_{D1}=3.2 V	tc-tl-90	–	–	ns	
LP falling edge to XSCL rising edge	tLPXS		6*tc-90	–	–	ns	
LCD data setup time	tDS		tc-90	–	–	ns	
LCD data hold time	tDH		tc-90	–	–	ns	
YD H-level pulse width	tHYD		tc(f_{OSC1})-3	–	–	µs	
LP H-level pulse width	tHLP		tl(f_{OSC1})-1.5	–	–	µs	
YD setup time	tYDLPL		tl(f_{OSC1})-1.5	–	–	µs	
YD hold time	tLPYD		th(f_{OSC1})-1.5	–	–	µs	
FR change from LP falling edge	tLPFR		-100	–	100	ns	

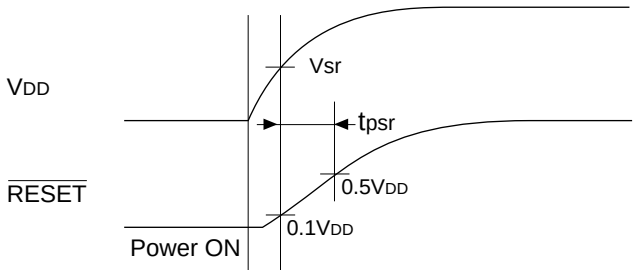
tc=OSC3 clock cycle time, th=OSC3 clock H pulse width, tl=OSC3 clock L pulse width, tc(f_{OSC1})=OSC1 clock cycle time
th(f_{OSC1})=OSC1 clock H pulse width, tl(f_{OSC1})=OSC1 clock L pulse width

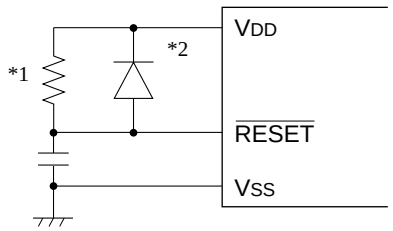


8.5.5 Power-on reset

Unless otherwise specified: V_{SS}=0 V, Ta=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating voltage	V_{sr}		2.6	–	–	V	
$\overline{RESET}$ input width	t_{psr}		10	–	–	ms	





*1 When the built-in pull up resistor is not used.

*2 Because the potential of the $\overline{RESET}$ terminal not reached V_{DD} level or higher.

8.5.6 Switching operating mode

Unless otherwise specified: V_{DD}=1.8 to 5.5 V, V_{SS}=0 V, Ta=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Stabilization time	t_{vdc}		5	–	–	ms	1

Note) 1. Stabilization time is the time from switching on the operating mode until operating mode is stabilized. For example, when turning the OSC3 oscillation circuit on, stabilization time is needed after the operating mode is switched on.

8.6 Oscillation Characteristics

Oscillation characteristics change depending on conditions (board pattern, components used, etc.). Use the following characteristics as reference values. In particular, when a ceramic oscillator or crystal oscillator is used for OSC3, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance. The oscillation start time is important because it becomes the waiting time when OSC3 clock is used. (If OSC3 is used as CPU clock before oscillation stabilizes, the CPU may malfunction.)

OSC1 crystal oscillation

Unless otherwise specified: V_{DD}=1.8 to 5.5 V, V_{SS}=0 V, Ta=25°C,
Crystal oscillator=Q12C2(made by Seiko Epson corporation), C_{G1}=25 pF(External), C_{D1}=Built-in

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				3	s	
External gate capacitance	C_{G1}	Including board capacitance	5		25	pF	1
Built-in drain capacitance	C_{D1}	In case of the chip		15		pF	
Frequency/IC deviation	∂f/∂IC	V_{DD}=constant	-10		10	ppm	
Frequency/supply voltage deviation	∂f/∂V				1	ppm/V	
Frequency adjustment range	∂f/∂C_G	V_{DD}=constant, C_G=5 to 25 pF	25			ppm	
Frequency/operating mode deviation	∂f/∂MD	V_{DD}=constant			20	ppm	

Note) 1. When crystal oscillation is selected by mask option.

OSC1 CR oscillation

Unless otherwise specified: V_{DD}=1.8 to 5.5 V, V_{SS}=0 V, Ta=25°C, R_{CR}=1.8 MΩ

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				3	ms	
Frequenct/IC deviation	∂f/∂IC	R_{CR}=constant	-25		25	%	

OSC3 crystal oscillation

Unless otherwise specified: V_{DD}=2.6/3.5 to 5.5 V, V_{SS}=0 V, Ta=25°C, Crystal oscillator=Q21CA301xxx(made by Seiko Epson corporation), R_F=1 MΩ, C_{G2}=C_{D2}=15 pF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				20	ms	1

Note) 1. The crystal oscillation start time changes by the crystal oscillator to be used, C_{G2} and C_{D2}.

OSC3 ceramic oscillation

Unless otherwise specified: V_{DD}=2.6/3.5 to 5.5 V, V_{SS}=0 V, Ta=25°C, Ceramic oscillator=CSA4.00MG/CSA8.00MTZ(made by Murata Mfg. corporation), R_F=1 MΩ, C_{G2}=C_{D2}=30 pF

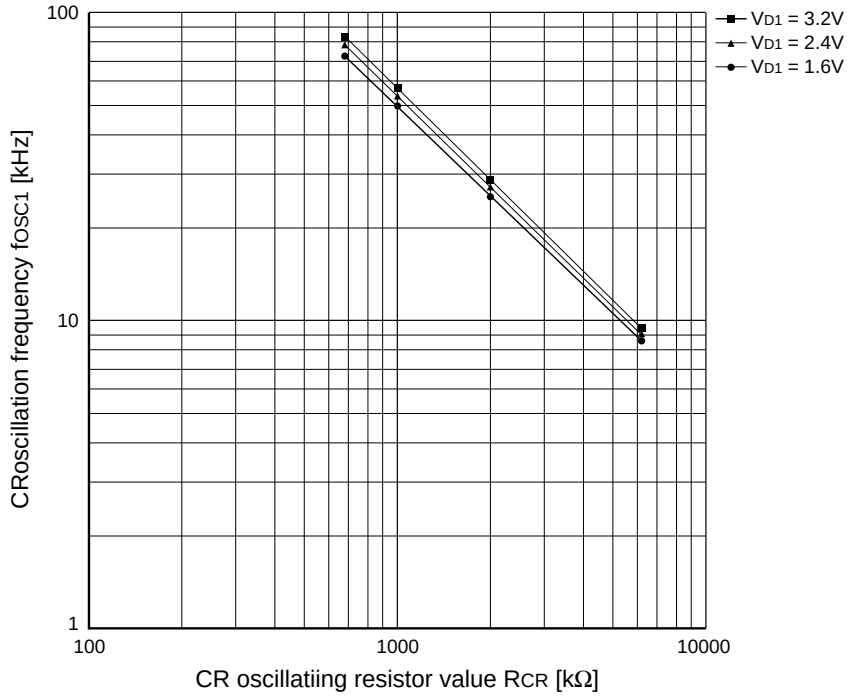
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				5	ms	

OSC3 CR oscillation

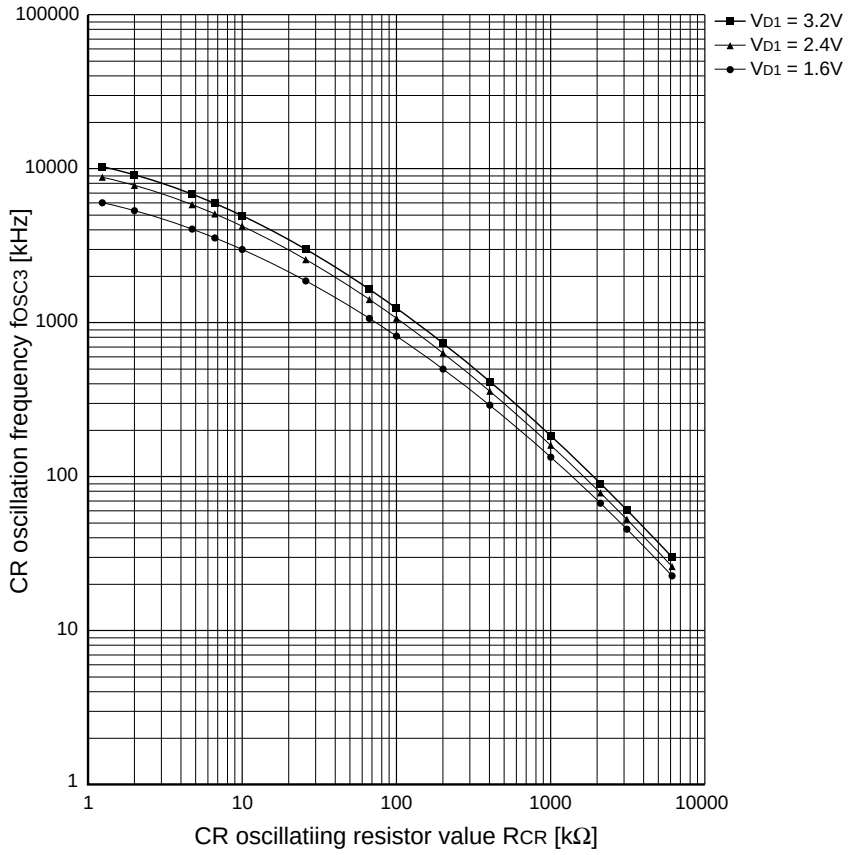
Unless otherwise specified: V_{DD}=2.6/3.5 to 5.5 V, V_{SS}=0 V, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				1	ms	
Frequenct/IC deviation	∂f/∂IC	R_{CR}=constant	-25		25	%	

OSC1 CR oscillation characteristics (for reference)



OSC3 CR oscillation characteristics (for reference)

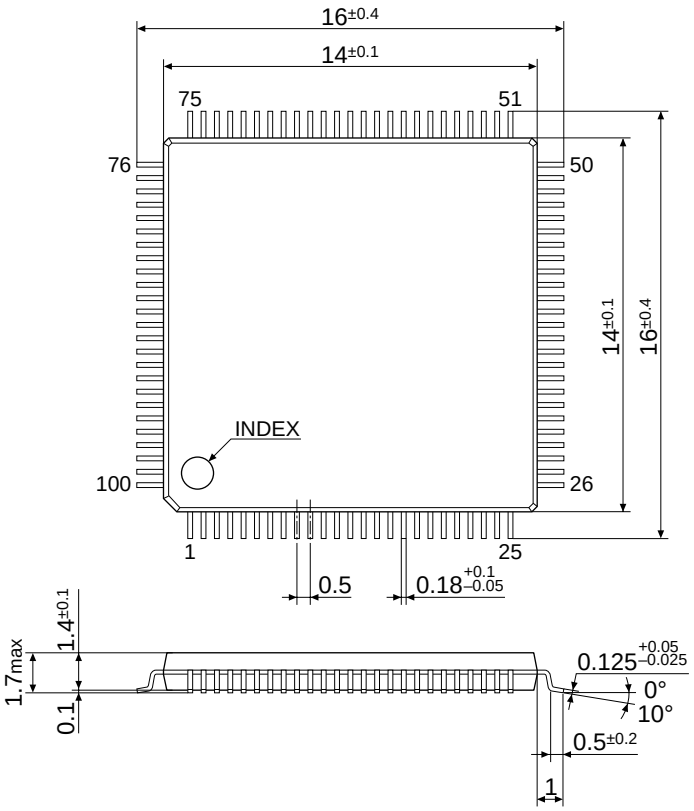


CHAPTER 9 PACKAGE

9.1 Plastic Package

QFP15-100pin

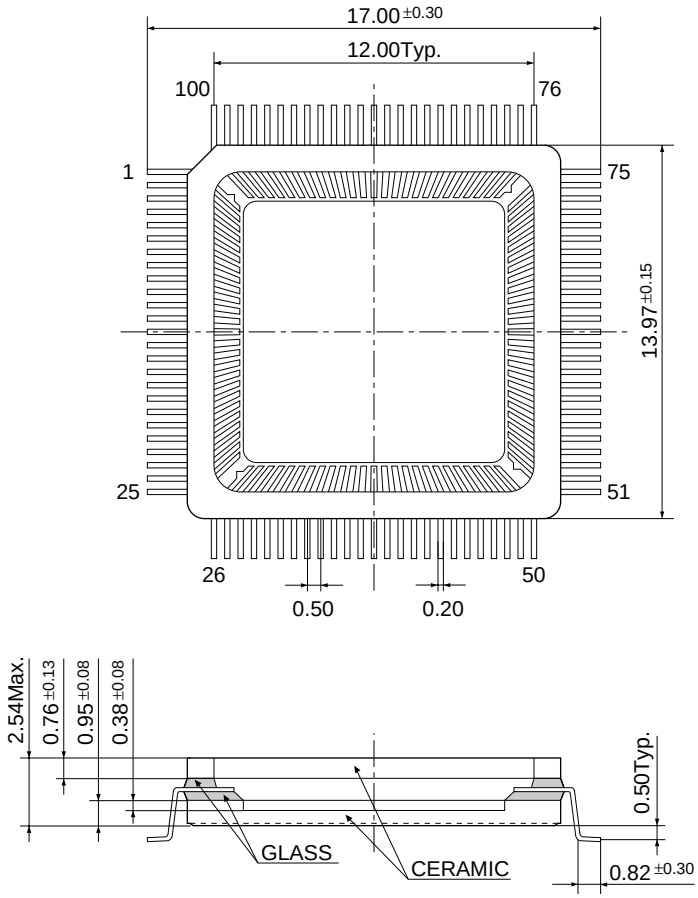
(Unit: mm)



Note: The dimensions are subject to change without notice.

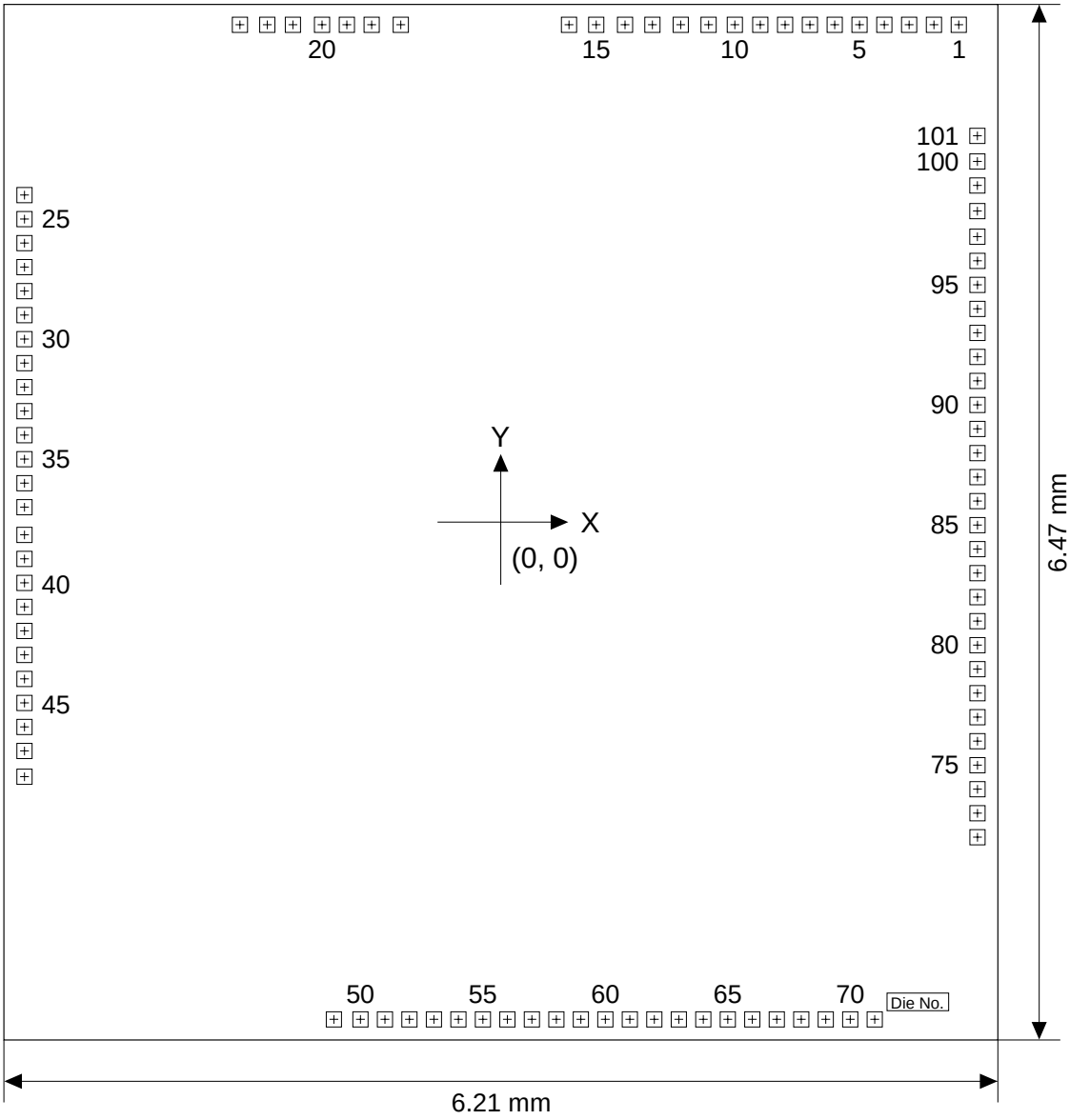
9.2 Ceramic Package for Test Samples

(Unit: mm)



CHAPTER 10 PAD LAYOUT

10.1 Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 95 µm

10.2 Pad Coordinates

Table 10.2.1 Pad coordinate

No.	Pad name	X	Y	No.	Pad name	X	Y
1	N.C.	2,860	3,107	52	P15 (SOUT/IRO)	-572	-3,107
2	N.C.	2,705	3,107	53	P16 ($\overline{\text{SCLK}}$)	-419	-3,107
3	SD7	2,550	3,107	54	P17 ($\overline{\text{SRDY}}$)	-266	-3,107
4	SD6	2,395	3,107	55	P20	-113	-3,107
5	SD5	2,240	3,107	56	P21	40	-3,107
6	SD4	2,085	3,107	57	P22	193	-3,107
7	SD3	1,930	3,107	58	P23	346	-3,107
8	SD2	1,775	3,107	59	P30	499	-3,107
9	SD1	1,620	3,107	60	P31	652	-3,107
10	SD0	1,461	3,107	61	P32	805	-3,107
11	LP	1,297	3,107	62	P33	958	-3,107
12	XSCL	1,123	3,107	63	P34	1,111	-3,107
13	FR	946	3,107	64	P35	1,264	-3,107
14	YD	775	3,107	65	P36	1,417	-3,107
15	DOFF	595	3,107	66	P37	1,570	-3,107
16	LCDEN	425	3,107	67	R00 (A00)	1,723	-3,107
17	V_{DD}	-626	3,107	68	R01 (A01)	1,876	-3,107
18	OSC4	-808	3,107	69	R02 (A02)	2,029	-3,107
19	OSC3	-963	3,107	70	R03 (A03)	2,182	-3,107
20	V_{D1}	-1,118	3,107	71	R04 (A04)	2,335	-3,107
21	OSC2	-1,300	3,107	72	R05 (A05)	2,977	-1,969
22	OSC1	-1,460	3,107	73	R06 (A06)	2,977	-1,819
23	V_{SS}	-1,631	3,107	74	R07 (A07)	2,977	-1,669
24	MCU/$\overline{\text{MPU}}$	-2,977	2,043	75	R10 (A08)	2,977	-1,519
25	K00	-2,977	1,893	76	R11 (A09)	2,977	-1,369
26	K01	-2,977	1,743	77	R12 (A10)	2,977	-1,219
27	K02	-2,977	1,593	78	R13 (A11)	2,977	-1,069
28	K03	-2,977	1,443	79	R14 (A12)	2,977	-919
29	K04	-2,977	1,293	80	R15 (A13)	2,977	-769
30	K05	-2,977	1,143	81	R16 (A14)	2,977	-619
31	K06	-2,977	993	82	R17 (A15)	2,977	-469
32	K07	-2,977	843	83	R20 (A16)	2,977	-319
33	K10 (EXCL00)	-2,977	693	84	R21 (A17)	2,977	-169
34	K11 (EXCL01)	-2,977	543	85	R22 (A18)	2,977	-19
35	K12	-2,977	393	86	R23 (A19)	2,977	132
36	K13	-2,977	243	87	R24 (A20)	2,977	282
37	$\overline{\text{TEST}}$	-2,977	93	88	R25 (A21)	2,977	432
38	$\overline{\text{RESET}}$	-2,977	-80	89	R26 ($\overline{\text{RD}}$)	2,977	583
39	P00 (D0)	-2,977	-230	90	R27 ($\overline{\text{WR}}$)	2,977	733
40	P01 (D1)	-2,977	-380	91	R30 ($\overline{\text{CE0}}$)	2,977	883
41	P02 (D2)	-2,977	-530	92	R31 ($\overline{\text{CE1}}$)	2,977	1,033
42	P03 (D3)	-2,977	-680	93	R32 ($\overline{\text{CE2}}$)	2,977	1,183
43	P04 (D4)	-2,977	-830	94	R40 (TOUT0/FOUT3)	2,977	1,333
44	P05 (D5)	-2,977	-980	95	R41 (TOUT1/FOUT1)	2,977	1,483
45	P06 (D6)	-2,977	-1,130	96	R42 (BZ)	2,977	1,633
46	P07 (D7)	-2,977	-1,280	97	N.C.	2,977	1,783
47	P10 (SIN)	-2,977	-1,430	98	N.C.	2,977	1,943
48	P11 (SOUT)	-2,977	-1,590	99	N.C.	2,977	2,103
49	P12 ($\overline{\text{SCLK}}$)	-1,044	-3,107	100	N.C.	2,977	2,253
50	P13 ($\overline{\text{SRDY}}$)	-878	-3,107	101	N.C.	2,977	2,413
51	P14 (SIN/IRI)	-725	-3,107	–	–	–	–

(Unit: µm)

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