GENERAL DESCRIPTION

The EM84502 Mouse Controller is specially designed to control PS/2 mouse device.This single chip can interface three key-switches and four photo-couples direct to 8042. EM84502 can receive command and echo status or data format which are compatible with IBM PS/2 mode mouse. Key debouncing circuit is provided to prevent false entry and improve the accuracy.
In the conventional mouse, a great number of noises are generated when the grid is partially closed or opened. These noise are usually mistaken for movement signals by conventional mouse controller and the cursor of the dispaly screen is thus moved frequently up and down or back and forth. This will consumes a great amount of energy.The EM84502 PS/2 mouse controller provides noise immunity circuits to eliminate these noise in order to reduce energy consumption.

FEATURES

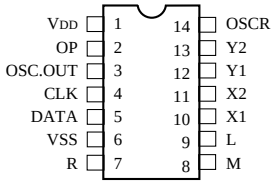
- Being compatiable with PS/2 mouse mode.
- Built-in noise immunity circuit.
- Low power dissipation.
- RC oscillation.
- Three key-switches and four photo-couples inputs.
- Both key-press and key-release debounce interval 12 ms.
- Through three key-switches input, EM84502 can exert seven different output.
- The motion detector of the EM84502 could sense 8 m/sec maximun with 200 DPI wheels.

APPLICATIONS

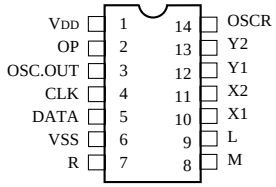
- Optical mouse or pen-mouse.
- Mechanical mouse or pen-mouse.
- Optomechanical mouse or pen-mouse.
- Mechanical track ball.
- Optomechanical track ball.

PIN ASSIGNMENT

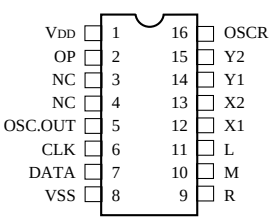
EM84502AP



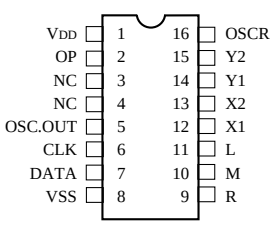
EM84502AM



EM84502BP

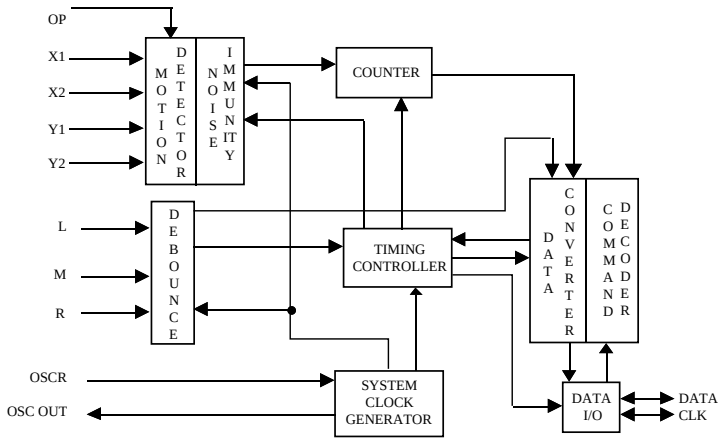


EM84502BM*



* (Under developed)

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

Symbol	I/O	Function
V_{DD}		Power
OP	I	X, Y inputs. Floating : Comparator input. GND : Schmitt trigger input. Short to OSC OUT : Testing Mode.
OSCOUT	O	Clock output.
CLK	I/O	8042 auxiliary port CLK line.
DATA	I/O	8042 auxiliary port DATA line.
V_{SS}		Ground
R M L	I	Three key-switches exert seven different combinations totally. Both key-pressed and key-released signals will be sent accomplanied with horizontal and vertical state. The status of the key-switches will be preserved, whenever the value of horizontal or vertical counters will present at DATA. And the debounce interval for both key-press and key-release is 12 ms.
X1 X2 Y1 Y2	I	Four photo-couple signals denote UP, DOWN, LEFT, and RIGHT state. During the scaning period, as long as the photo-couples change their states, the value of vertical or horizontal counter will increase or decrease accordingly.
OSCR	I	30 Kohm ±5% pull low for 35 KHz oscillation.

FUNCTION DESCRIPTIONS

A) Operating mode

There are four operating modes in PS/2 mouse:

i). Reset Mode:
In this mode a self-test is initiated during power-on or by a Reset command. After reset signal, PS/2 mouse will send:
1). Completion code AA & ID code 00.

2). Set default:
sampling rate: 100 reports/s
non-autospeed
stream mode
2 dot/count
disable

ii). Stream Mode:
The maximum rate of transfer is the programmed sample rate.
Data report is transmitted if
1). switch is pressed
2). movement has been detect

iii). Remote Mode:
Data is transmitted only in response to a Read Data command.

iv). Wrap Mode:

Any byte of data sent by the system, except hex EC (Reset wrap mode) or hex FF (Reset), is returned by EM84502.

B). PS/2 Mouse Data Report:

i). In stream mode: A data report is sent at the end of a sample interval.

ii). In remote mode: A data report is sent in response to Read Data command.

iii). Data report format:

Byte	Bit	Description
1	0	Left button status; 1 = pressed
	1	Right button status; 1 = pressed
	2	Middle button status; 1 = pressed
	3	Reserve
	4	X data sign; 1 = negative
	5	Y data sign; 1 = negative
	6	X data overflow; 1 = overflow
	7	Y data overflow; 1 = overflow
2	0-7	X data (D0 - D7)
3	0-7	Y data (D0 - D7)

C) PS/2 mouse Data Transmission:

i). EM84502 generates the clocking signal when sending data to and receiving data from the system.

ii). The system requests EM84502 receive system data output by forcing the DATA line to an inactive level and allowing CLK line to go to an active level.

iii). Data transmission frame:

Bit	Function
1	Start bit (always 0)
2-9	Data bits (D0 - D7)
10	Parity bit (odd parity)
11	Stop bit (always 1)

iv). Data Output (data from EM84502 to system):

If CLK is low (inhibit status) , data is no transmission.

If CLK is high and DATA is low (request-to-send), data is updated. Data is received from the system and no transmission are started by EM84502 until CLK and DATA both high. If CLK and DATA are both high, the transmission is ready. DATA is valid prior to the falling edge of CLK and beyond the rising edge of CLK. During transmission, EM84502 check for line contention by checking for an inactive level on CLK at intervals not to exceed 100u sec. Contention occurs when the system lowers CLK to inhibit EM84502 output after EM84502 has started a transmission. If this occurs before the rising edge of the tenth clock, EM84502 internal store its data in its buffer and returns DATA and CLK to an active level. If the contention does not occur by the tenth clock, the transmission is complete.
Following a transmission, the system inhibits EM84502 by holding CLK low until it can service the input or until the system receives a request to send a response from EM84502.

v). Data Input (from system to EM84502):

System first check if EM84502 is transmitting data. If EM84502 is transmitting, the system can override the output forcing CLK to an inactive level prior to the tenth clock. If EM84502 transmission is beyond the tenth clock, the system receives the data. If EM84502 is not transmitting or if the system choose to override the output, the system force CLK to an inactive level for a period of not less than 100μ sec while preparing for output. When the system is ready to output start bit (0), it allows CLK go to active level. If request-to-send is detected, EM84502 clocks 11 bits. Following the tenth clock EM84502 checks for an active level on the DATA line, and if found, force DATA low , and clock once more. If occurs framing error, EM84502 continue to clock until DATA is high, then clocks the line control bit and request a Resend. When the system sends out a command or data transmission that requires a response, the system waits for EM84502 to response before sending its next output.

D). PS/2 Mouse Error Handling:

i). A Resend command (FE) following receipt of an invalid input or any input with incorrect parity.

ii). If two invalid input are received in succession, an error code of hex FC send to the system.

iii). The counter accumulators are cleared after receiving any command except “Resend”.

iv). EM84501 receives a Resend command (FE), it transmit its last packet of data.

v). In the stream mode “Resend” is received by EM84502 following a 3-byte data packet transmission to the system. EM84502 resend the 3-byte data packet prior to clearing the counter.

vi). A response is sent within 25 ms if

a). The system requires a response
b). An error is detected in the transmission

vii). When a command requiring a response is issued by the system ,another command should not be issue until either the response is received or 25ms has passed.

E). PS/2 Mouse Commands Description:

There are 16 valid commands that transmits between the system and EM84502. The "FA" code is always the first response to any valid input received from the system other than a Set Wrap Mode or Resend command. The following table list the commands:

Hex Code	Command	EM84502 echo code
FF	Reset	FA,AA,00
FE	Resend	XX,(XX,XX)
F6	Set Default	FA
F5	Disable	FA
F4	Enable	FA
F3,XX	Set Sampling Rate	FA,FA
F2	Read Device Type	FA,00
F0	Set Remote Mode	FA
EE	Set Wrap Mode	FA
EC	Reset Wrap Mode	FA
EB	Read Data	FA,XX,XX,XX
EA	Set Stream Mode	FA
E9	Status Request	FA,XX,XX,XX
E8,XX	Set Resolution	FA,FA
E7	Set Autospeed	FA
E6	Reset Autospeed	FA

The following describes valid commands:

a). Reset (FF)
EM84502 operation:
i). Completion the reset.
ii). Transmitted FA,AA,00 to the system.
iii). Set default:
sampling rate: 100 reports/s
non-autospeed
stream mode
2 dots/count
disable

b). Resend (FE)
i). Any time EM84502 receives an invalid command, it returns a Resend command to the system.
ii). When EM84502 receives a Resend command, it retransmits its last packet of data. If the last packet was a Resend command, it transmits the packet just prior to the Resend command.
iii). In stream mode, if a Resend command is received by EM84502 immediately following a 3-byte data packet transmission to the system.

c). Set Default (F6)

The command reinitializes all conditions to the power-on defaults.

d). Disable (F5)

This command is used in the stream mode to stop transmissions from EM84502.

e). Enable (F4)

Begins transmissions, if in stream mode.

f). Set Sampling Rate (F3,XX)

In the stream mode, this command sets the sampling rate to the value indicated by byte hex XX, shown in following:

Second byte XX	Sample Rate
0A	10/sec
14	20/sec
28	40/sec
3C	60/sec
50	80/sec
64	100/sec
C8	200/sec

g). Read Device Type (F2)

EM84502 always echoes " FA,00 " following this command.

h). Set Remote Mode (F0)

Data value are reported only in response to a Read Data command.

i). Set Wrap Mode (EE)

Wrap mode remains until Reset (FF) or Reset Wrap Mode(EC) is received.

j). Reset Wrap Mode (EC)

EM84502 returns to the previous mode of operation after receiving this command.

k). Read Data (EB)

This command is executed in either remote or stream mode. The data is transmitted even if there has been no movement since the last report or the button status is unchanged. Following a Read Data command, the registers are cleared after a data transmission.

l). Set Stream Mode (EA)

This command sets EM84502 in stream mode.

m). Status Request (E9)

When this command is issued by the system, EM84502 respond with a 3-byte status report as follows:

Byte	Bit	Description
1	0	1 = Right button pressed
	1	1 = Middle button pressed
	2	1 = Left button pressed

	3	Reserved
	4	0 = Normal speed, 1 = Autospeed
	5	0 = Disabled, 1 = Enabled
	6	0 = Stream mode, 1 = Remote mode
	7	Reserved
2	0-7	Current resolution setting (D0 - D7)
3	0-7	Current sampling rate (D0 - D7)

n). Set Resolution (E8,XX)

EM84502 provides four resolutions selected by the second byte of this command as follows:

Second Byte XX	Resolution
00	8 dot/count
01	4 dot/count
02	2 dot/count
03	1 dot/count

o). Set Autospeed (E7)

At the end of a sample interval in the stream mode, the current X and Y data values are converted new values. The sign bits are not involved in this conversion. The conversion is only in stream mode. The relationship between the input and output count follows:

Input	Ouput
0	0
1	1
2	1
3	3
4	6
5	9
N(≥6)	2.0*N

p). Reset Autospeed (E6)

This command restore normal speed.

F) Testing mode

Whenever OPT is connected to OSC OUT, the chip will enter buyer's testing mode. The X direction output signals of comparators will present to L and M pin. Pressing "R" key can toggle the output from X direction to Y direction.

ABSOLUTE MAXIMUM RATINGS

Parameter	Sym.	Ratings	Unit
Temperature under bias	T_{OPR}	0~70	°C
Storage temperature range	T_{STR}	-65~150	°C
Input voltage	V_{IN}	-0.3~6.0	V
Output voltage	V_O	-0.3~6.0	V

DC ELECTRICAL CHARACTERISTICS (T_A=25°C to 70°C)

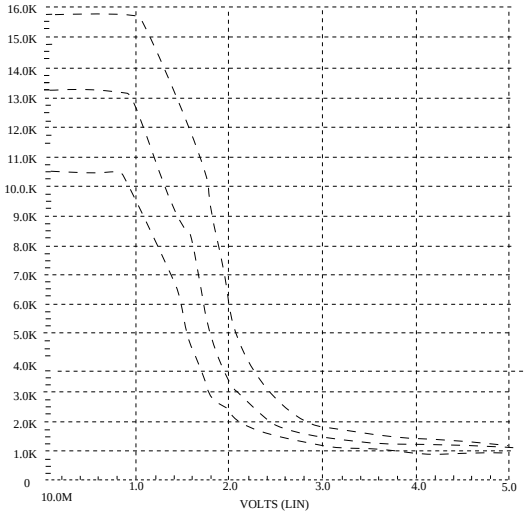
Parameters	Sym.	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD}	4.5	5	5.5	V
Operating current (no load)	I_{Op}	-	-	1.2	mA
X,X2,Y1,Y2 low input reference current	I_{PL}	70	-	-	µA
X,X2,Y1,Y2 high input reference current	I_{Ph}	-	-	106	µA
X,X2,Y1,Y2 input current Schmitt trigger input (76µA)	V_{PI}	0.8	-	1.2	V
X,X2,Y1,Y2 input current Comparator input (80µA)	V_{PI}	0.8	-	1.2	V
X,X2,Y1,Y2 input current Comparator input (500µA)	V_{PI}	1.5	-	2.1	V
CLK, DATA postive-going threshold voltage	Vt+	3.2	-	3.8	V
CLK, DATA negative-going threshold voltage	Vt -	1.2	-	1.9	V
Low input voltage, other pins	Vail	-	-	1.5	V
High input voltage, other pins	Vaih	3.5	-	-	V
L, M, R input current (pull low resistor Vin=5V)	Imi	16.6	-	50	µA
PS/2 mouse mode DATA, CLK input Current (pull up resistor) (VIN=0V)	Idc	0.56	-	1.86	mA
PS/2 mouse mode DATA, CLK low output voltage (Iprl=-2mA)	Vprl	-	-	0.4	V
L, M, R, X1, X2, Y1, Y2 input leakage current (Vin=0V)	Iil	0	-	1.0	µA

* All voltages in above table are compared with V_{SS}.
* All parameters in above table are tested under V_{DD}=5V.
* CLK & DATA output gates are open drains that connect to pull up resistors.
* X1, X2,Y1,T2 Input Impedance

MAX.

TYP.

MIN.



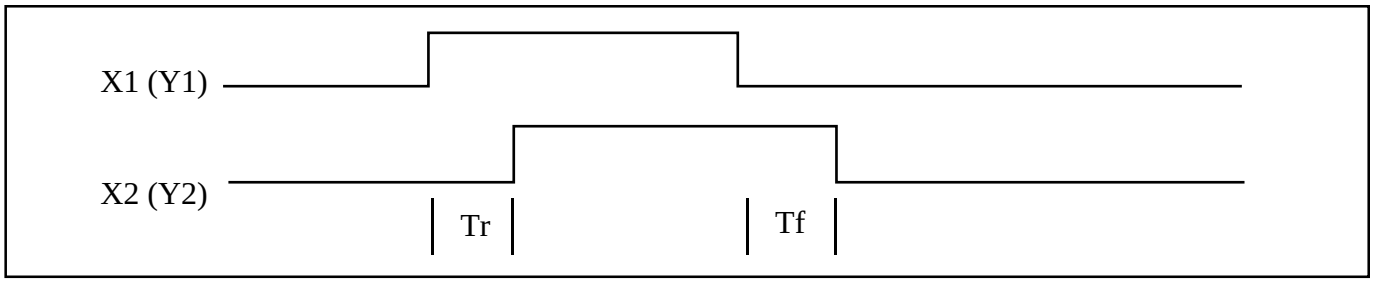
AC ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C)

Parameters	Sym.	Min.	Typ.	Max.	Unit
Oscillating Frequency	Fosc	34.3-10%	34.3	34.3+10%	KHz
Key Debounce	Tkd	-	12	-	ms
Rising Edge Crossed Width Fosc=35 KHz	Tr	14.3	-	-	us
Falling Edge Crossed Width Fosc=35 KHz	Tf	14.3	-	-	us
Mouse CLK Active Time	Tmca	-	42.9	-	us
Mouse CLK Inactive Time	Tmci	-	42.9	-	us
Mouse Sample DATA from CLK rising Edge	Tmdc	-	14.3	-	us
System CLK Active Time	Tsca	-	42.9	-	us
System CLK Inactive Time	Tsci	-	42.9	-	us
Time from DATA Transition to Falling Edge of CLK	Tsdc	-	14.3	-	us
Time from rising Edge of CLK to DATA Transition	Tscd	-	28.6	-	us
Time to mouse Inhibit after the 11th CLK to ensure mouse does not start another Transmission	Tpi	0	-	50	us

PS. The AC timings are measured under using 35 KHz system clock signal.

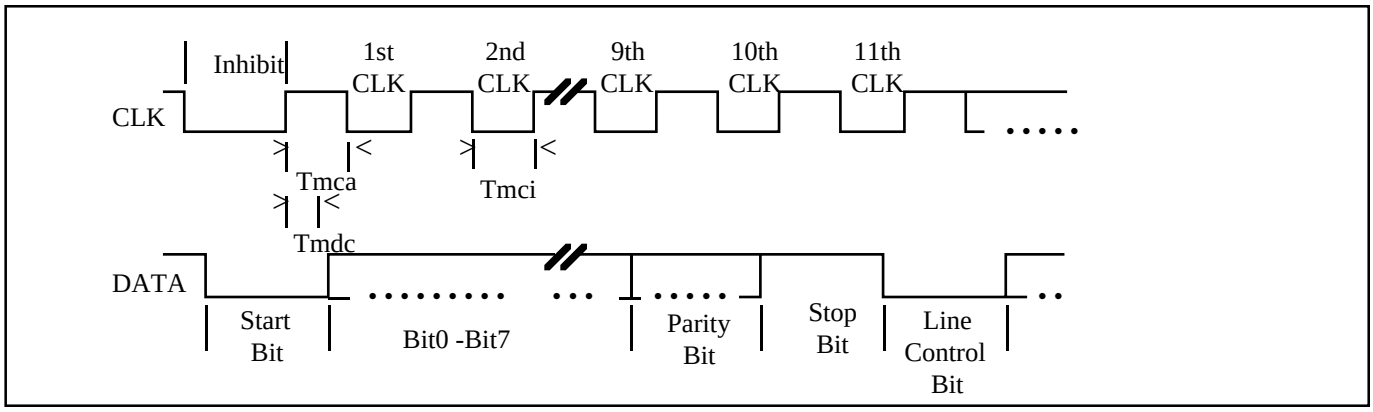
TIMING DIAGRAM

(1) Photo-couples pulse width :

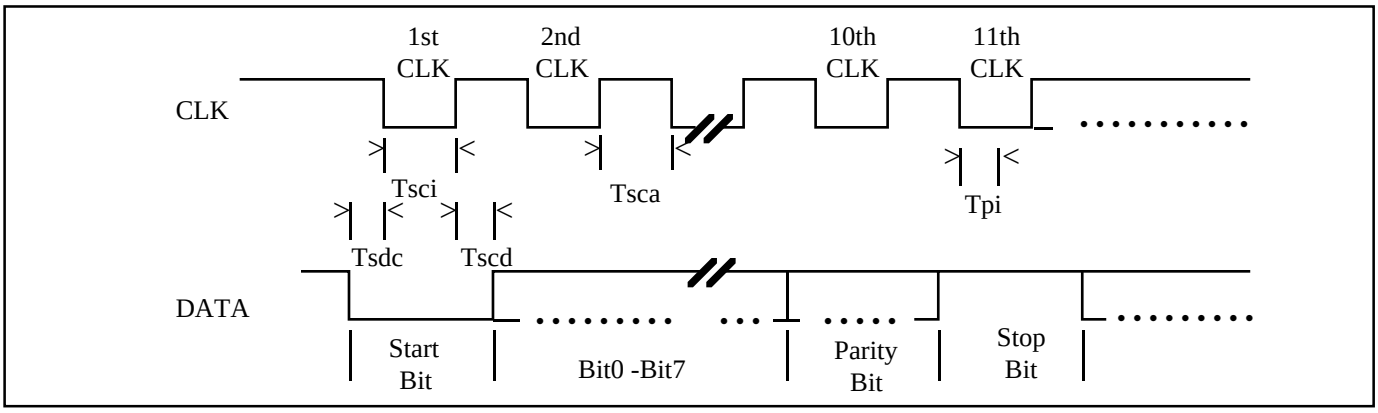


(2) PS/2 Mouse

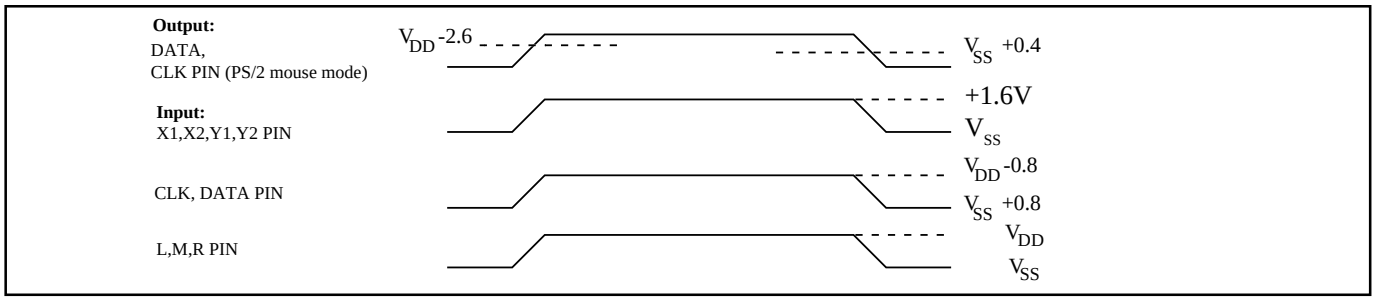
(A) Receiving DATA



(B) Sending DATA

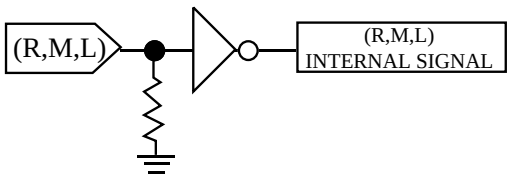


AC Timing point:

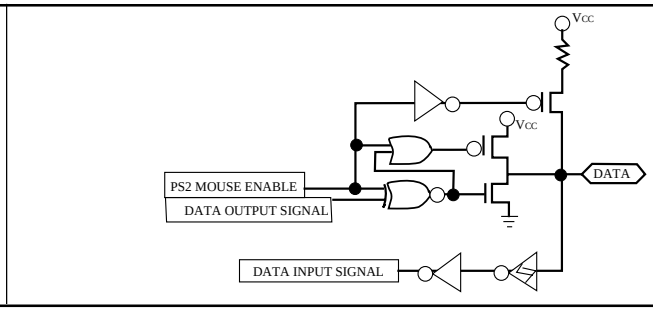


EM84502 I/O pin equivalent circuit :

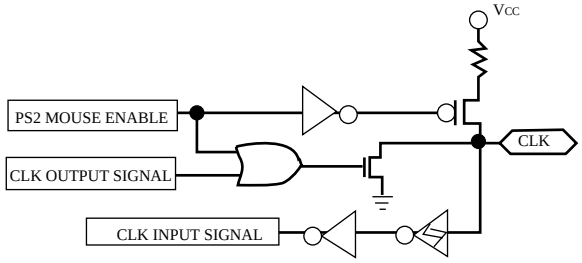
R,M,L :



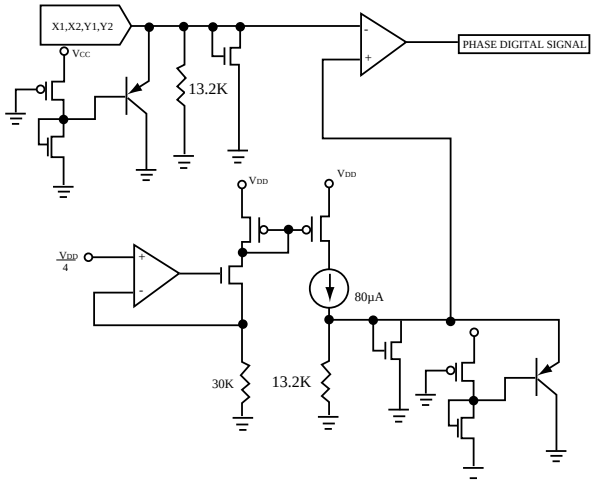
DATA :



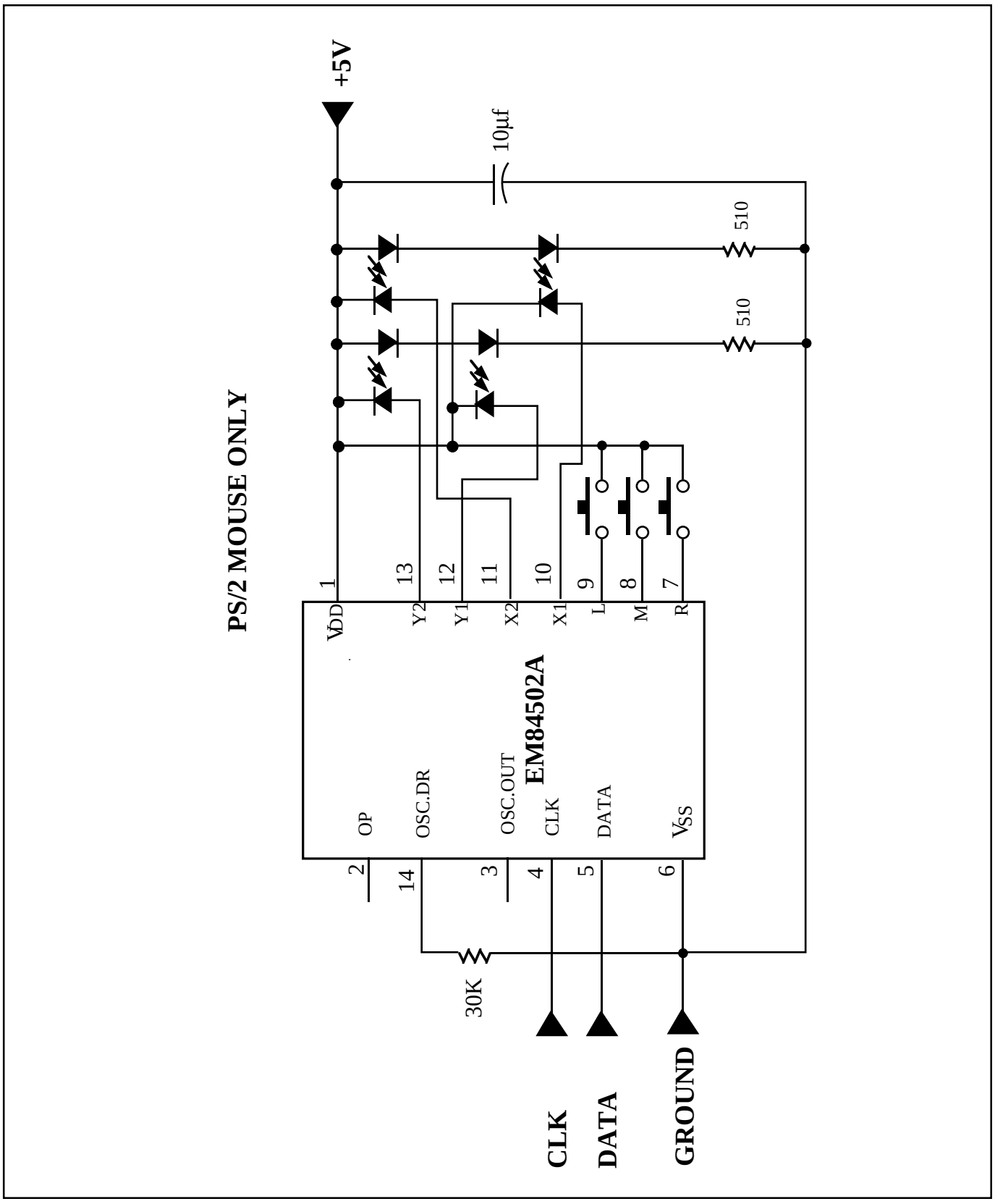
CLK :



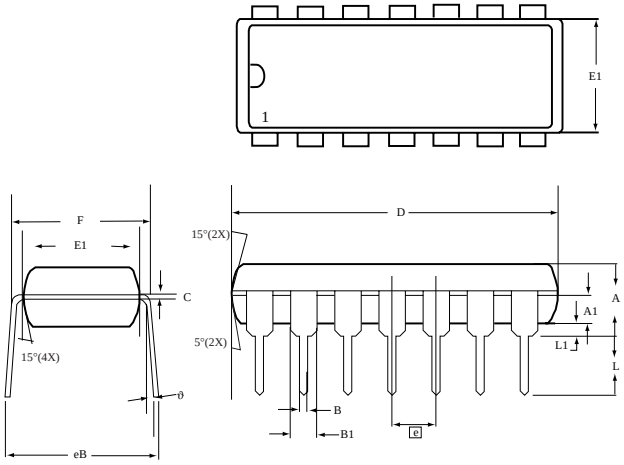
X1,X2,Y1,Y2 :



APPLICATION CIRCUIT



14 PDIP



Symbol	Inches			Milimeters		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	-	.130	-	-	3.302	-
A1	.059	.060	.061	1.499	1.524	1.549
B	-	.018	-	-	0.457	-
B1	-	.060	-	-	1.524	-
C	-	.010	-	-	0.254	-
D	.740	.750	.760	18.796	19.050	19304
E1	.259	.260	-	6.579	6.604	-
F	.290	.300	.310	7.366	7.620	7.874
L	-	.130	-	-	3.302	-
L1	-	.020	-	-	0.506	-
e	-	.100	-	-	2.540	-
eB	.345	.355	.365	8.763	9.017	9.271
ϑ	0°	7.5°	15°	0°	7.5°	15°