EM78458/459

8-Bit Microcontroller with MASK ROM

Product Specification

DOC. VERSION 1.4

ELAN MICROELECTRONICS CORP.

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ELAN MICROELECTRONICS CORPORATION

Contents

APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	
1.1	Modify ERC frequency	2003/03/06
1.2	Add AD & OP spec	2003/05/07
1.3	Change Power on reset content	2003/07/01
1.4	Cancel Code Option CLAMP	2005/05/27

1   GENERAL DESCRIPTION

EM78458 and EM78459 are 8-bit microprocessors designed and developed with low-power and high-speed CMOS technology. There is a 4K*13-bit Read Only Memory (ROM) within it.

2   FEATURES

- Operating voltage range: 2.3V~5.5V

- Operating temperature range: 0°C~70°C

- Operating frequency range(base on 2 clocks):
  - Crystal mode: DC ~ 20MHz/2clks,5V; DC ~ 8MHz/2clks,3V
  - RC mode: DC ~ 4MHz/2clks,5V; DC ~ 4MHz/2clks,3V

- Low power consumption:
  - Less than 1.5 mA at 5V/4MHz
  - Typically 15 μA, at 3V/32KHz
  - Typically 1 μA, during sleep mode

- 4K × 13 bits on chip ROM

- 84 × 8 bits on chip registers (SRAM)

- 2 bi-directional I/O ports

- 8 level stacks for subroutine nesting

- 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt

- 8-bit multichannel Analog-to-Digital Converter with 8-bit resolution

- Dual Pulse Width Modulation (PWM) with 10-bit resolution

- One pair of comparators

- Power-down (SLEEP) mode

- Six available interruptions
  - TCC overflow interrupt
  - Input-port status changed interrupt (wake up from the sleep mode)
  - External interrupt
  - ADC completion interrupt
  - PWM period match completion
  - Comparator high interrupt

- Programmable free running watchdog timer

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(This specification is subject to change without further notice)

■ 8 Programmable pull-down I/O pins

■ 7 programmable pull-high I/O pins

■ 8 programmable open-drain I/O pins

■ Two clocks per instruction cycle

■ Package types:
   ● 20 pin DIP 300mil: EM78458AP
   ● 20 pin SOP 300mil: EM78458AM
   ● 24 pin skinny DIP 300mil: EM78459AK
   ● 24 pin SOP 300mi: EM78459AM

■ Power on voltage detector available (2.0V± 0.15V)

3 PIN ASSIGNMENT
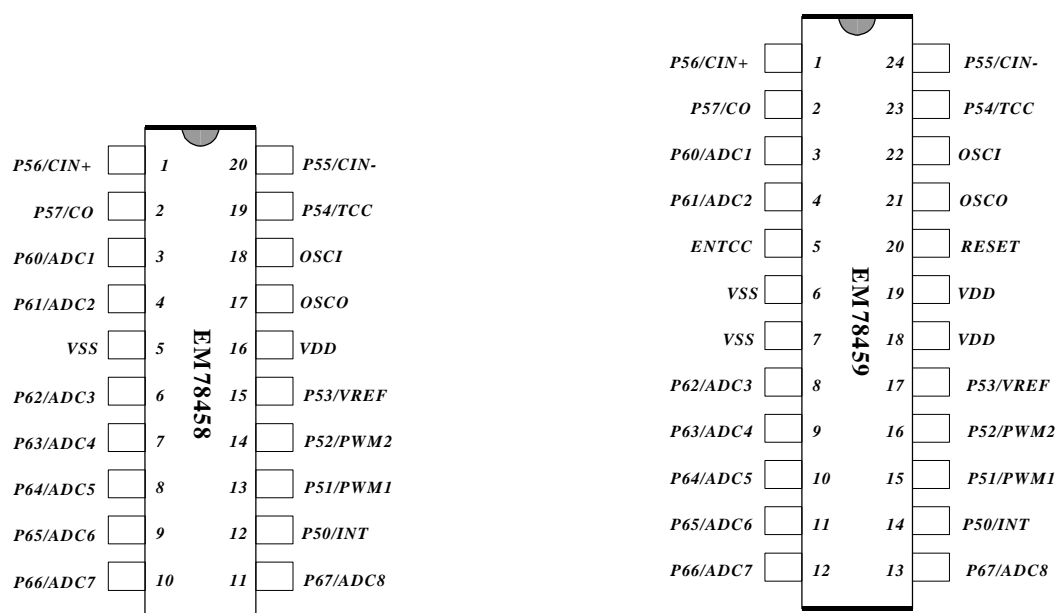
Fig. 1 Pin Assignment

3.1 EM78458 Pin Description

Symbol	Pin No.	Type	Function
VDD	16	-	Power supply.
OSCI	18	I	* XTAL type: Crystal input terminal or external clock input pin. * RC type: RC oscillator input pin.
OSCO	17	O	*XTAL type: Output terminal for crystal oscillator or external clock input pin. *RC type: Clock output with a period of one instruction cycle time, the prescaler is determined by the CONT register. * External clock signal input.
P50	12	I	* General-purpose Input only. * Default value while power-on reset.
P51 ~ P57	13~15 19, 20, 1, 2	I/O	* General-purpose I/O pin. * Default value while power-on reset.
P60 ~ P67	3, 4, 6~11	I/O	* General-purpose I/O pin. * Default value while power-on reset.
INT	12	I	* External interrupt pin triggered by falling edge.
ADC1~ADC8	3, 4, 6 ~ 11	I	* Analog to Digital Converter. * Defined by AD-CMPCON (IOCA0)<2:4>.
PWM1, PWM2	13, 14	O	* Pulse width modulation outputs. * Defined by PWMCON (IOC51)<6, 7>
VREF	15	I	* External reference voltage for ADC * Defined by AD-CMPCON (IOCA0)<7>.
CIN-, CIN+, CO	20, 1,2	I O	* "-" -> the input pin of Vin- of the comparator. * "+"-> the input pin of Vin+ of the comparator. * Pin CO is the output of the comparator. * Defined by AD-CMPCON (IOCA0) <5, 6>
TCC	19	I	* Real time clock/counter with Schmitt trigger input pin; it must be tied to VDD or VSS if it is not in use.
VSS	5	-	Ground.

(This specification is subject to change without further notice)

3.2   EM78459 Pin Description

Symbol	Pin No.	Type	Function
VDD	19, 18	-	Power supply.
OSCI	22	I	* XTAL type: Crystal input terminal or external clock input pin. * RC type: RC oscillator input pin.
OSCO	21	O	* XTAL type: Output terminal for crystal oscillator or external clock input pin. * RC type: Clock output with a period of one instruction cycle time, the prescaler is determined by the CONT register. * External clock signal input.
P50	14	I	* General-purpose Input only. * Default value while power-on reset.
P51 ~ P57	15~17 23, 24 1, 2	I/O	* General-purpose I/O pin. * Default value while power-on reset.
P60 ~ P67	3, 4, 8~13	I/O	* General-purpose I/O pin. * Default value while power-on reset.
INT	14	I	* External interrupt pin triggered by falling edge.
ADC1~ADC8	3, 4, 8~13	I	* Analog to Digital Converter. * Defined by AD-CMPCON (IOCA0)<2:4>.
PWM1, PWM2	15, 16	O	* Pulse width modulation outputs. * Defined by PWMCON (IOC51)<6, 7>
VREF	17	I	* External reference voltage for ADC * Defined by AD-CMPCON (IOCA0)<7>.
CIN-, CIN+, CO	24, 1, 2	I	* '-' -> the Vin- input pins of the comparators. * '+' -> the Vin+ input pins of the comparators. * Pin CO is the output of the comparator. * Defined by AD-CMPCON (IOCA0) <5, 6>
/RESET	20	I	* If it remains at logic low, the device will be reset. * Wake up from sleep mode when pins status changes. * Voltage on /RESET/Vpp must not be over Vdd during normal mode. * Pull-high is on if /RESET is asserted.
TCC	23	I	* Real time clock/counter with Schmitt trigger input pin; it must be tied to VDD or VSS if it is not in use.
ENTCC	5	I	1: Enable TCC; 0: Disable TCC.
VSS	6, 7	-	Ground.

4   FUNCTION DESCRIPTION

Fig. 2 The Functional Block Diagram of EM78458/459

4.1   Operational Registers

4.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect addressing pointer. Any instruction using R0 as a pointer, actually accesses data pointed by the RAM Select Register (R4).

4.1.2 R1 (Time Clock /Counter)

■   Increased by an external signal edge through the TCC pin, or by the instruction cycle clock.

■   The signals to increase the counter are decided by Bit 4 and Bit 5 of the CONT register.

■   Writable and readable as any other registers.

4.1.3 R2 (Program Counter) & Stack

■   R2 and hardware stacks are 12-bit wide. The structure is depicted in Fig. 4.

■   Generates 4K×13 bits on-chip ROM addresses to the relative programming instruction codes. One program page is 1024 words long.

■   The contents of R2 are set to all "0"s upon a RESET condition.

■ "JMP" instruction allows the direct loading of the lower 10 program counter bits. Thus, "JMP" allows PC to jump to any location within a page.

■ "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.

■ "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top of stack.

■ "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and tenth bits of the PC are cleared.

■ "MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC are cleared.

■ Any instruction that is written to R2 (e.g. "ADD R2, A", "MOV R2, A", "BC R2, 6",·····) will cause the ninth bit and the tenth bit (A8~A9) of the PC to be cleared. Thus, the computed jump is limited to the first 256 locations of a page.

■ In the case of EM78458/459, the most two significant bits (A11 and A10) will be loaded with the content of PS1 and PS0 in the status register (R3) upon the execution of a "JMP", "CALL", or any other instructions set which write to R2.

■ All instructions are single instruction cycle (fclk/2 or fclk/4) except for the instructions which write to R2, need one more instruction cycle.
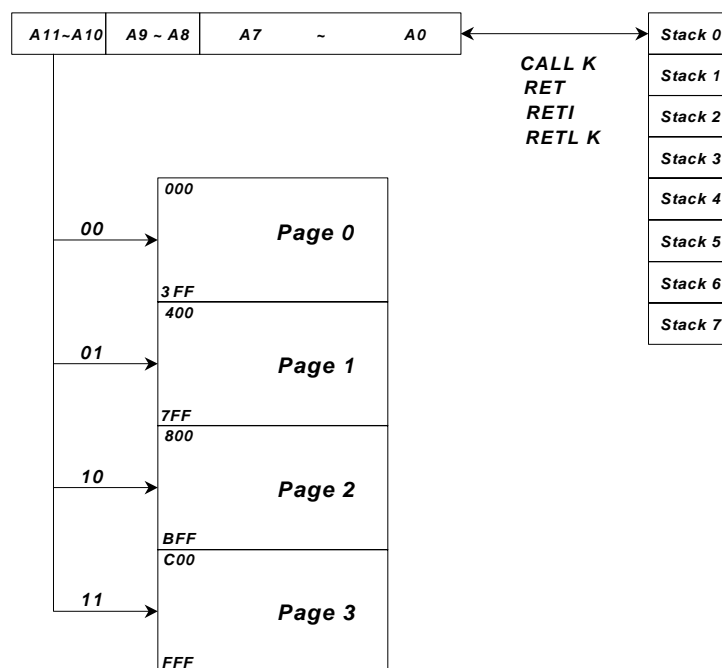
Fig. 3 Program Counter Organization

4.1.4 R3 (Status Register)

7	6	5	4	3	2	1	0
CMPOUT	PS1	PS0	T	P	Z	DC	C

Bit 7 (CMPOUT) the result of the comparator output.

Bit 6 (PS1) ~ 5 (PS0) Page select bits. PS0~PS1 are used to select a program memory page. When executing a "JMP", "CALL", or other instructions which cause the program counter to be changed (e.g. MOV R2, A), PS0~PS1 are loaded into the 11th and 12th bits of the program counter where it selects one of the available program memory pages. Note that RET (RETL, RETI) instruction does not change the PS0~PS1 bits. That is, the return will always be to the page from the place where the subroutine was called, regardless of the current setting of PS0~PS1 bits.

PS1	PS0	Program memory page [Address]
0	0	Page 0 [000-3FF]
0	1	Page 1 [400-7FF]
1	0	Page 2 [800-BFF]
1	1	Page 3 [C00-FFF]

Bit 4 (T) Time-out bit. Set to 1 by the "SLEP" and "WDTC" commands, or duringPower on and reset to 0 by WDT time-out.

Bit 3 (P) Power-down bit. Set to 1 during power-on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 2 (Z) Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC) Auxiliary carry flag

Bit 0 (C) Carry flag

4.1.5 R4 (RAM Select Register)

Bits 0~5 are used to select registers (address: 00~3F) in the indirect address mode.

Bit 6 is used to select bank 0 or bank 1.

Bit 7 is a general-purpose read/write bit.

See the configuration of the data memory in Fig. 4.

4.1.6 R5 ~ R6(Port 5 ~ Port 6)

■ R5 and R6 are I/O registers.

4.1.7 R7 ~ R8

■ All of these are 8-bit general-purpose registers.

00	R0				
01	R1 (TCC)				
02	R2 (PC)	←→	STACK 0	R9<5> (IOCS)	
03	R3 (Status)		STACK 1		
04	R4 (RSR)		STACK 2	0	1
05	R5 (Port 5)		STACK 3	IOC50	IOC51 (PWMCON)
06	R6 (Port 6)		STACK 4	IOC60	IOC61 (DT1L)
07	R7		STACK 5		IOC71 (DT1H)
08	R8		STACK 6		IOC81 (PRD1)
09	R9 (ADCON)		STACK 7	IOC90 (GCON)	IOC91 (DT2L)
0A	RA (ADDATA)			IOCA0 (AD-CMPCON)	IOCA1 (DT2H)
0B	RB (TMR1L)			IOCB0	IOCB1 (PRD2)
0C	RC (TMR1H)			IOCC0	IOCC1 (DL1L)
0D	RD (TMR2L)			IOCD0	IOCD1 (DL1H)
0E	RE (TMR2H)			IOCE0	IOCE1 (DL2L)
0F	RF			IOCF0	IOCF1 (DL2H)

10	
11	
	16x8 Common Register
1E	
1F	

PSR7, PSR6

	00		01
20	20		20
21			
	32x8 Bank Register (Bank 0)		32x8 Bank Register (Bank 1)
3F	3F		3F

Fig. 4 Data Memory Configuration

4.1.8 R9 (ADCON: Analog to Digital Control)

7	6	5	4	3	2	1	0
-	-	IOCS	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

Bit 7:Bit 6   Unemployed, read as '0';

Bit 5(IOCS):   Select the Segment of IO control register.

  1 = Segment 1 (IOC51~IOCF1) selected;

  0 = Segment 0 (IOC50~IOCF0) selected;

Bit 4 (ADRUN): ADC starts to RUN.

  1 = an A/D conversion is started. This bit can be set by software;

  0 = reset on completion of the conversion. This bit can not be reset though software;

Bit 3 (ADPD): ADC Power-down mode.

  1 = ADC is operating;

  0 = switch off the resistor reference to save power even while the CPU is operating.

Bit2:Bit0 (ADIS2:ADIS0): Analog Input Select.

  000 = AN0;

  001 = AN1;

  010 = AN2;

  011 = AN3;

  100 = AN4;

  101 = AN5;

  110 = AN6;

  111 = AN7;

They can only be changed when the ADIF bit and the ADRUN bit are both LOW.

4.1.9 RA (ADDATA: the converted value of ADC)

When the A/D conversion is complete, the result is loaded into the ADDATA. The START//END bit is cleared, and the ADIF is set.

4.1.10 RB

An 8-bit general-purpose register.

4.1.11   RC

A 2-bit, Bit 0and Bit 1 register.

4.1.12   RD

An 8-bit general-purpose register.

4.1.13   RE

A 2-bit, Bit 0 and Bit 1 register.

4.1.14   RF (Interrupt Status Register)

7	6	5	4	3	2	1	0
-	CMPIF	PWM2IF	PWM1IF	ADIF	EXIF	ICIF	TCIF

"1" means interrupt request, and "0" means no interrupt occurs.

Bit 0 (TCIF)   TCC overflow interrupt flag. Set when TCC overflows, reset by software.

Bit 1 (ICIF)   Port 6 input status change interrupt flag. Set when Port 6 input changes, reset by software.

Bit 2 (EXIF)   External interrupt flag. Set by falling edge on /INT pin, reset by software.

Bit 3 (ADIF)   Interrupt flag for analog to digital conversion. Set when AD conversion is completed, reset by software.

Bit 4 (PWM1IF) PWM1 (Pulse Width Modulation) interrupt flag. Set when a selected period is reached, reset by software.

Bit 5 (PWM2IF) PWM2 (Pulse Width Modulation) interrupt flag. Set when a selected period is reached, reset by software.

Bit 6 (CMPIF)   High-compared interrupt flag. Set when a change occurs in the output of Comparator, reset by software.

Bit 7   Unemployed, read as '0';

- RF can be cleared by instruction but cannot be set.

- IOCF0 is the interrupt mask register.

- Note that to read RF will result to "logic AND" of RF and IOCF0.

4.2.15   R10 ~ R3F

- All of these are 8-bit general-purpose registers.

4.2 Special Purpose Registers

4.2.1 A (Accumulator)

■ Internal data transfer, or instruction operand holding

■ It can not be addressed.

4.2.2 CONT (Control Register)

7	6	5	4	3	2	1	0
-	CMPIF	PWM2IF	PWM1IF	ADIF	EXIF	ICIF	TCIF

Bit 0 (PSR0) ~ Bit 2 (PSR2) TCC/WDT prescaler bits.

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3 (PAB) Prescaler assignment bit.

      0: TCC;

      1: WDT.

Bit 4 (TE) TCC signal edge

      0: increment if the transition from low to high takes place on the TCC pin;

      1: increment if the transition from high to low takes place on the TCC pin.

Bit 5 (TS) TCC signal source

      0: internal instruction cycle clock. If P54 is used as I/O pin, TS must be 0.

      1: transition on the TCC pin

Bit 6 (INT) Interrupt enable flag

      0: masked by DISI or hardware interrupt

      1: enabled by the ENI/RETI instructions

Bit 7 (INTE) INT signal edge

      0: interrupt occurs at the rising edge on the INT pin

      1: interrupt occurs at the falling edge on the INT pin

CONT register is both readable and writable.

4.2.3 IOC50 ~ IOC60 (I/O Port Control Register)

"1" puts the relative I/O pin into high impedance, while "0" defines the relative I/O pin as output.

IOC50 and IOC60 registers are both readable and writable.

4.2.4   IOC90 (GCON: I/O Configuration & Control of ADC)

7	6	5	4	3	2	1	0
OP2E	OP1E	G22	G21	G20	G12	G11	G10

Bit 7 (OP2E) Enable the gain amplifier which input is connected to P64 and output is connected to the 8-1 analog switch.

0 = OP2 is off (default value), and bypasses the input signal to the ADC;

1 = OP2 is on.

Bit 6 (OP1E) Enable the gain amplifier whose input is connected to P60 and output is connected to the 8-1 analog switch.

0 = OP1 is off (default value), and bypasses the input signal to the ADC;

1 = OP1 is on.

Bit 5:Bit 3 (G22 and G20): Select the gain of OP2.

000 = IS x 1 (default value);

001 = IS x 2;

010 = IS x 4;

011 = IS x 8;

100 = IS x 16;

101 = IS x 32;

Legend: IS = the input signal

Bit 2:Bit 0 (G12 and G10): Select the gain of OP1.

000 = IS x 1 (default value);

001 = IS x 2;

010 = IS x 4;

011 = IS x 8;

100 = IS x 16;

101 = IS x 32;

Legend: S = the input signal

4.2.5 IOCA0 (AD-CMPCON)

7	6	5	4	3	2	1	0
VREFS	CE	COE	IMS2	IMS1	IMS0	CKR1	CKR0

Bit 7: The input source of the Vref of the ADC.

0 = The Vref of the ADC is connected to Vdd (default value), and the P53/VREF pin carries out the function of P53;

1 = The Vref of the ADC is connected to P53/VREF.

Bit 6 (CE): Comparator enable bit

0 = Comparator is off (default value);

1 = Comparator is on.

Bit 5 (COE): Set P57 as the output of the comparator

0 = the comparator acts as an OP if CE=1.

1 = act as a comparator if CE=1.

Bit4:Bit2 (IMS2:IMS0):

Input Mode Select. ADC configuration definition bit. The following Table describes how to define the characteristic of each pin of R6.

Description of AD Configuration Control Bits

IMS2:IMS0	P60	P61	P62	P63	P64	P65	P66	P67
000	A	D	D	D	D	D	D	D
001	A	A	D	D	D	D	D	D
010	A	A	A	D	D	D	D	D
011	A	A	A	A	D	D	D	D
100	A	A	A	A	A	D	D	D
101	A	A	A	A	A	A	D	D
110	A	A	A	A	A	A	A	D
111	A	A	A	A	A	A	A	A

Bit 1: Bit 0 (CKR1: CKR0): The prescaler of oscillator clock rate of ADC

00 = 1: 4 (default value);

01 = 1: 16;

10 = 1: 64;

11 = The oscillator clock source of ADC is from WDT ring oscillator frequency.

(frequency=256/18ms   14.2Khz)

4.2.6 IOCB0 (Pull-down Control Register)

7	6	5	4	3	2	1	0
/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0

Bit 0 (/PD0) Control bit is used to enable the pull-down of the P60 pin.

> 0: Enable internal pull-down;

> 1: Disable internal pull-down.

Bit 1 (/PD1) Control bit is used to enable the pull-down of the P61 pin.

Bit 2 (/PD2) Control bit is used to enable the pull-down of the P62 pin.

Bit 3 (/PD3) Control bit is used to enable the pull-down of the P63 pin.

Bit 4 (/PD4) Control bit is used to enable the pull-down of the P64 pin.

Bit 5 (/PD5) Control bit is used to enable the pull-down of the P65 pin.

Bit 6 (/PD6) Control bit is used to enable the pull-down of the P66 pin.

Bit 7 (/PD7) Control bit is used to enable the pull-down of the P67 pin.

IOCB0 register is both readable and writable.

4.2.7 IOCC0 (Open-Drain Control Register)

7	6	5	4	3	2	1	0
/OD7	/OD6	/OD5	/OD4	/OD3	/OD2	/OD1	/OD0

Bit 0 (OD0) Control bit used to enable the open-drain of the P64 pin.

> 0: Enable open-drain output

> 1: Disable open-drain output

Bit 1 (OD1) Control bit is used to enable the open-drain of the P65 pin.

Bit 2 (OD2) Control bit is used to enable the open-drain of the P66 pin.

Bit 3 (OD3) Control bit is used to enable the open-drain of the P67 pin.

Bit 4 (OD4) Control bit is used to enable the open-drain of the P51 pin.

Bit 5 (OD5) Control bit is used to enable the open-drain of the P52 pin.

Bit 6 (OD6) Control bit is used to enable the open-drain of the P54 pin.

Bit 7 (OD7) Control bit is used to enable the open-drain of the P57 pin.

IOCC0 register is both readable and writable.

4.2.8 IOCD0 (Pull-high Control Register)

7	6	5	4	3	2	1	0
/PH7	/PH6	/PH5	-	/PH3	/PH2	/PH1	/PH0

Bit 0 (/PH0)   Control bit is used to enable the pull-high of the P60 pin.

0: Enable internal pull-high;

1: Disable internal pull-high.

Bit 1 (/PH1)   Control bit is used to enable the pull-high of the P61 pin.

Bit 2 (/PH2)   Control bit is used to enable the pull-high of the P62 pin.

Bit 3 (/PH3)   Control bit is used to enable the pull-high of the P63 pin.

Bit 4   Not used.

Bit 5 (/PH5)   Control bit is used to enable the pull-high of the P53 pin.

Bit 6 (/PH6)   Control bit is used to enable the pull-high of the P55 pin.

Bit 7 (/PH7)   Control bit is used to enable the pull-high of the P56 pin.

IOCD0 register is both readable and writable.

4.2.9 IOCE0 (WDT Control Register)

7	6	5	4	3	2	1	0
WDTE	EIS	-	-	-	-	-	-

Bit 7 (WDTE) Control bit is used to enable Watchdog Timer.

0: Disable WDT;

1: Enable WDT.

WDTE is both readable and writable

Bit 6 (EIS)   Control bit is used to define the function of the P50 (/INT) pin.

0: P50, input pin only;

1: /INT, external interrupt pin. In this case, the I/O control bit of P50 (bit 0 of IOC50) must be set to "1".

When EIS is "0", the path of /INT is masked. When EIS is "1", the status of /INT pin can also be read by way of reading Port 5 (R5). Refer to Fig. 7.

EIS is both readable and writable.

Bits 0~5   Not used.

(This specification is subject to change without further notice)

4.2.10 IOCF0 (Interrupt Mask Register)

7	6	5	4	3	2	1	0
-	CMPIE	PWM2IE	PWM1IE	ADIE	EXIE	ICIE	TCIE

Bit 0 (TCIE)   TCIF interrupt enable bit.

0: disable TCIF interrupt

1: enable TCIF interrupt

Bit 1 (ICIE)   ICIF interrupt enable bit.

0: disable ICIF interrupt

1: enable ICIF interrupt

Bit 2 (EXIE)   EXIF interrupt enable bit.

0: disable EXIF interrupt

1: enable EXIF interrupt

Bit 3 (ADIE)   ADIF interrupt enable bit.

0: disable ADIF interrupt

1: enable ADIF interrupt

Bit 4 (PWM1IE) PWM1IF interrupt enable bit.

0: disable PWM1 interrupt

1: enable PWM1 interrupt

Bit 5 (PWM2IE) PWM2IF interrupt enable bit.

0: disable PWM2 interrupt

1: enable PWM2 interrupt

Bit 6 (CMPIE) CMPIF interrupt enable bit.

0: disable CMPIF interrupt

1: enable CMPIF interrupt

Bit 7:   Unimplemented, read as '0'.

Individual interrupt is enabled by setting its associated control bit in the IOCF0 to "1".

Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Fig. 11.

IOCF0 register is both readable and writable.

4.2.11 IOC51 (PWMCON)

7	6	5	4	3	2	1	0
PWM2E	PWM1E	T2EN	T1EN	T2P1	T2P0	T1P1	T1P0

Bit 7 (PWM2E): PWM2 enable bit

0 = PWM2 is off (default value), and its related pin carries out the P52 function.

1 = PWM2 is on, and its related pin will be set to output automatically.

Bit 6 (PWM1E): PWM1 enable bit

0 = PWM1 is off (default value), and its related pin carries out the P51 function;

1 = PWM1 is on, and its related pin will be set to output automatically.

Bit 5 (T2EN): TMR2 enable bit

0 = TMR2 is off (default value).

1 = TMR2 is on.

Bit 4 (T1EN): TMR1 enable bit

0 = TMR1 is off (default value).

1 = TMR1 is on.

Bit 3: Bit 2 (T2P1:T2P0): TMR2 clock prescale option bits.

T2P1	T2P0	Prescale
	0	1:2(Default)
0	1	1:8
1	0	1:32
1	1	1:64

Bit 1 : Bit 0 (T1P1:T1P0): TMR1 clock prescale option bits.

T1P1	T1P0	Prescale
0	0	1:2(Default)
0	1	1:8
1	0	1:32
1	1	1:64

4.2.12 IOC61 (DT1L: the Least Significant Byte (Bit 7 ~ Bit 0) of Duty Cycle of PWM1)

A specified value keeps the output of PWM1 to stay at high until the value matches with TMR1.

4.2.13 IOC71 (DT1H: the Most Significant Byte (Bit 1 ~ Bit 0) of Duty Cycle of PWM1)

7	6	5	4	3	2	1	0
CALI1	SIGN1	VOF1[2]	VOF1[1]	VOF1[0]	-	PWM1[9]	PWM1[8]

Bit 7 (CALI1): Calibration enable bit

0 = Calibration disable;

1 = Calibration enable.

Bit 6 (SIGN1): Polarity bit of offset voltage

0 = Negative voltage;

1 = Positive voltage.

Bit 5:Bit 3 (VOF1[2]:VOF1[0]): Offset voltage bits.

Bit 1:Bit 0 (PWM1[9]:PWM1[8]): The Most Significant Byte of PWM1 Duty Cycle

A specified value keeps the PWM1 output to stay at high until the value matches with TMR1.

4.2.14 IOC81 (PRD1: Period of PWM1)

The content of IOC81 is a period (time base) of PWM1. The frequency of PWM1 is the reverse of the period.

4.2.15 IOC91 (DT2L: the Least Significant Byte (Bit 7 ~ Bit 0) of Duty Cycle of PWM2)

A specified value keeps the of PWM1 output to stay at high until the value matches with TMR2.

4.2.16 IOCA1 (DT2H: the Most Significant Byte (Bit 1 ~ Bit 0) of Duty Cycle of PWM2)

7	6	5	4	3	2	1	0
CALI2	SIGN2	VOF2[2]	VOF2[1]	VOF2[0]	-	PWM2[9]	PWM2[8]

Bit 7 (CALI2): Calibration enable bit

0 = Calibration disable;

1 = Calibration enable.

Bit 6 (SIGN2): Polarity bit of offset voltage

0 = Negative voltage;

1 = Positive voltage.

Bit 5:Bit 3 (VOF2[2]:VOF2[0]): Offset voltage bits

Bit 1:Bit 0 (PWM2[9]:PWM2[8]): The Most Significant Byte of PWM1 Duty Cycle

A specified value keeps the PWM2 output to stay at high until the value matches with TMR2.

4.2.17 IOCB1 (PRD2: Period of PWM2)

The content of IOCB1 is a period (time base) of PWM2. The frequency of PWM2 is the reverse of the period.

4.2.18 IOCC1 (DL1L: the Least Significant Byte (Bit 7 ~ Bit 0) of Duty Cycle Latch of PWM1)

The content of IOCC1 is read-only.

4.2.19 IOCD1 (DL1H: the Most Significant Byte (Bit 1 ~ Bit 0) of Duty Cycle Latch of PWM1)

The content of IOCD1 is read-only.

4.2.20 IOCE1 (DL2L: the Least Significant Byte (Bit 7 ~ Bit 0) of Duty Cycle Latch of PWM2)

The content of IOCE1 is read-only.

4.2.21 IOCF1 (DL2H: the Most Significant Byte (Bit 1 ~ Bit 0) of Duty Cycle Latch of PWM2)

The content of IOCF1 is read-only.

4.3 TCC/WDT & Prescaler

An 8-bit counter is available as prescaler for the TCC or WDT. The prescaler is available for either the TCC or WDT only at any given time, and the PAB bit of CONT register is used to determine the prescaler assignment. The PSR0~PSR2 bits determine the prescale ratio. The prescaler is cleared each time the instruction is written to TCC under TCC mode. The WDT and prescaler, when assigned to WDT mode, are cleared by the WDTC or SLEP instructions. Fig. 5 depicts the circuit diagram of TCC/WDT.

■ R1(TCC) is an 8-bit timer/counter. The TCC clock source can be internal or external clock input (edge selectable from TCC pin). If TCC signal source is from internal clock, TCC will increase by 1 at every instruction cycle (without prescaler). Referring to Fig. 5, selection of CLK=Fosc/2 or CLK=Fosc/4 depends on the CODE Option bit CLKS. CLK=Fosc/2 if CLKS bit is "0", and CLK=Fosc/4 if CLKS bit is "1".

■ If TCC signal source is from external clock input, TCC will increase by 1 at every falling edge or rising edge of TCC pin.

■ The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during the normal mode by software programming. Refer to WDTE bit of IOCE0 register. Without presacler, the WDT time-out period is approximately 18 ms**1**.
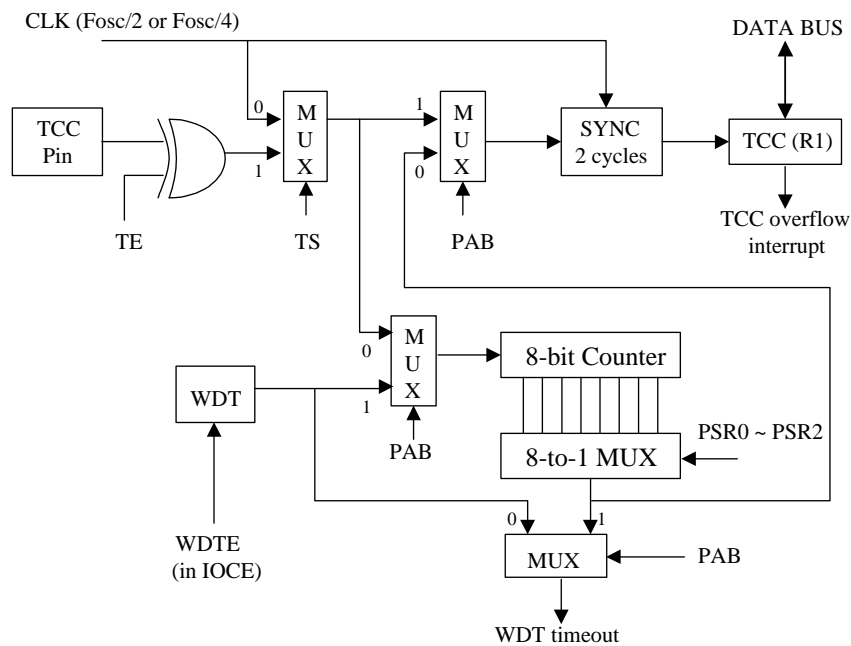
Fig. 5 Block Diagram of TCC and WDT

4.4   I/O Ports

Port 5, Port 6, and the I/O registers are bi-directional tri-state I/O ports. The function of Pull-high, Pull-down, and Open-drain can be set internally by IOCB0, IOCC0, and IOCD0, respectively. Port 6 features an input status changed interrupt (or wake-up) function. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC50 ~ IOC60). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 and Port 6 are shown in the following Fig. 6, Fig. 7, and Fig. 8 respectively.

---

[1] NOTE:VDD=5V,Setup time period = 16ms ± 5%.
        VDD=3V,Setup time period = 19ms ± 5%.
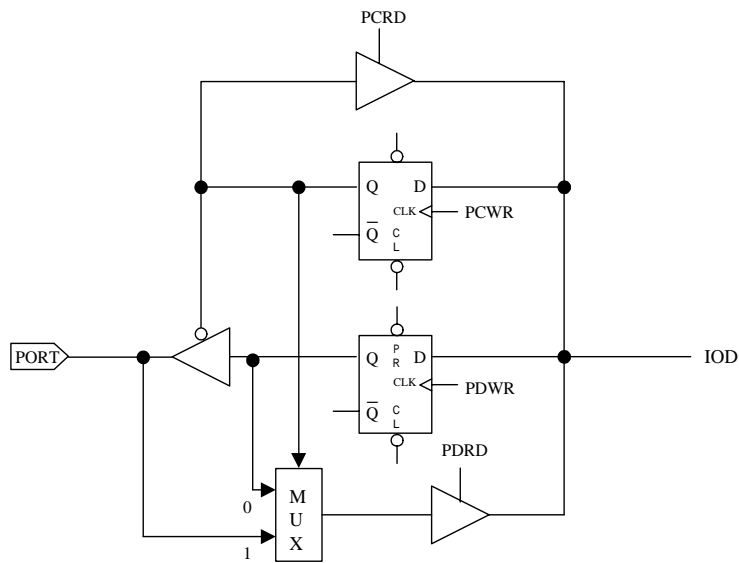
NOTE: Pull-down is not shown in the figure.
Fig. 6 The Ccircuit of I/O Port and I/O Control Register for Port 5
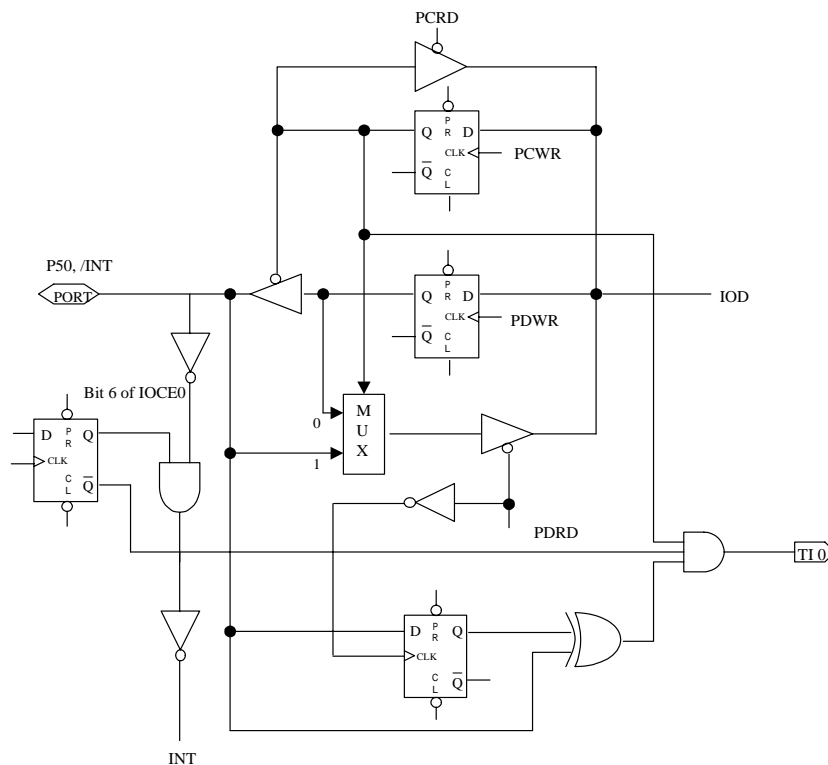
NOTE: Pull-high (down) and Open-drain are not shown in the figure.
Fig. 7 The Circuit of I/O Port and I/O Control Register for P50(/INT)
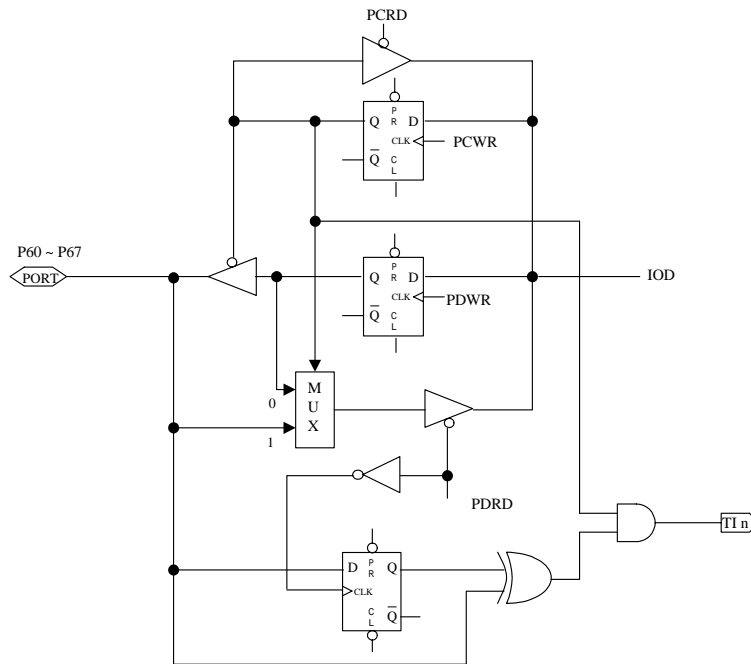
NOTE: Pull-high (down) and Open-drain are not shown in the figure.
Fig. 8 The Circuit of I/O Port and I/O Control Register for P60~P67
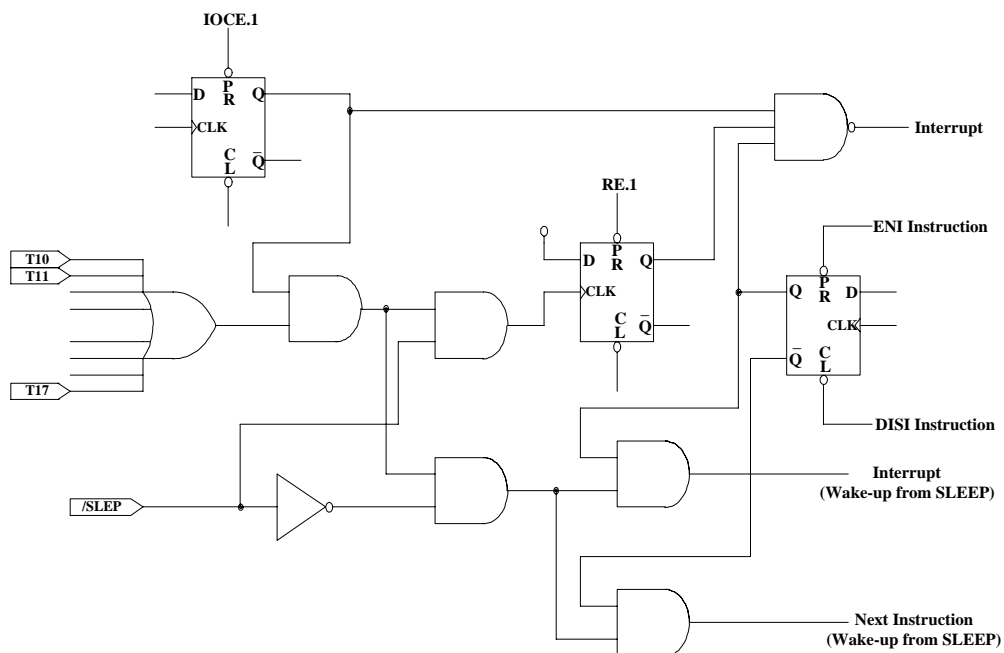
Fig. 9 Block Diagram of Port 6 with Input Changed Interrupt/Wake-up

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(This specification is subject to change without further notice)

Table 3 Usage of Port 6 Input Changed Wake-up/Interrupt Function

Usage of Port 6 Input Status Changed Wake-up/Interrupt	
(I) Wake-up from Port 6 Input Status Change	(II) Port 6 Input Status Change Interrupt
(a) Before SLEEP 　　1. Disable WDT 　　2. Read I/O Port 6 (MOV R6,R6) 　　3. Execute "ENI" or "DISI" 　　4. Enable interrupt (Set IOCF0.1) 　　5. Execute "SLEP" instruction (b) After wake-up 　　1. IF "ENI" $\rightarrow$ Interrupt vector (008H) 　　2. IF "DISI" $\rightarrow$ Next instruction	1. Read I/O Port 6 (MOV R6,R6) 2. Execute "ENI" 3. Enable interrupt (Set IOCF0.1) 4. IF Port 6 changed (interrupt) $\rightarrow$ Interrupt vector (008H)

4.5   RESET and Wake-up

4.5.1   The Function of RESET and Wake-up

A RESET is initiated by one of the following events-

(1) Power-on reset

(2) /RESET pin input "low", or

(3) WDT time-out (if enabled).

The device is kept in a RESET condition for a period of approximately 18ms (one oscillator start-up timer period) after the reset is detected. Once the RESET occurs, the following functions are performed.

■　　The oscillator is running, or will be started.

■　　The Program Counter (R2) is set to all "0".

■　　All I/O port pins are configured as input mode (high-impedance state).

■　　The Watchdog Timer and prescaler are cleared.

■　　When power is switched on, the upper 3 bits of R3 are cleared.

■　　The bits of the CONT register are set to all "1" except for the Bit 6 (INT flag).

■　　The bits of the IOCB0 register are set to all "1".

■　　The IOCC0 register is cleared.

■　　The bits of the IOCD0 register are set to all "1".

■　　Bit 7 of the IOCE0 register is set to "1", and Bit 6 is cleared.

■　　Bits 0~6 of RF register and bits 0~6 of IOCF0 register are cleared.

　　　Executing the "SLEP" instruction will assert the sleep (power down) mode. While entering sleep mode, the WDT (if enabled) is cleared but keeps on running. The controller can be awakened by-

(This specification is subject to change without further notice)

(1) External reset input on /RESET pin.

(2) WDT time-out (if enabled).

(3) Port 6 input status change (if enabled).

(4) Comparator high.

The first two cases will cause the EM78458/459 to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Case 3 is considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) decides whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the address 0x8 after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after wake-up.

Only one of the Cases 2, to 4 can be enabled before entering into sleep mode. That is,

[a] if Port 6 Input Status Change Interrupt is enabled before SLEP , WDT must be disabled by software. However, the WDT bit in the option register remains enabled. Hence, the EM78458/459 can be awakened only by Case 1 or 3.

[b] if WDT is enabled before SLEP, Port 6 Input Status Changed Interrupt must be disabled. Hence, the EM78458/459 can be awakened only by Case 1 or 2. Refer to the section on Interrupt for further details.

[c] if Comparator High Interrupt is enabled before SLEP, WDT must be disabled by software. However, the WDT bit in the option register remains enabled. Hence, the EM78458/459 can be awakened only by Case 1 or 4.

If Port 6 Input Status Change Interrupt is used to wake up the EM78458/459 (as in Case [a] above), the following instructions must be executed before SLEP:

```
MOV A, @0Bxx000110      ; Select internal TCC clock
CONTW
CLR R1                  ; Clear TCC and prescaler
MOV A, @0Bxxxx1110      ; Select WDT prescaler
CONTW
WDTC                    ; Clear WDT and prescaler
MOV A, @0B0xxxxxxx      ; Disable WDT
IOW RE
MOV R6, R6              ; Read Port 6
MOV A, @0B00000x1x      ; Enable Port 6 input change interrupt
IOW RF
ENI (or DISI)           ; Enable (or disable) global interrupt
SLEP                    ; Sleep
NOP
```

Similarly, if the Comparator High Interrupt is used to wake up the EM78458/459 (as in Case [c] above), the following instructions must be executed before SLEP:

```
MOV A, @0Bxx000110        ; Select internal TCC clock
CONTW
CLR R1                    ; Clear TCC and prescaler
MOV A, @0Bxxxx1110        ; Select WDT prescaler
CONTW
WDTC                      ; Clear WDT and prescaler
MOV A, @0B0xxxxxxx        ; Disable WDT
IOW RE
MOV A, @0B01xxxxxx        ; Enable comparator high interrupt
IOW RF
ENI (or DISI)            ; Enable (or disable) global interrupt
SLEP                      ; Sleep
NOP
```

One problem user must be aware of, is that after waking up from the sleep mode, the WDT function will enable automatically. The WDT operation (being enabled or disabled) should be handled appropriately by software after waking up from the sleep mode.

4.5.2 The Status of T, and P of STATUS Register

A RESET condition is initiated by one of the following events:

(1) A power-on condition,

(2) A high-low-high pulse on /RESET pin, or

(3) Watchdog Timer time-out.

The values of T and P, as listed in Table 5 below, are used to check how the processor wakes up. Table 6 shows the events, which may affect the status of T and P.

Table 4   The Values of RST, T, and P after RESET

Reset Type	T	P
Power-on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during SLEEP mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during SLEEP mode	0	0
Wake-up on pin change during SLEEP mode	1	0

*P: Previous status before reset

Table 5 The Status of RST, T and P being Affected by Events

Event	T	P
Power-on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin changed during SLEEP mode	1	0

*P: Previous value before reset
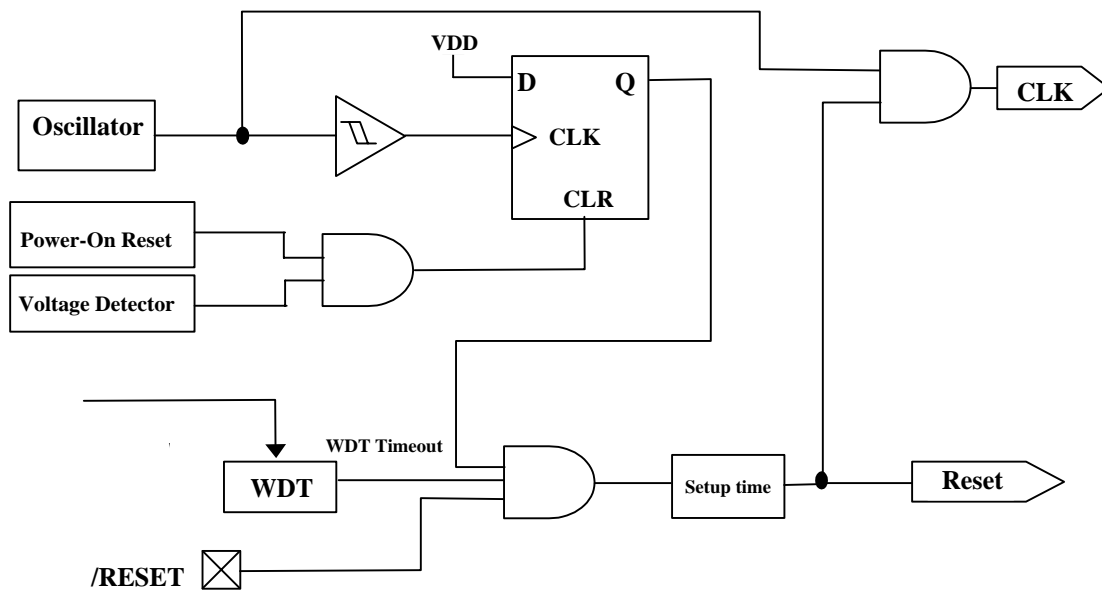
Fig. 10 Block Diagram of Reset of Controller

4.6   Interrupt

The EM78458/459 has six interrupts as listed below:

(1) TCC overflow interrupt

(2) Port 6 Input Status Change Interrupt

(3) External interrupt [(P50, /INT) pin].

(4) Analog to Digital conversion completed.

(5) When TMR1/TMR2 matches with PRD1/PRD2 respectively in PWM.

(6) When the comparators output changes.

Before the Port 6 Input Status Change Interrupt is enabled, reading Port 6 (e.g. "MOV R6,R6") is necessary. Each Port 6 pin will have this feature if its status changes. Any pin configured as output or P50 pin configured as /INT, is excluded from this function. Port 6 Input Status Change Interrupt will wake up the EM78458/459 from the sleep mode if it is enabled prior to going into the sleep mode by executing SLEP. When the controller is wake-up, it will continue to execute the succeeding program if the global

interrupt is disabled, or branches out to the interrupt vector 008H if the global interrupt is enabled.

RF, the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF0 is an interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (when enabled) occurs, the next instruction will be fetched from address 008H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or the execution of ENI. Note that the outcome of RF will be the logic AND of RF and IOCF0 (refer to Fig. 11). The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

When an interrupt is generated by the INT instruction (when enabled), the next instruction will be fetched from address 001H.
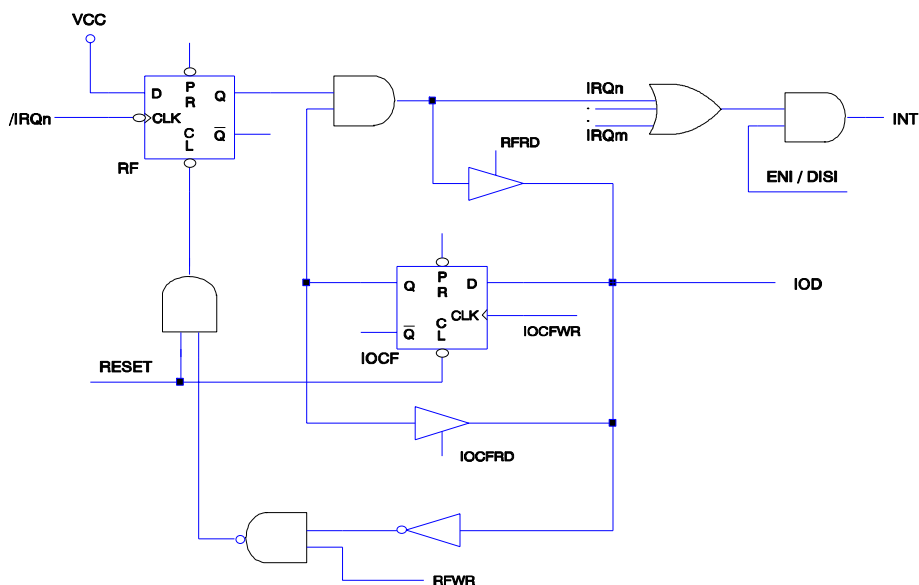
Fig. 11 Interrupt Input Circuit

4.7   Analog-To-Digital Converter (ADC)

The analog-to-digital circuitry consists of an 8-bit analog multiplexer, three control registers (ADCON/R9, AD-CMP-CON/IOCA0, GCON/IOC90), one data register (ADDATA/RA) and an ADC with 8-bit resolution. The functional block diagram of the ADC is shown in Fig. 12. The analog reference voltage (Vref) and analog ground are connected via separate input pins.

The ADC module utilizes successive approximation to convert the unknown analog signal into a digital value. The result is fed to the ADDATA. Input channels are

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selected by the analog input multiplexer via the ADCON register Bits ADIS0, ADIS1, and ADIS2.
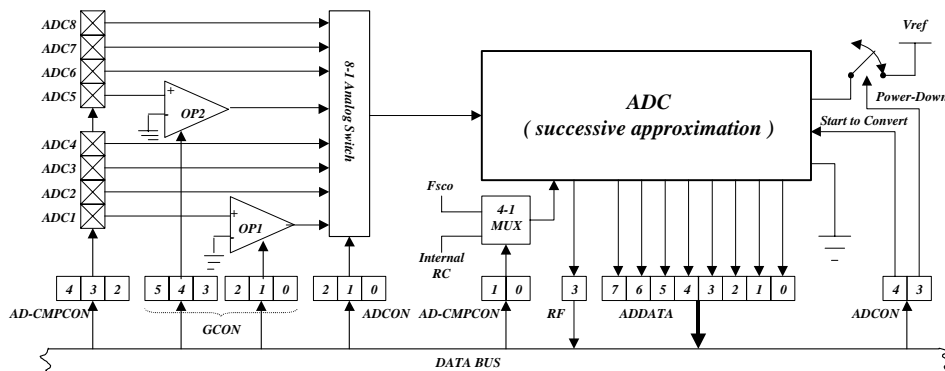
Fig. 12 The Functional Block Diagram of Analog-to-Digital Conversion

4.7.1 ADC Control Register (ADCON/R9, AD-CMP-CON/IOCA0, GCON/IOC90)

4.7.1.1 ADCON/R9

The ADCON register controls the operation of the A/D conversion and decides which pin should be currently active.

BIT	7	6	5	4	3	2	1	0
SYMBOL	-	-	IOCS	ADRUN	ADPD	ADIS2	ADIS1	ADIS0
*Init_Value	0	0	0	0	0	0	0	0

*Init_Value: Initial value at power on reset

ADRUN (bit 4): ADC starts to RUN.

> 1 = an A/D conversion is started. This bit can be set by software.

> 0 = reset on completion of the conversion. This bit can not be reset in software.

ADPD (bit 3): ADC Power-down Mode.

> 1 = ADC is operating;

> 0 = switch off the resistor reference to save power even when the CPU is operating

(This specification is subject to change without further notice)

ADIS2~ADIS0 (bit 2~0): Analog Input Select.

000 = AN0;

001 = AN1;

010 = AN2;

011 = AN3;

100 = AN4;

101 = AN5;

110 = AN6;

111 = AN7;

Change occurs only when the ADIF bit and the ADRUN bit are both LOW.

4.7.1.2 AD-CMP-CON/IOCA0

The AD-CMP-CON register defines the pins of Port 6 as analog inputs or as digital I/O, individually.

BIT	7	6	5	4	3	2	1	0
SYMBOL	VREFS	CE	COE	IMS2	IMS1	IMS0	CKR1	CKR0
*Init_Value	0	0	0	0	0	0	0	0

*Init_Value: Initial value at power on reset

■ VREFS (Bit 7): The input source of the Vref of the ADC.

  0 = The Vref of the ADC is connected to Vdd (default value), and the P53/VREF pin carries out the function of P53;

  1 = The Vref of the ADC is connected to P53/VREF.

■ CE (Bit 6): Control bit used to enable comparator.

  0 = Disable comparator

  1 = Enable comparator

■ COE (Bit 5): Set P57 as the output of the comparator

  0 = the comparator acts as an OP if CE=1.

  1 = act as a comparator if CE=1.

■ IMS2~IMS0 (Bit 4 ~ Bit 2): ADC configuration definition bit.

■ CKR1 and CKR0 (Bit 1 and Bit 0): The conversion time select.

  00 = Fosc/4;

  01 = Fosc/16;

  10 = Fsco/64;

  11 = The oscillator clock source of ADC is from WDT ring oscillator frequency.

  (frequency=256/18ms   14.2Khz)

(This specification is subject to change without further notice)

4.7.1.3 GCON/IOC90

As shown in Fig. 12, OP1 and OP2, the gain amplifiers, are located in the middle of the analog input pins (ADC1 and ADC5) and the 8-1analog switch. The GCON register controls the gains.

Table 6 Table 7 Shows the Gains and the Operating Range of ADC.

BIT	7	6	5	4	3	2	1	0
SYMBOL	OP2E	OP1E	G22	G21	G20	G12	G11	G10
*Init_Value	0	0	0	0	0	0	0	0

Table 7 The Gains and the Operating Range of ADC

G10:G12/G20:G22	Gain	Range of Operating Voltage
000	1	0 ~ Vref
001	2	0 ~ (1/2)Vref-
010	4	0 ~ (1/4)Vref
011	8	0 ~ (1/8)Vref
100	16	0 ~ (1/16)Vref
101	32	0 ~ (1/32)Vref

NOTE
Vref can not be less than 3 volts.

4.7.2 ADC Data Register (ADDATA/RA)

When the A/D conversion is complete, the result is loaded to the ADDATA. The START/END bit is clear, and the ADIF is set.

4.7.3 A/D Sampling Time

The accuracy, linearity, and speed of the successive approximation A/D converter are dependent on the properties of the ADC and the comparator. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 1 μs for each KΩ of the analog source impedance and at least 1 μs for the low-impedance source. After the analog input channel is selected, this acquisition time must be done before the conversion can be started.

4.7.4 A/D Conversion Time

CKR0 and CKR1 select the conversion time (Tct), in terms of instruction cycles. This allows the MCU to run at the maximum frequency without sacrificing the accuracy of A/D conversion. For the EM78458/459, the conversion time per bit is about 4μs. Table 8 shows the relationship between Tct and the maximum operating frequencies.

Table 8 Tct vs. the Maximum Operation Frequency

CKR0:CKR1	Operation Mode	Max. operation frequency
00	Fsco/4	1 MHz
01	Fsco/16	4 MHz
10	Fsco/64	16MHz
11	Internal RC	-

4.7.5 A/D Operation During Sleep Mode

In order to reduce power consumption, the A/D conversion remains operational during sleep mode, and is obligated to implement the internal RC clock source mode. As the SLEP instruction is executed, all the operations of the MCU will stop except for the A/D conversion. The RUN bit will be cleared and the result will be fed to the ADDATA when the conversion is completed. If the ADIE is enabled, the device will wake up. Otherwise, the A/D conversion will be shut off, no matter what the status of ADPD bit is.

4.7.6 Programming Steps/Considerations

4.7.6.1 Programming steps

Follow these steps to obtain data from the ADC:

(1) Write to the three bits (IMS2:IMS0) on the AD-CMP-CON1 register to define the characteristics of R6: Digital I/O, analog channels, and voltage reference pin;

(2) Write to the ADCON register to configure AD module:

   (a) Select A/D input channel (ADAS2:ADAS0);

   (b) Select the proper gains by writing to the GCON register (optional);

   (c) Define A/D conversion clock rate (CKR1:CKR0);

   (d) Set the ADPD bit to 1 to begin sampling.

(3) Put "ENI" instruction, if the interrupt function is employed.

(4) Set the ADRUN bit to 1.

(5) Wait for either the interrupt flag to be set or the ADC interrupt to occur.

(6) Read ADDATA, the conversion data register.

(7) Clear the interrupt flag bit (ADIF).

(8) For next conversion, go to Step 1 or Step 2 as required. At least 2 Tct is required before next acquisition starts.

NOTE
To obtain an accurate value, it is necessary to avoid any data transition on I/O pins during AD conversion.

(This specification is subject to change without further notice)

4.7.6.2 The Demonstration Programs

; To define the general registers

R_0 == 0   ; Indirect addressing register

PSW == 3   ; Status register

PORT5 == 5

PORT6 == 6

R_F== 0XF   ; Interrupt status register

; To define the control register

IOC50 == 0X5   ; Control Register of Port 5

IOC60 == 0X6   ; Control Register of Port 6

C_INT== 0XF   ; Interrupt Control Register

;ADC Control Registers

ADDATA == 0xA   ; The contents are the results of ADC

ADCON R== 0x9;	7	6	5	4	3	2	1	0
;		-	-	IOCS	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

ADCONC== 0xA;	7	6	5	4	3	2	1	0
;		VREFS	X	X	IMS2	IMS1	IMS0	CKR1	CKR0

GCON == 0x9;	7	6	5	4	3	2	1	0
;		OPE2	OPE1	G22	G21	G20	G12	G11	G10

;To define bits

;In ADCONR

ADRUN == 0x4   ; ADC is executed as the bit is set

ADPD == 0x3   ; Power Mode of ADC

ORG 0; Initial address

JMP INITIAL;

ORG 0x08; Interrupt vector

(User program)

CLR R_F	; To clear the ADCIF bit
BS ADCONR, ADRUN	; To start to execute the next AD conversion if necessary
RETI	
INITIAL:	
MOV A, @0bXXXX1XXX	; Enable the interrupt function of ADC, "X" by application
IOW C_INT	
MOV A, @0xXX	; Interrupt disabled:<6>
CONTW	
MOV A, @0b00000000	; To employ Vdd as the reference voltage, to define P60
as	IOW ADCONC; an analog input and set clock rate at
fosc/4	
En_ADC:	
MOV A, @0xXXXXXXX1	; To define P60 as an input pin, and the others are
dependent	
IOW PORT6	; on applications
MOV A, @0b01000101	; To enable the OP1, and set the gain as 32
IOW GCON	
BS ADCONR, ADPD	; To disable the power-down mode of ADC
ENI	; Enable the interrupt function
BS ADCONR, ADRUN	; Start to run the ADC

; If the interrupt function is employed, the following three lines may be ignored

POLLING:	
JBC ADCONR, ADRUN	; To check the ADRUN bit continuously;
JMP POLLING	; ADRUN bit will be reset as the AD conversion is
completed	

(User program)

:

:

:

4.8 Dual Sets of PWM (Pulse Width Modulation)

4.8.1 Overview

In PWM mode, both PWM1 and PWM2 pins produce up to a 10-bit resolution PWM output (see. Fig. 13 for the functional block diagram). A PWM output has a period and a duty cycle, and it keeps the output in high. The baud rate of the PWM is the inverse of the period. Fig. 14 depicts the relationships between a period and a duty cycle.
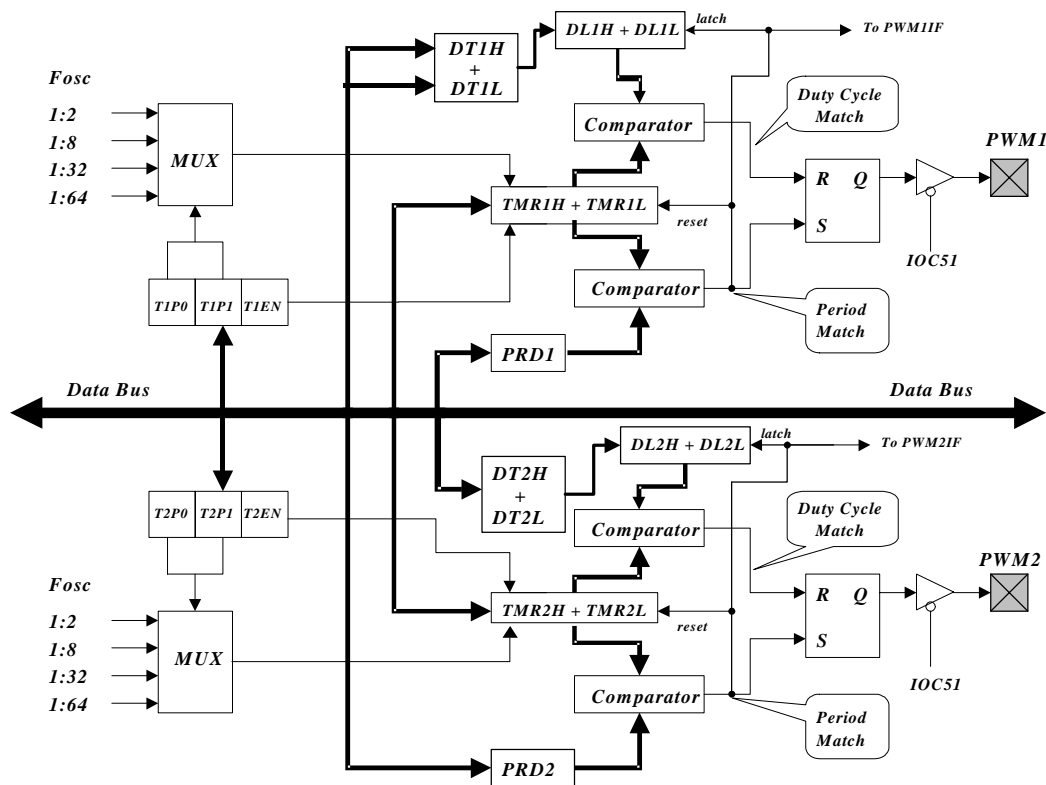
Fig. 13 The Functional Block Diagram of the Dual PWMs
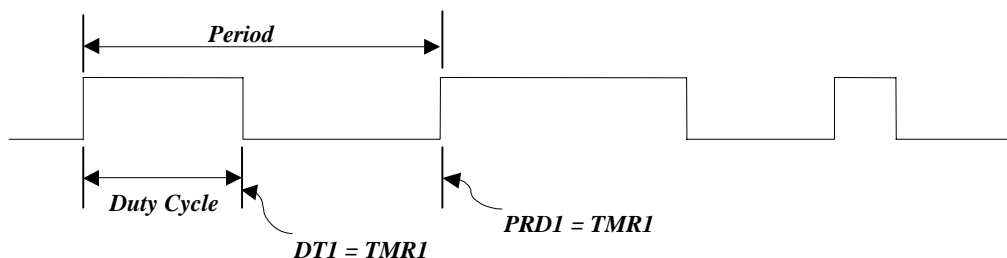
Fig. 14 The Output Timing of the PWM

4.8.2 Increment Timer Counter (TMRX: TMR1H/TWR1L or TMR2H/TWR2L)

TMRX are ten-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read, written, and cleared at any reset conditions. If employed, they can be turned down for power saving by setting T1EN bit [PWMCON<4>] or T2EN bit [PWMCON<5>] to 0.

4.8.3 PWM Period (PRDX : PRD1 or PRD2)

The PWM period is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

■ TMRX is cleared.

■ The PWMX pin is set to 1.

■ The PWM duty cycle is latched from DT1/DT2 to DTL1/DTL2.

NOTE
The PWM output will not be set, if the duty cycle is 0;

■ The PWMXIF pin is set to 1.

The following formula describes how to calculate the PWM period:

PERIOD = (PRDX + 1) * 4 * (1/Fosc) * (TMRX prescale value)

4.8.4 PWM Duty Cycle (DTX: DT1H/ DT1L and DT2H/ DT2L; DTL: DL1H/DL1L and DL2H/DL2L)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded at any time. However, it cannot be latched into DTL until the current value of DLX is equal to TMRX.

The following formula describes how to calculate the PWM duty cycle:

Duty Cycle = (DTX) * (1/Fosc) * (TMRX prescale value)

4.8.5 Comparator X

To change the output status while the match occurs, the TMRXIF flag will be set at the same time.

4.8.6 PWM Programming Procedures/Steps

(1) Load PRDX with the PWM period.

(2) Load DTX with the PWM Duty Cycle.

(3) Enable interrupt function by writing IOCF0, if required.

---

(4) Set PWMX pin to be output by writing a desired value to IOC51.

(5) Load a desired value to IOC51 with TMRX prescaler value and enable both PWMX and TMRX.

4.9 Timer

4.9.1 Overview

Timer1 (TMR1) and Timer2 (TMR2) (TMRX) are 10-bit clock counters with programmable prescalers, respectively. They are designed for the PWM module as baud rate clock generators. TMRX can be read, written, and cleared at any reset conditions.

4.9.2 Function description

Fig. 15 shows TMRX block diagram. Each signal and block are described as follows:

TMR1X = TMR1H + TMR1L;
TMR2X = TMR2H +TMR2L
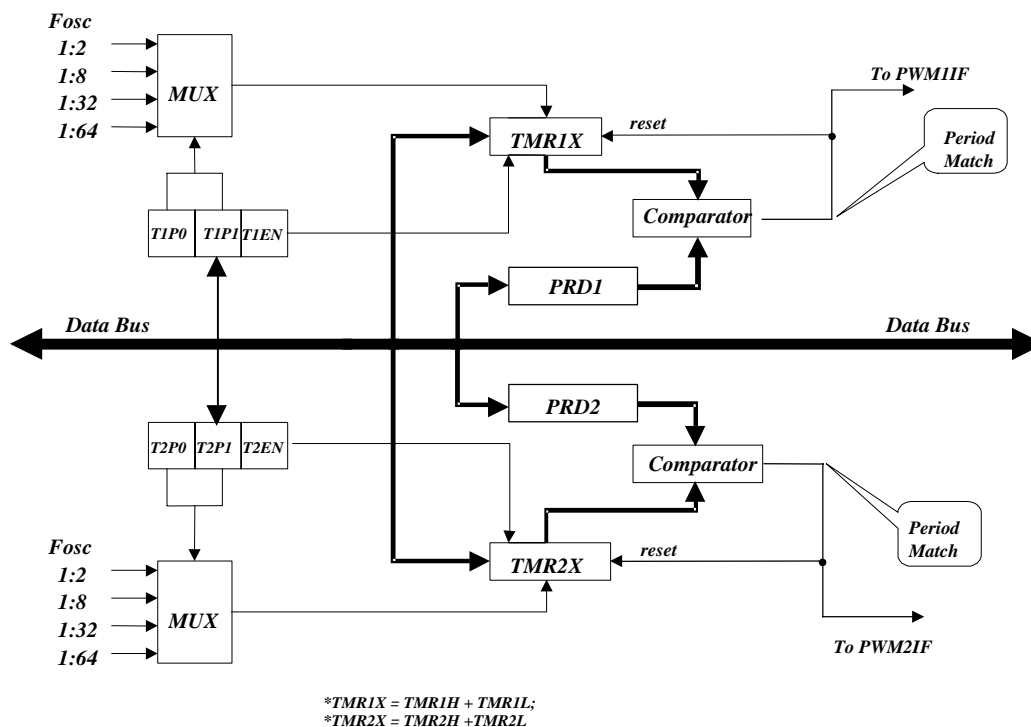
Fig. 15 TMRX Block Diagram

Fosc: Input clock.

Prescaler (T1P0 and T1P1/T2P1 and T2P0): Options of 1:2, 1:8, 1:32, and 1:64 are defined by TMRX. It is cleared when any type of reset occurs.

TMR1X and TMR2X (TMR1H/TWR1L and TMR2H/TMR2L):Timer X register; TMRX is increased until it matches with PRDX, and then is reset to 0. TMRX cannot be read.

PRDX (PRD1 and PRD2): PWM period register.

ComparatorX (Comparator 1 and Comparator 2): To reset TMRX while a match occurs and the TMRXIF flag is set at the same time.

4.9.3 Programming the Related Registers

When defining TMRX, refer to the related registers of its operation as shown in Table 9.It must be noted that the PWMX bits must be disabled if their related TMRXs are employed. That is, bit 7 and bit 6 of the PWMCON register must be set to '0'.

Table 9 Related Control Registers of TMR1 and TMR2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC51	PWMCON/IOC51	PWM2E	PWM1E	T2EN	T1EN	T2P1	T2P0	T1P1	T1P0

4.9.4 Timer programming procedures/steps

(1) Load PRDX with the TIMER period.

(2) Enable interrupt function by writing IOCF0, if required

(3) Load a desired value to PWMCON with the TMRX prescaler value and enable both TMRX and disable PWMX.

4.10 Comparator

EM78458/459 has one comparator, which has two analog inputs and one output. The comparator can be employed to wake up from the sleep mode. Fig. 16 shows the circuit of the comparator.
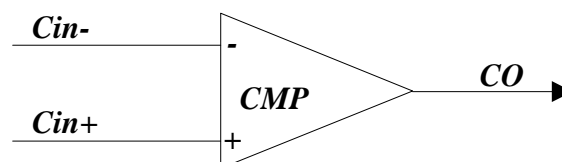
Fig. 16 Comparator Operating Mode

4.10.1 External Reference Signal

The analog signal that is presented at Cin- compares to the signal at Cin+, and the digital output (CO) of the comparator is adjusted accordingly.

■   The reference signal must be between Vss and Vdd.

■   The reference voltage can be applied to either pi of comparator.

■   Threshold detector applications may be of the same reference.

■   The comparator can operate from the same or different reference source.

4.10.2   Comparator Outputs

■   The compared result is stored in the CMPOUT of R3.

■   The comparator outputs is output to P57 by programming bit5<COE> of the AD-CMPCON register to 1.

■   P57 must be defined as an output if implemented as the comparator output.

■   Fig. 17 shows the comparator output block diagram.
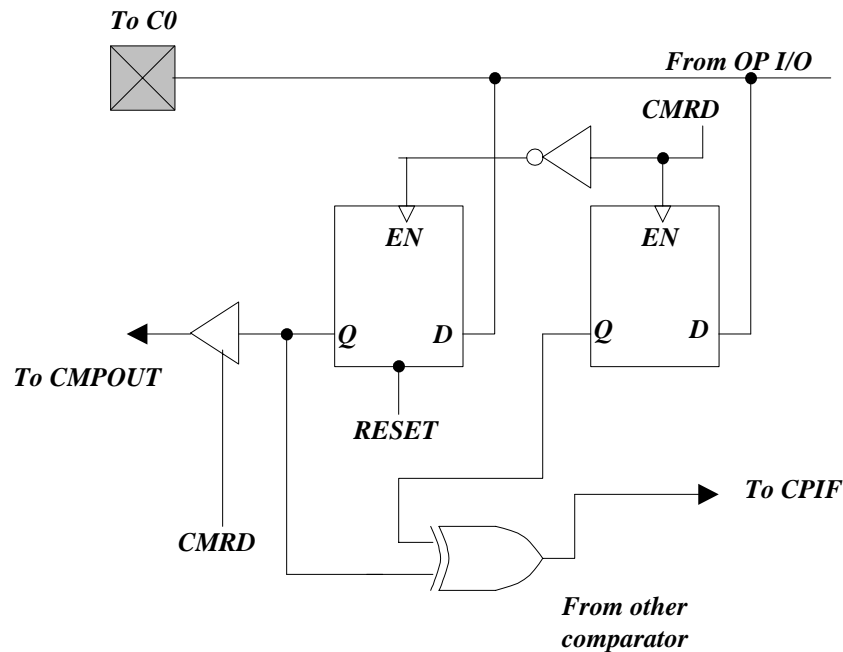
Fig. 17 The Output Configuration of a Comparator

4.10.3   Using as An Operation Amplifier

The comparator can be used as an operation amplifier if a feedback resistor is connected from the input to the output externally. In this case, the Schmitt trigger can be disabled for power saving by setting CE to 1 and COE to 0.

4.10.4   Interrupt

■   CMPIE (IOCF0.6) must be enabled.

■   Interrupt occurs at the rising edge of the comparator output pin.

■   The actual change on the pin can be determined by reading the Bit CMPOUT, R3<7>.

■   CMPIF (RF.6), the comparator interrupt flag, can only be cleared by software.

4.10.5 Wake-up from SLEEP Mode

■ If enabled, the comparator remains active and the interrupt remains functional, even under SLEEP mode.

■ If a mismatch occurs, the interrupt will wake up the device from SLEEP mode.

■ The power consumption should be taken into consideration for the benefit of energy conservation.

■ If the function is unemployed during SLEEP mode, turn off comparator before entering into sleep mode.

4.11 The Initialized Values after Reset

Table 10 The Summary of the Initialized Values for Registers

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC50	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOC60	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCB0	Bit Name	/PD7	/PD6	*/PD5	*/PD4	/PD3	/PD2	/PD1	/PD0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCC0	Bit Name	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCD0	Bit Name	/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCE0	Bit Name	WDTE	EIS	X	X	X	X	X	X
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	1	1	1	1	1	1

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOCF0	Bit Name	X	CMPIE	PMW2IE	PWM1IE	ADIE	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	0	P	P	P	P	P	P	P
N/A	IOC90 (GCON)	Bit Name	OP2E	OP1E	G22	G21	G20	G12	G11	G10
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCA0 (AD-CMP CON)	Bit Name	VREFS	CE	COE	IMS2	IMS1	IMS0	CKR1	CKR0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	
N/A	IOC51 (PWMCON)	Bit Name	PWM2E	PWM2E	T2EN	T1EN	T2P1	T2P0	T1P1	
		Power-on	0	0	0	0	0	0	0	
		/RESET and WDT	0	0	0	0	0	0	0	
		Wake-up from Pin Changed	P	P	P	P	P	P	P	
N/A	IOC61 (DT1L)	Bit Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	
		Power-on	0	0	0	0	0	0	0	
		/RESET and WDT	0	0	0	0	0	0	0	
		Wake-up from Pin Changed	P	P	P	P	P	P	P	
N/A	IOC71 (DT1H)	Bit Name	CALI1	SIGN1	VOF1[2]	VOF1[1]	VOF1[0]	X	Bit1	
		Power-on	0	1	1	0	0	0	0	
		/RESET and WDT	0	1	1	0	0	0	0	
		Wake-up from Pin Changed	P	P	P	P	P	0	P	
N/A	IOC81 (PRD1)	Bit Name	-	-	-	-	-	-	-	
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOC91 (DT2L)	Bit Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCA1 (DT2H)	Bit Name	CALI2	SIGN2	VOF2[2]	VOF2[1]	VOF2[0]	X	Bit1	Bit0

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Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	0	1	1	0	0	0	0	0
		/RESET and WDT	0	1	1	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	0	P	P
N/A	IOCB1 (PRD2)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCC1 (DL1L)	Bit Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCD1 (DL1H)	Bit Name	X	X	X	X	X	X	Bit1	Bit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	0	0	0	0	0	0	P	P
N/A	IOCE1 (DL2L)	Bit Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	IOCF1 (DL2H)	Bit Name	X	X	X	X	X	X	Bit1	Bit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	0	0	0	0	0	0	P	P
N/A	CONT	Bit Name	INTE	INT	TS	TE	PAB	PSR2	PSR1	PSR0
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x00	R0(IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x01	R1(TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x02	R2(PC)	Bit Name	-	-	-	-	-	-	-	-

(This specification is subject to change without further notice)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	Jump to address 0x08 or continue to execute next instruction							
0x03	R3(SR)	Bit Name	GP2	PS1	PS0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Changed	P	P	P	t	t	P	P	P
0x04	R4(RSR)	Bit Name	BS7	BS6	-	-	-	-	-	-
		Power-on	0	0	U	U	U	U	U	U
		/RESET and WDT	0	0	P	P	P	P	P	P
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x05	P5	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x06	P6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x7~0x8	R7~R8	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x9	R9 (ADCON)	Bit Name	X	X	IOCS	ADRUN	ADPD	ADAS2	ADAS1	ADAS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0xA	RA (ADDDATA)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0xB	RB (TMR1L)	Bit Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xC	RC (TMR1H)	Bit Name	X	X	X	X	X	X	Bit1	Bit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	0	0	0	0	0	0	P	P
0xD	RD (TMR2L)	Bit Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0xE	RE (TMR2H)	Bit Name	X	X	X	X	X	X	Bit1	Bit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	0	0	0	0	0	0	P	P
0xF	RF (ISR)	Bit Name	X	CMPIF	PWM2IF	PWM1IF	ADIF	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	0	P	P	P	P	P	P	P
0x10~0x3F	R10~R3F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P

X: not used.　U: unknown or don't care.　P: previous value before reset.

t: check Table 5

4.12 Oscillator

4.12.1 Oscillator Modes

The EM78458 and EM78459 can be operated in four different oscillator modes, such as High XTAL oscillator mode (HXT), Low XTAL oscillator mode (LXT), External RC oscillator mode (ERC), and RC oscillator mode with Internal capacitor (IC). Users can select one of them by programming the MASK Option. The up-limited operation frequency of crystal/resonator on the different VDDs is listed in Table 11

Table 11 The Summary of Maximum Operating Speeds

Conditions	VDD	Fxt max.(MHz)
Two clocks	2.3	4
	3.0	8
	5.0	20

(This specification is subject to change without further notice)

4.12.2 Crystal Oscillator/Ceramic Resonators (XTAL)

EM78458/459 can be driven by an external clock signal through the OSCI pin as shown in Fig. 18 below.
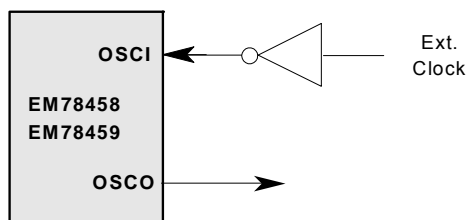

Fig. 18 Circuit for External Clock Input

In the most applications, pin OSCI and pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Fig. 19 depicts such circuit. The same applies to the HXT mode and the LXT mode. Table 12 provided the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to their specifications for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.
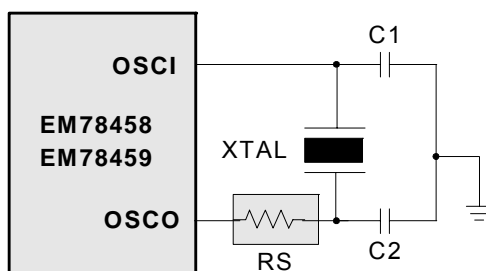

Fig. 19 Circuit for Crystal/Resonator

Table 12 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonators

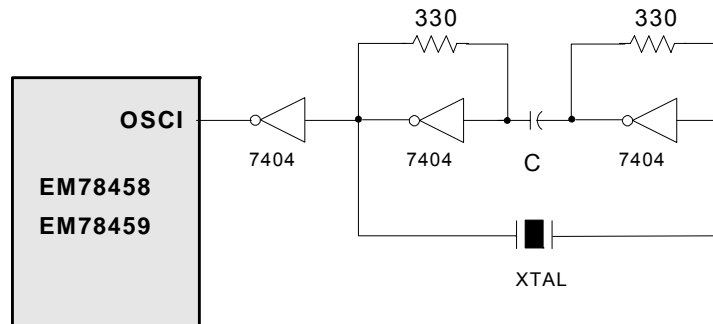| Oscillator Type	Frequency Mode	Frequency	C1(pF)	C2(pF)
Ceramic Resonators	HXT	455 kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768kHz	25	15
		100KHz	25	25
		200KHz	25	25
	HXT	455KHz	20~40	20~150
		1.0MHz	15~30	15~30
		2.0MHz	15	15
		4.0MHz	15	15

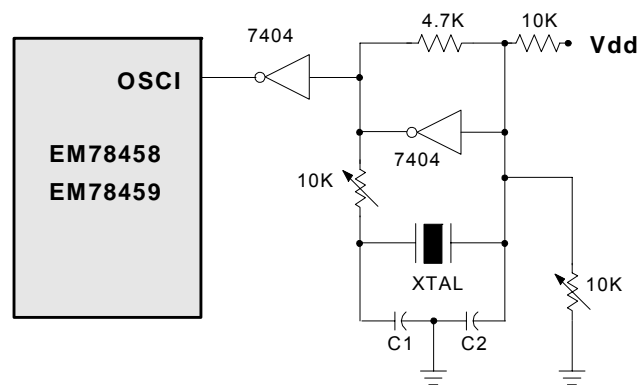*Fig. 20 Circuit for Crystal/Resonator-Series Mode*

Fig. 21 Circuit for Crystal/Resonator-Parallel Mode

4.12.3 External RC Oscillator Mode

For some applications that do not require precise timing calculation, the RC oscillator (Fig. 22) could offer users with an effective cost savings. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor(Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to the manufacturing process variation.

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and that the value of Rext should not be greater than 1M ohm. If they cannot be kept in this range, the frequency can be affected easily by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator becomes unstable because the NMOS cannot discharge the current of the capacitance correctly.

Based on the above reasons, it must be kept in mind that all supply voltage, the operation temperature, the components of the RC oscillator, the package types, and the way the PCB is layout, have certain effect on the system frequency.
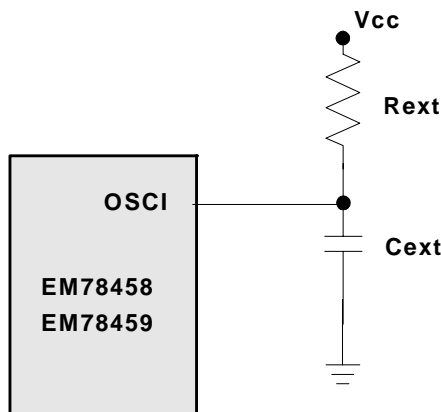
Fig. 22 Circuit for External RC Oscillator Mode

Table 13 RC Oscillator Frequencies

Cext	Rext	Average Fosc 5V,25°C	Average Fosc 3V,25°C
20 pF	3.3k	3.57 MHz	2.94 MHz
	5.1k	2.63MHz	1.92 MHz
	10k	1.30 MHz	1.22 MHz
	100k	150 KHz	153 KHz
100 pF	3.3k	1.43 MHz	1.35 MHz
	5.1k	980 KHz	877 KHz
	10k	520 KHz	465 KHz
	100k	57 KHz	54 KHz
300 pF	3.3k	510 KHz	470 KHz
	5.1k	340 KHz	320 KHz
	10k	175 KHz	170 KHz
	100k	19 KHz	19 KHz

NOTE
1. Measured on DIP packages.
2. Design reference only

4.12.4   RC Oscillator Mode with Internal Capacitor

If both precision and cost are taken into consideration, EM78P257A/B also offers a special oscillation mode. It is equipped with an internal capacitor and an external resistor (connected to Vcc). The internal capacitor functions as temperature compensator. In order to obtain more accurate frequency, a precise resistor is recommended.
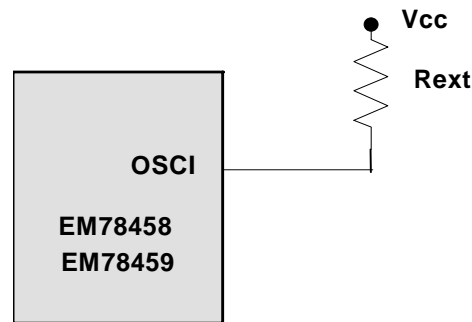
Fig. 23 Circuit for Internal C Oscillator Mode

Table 14 R Oscillator Frequencies

Rext	Average Fosc 5V,25°C	Average Fosc 3V,25°C
51k	2.22 MHz	2.17 MHz
100k	1.15 MHz	1.14 MHz
300k	375 KHz	370 KHz

NOTE
1. Measured on DIP packages.
2. Design reference only

4.13 Power-on Considerations

Any microcontroller is not warranted to start proper operation before the power supply stabilizes in steady state.

EM78458/459 POR voltage range is 1.2V~1.8V. Under customer application, when power is OFF, Vdd must drop to below 1.2V and remains OFF for 10us before power can be switched ON again. This way, the EM78458/459 will reset and work normally. The extra external reset circuit will work well if Vdd can rise at very fast speed (50 ms or less). However, under most cases where critical applications are involved, extra devices are required to assist in solving the power-up problems.

4.13.1 External Power on Reset Circuit

The circuit shown in Fig IV.13.1-1 implements an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough to allow Vdd to reach minimum operation voltage. This circuit is used when the power supply has a slow rise time. Because the current leakage from the /RESET pin is about ±5μA, it is recommended that R should not be great than 40 K. In this way, the voltage at Pin /RESET is held below 0.2V. The diode (D) acts as a short circuit at power-down. The capacitor, C, is discharged rapidly and fully. Rin, the current-limited resistor, prevents high current discharge or ESD (electrostatic discharge) from flowing into Pin /RESET.
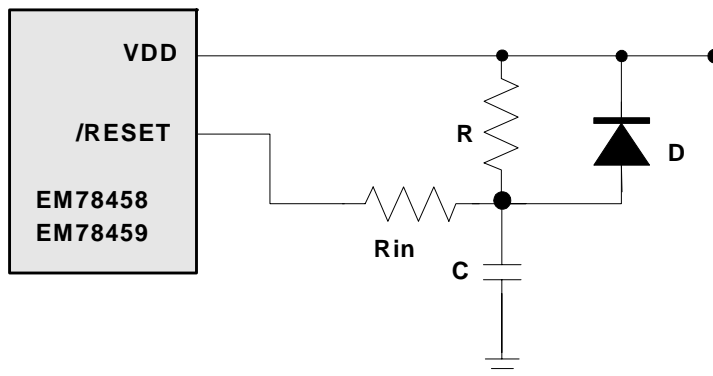
Fig. 24 External Power on Reset Circuit

4.13.2   *Residue-Voltage Protection*

When battery is replaced, device power (Vdd) is taken off but residue-voltage remains. The residue-voltage may trips below Vdd minimum, but not to zero. This condition may cause a poor power on reset. Fig. 25 and Fig. 26 show how to build a residue-voltage protection circuit
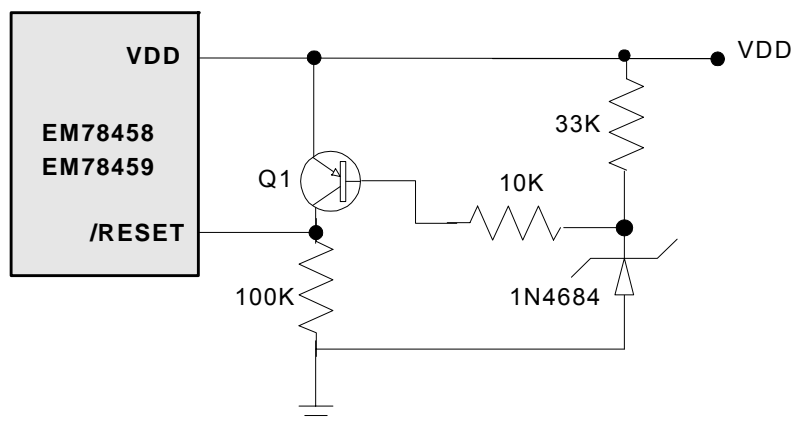
Fig. 25 Circuit 1 for the Residue Voltage Protection
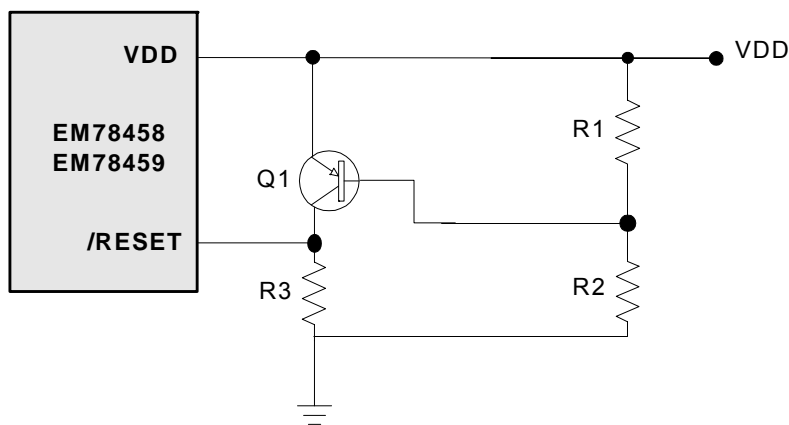
Fig. 26 Circuit 2 for the Residue Voltage Protection

4.14 CODE OPTION

Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ENWDTB	CK2	MS	HLF	RCT	-

Bit 0:   Reserved..

The bit0 set to "0" all the time.

Bit 1 (RCT):   RC type.

0: Internal C, External R

1: External RC

Bit 2 (HLF):   Frequency mode.

0: Low frequency(<32.768KHz)

1: High frequency(≥32.768KHz)

Bit 3 (MS):   Oscillator types.

0: RC type

1: Crystal type

Bit 4 (CK2):   Clocks per instruction.

0: 2 clocks

1: 4 clocks

Bit 5 (ENWDTB): WatchDog Timer (WDT) control.

0: Enable WDT

1: Always disable WDT

4.15 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2", ····). In this case, the execution takes two instruction cycles.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O registers can be regarded as general registers. That is, the same instruction can operate on I/O registers.

The symbol "R" represents a register designator that specifies which one of the registers (including operational registers and general-purpose registers) is to be utilized by the instruction. The symbol "b" represents a bit field designator that selects the value for the bit located in the register "R" that is affected by the operation. The symbol "k" represents an 8 or 10-bit constant or literal value.

Table 15 The list of the instruction set of EM78458/459

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000				
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None <Note1>
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None <Note1>
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1),	C

(This specification is subject to change without further notice)

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
			R(0) → C, C → A(7)	
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None <Note2>
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None <Note3>
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1 1110 0000 0001	1E01	INT	PC+1 → [SP], 001H → PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC
0 0000 0010 0000	0020	TBL	R2+A → R2 Bits 8~9 of R2 unchanged	Z,C,DC

NOTE
1. This instruction is applicable to IOC50~IOC60, IOC90~IOCF0, IOC51~IOCF1 only.
2. This instruction is not recommended for RF operation.
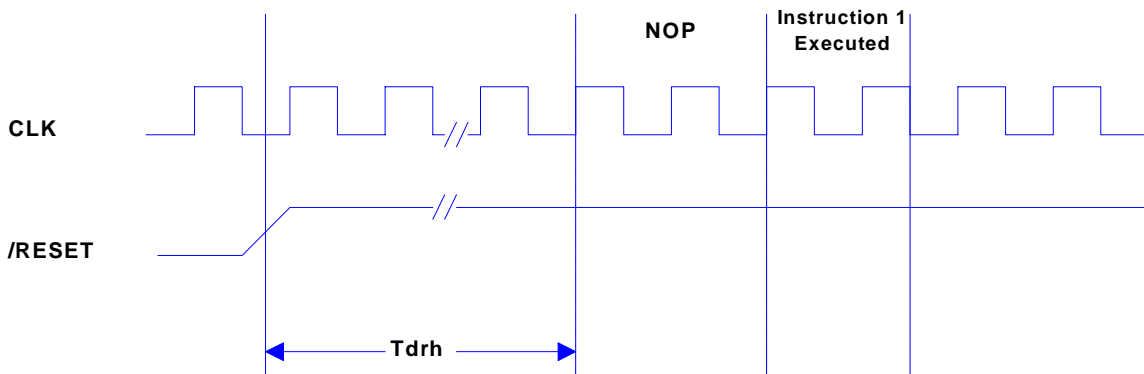3. This instruction cannot operate under RF.

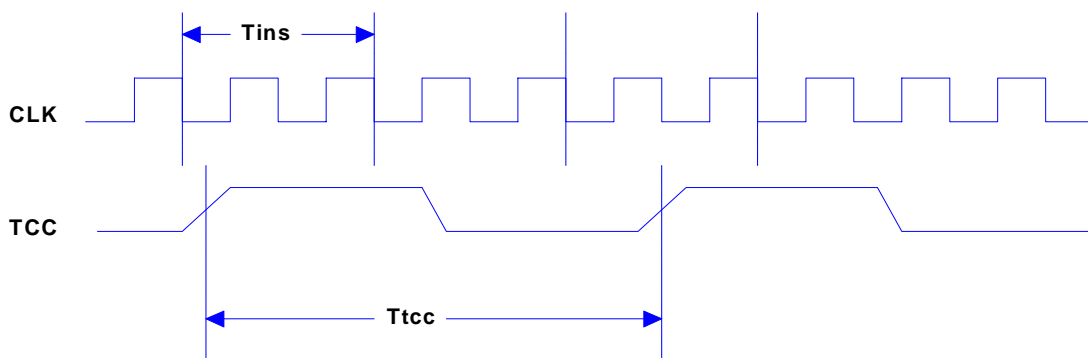## 4.16 Timing Diagrams

AC Test Input/Output Waveform
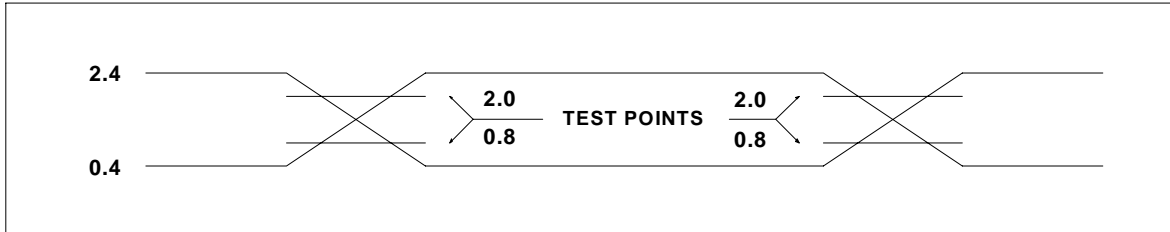
AC Testing : Input is driven at 2.4V for logic "1",and 0.4V for logic "0".Timing measurements are made at 2.0V for logic "1",and 0.8V for logic "0".

RESET Timing (CLK="0")

TCC Input Timing (CLKS="0")

5   ABSOLUTE MAXIMUM RATINGS

Items	Rating		
Temperature under bias	0°C	to	70°C
Storage temperature	-65°C	to	150°C
Input voltage	-0.3V	to	+6.0V
Output voltage	-0.3V	to	+6.0V

6   ELECTRICAL CHARACTERISTICS

6.1   DC Electrical Characteristic(Ta=0°C ~ 70 °C, VDD=5.0V±5%, VSS=0V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Fxt	XTAL: VDD to 3V	Two cycle with two clocks	DC		8	MHz
	XTAL: VDD to 5V		DC		20	MHz
	RC: VDD to 5V	R: 5.1KΩ, C: 100pF	F±30%	760	F±30%	KHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS			±1	µA
VIH	Input High Voltage	Ports 5, 6	2.0			V
VIL	Input Low Voltage	Ports 5, 6			0.8	V
VIHT	Input High Threshold Voltage	/RESET, TCC	2.0			V
VILT	Input Low Threshold Voltage	/RESET, TCC			0.8	V
VIHX	Clock Input High Voltage	OSCI	2.5			V
VILX	Clock Input Low Voltage	OSCI			1.0	V
VIH2	Input High Voltage,VDD=3V	Ports 5, 6	1.5			V
VIL2	Input Low Voltage,VDD=3V	Ports 5, 6			0.4	V
VIHT2	Input High Threshold Voltage,VDD=3V	/RESET, TCC	1.5			V
VILT2	Input Low Threshold Voltage,VDD=3V	/RESET, TCC			0.4	V
VIHX2	Clock Input High Voltage,VDD=3V	OSCI	1.5			V
VILX2	Clock Input Low Voltage,VDD=3V	OSCI			0.6	V
VOH1	Output High Voltage (Ports 5, 6)	IOH = -12.0 mA	2.4			V
VOL1	Output Low Voltage (P51~P57, P60~P63, P66~P67)	IOL = 12.0 mA			0.4	V
VOL2	Output Low Voltage (P64,P65)	IOL = 16.0 mA			0.4	V
IPH	Pull-high current	Pull-high active, input pin at VSS	-50	-100	-240	µA
IPD	Pull-down current	Pull-down active, input pin at VDD	25	50	120	µA
ISB	Power down current	All input and I/O pins at VDD, output pin floating, WDT enabled			10	µA
ISB	Power down current	All input and I/O pins at VDD, output pin floating, WDT disabled			1	µA
ICC1	Operating supply current (VDD=3V)	/RESET='High',Fosc=32KHz		15	30	µA

(This specification is subject to change without further notice)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	at two clocks	(Crystal type, two clocks), output pin floating, WDT disabled				
ICC2	Operating supply current (VDD=3V) at two clocks	/RESET='High',Fosc=32KHz (Crystal type, two clocks), output pin floating, WDT enabled		19	35	µA
ICC3	Operating supply current (VDD=5.0V) at two clocks	/RESET='High', Fosc=2MHz (Crystal type, two clocks), output pin floating			2	mA
ICC4	Operating supply current (VDD=5.0V) at two clocks	/RESET='High', Fosc=4MHz (Crystal type, two clocks), output pin floating			4.0	mA

6.2 AC Electrical Characteristic (Ta=0°C ~ 70 °C, VDD=5V±5%, VSS=0V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle		45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type RC type	100 500		DC DC	ns ns
Ttcc	TCC input period		(Tins+20)/N*			ns
Tdrh	Device reset hold time	Ta = 25°C	9	18	30	ms
Trst	/RESET pulse width	Ta = 25°C	2000			ns
Twdt	Watchdog timer period	Ta = 25°C	9	18	30	ms
Tset	Input pin setup time			0		ms
Thold	Input pin hold time			20		ms
Tdelay	Output pin delay time	Cload=20pF		50		ms

* N= selected prescaler ratio.

6.3 A/D Converter Characteristic(Vdd=3.0V to 5.5V,Vss=0V,Ta=0 to 70)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VAREF	Analog reference voltage	VAREF - VASS 2.5V	3.0		Vdd	V
VASS					Vss	V
VAI	Analog input voltage		VASS		VAREF	V
IAI	Analog supply current	Vdd=VAREF=5.0V, VASS=0.0V	500	700	1000	uA
RN	Resolution	Vdd=VAREF=5.0V, VASS=0.0V	6	7	8	Bits
LN	Linearity error	Vdd = 2.5 to 5.5V Ta=25	0	±2	±4	LSB
DNL	Differential nonlinear error	Vdd = 2.5 to 5.5V Ta=25	0	±0.5	±0.9	LSB
FSE	Full scale error	Vdd=VAREF=5.0V, VASS=0.0V	±0	±2	±4	LSB
OE	Offset error	Vdd=VAREF=5.0V, VASS=0.0V	±0	±1	±2	LSB

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ZAI	Recommended impedance of analog voltage source		0	8	10	KΩ
TAD	A/D clock period	Vdd=VAREF=5.0V, VASS =0.0V	3	3.5	4	us
TCN	A/D conversion time	Vdd=VAREF=5.0V, VASS =0.0V	10		10	TAD
ADIV	A/D OP input voltage range	Vdd=VAREF=5.0V, VASS =0.0V	0		5	V
ADOV	A/D OP output voltage swing	Vdd=VAREF=5.0V, VASS =0.0V,RL=10KΩ	0	0.2	0.3	V
			4.7	4.8	5	
ADSR	A/D OP slew rate	Vdd=VAREF=5.0V, VASS =0.0V	0.1	0.3		V/us
PSR	Power Supply Rejection	Vdd=5.0V±0.5V	±0		±2	LSB

NOTE
1.These parameters are characterized but not tested.
2.These parameters are for design guidance only and are not tested.
3.It will not consume any current other than minor leakage current, when A/D is off.
4.The A/D conversion result never decrease with an increase in the input voltage, and has no missing code.
5.Specifications subject to change without notice.

6.4 Comparator(OP) Characteristic(Vdd = 5.0V,Vss=0V,Ta=0 to 70)

Symbo	Parameter	Condition	Min.	Typ.	Max.	Unit
SR	Slew rate		0.1	0.2		V/us
IVR	Input voltage range	Vdd =5.0V, VSS =0.0V	0		5	V
OVS	Output voltage swing	Vd =5.0V, VSS =0.0V,RL=10KΩ	0	0.2	0.3	V
			4.7	4.8	5	
Iop	Supply current of OP		250	350	500	uA
PSRR	Power-supply Rejection Ration for OP	Vdd= 5.0V, VSS =0.0V	50	60	70	dB
Vos	Offset voltage	Vdd= 5.0V, VSS =0.0V		±10	±20	mV
Vs	Operating range		2.5		5.5	V

NOTE
1.These parameters are characterized but not tested.
2.These parameters are for design guidance only and are not tested.
3.Specifications subject to change without notice.

APPENDIX

A Package Types

OTP MCU	Package Type	Pin Count	Package Size
EM78458AP	DIP	20 pin	300mil
EM78458AM	SOP	20 pin	300mil
EM78459AK	Skinny DIP	24 pin	300mil
EM78459AM	SOP	24 pin	300mil

(This specification is subject to change without further notice)