



**Elan Microelectronics Corp.**

**CONFIDENTIAL**

**EM65565A**

**65 COM/ 132 SEG STN LCD Driver**

**January 13, 2003**

**Version 0.1 ( Preliminary )**

<b>EM65565A Specification Revision History</b>		
<b>Version</b>	<b>Content</b>	<b>Date</b>
0.1	Initial version	January 13, 2003

Preliminary

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## GENERAL DESCRIPTION

The EM65565A is a 65 Common 132 Segment dot matrix *liquid crystal display (LCD)* driver LSI, it can be connected directly to a microprocessor bus, be selected 8-bit parallel or serial data input interface. The chip of EM65565A contains 65x132 bits of *display data RAM (DDRAM)* and there is a one-to-one correspondence between the *LCD* panel pixels and the internal RAM bits.

The EM65565A chip can drive a 65\*132 dot display. Moreover, the capacity of the display can be extended by master/slave structures between chips. The chips are able to minimize power consumption because no external operating clock is necessary for the *DDRAM* read/write operation. Furthermore, because each chip is equipped internally with a low-power *LCD* driver power supply, resistors for *LCD* driver power voltage adjustment and a display clock CR oscillator circuit, the EM65565A chip can be used to create the lowest power display system with the fewest components for high-performance portable devices.

## FEATURE

- Direct display of RAM data through the *DDRAM*.RAM bit data: “0” Illuminated, “1” Non-illuminated
- RAM capacity 65\*132 = 8,580 bits
- Display driver circuits: 65 common output and 132 segment outputs
- High-speed 8-bit MPU interface (80-series and 68-series) / Serial interfaces are supported.
- Abundant command functions: display data Read/Write, display ON/OFF, status read, Normal/Reverse display mode, page address set, display start line set, column address set, display all points ON/OFF, *LCD* bias set, electronic volume, read-modify-write, segment driver direction select, power saver, static indicator, common output status select,  $V_0$  voltage regulation internal resistor ratio set.
- Static drive circuit equipped internally for indicators
- Low-power *LCD* power supply circuit equipped internally. Booster circuit (with Boost ratios of Two/Three/Four/Five times, where the step-up voltage reference power supply can be input externally) High-accuracy voltage adjustment circuit (external input)  $V_0$  voltage regulator resistors equipped internally,  $V_1$  to  $V_4$  voltage divider resistors equipped internally, electronic volume function equipped internally, voltage follower.
- Internal CR oscillator circuit (external clock can also be input)
- Extremely low power consumption,
- Power supply, Operable on the low 1.8 voltage, Logic power supply  $V_{DD} - V_{SS} = 2.4$  to 3.3 V, Boost reference voltage:  $V_{CI} = 2.4$  to 3.3 V, *LCD* drive power supply:  $V_{LCD} = V_0 - V_{SS} = 4.5$  to 12.0 V
- These chips not designed for resistance to light or resistance to radiation.
- Package (Ordering information)

Part Number	Package	Description	Package information
EM65565AAGH	Gold bumped chip	NA	Page 5

**Note:** The EM65565A series has the following sub-codes depending on their shapes.

**H:** Bare chip (Aluminum pad without bumped); **GH:** Gold bumped chip;

**F:** COF package; **T:** TAB (TCP) package

Example EM65565AAGH → EM65565A: Elan number ; A: Package Version ; GH: Gold bumped chip

**PIN CONFIGURATIONS**

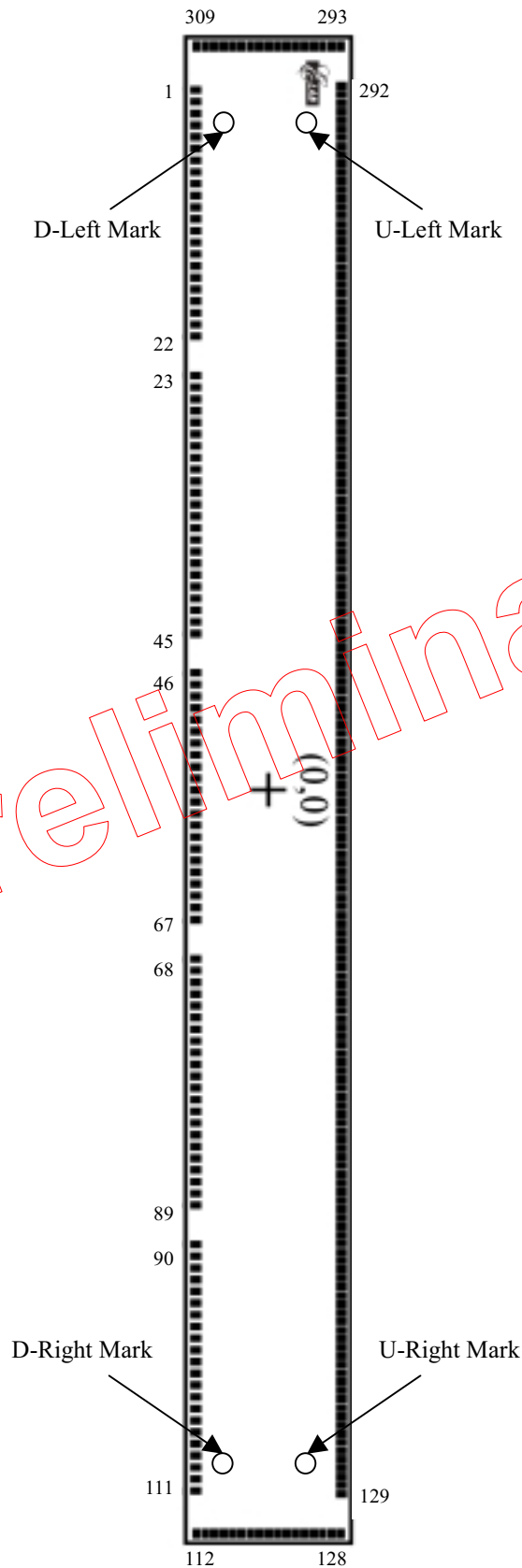


Figure 1. Pin configuration

**Note:** With the Elan logo in upper left the pin 1 is in the down left corner.

**MARK DIMENSIONS**

Mark	Coordinate (X,Y)	Mark	Coordinate (X,Y)
U-Left	-4714.25 ,124.55	U-Right	4544.1 ,124.55
D-Left	-4714.25 ,-215.4	D-Right	4544.1 ,-215.4

**PIN DIMENSIONS**

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	10570	1210	μm
Bump Size	1 ~ 309	43	60	
Pad Pitch	60 (min.)			
Die thickness (excluding bumps)	525 +/- 25			
Bump Height	All Pad 17 +/- 3 (within die)			
Minimum Bump Gap	17			
Coordinate Origin	Chip center			

Preliminary



**PAD Coordinates Table**

<i>Pin NO</i>	<i>Pad Name</i>	<i>Coordinate (X,Y)</i>	<i>Pin NO</i>	<i>Pad Name</i>	<i>Coordinate (X,Y)</i>
1	NC1	-4861.2 , -485.0	51	V <sub>SS</sub>	-404.4 , -485.0
2	NC2	-4779.7 , -485.0	52	V <sub>SS</sub>	-322.9 , -485.0
3	NC3	-4698.2 , -485.0	53	V <sub>SS</sub>	-241.4 , -485.0
4	NC4	-4616.7 , -485.0	54	V <sub>SS</sub>	-159.9 , -485.0
5	NC5	-4535.2 , -485.0	55	V <sub>SS</sub>	-78.4 , -485.0
6	TEST1	-4453.7 , -485.0	56	V <sub>SS</sub>	3.1 , -485.0
7	TEST2	-4372.2 , -485.0	57	V <sub>OUT</sub>	84.6 , -485.0
8	TEST3	-4290.7 , -485.0	58	V <sub>OUT</sub>	166.1 , -485.0
9	FRS	-4209.2 , -485.0	59	CAP4+	247.6 , -485.0
10	FR	-4127.7 , -485.0	60	CAP4+	329.1 , -485.0
11	FR	-4046.2 , -485.0	61	CAP4+	410.6 , -485.0
12	DCLK	-3964.7 , -485.0	62	CAP3+	492.1 , -485.0
13	/BCT	-3883.2 , -485.0	63	CAP3+	573.6 , -485.0
14	V <sub>SS</sub>	-3801.7 , -485.0	64	CAP3+	655.1 , -485.0
15	V <sub>SS</sub>	-3720.2 , -485.0	65	CAP1-	736.6 , -485.0
16	/CS1	-3638.7 , -485.0	66	CAP1-	818.1 , -485.0
17	CS2	-3557.2 , -485.0	67	CAP1-	899.6 , -485.0
18	V <sub>DD</sub>	-3475.7 , -485.0	68	CAP1+	1172.0 , -485.0
19	/RST	-3394.2 , -485.0	69	CAP1+	1253.5 , -485.0
20	D/I	-3312.7 , -485.0	70	CAP1+	1335.0 , -485.0
21	V <sub>SS</sub>	-3231.2 , -485.0	71	CAP2+	1416.5 , -485.0
22	/WR	-3149.7 , -485.0	72	CAP2+	1498.0 , -485.0
23	/RD	-2877.3 , -485.0	73	CAP2+	1579.5 , -485.0
24	V <sub>DD</sub>	-2795.8 , -485.0	74	CAP2-	1661.0 , -485.0
25	D0	-2714.3 , -485.0	75	CAP2-	1742.5 , -485.0
26	D1	-2632.8 , -485.0	76	CAP2-	1824.0 , -485.0
27	D2	-2551.3 , -485.0	77	V <sub>DD</sub>	1905.5 , -485.0
28	D3	-2469.8 , -485.0	78	V <sub>RS</sub>	1987.0 , -485.0
29	D4	-2388.3 , -485.0	79	V <sub>RS</sub>	2068.5 , -485.0
30	D5	-2306.8 , -485.0	80	V <sub>SS</sub>	2150.0 , -485.0
31	D6	-2225.3 , -485.0	81	V <sub>1</sub>	2231.5 , -485.0
32	D7	-2143.8 , -485.0	82	V <sub>1</sub>	2313.0 , -485.0
33	V <sub>SS</sub>	-2062.3 , -485.0	83	V <sub>1</sub>	2394.5 , -485.0
34	V <sub>DD</sub>	-1980.8 , -485.0	84	V <sub>2</sub>	2476.0 , -485.0
35	V <sub>SS</sub>	-1899.3 , -485.0	85	V <sub>2</sub>	2557.5 , -485.0
36	V <sub>DD</sub>	-1817.8 , -485.0	86	V <sub>2</sub>	2639.0 , -485.0
37	V <sub>DD</sub>	-1736.3 , -485.0	87	V <sub>3</sub>	2720.5 , -485.0
38	V <sub>DD</sub>	-1654.8 , -485.0	88	V <sub>3</sub>	2802.0 , -485.0
39	V <sub>DD</sub>	-1573.3 , -485.0	89	V <sub>3</sub>	2883.5 , -485.0
40	V <sub>DD</sub>	-1491.8 , -485.0	90	V <sub>4</sub>	3155.9 , -485.0
41	V <sub>DD</sub>	-1410.3 , -485.0	91	V <sub>4</sub>	3237.4 , -485.0
42	V <sub>DD</sub>	-1328.8 , -485.0	92	V <sub>4</sub>	3318.9 , -485.0
43	V <sub>Cl</sub>	-1247.3 , -485.0	93	V <sub>0</sub>	3400.4 , -485.0
44	V <sub>Cl</sub>	-1165.8 , -485.0	94	V <sub>0</sub>	3481.9 , -485.0
45	V <sub>Cl</sub>	-1084.3 , -485.0	95	V <sub>0</sub>	3563.4 , -485.0
46	V <sub>SS</sub>	-811.9 , -485.0	96	V <sub>R</sub>	3644.9 , -485.0
47	V <sub>SS</sub>	-730.4 , -485.0	97	V <sub>R</sub>	3726.4 , -485.0
48	V <sub>SS</sub>	-648.9 , -485.0	98	V <sub>R</sub>	3807.9 , -485.0
49	V <sub>SS</sub>	-567.4 , -485.0	99	V <sub>SS</sub>	3889.4 , -485.0
50	V <sub>SS</sub>	-485.9 , -485.0	100	V <sub>SS</sub>	3970.9 , -485.0



Pin NO	Pad Name	Coordinate (X,Y)	Pin NO	Pad Name	Coordinate (X,Y)
101	V <sub>DD</sub>	4052.4 , -485.0	151	SEG6	3569.9 ,485.0
102	M/S	4133.9 , -485.0	152	SEG7	3509.9 ,485.0
103	DCLKS	4215.4 , -485.0	153	SEG8	3449.9 ,485.0
104	V <sub>SS</sub>	4296.9 , -485.0	154	SEG9	3389.9 ,485.0
105	MPUS	4378.4 , -485.0	155	SEG10	3329.9 ,485.0
106	P/S	4459.9 , -485.0	156	SEG11	3269.9 ,485.0
107	V <sub>DD</sub>	4541.4 , -485.0	157	SEG12	3209.9 ,485.0
108	/PCT	4622.9 , -485.0	158	SEG13	3149.9 ,485.0
109	V <sub>SS</sub>	4704.4 , -485.0	159	SEG14	3089.9 ,485.0
110	IRS	4785.9 , -485.0	160	SEG15	3029.9 ,485.0
111	V <sub>DD</sub>	4867.4 , -485.0	161	SEG16	2969.9 ,485.0
112	COM31	5165.0 , -480.0	162	SEG17	2909.9 ,485.0
113	COM30	5165.0 , -420.0	163	SEG18	2849.9 ,485.0
114	COM29	5165.0 , -360.0	164	SEG19	2789.9 ,485.0
115	COM28	5165.0 , -300.0	165	SEG20	2729.9 ,485.0
116	COM27	5165.0 , -240.0	166	SEG21	2669.9 ,485.0
117	COM26	5165.0 , -180.0	167	SEG22	2609.9 ,485.0
118	COM25	5165.0 , -120.0	168	SEG23	2549.9 ,485.0
119	COM24	5165.0 , -60.0	169	SEG24	2489.9 ,485.0
120	COM23	5165.0 , 0.0	170	SEG25	2429.9 ,485.0
121	COM22	5165.0 , 60.0	171	SEG26	2369.9 ,485.0
122	COM21	5165.0 , 120.0	172	SEG27	2309.9 ,485.0
123	COM20	5165.0 , 180.0	173	SEG28	2249.9 ,485.0
124	COM19	5165.0 , 240.0	174	SEG29	2189.9 ,485.0
125	COM18	5165.0 , 300.0	175	SEG30	2129.9 ,485.0
126	COM17	5165.0 , 360.0	176	SEG31	2069.9 ,485.0
127	COM16	5165.0 , 420.0	177	SEG32	2009.9 ,485.0
128	COM15	5165.0 , 480.0	178	SEG33	1949.9 ,485.0
129	COM14	4889.9 ,485.0	179	SEG34	1889.9 ,485.0
130	COM13	4829.9 ,485.0	180	SEG35	1829.9 ,485.0
131	COM12	4769.9 ,485.0	181	SEG36	1769.9 ,485.0
132	COM11	4709.9 ,485.0	182	SEG37	1709.9 ,485.0
133	COM10	4649.9 ,485.0	183	SEG38	1649.9 ,485.0
134	COM9	4589.9 ,485.0	184	SEG39	1589.9 ,485.0
135	COM8	4529.9 ,485.0	185	SEG40	1529.9 ,485.0
136	COM7	4469.9 ,485.0	186	SEG41	1469.9 ,485.0
137	COM6	4409.9 ,485.0	187	SEG42	1409.9 ,485.0
138	COM5	4349.9 ,485.0	188	SEG43	1349.9 ,485.0
139	COM4	4289.9 ,485.0	189	SEG44	1289.9 ,485.0
140	COM3	4229.9 ,485.0	190	SEG45	1229.9 ,485.0
141	COM2	4169.9 ,485.0	191	SEG46	1169.9 ,485.0
142	COM1	4109.9 ,485.0	192	SEG47	1109.9 ,485.0
143	COM0	4049.9 ,485.0	193	SEG48	1049.9 ,485.0
144	COMS	3989.9 ,485.0	194	SEG49	989.9 ,485.0
145	SEG0	3929.9 ,485.0	195	SEG50	929.9 ,485.0
146	SEG1	3869.9 ,485.0	196	SEG51	869.9 ,485.0
147	SEG2	3809.9 ,485.0	197	SEG52	809.9 ,485.0
148	SEG3	3749.9 ,485.0	198	SEG53	749.9 ,485.0
149	SEG4	3689.9 ,485.0	199	SEG54	689.9 ,485.0
150	SEG5	3629.9 ,485.0	200	SEG55	629.9 ,485.0





Pin NO	Pad Name	Coordinate (X,Y)	Pin NO	Pad Name	Coordinate (X,Y)
201	SEG56	569.9 ,485.0	251	SEG106	-2430.1 ,485.0
202	SEG57	509.9 ,485.0	252	SEG107	-2490.1 ,485.0
203	SEG58	449.9 ,485.0	253	SEG108	-2550.1 ,485.0
204	SEG59	389.9 ,485.0	254	SEG109	-2610.1 ,485.0
205	SEG60	329.9 ,485.0	255	SEG110	-2670.1 ,485.0
206	SEG61	269.9 ,485.0	256	SEG111	-2730.1 ,485.0
207	SEG62	209.9 ,485.0	257	SEG112	-2790.1 ,485.0
208	SEG63	149.9 ,485.0	258	SEG113	-2850.1 ,485.0
209	SEG64	89.9 ,485.0	259	SEG114	-2910.1 ,485.0
210	SEG65	29.9 ,485.0	260	SEG115	-2970.1 ,485.0
211	SEG66	-30.1 ,485.0	261	SEG116	-3030.1 ,485.0
212	SEG67	-90.1 ,485.0	262	SEG117	-3090.1 ,485.0
213	SEG68	-150.1 ,485.0	263	SEG118	-3150.1 ,485.0
214	SEG69	-210.1 ,485.0	264	SEG119	-3210.1 ,485.0
215	SEG70	-270.1 ,485.0	265	SEG120	-3270.1 ,485.0
216	SEG71	-330.1 ,485.0	266	SEG121	-3330.1 ,485.0
217	SEG72	-390.1 ,485.0	267	SEG122	-3390.1 ,485.0
218	SEG73	-450.1 ,485.0	268	SEG123	-3450.1 ,485.0
219	SEG74	-510.1 ,485.0	269	SEG124	-3510.1 ,485.0
220	SEG75	-570.1 ,485.0	270	SEG125	-3570.1 ,485.0
221	SEG76	-630.1 ,485.0	271	SEG126	-3630.1 ,485.0
222	SEG77	-690.1 ,485.0	272	SEG127	-3690.1 ,485.0
223	SEG78	-750.1 ,485.0	273	SEG128	-3750.1 ,485.0
224	SEG79	-810.1 ,485.0	274	SEG129	-3810.1 ,485.0
225	SEG80	-870.1 ,485.0	275	SEG130	-3870.1 ,485.0
226	SEG81	-930.1 ,485.0	276	SEG131	-3930.1 ,485.0
227	SEG82	-990.1 ,485.0	277	COM32	-3990.1 ,485.0
228	SEG83	-1050.1 ,485.0	278	COM33	-4050.1 ,485.0
229	SEG84	-1110.1 ,485.0	279	COM34	-4110.1 ,485.0
230	SEG85	-1170.1 ,485.0	280	COM35	-4170.1 ,485.0
231	SEG86	-1230.1 ,485.0	281	COM36	-4230.1 ,485.0
232	SEG87	-1290.1 ,485.0	282	COM37	-4290.1 ,485.0
233	SEG88	-1350.1 ,485.0	283	COM38	-4350.1 ,485.0
234	SEG89	-1410.1 ,485.0	284	COM39	-4410.1 ,485.0
235	SEG90	-1470.1 ,485.0	285	COM40	-4470.1 ,485.0
236	SEG91	-1530.1 ,485.0	286	COM41	-4530.1 ,485.0
237	SEG92	-1590.1 ,485.0	287	COM42	-4590.1 ,485.0
238	SEG93	-1650.1 ,485.0	288	COM43	-4650.1 ,485.0
239	SEG94	-1710.1 ,485.0	289	COM44	-4710.1 ,485.0
240	SEG95	-1770.1 ,485.0	290	COM45	-4770.1 ,485.0
241	SEG96	-1830.1 ,485.0	291	COM46	-4830.1 ,485.0
242	SEG97	-1890.1 ,485.0	292	COM47	-4890.1 ,485.0
243	SEG98	-1950.1 ,485.0	293	COM48	-5165.0 ,480.0
244	SEG99	-2010.1 ,485.0	294	COM49	-5165.0 ,420.0
245	SEG100	-2070.1 ,485.0	295	COM50	-5165.0 ,360.0
246	SEG101	-2130.1 ,485.0	296	COM51	-5165.0 ,300.0
247	SEG102	-2190.1 ,485.0	297	COM52	-5165.0 ,240.0
248	SEG103	-2250.1 ,485.0	298	COM53	-5165.0 ,180.0
249	SEG104	-2310.1 ,485.0	299	COM54	-5165.0 ,120.0
250	SEG105	-2370.1 ,485.0	300	COM55	-5165.0 ,60.0



<i>Pin NO</i>	<i>Pad Name</i>	<i>Coordinate (X,Y)</i>	<i>Pin NO</i>	<i>Pad Name</i>	<i>Coordinate (X,Y)</i>
301	COM56	-5165.0 ,0.0			
302	COM57	-5165.0 ,-60.0			
303	COM58	-5165.0 ,-120.0			
304	COM59	-5165.0 ,-180.0			
305	COM60	-5165.0 ,-240.0			
306	COM61	-5165.0 ,-300.0			
307	COM62	-5165.0 ,-360.0			
308	COM63	-5165.0 ,-420.0			
309	COMS	-5165.0 ,-480.0			

Note : For PCB layout, IC substrate must be connected to VSS.

Preliminary

## PIN DESCRIPTION

Table 1

Pin Name	I/O	Function	No. of Pins															
V <sub>DD</sub>	Power Supply	Shared with the MPU power supply terminal V <sub>CC</sub>	14															
V <sub>SS</sub>	Power Supply	This is a 0 V terminal connected to the system GND.	20															
V <sub>CI</sub>	I	This is the reference power supply for the step-up voltage circuit for the liquid crystal drive.	3															
V <sub>RS</sub>	I	This is the externally input V <sub>REG</sub> power supply for the LCD power supply voltage regulator. These are only enabled for the models with the V <sub>REG</sub> external input option.	3															
V <sub>0</sub> V <sub>1</sub> V <sub>2</sub> V <sub>3</sub> V <sub>4</sub>	I/O	<p>This is a multi-level power supply for the liquid crystal drive. The voltage applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divider or through changing the impedance using an Op. Amp. Voltage levels are determined based on V<sub>0</sub>, and must maintain the relative magnitudes shown below.</p> $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$ <p>Master operation: When the power supply turns ON, the internal power supply circuits produce the V<sub>1</sub> to V<sub>4</sub> voltages shown below. The voltage settings are selected using the LCD bias set command.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th></th> <th>1/9 bias</th> <th>1/7 bias</th> </tr> </thead> <tbody> <tr> <td>V<sub>1</sub></td> <td>8/9•V<sub>0</sub></td> <td>6/7•V<sub>0</sub></td> </tr> <tr> <td>V<sub>2</sub></td> <td>7/9•V<sub>0</sub></td> <td>5/7•V<sub>0</sub></td> </tr> <tr> <td>V<sub>3</sub></td> <td>2/9•V<sub>0</sub></td> <td>2/7•V<sub>0</sub></td> </tr> <tr> <td>V<sub>4</sub></td> <td>1/9•V<sub>0</sub></td> <td>1/7•V<sub>0</sub></td> </tr> </tbody> </table>		1/9 bias	1/7 bias	V <sub>1</sub>	8/9•V <sub>0</sub>	6/7•V <sub>0</sub>	V <sub>2</sub>	7/9•V <sub>0</sub>	5/7•V <sub>0</sub>	V <sub>3</sub>	2/9•V <sub>0</sub>	2/7•V <sub>0</sub>	V <sub>4</sub>	1/9•V <sub>0</sub>	1/7•V <sub>0</sub>	15
	1/9 bias	1/7 bias																
V <sub>1</sub>	8/9•V <sub>0</sub>	6/7•V <sub>0</sub>																
V <sub>2</sub>	7/9•V <sub>0</sub>	5/7•V <sub>0</sub>																
V <sub>3</sub>	2/9•V <sub>0</sub>	2/7•V <sub>0</sub>																
V <sub>4</sub>	1/9•V <sub>0</sub>	1/7•V <sub>0</sub>																
CAP1+	O	Capacitor 1 positive connection pin for voltage converter	3															
CAP1-	O	Capacitor 1 negative connection pin for voltage converter	3															
CAP2+	O	Capacitor 2 positive connection pin for voltage converter	3															
CAP2-	O	Capacitor 2 negative connection pin for voltage converter	3															
CAP3+	O	Capacitor 3 positive connection pin for voltage converter	3															
CAP4+	O	Capacitor 4 positive connection pin for voltage converter	3															
V <sub>OUT</sub>	I/O	DC/DC voltage converter input/output pin, connect a capacitor between this terminal and V <sub>SS</sub>	2															
V <sub>R</sub>	I	Output voltage regulator terminal. These are only enabled when the V <sub>0</sub> voltage regulator internal resistors are not used (IRS = "L"). These cannot be used when the V <sub>0</sub> voltage regulator internal resistors are used (IRS = "H").	3															
D7 to D0	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the chip select is inactive, D0 to D7 are set to high impedance. When the serial interface is selected (P/S = "L"), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance.	8															
D/I	I	<p>Determines whether the data bits are data or the instruction (command).</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>D/I</th> <th>D0 to D7</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>Display data</td> </tr> <tr> <td>L</td> <td>Instruction (Command)</td> </tr> </tbody> </table>	D/I	D0 to D7	H	Display data	L	Instruction (Command)	1									
D/I	D0 to D7																	
H	Display data																	
L	Instruction (Command)																	
/RST	I	When /RST is set to "L," the settings are initialized.	1															
/CS1 CS2	I	This is the chip select signal. When /CS1 = "L" and CS2 = "H," then the chip select CS2 becomes active, and data/command I/O is enabled.	2															
/RD (E)	I	Enable clock signal input for the 68-series MPU, active high. Active low input pin for the 80-series MPU /RD signal	1															
/WR (R/W)	I	Read/Write control signal with 68-series MPU R/W="H": Read, R/W="L": Write Active low input pin for the 80 series MPU /WR signal	1															
MPUS	I	This is the MPU interface switch terminal. MPUS = "H": 68-series MPU interface. MPUS = "L": 80-series MPU interface.	1															

(Continuous)

Pin Name	I/O	Function	No. of Pins																																						
P/S	I	<p>Selects the Parallel or Serial data input interface P/S = "H": Parallel data input interface, P/S = "L": Serial data input interface The following applies depending on the P/S status:</p> <table border="1"> <thead> <tr> <th>P/S</th> <th>Data/Command</th> <th>Data</th> <th>Read/Write</th> <th>Serial Clock</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>D/I</td> <td>D0 to D7</td> <td>/RD, /WR</td> <td></td> </tr> <tr> <td>L</td> <td>D/I</td> <td>D7 (SI)</td> <td>Write only</td> <td>D6 (SCL)</td> </tr> </tbody> </table> <p>When P/S = "L", D0 to D5 are HZ. D0 to D5 may be "H", "L" or Open. RD (E) and WR (P/W) are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported.</p>	P/S	Data/Command	Data	Read/Write	Serial Clock	H	D/I	D0 to D7	/RD, /WR		L	D/I	D7 (SI)	Write only	D6 (SCL)	1																							
P/S	Data/Command	Data	Read/Write	Serial Clock																																					
H	D/I	D0 to D7	/RD, /WR																																						
L	D/I	D7 (SI)	Write only	D6 (SCL)																																					
DCLKS	I	<p>Terminal to select whether or enable or disable the display clock internal oscillator circuit. DCLKS = "H": Internal oscillator circuit is enabled DCLKS = "L": Internal oscillator circuit is disabled (requires external input) When DCLKS = "L", input the display clock through the DCLK terminal.</p>	1																																						
M/S	I	<p>M/S = "H": Master operation M/S = "L": Slave operation The following is true depending on the M/S and DCLKS status:</p> <table border="1"> <thead> <tr> <th>M/S</th> <th>DCLKS</th> <th>Oscillator circuit</th> <th>Power Supply Circuit</th> <th>DCLK</th> <th>FR</th> <th>FRS</th> <th>/BCT</th> </tr> </thead> <tbody> <tr> <td rowspan="2">H</td> <td>H</td> <td>Enable</td> <td>Enable</td> <td>O</td> <td>O</td> <td>O</td> <td>O</td> </tr> <tr> <td>L</td> <td>Disable</td> <td>Enable</td> <td>I</td> <td>O</td> <td>O</td> <td>O</td> </tr> <tr> <td rowspan="2">L</td> <td>H</td> <td>Disable</td> <td>Disable</td> <td>I</td> <td>I</td> <td>O</td> <td>I</td> </tr> <tr> <td>L</td> <td>Disable</td> <td>Disable</td> <td>I</td> <td>I</td> <td>O</td> <td>I</td> </tr> </tbody> </table> <p>O: Output, I: Input</p>	M/S	DCLKS	Oscillator circuit	Power Supply Circuit	DCLK	FR	FRS	/BCT	H	H	Enable	Enable	O	O	O	O	L	Disable	Enable	I	O	O	O	L	H	Disable	Disable	I	I	O	I	L	Disable	Disable	I	I	O	I	1
M/S	DCLKS	Oscillator circuit	Power Supply Circuit	DCLK	FR	FRS	/BCT																																		
H	H	Enable	Enable	O	O	O	O																																		
	L	Disable	Enable	I	O	O	O																																		
L	H	Disable	Disable	I	I	O	I																																		
	L	Disable	Disable	I	I	O	I																																		
DCLK	I/O	<p>This is the display clock input terminal The following is true depending on the M/S and DCLKS status.</p> <table border="1"> <thead> <tr> <th>M/S</th> <th>DCLKS</th> <th>DCLK</th> </tr> </thead> <tbody> <tr> <td rowspan="2">H</td> <td>H</td> <td>Output</td> </tr> <tr> <td>L</td> <td>Input</td> </tr> <tr> <td rowspan="2">L</td> <td>H</td> <td>Input</td> </tr> <tr> <td>L</td> <td>Input</td> </tr> </tbody> </table> <p>When the EM65565A chips are used in master/slave mode, the various DCLK terminals must be connected.</p>	M/S	DCLKS	DCLK	H	H	Output	L	Input	L	H	Input	L	Input	1																									
M/S	DCLKS	DCLK																																							
H	H	Output																																							
	L	Input																																							
L	H	Input																																							
	L	Input																																							
FR	I/O	<p>This is the liquid crystal alternating current signal I/O terminal. M/S = "H": Output, M/S = "L": Input When the EM65565A Series chip is used in master/slave mode, the various FR terminals must be connected.</p>	2																																						
/BCT	I/O	<p>This is the LCD blanking control terminal. M/S = "H": Output, M/S = "L": Input When the EM65565A chip is used in master/slave mode, the various /BCT terminals must be connected.</p>	1																																						
FRS	O	<p>This is the output terminal for the static drive. This terminal is only enabled when the static indicator display is ON when in master operation mode, and is used in conjunction with the FR terminal.</p>	1																																						
IRS	I	<p>This terminal selects the resistors for the V<sub>0</sub> voltage level adjustment. IRS = "H": Use the internal resistors IRS = "L": Do not use the internal resistors. The V<sub>0</sub> voltage level is regulated by an external resistive voltage divider attached to the V<sub>R</sub> terminal. This pin is enabled only when the master operation mode is selected. It is fixed to either "H" or "L" when the slave operation mode is selected.</p>	1																																						
/PCT	I	<p>This is the power control terminal for the power supply circuit for liquid crystal drive. /PCT = "H": Normal mode, /PCT = "L": High power mode This pin is enabled only when the master operation mode is selected. It is fixed to either "H" or "L" when the slave operation mode is selected.</p>	1																																						

(Continuous)

Pin Name	I/O	Function	No. of Pins																												
SEG0 To SEG131	O	<p>These are the liquid crystal segment drive outputs. Through a combination of the contents of the display RAM and with the FR signal, a single level is selected from <math>V_0</math>, <math>V_2</math>, <math>V_3</math>, and <math>V_{SS}</math>.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left;">RAM DATA</th> <th style="text-align: left;">FR</th> <th colspan="2" style="text-align: left;">Output Voltage</th> </tr> <tr> <td></td> <td></td> <th style="text-align: left;">Normal Display</th> <th style="text-align: left;">Reverse Display</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td><math>V_0</math></td> <td><math>V_2</math></td> </tr> <tr> <td>H</td> <td>L</td> <td><math>V_{SS}</math></td> <td><math>V_3</math></td> </tr> <tr> <td>L</td> <td>H</td> <td><math>V_2</math></td> <td><math>V_0</math></td> </tr> <tr> <td>L</td> <td>L</td> <td><math>V_3</math></td> <td><math>V_{SS}</math></td> </tr> <tr> <td>Power Save &amp; Display OFF</td> <td>--</td> <td colspan="2"><math>V_{SS}</math></td> </tr> </tbody> </table>	RAM DATA	FR	Output Voltage				Normal Display	Reverse Display	H	H	$V_0$	$V_2$	H	L	$V_{SS}$	$V_3$	L	H	$V_2$	$V_0$	L	L	$V_3$	$V_{SS}$	Power Save & Display OFF	--	$V_{SS}$		132
RAM DATA	FR	Output Voltage																													
		Normal Display	Reverse Display																												
H	H	$V_0$	$V_2$																												
H	L	$V_{SS}$	$V_3$																												
L	H	$V_2$	$V_0$																												
L	L	$V_3$	$V_{SS}$																												
Power Save & Display OFF	--	$V_{SS}$																													
COM 0 To COM 63	O	<p>These are the LCD common drive outputs. COM0 to COM63 Through a combination of the contents of the scan data and with the FR signal, a single level is selected from <math>V_0</math>, <math>V_1</math>, <math>V_4</math>, and <math>V_{SS}</math>.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left;">Scan Data</th> <th style="text-align: left;">FR</th> <th colspan="2" style="text-align: left;">Output Voltage</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td colspan="2"><math>V_{SS}</math></td> </tr> <tr> <td>H</td> <td>L</td> <td colspan="2"><math>V_0</math></td> </tr> <tr> <td>L</td> <td>H</td> <td colspan="2"><math>V_1</math></td> </tr> <tr> <td>L</td> <td>L</td> <td colspan="2"><math>V_4</math></td> </tr> <tr> <td>Power Save</td> <td>--</td> <td colspan="2"><math>V_{SS}</math></td> </tr> </tbody> </table>	Scan Data	FR	Output Voltage		H	H	$V_{SS}$		H	L	$V_0$		L	H	$V_1$		L	L	$V_4$		Power Save	--	$V_{SS}$		64				
Scan Data	FR	Output Voltage																													
H	H	$V_{SS}$																													
H	L	$V_0$																													
L	H	$V_1$																													
L	L	$V_4$																													
Power Save	--	$V_{SS}$																													
COMS	O	<p>These are the common output terminals for the indicator. Both terminals output the same signal. Leave these open if they are not used. When in master/slave mode, the same signal is output by both master and slave.</p>	2																												

Preliminary

**BLOCK DIAGRAM**

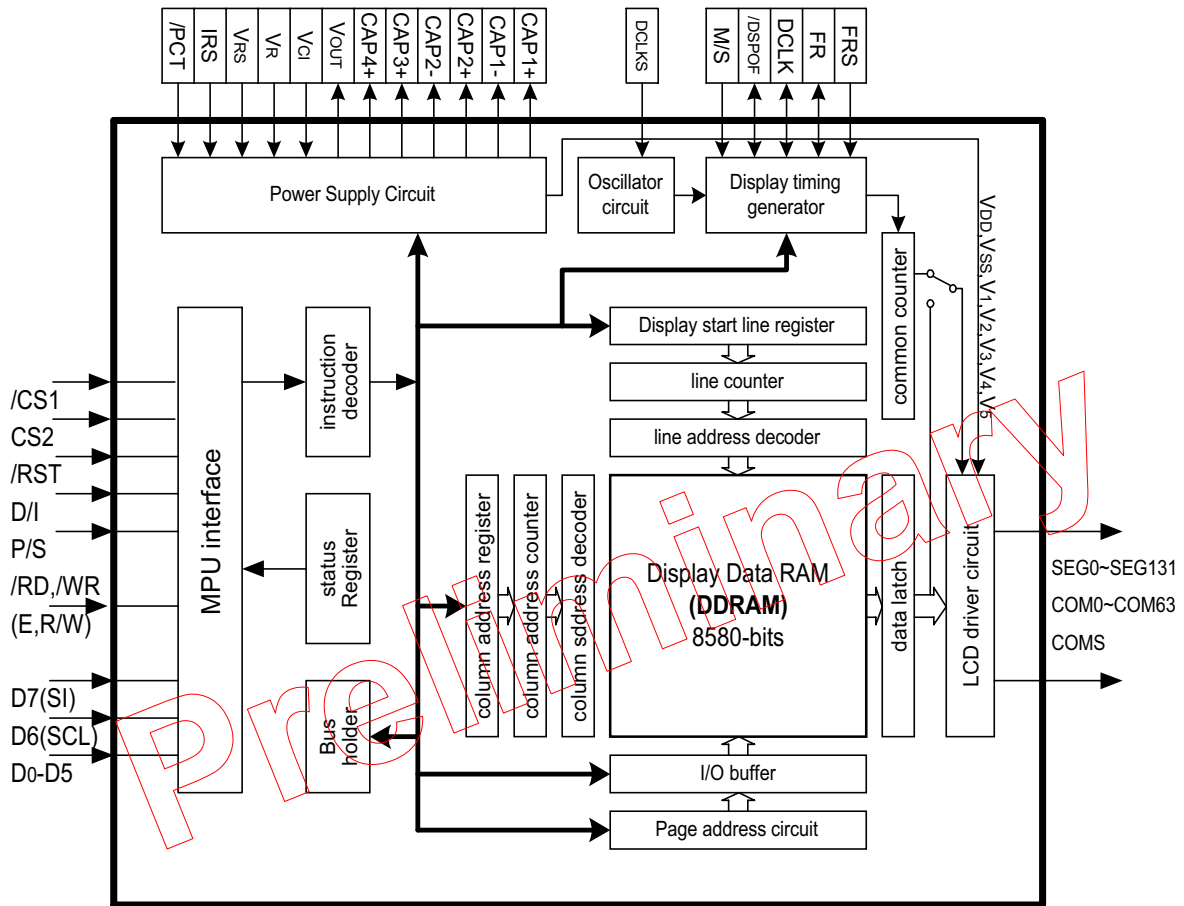


Fig. 1 Block diagram of System

## FUNCTIONAL DESCRIPTIONS

### The MPU Interface

#### Selecting the interface Type

The EM65565A chip can be selected either parallel interface or serial interface by the P/S terminal polarity to the “H” or “L”, as shown in Table 2

Table 2

PS	/CS1	CS2	D/I	/RD	/WR	MPUS	D7	D6	D5~D0
H: Parallel Input	↑	↑	↑	↑	↑	↑	↑	↑	↑
L: Serial Input	↑	↑	↑	--	--	--	SI	SCL	(HZ)

--“Indicates fixed to either “H” or to “L”

#### The Parallel Interface:

When the parallel interface has been selected (P/S=“H”), then it is possible to connect directly to either an 80-series MPU or a 68-series MPU by selecting the MPUS terminal to either “H” or to “L”.

Table 3

MPUS	/CS1	CS2	D/I	/RD	/WR	D7~D0
L: 80-series MPU	↑	↑	↑	↑	↑	↑
H: 68-series MPU	↑	↑	↑	E	R/W	↑

Identification of data bus signals by a combination of D/I, /RD (E), /WR (R/W) signals as shown in Table 4.

Table 4

D/I	68-Series	80-Series		Function
	R/W	/RD	/WR	
1	1	0	1	Reads display data
1	0	1	0	Writes display data
0	1	0	1	Read status
0	0	1	0	Write control data (command)

#### The Serial Interface:

When the chip is active state (/CS1=“L” and CS2=“H”) the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the SI pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the 8th serial clock for the processing.

The D/I input is used to determine whether or the serial data input is display data (D/I=“H”) or command data (D/I=“L”). The D/I input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active. Figure 2 is a serial interface signal chart.

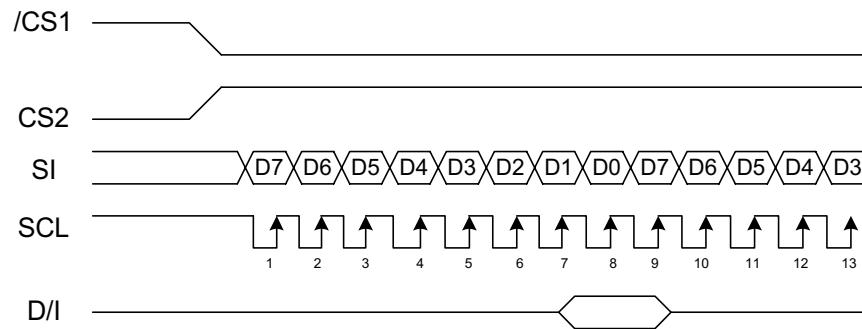


Fig. 2

**Notes:**

1. When the chip is not active, the shift registers and counter are reset to their initial states.
2. Reading is not possible while in serial interface mode.
3. Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

**The Chip Select**

The EM65565A chip have two chip select terminals: /CS1 and CS2. The MPU interface or the serial interface is enabled only when /CS1="L" and CS2="H". When the chip select is inactive. D0 to D7 enter a high impedance state, and the D/I, /RD, and /WR inputs are inactive. When the serial interface is selected. The shift register and the counter are reset.

**Accessing the *DDRAM* and the Internal Registers**

In order to make matching of operation frequencies between the MPU and *DDRAM* or internal register, the EM65565A performs a sort of LSI-LSI pipelining via the bus holder attached to the internal data bus.

When the MPU writes data to the *DDRAM*, once the data is stored in the bus holder, then it is written to the *DDRAM* before the next data write cycle. Moreover, when the MPU reads the *DDRAM*, the first data read cycle (dummy) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle.

There is a certain restriction in the read sequence of the *DDRAM*. Please be advised that data of the specified address is not generated by the read instruction issued immediately after the address setup. This data is generated in data read of the second time. Thus, a dummy read is required whenever the address setup or the write cycle operation is conducted. This relationship is shown in Figure 3.

**The Busy Flag**

The busy flag is output to pin D7 by a read status command. When the busy flag is "1" it indicates that the EM65565A chip is executing its internal operations, any command other than status read is rejected during this time. If the cycle time ( $t_{CYC}$ ) is maintained, this flag needs not be check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.



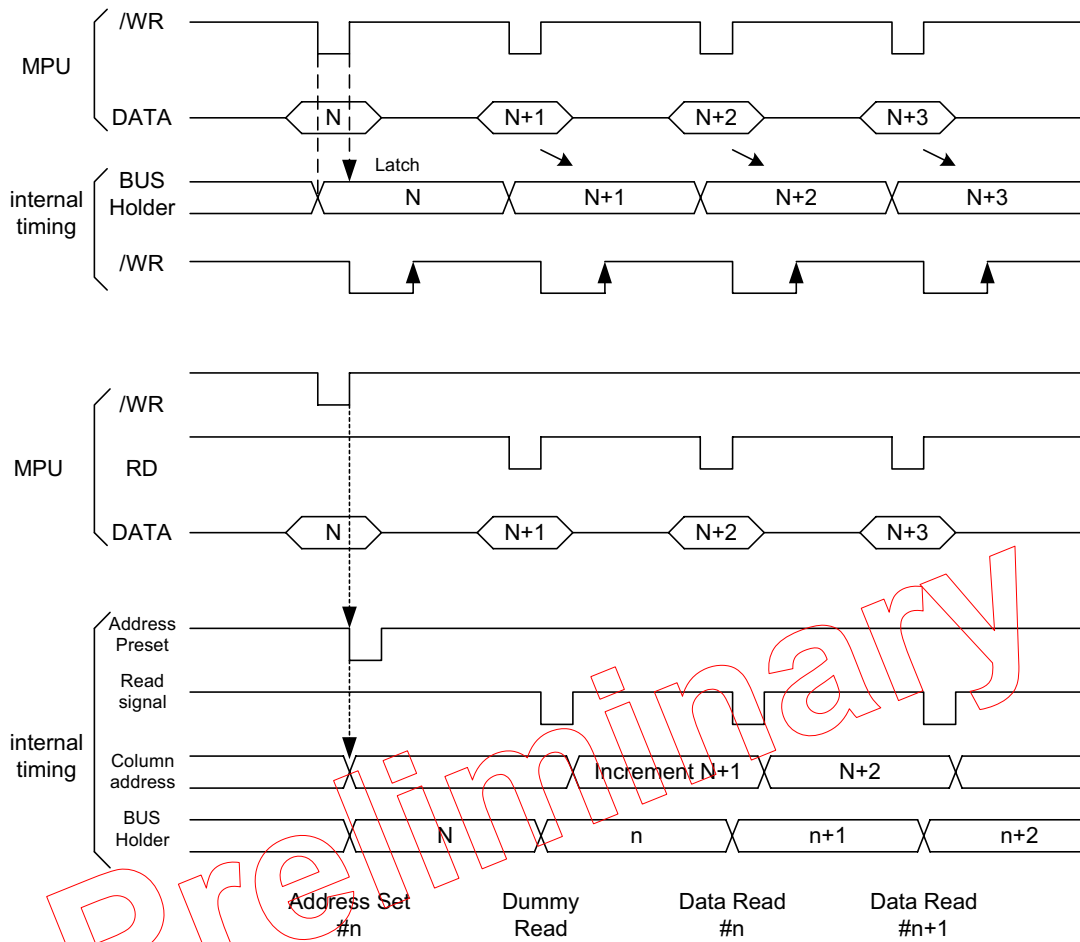


Fig. 3

### The Page Address Circuit

The page address of the *DDRAM* is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access. Page address 8 is the page for the RAM region used only by the static indicators, and only display data D0 is used.

### The Line Address Circuit

The line address circuit specifies the line address relating to the common output when the contents of the *DDRAM* are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COM63 output for EM65565A when the common output mode is reversed). The display area is a 65 lines area for the EM65565A from the display start line address.

If the line address is changed dynamically using the display start line address set command, screen scrolling, Page swapping, etc. can be performed.

**The Column Addresses circuit**

The *DDRAM* column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously. Moreover, the increment of column address stops with 83H. Because the column address is independent of the page address, when moving, for example, from page 0 column 83H to page 1 column 00H, it is necessary to specify both the page address and the column address.

Furthermore, the ADC command can be used to reverse the relationship between the *DDRAM* column address and the segment output. Because of this, the constraints on the IC layout when the *LCD* module is assembled can be minimized.

**Display Data RAM (DDRAM)**

The *DDRAM* is a RAM that stores the dot data for the display. It has a 65×132 bits. It is possible to access the desired bit by specifying the page address and the column address. The D7 to D0 display data from the MPU corresponds to the *LCD* common direction. There are few constraints at the time of display data transfer when multiple EM65565A chip is used. Thus and display structures can be created easily and with a high degree of freedom. Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the *DDRAM* is accessed asynchronously during *LCD*, it will not cause adverse effects on the display (such as flickering).

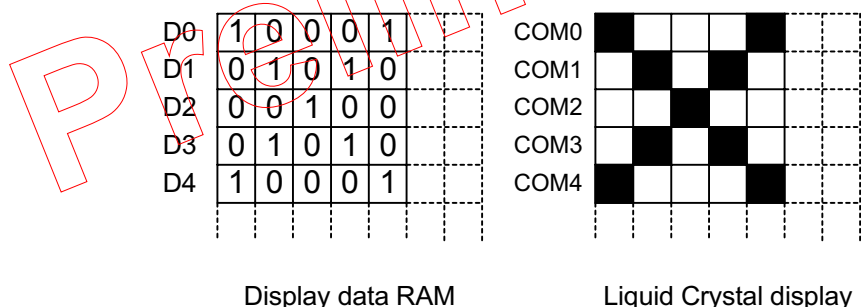


Fig. 4

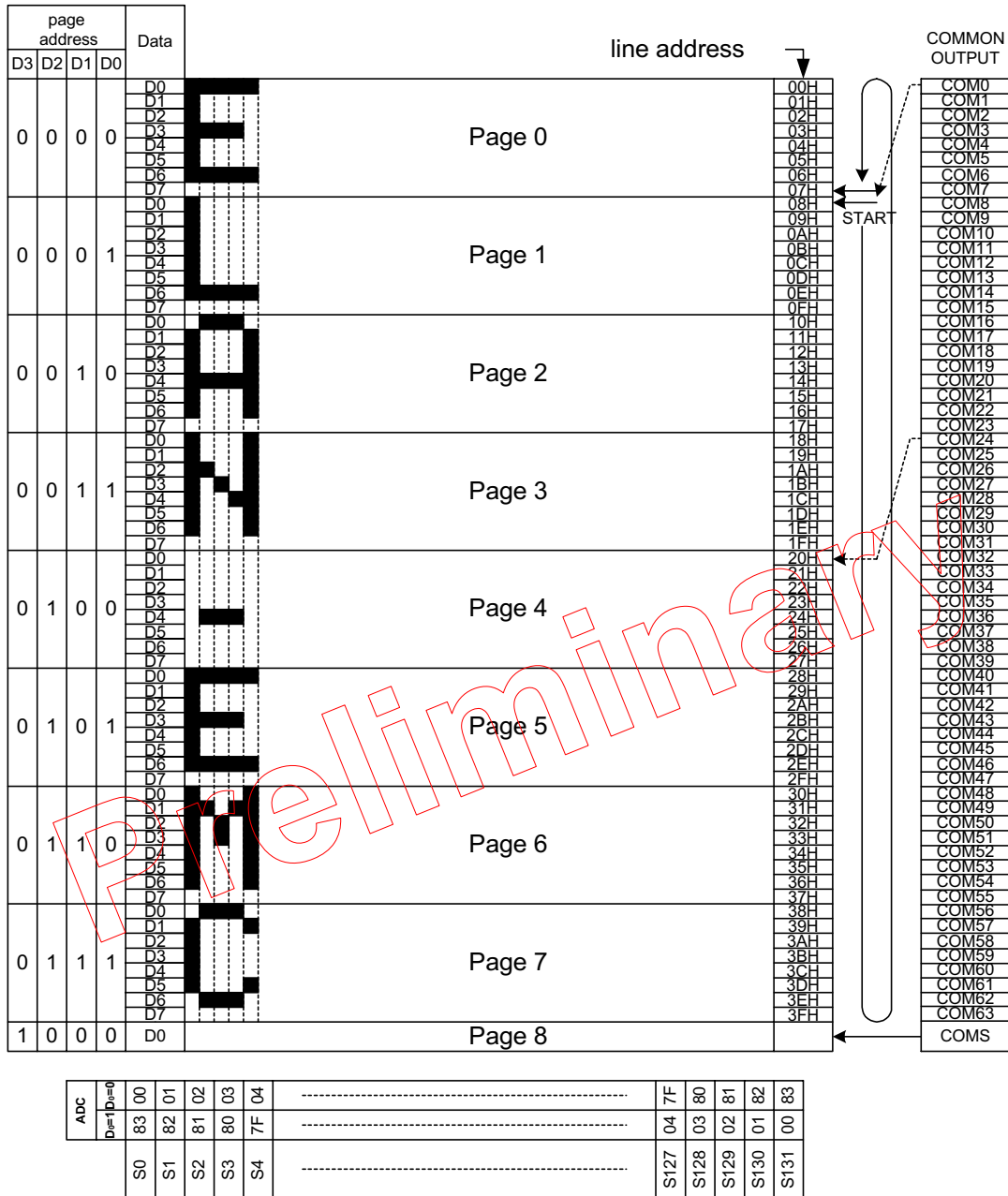


Fig. 5 DDRAM

**The Display Data Latch Circuit**

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver from the DDRAM. Because the display normal/reverse status, Display ON/OFF status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the DDRAM itself.

**The Oscillator Circuit**

This is a CR-type oscillator that produces the display clock. The oscillator circuit is only enabled when M/S="H" and DCLKS="H". When DCLKS="L" the oscillation stops, and the display clock is input through the DCLK terminal.

**Display Timing Generator Circuit**

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of accesses to the *DDRAM* by the MPU. Consequently, even if the *DDRAM* is accessed asynchronously during *LCD*, there is absolutely no adverse effect (such as flickering) on the display.

Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive wave from using a two-frames alternating current drive method, as is shown in Figure 6, for the liquid crystal drive circuit.

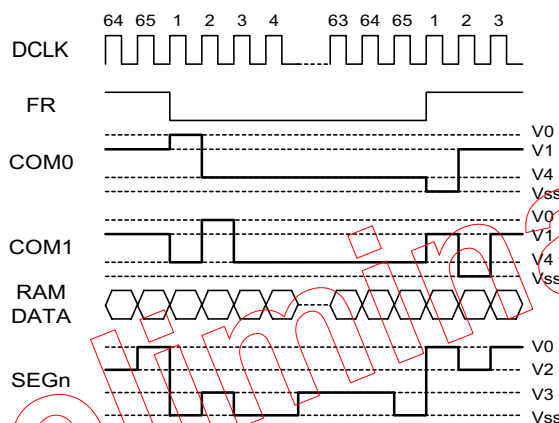


Fig. 6

When plural EM65565A chip are used. The slave chips must be supplied the display timing signals (FR, DCLK, /BCT) from the master chip(s). Explain as following Table 5.

Table 5

Operating Mode		FR	DCLK	/BCT
Master (M/S = "H")	The internal oscillator circuit is enabled (DCLKS="H")	O	O	O
	The internal oscillator circuit is disabled (DCLKS="L")	O	I	O
Slave (M/S = "L")	The internal oscillator circuit is enabled (DCLKS="H")	I	I	I
	The internal oscillator circuit is disabled (DCLKS="L")	I	I	I

O: Output, I: Input

Note: When the EM65565A is used for the master/slave configuration, each of the DCLKS pins is set to the same level together.

**The Common Output Status Select Circuit**

In the EM65565A chip, the COM output scan direction can be selected by the common output status select command. (See Table 6.) Consequently, the constrains in IC layout at the time of *LCD* module assembly can be minimized.

Table 6

Status	COM Scan Direction
Normal	COM0 → COM63
Reverse	COM63 → COM0

**The LCD Driver Circuits**

These are a 197-channel that generates four voltage levels for driving the liquid crystal. The combination of the display data, the COM scan signal, and the FR signal produces the liquid crystal drive voltage output. Figure 7 shows examples of the SEG and COM output waveform.

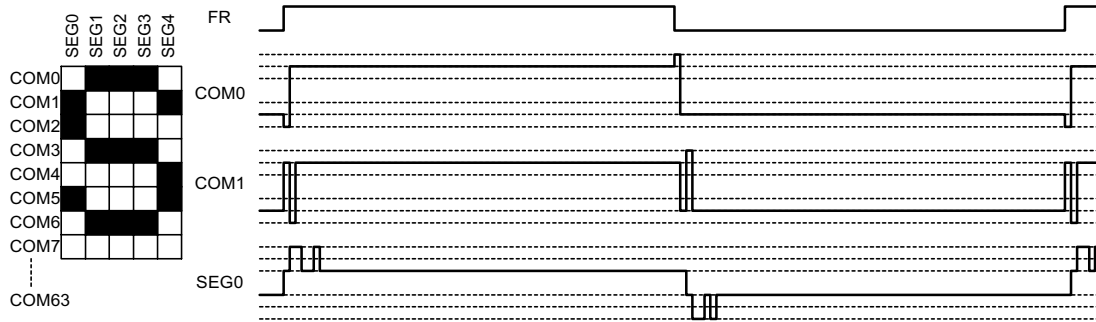


Fig. 7

**The Power Supply Circuits**

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for liquid crystal drivers. They comprise Booster (step-up voltage) circuits, Voltage regulator circuits, and voltage follower circuits. They are only enabled in master operation.

The power supply circuit can turn the Booster circuits, the voltage regulator circuits and the voltage follower circuit ON or OFF independently through the use of the Power Control Set command. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel.

**The Step-up Voltage Circuit:**

Using the step-up voltage circuit equipped within the EM65565A chip it is possible to produce a five times step-up, a four times step-up, and a three times, and a two times step-up of the  $V_{CI}$  voltage levels. The step-up voltage relationships are shown in Figure 8.

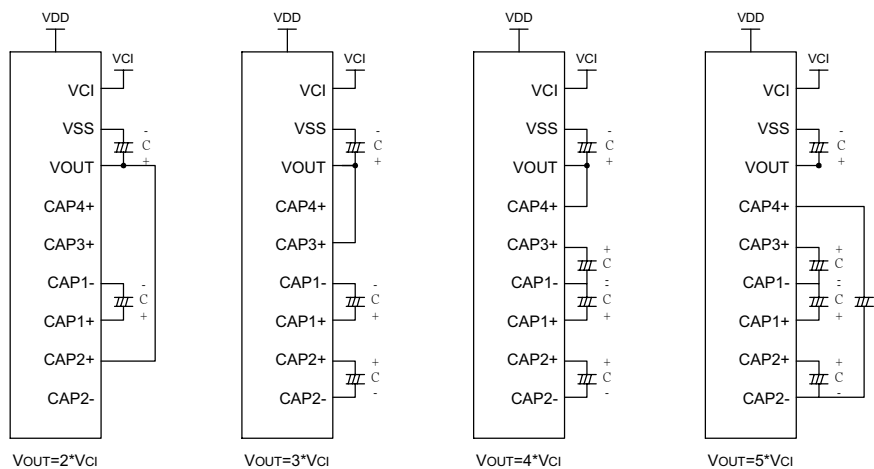


Fig. 8

**The Voltage Regulator Circuit**

The step-up voltage generated at  $V_{OUT}$  output the LCD driver voltage  $V_0$  through the voltage regulator circuit.

Because the EM65565A chip has an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the  $V_0$  voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components. Moreover, in the EM65565A, types of thermal gradients have been prepared as  $V_{REG}$  options: Approximately  $-0.05\%/^{\circ}C$ ,  $-0.2\%/^{\circ}C$  and external input (from  $V_{RS}$  pin)

(a) When the  $V_0$  voltage regulator internal resistors are used

Through the use of the  $V_0$  voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage  $V_0$  can be controlled by commands alone (without adding any external resistors), making it possible to adjust the LCD brightness. The  $V_0$  voltage can be calculated using equation A over the range where  $V_0 < V_{OUT}$ .

$$V_0 = \left(1 + \frac{R_b}{R_a}\right)V_{EV} = \left(1 + \frac{R_b}{R_a}\right)\left(1 - \frac{\alpha}{162}\right)V_{REG} \text{ -----(A)}$$

$$\therefore V_{EV} = \left(1 - \frac{\alpha}{162}\right)V_{REG}$$

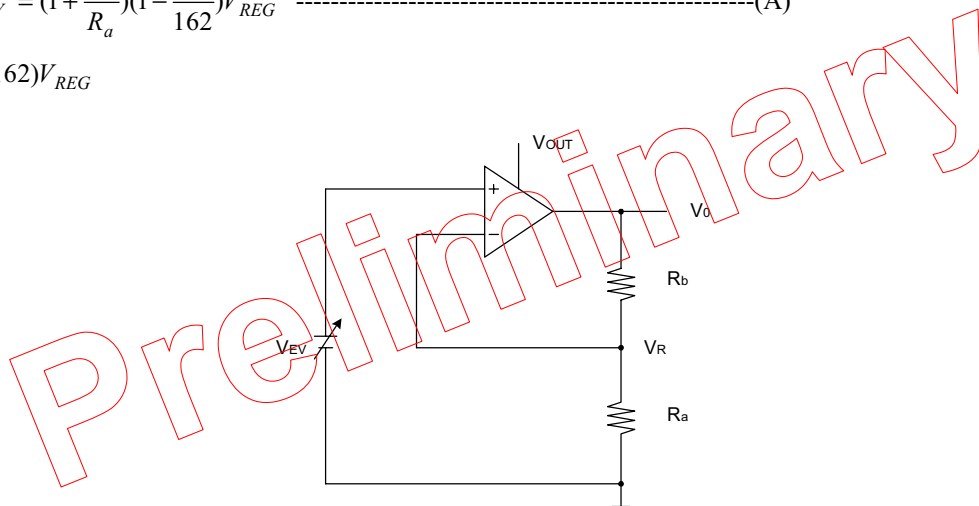


Fig. 9

$V_{REG}$  is the IC-internal fixed voltage supply, and its voltage at  $T_a=25^{\circ}C$  is shown as following:

Type of thermal gradient	$V_{REG}$
$-0.05\%/^{\circ}C$	2.1V
$-0.2\%/^{\circ}C$	2.1V
External input	$V_{RS}$

The  $\alpha$  is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume register. Table 7 shows the value for  $\alpha$  depending on the electronic volume register settings.

Table 7

D5	D4	D3	D2	D1	D0	$\alpha$
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
			:			:
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

$R_b/R_a$  is the  $V_0$  voltage regulator internal resistor ratio and can be set to 8 different levels through the  $V_0$  voltage regulator internal resistor ratio set command. The  $(1+R_b/R_a)$  ratio assumes the values shown in Table 8 depending on the 3-bit data settings in the  $V_0$  voltage regulator internal resistor ratio register.

Table 8

Register			Type of thermal gradients		
			-0.05%/°C	-0.2%/°C	External input
<b>D2</b>	<b>D1</b>	<b>D0</b>	<b>1+(Rb/Ra) ratio</b>		
0	0	0	3.0	3.0	1.5
0	0	1	3.5	3.5	2.0
0	1	0	4.0	4.0	2.5
0	1	1	4.5	4.5	3.0
1	0	0	5.0	5.0	3.5
1	0	1	5.5	5.5	4.0
1	1	0	6.0	6.0	4.5
1	1	1	6.4	6.4	5.0

Fig.9 show,  $V_0$  voltage measured by values of the internal resistance ratio resistor for  $V_0$  voltage adjustment and electric volume resistor for each temperature grade model. When  $T_a=25^\circ\text{C}$ . The  $V_0$  voltage as a function of the  $V_0$  voltage regulator, internal resistor ratio register and the electronic volume register.

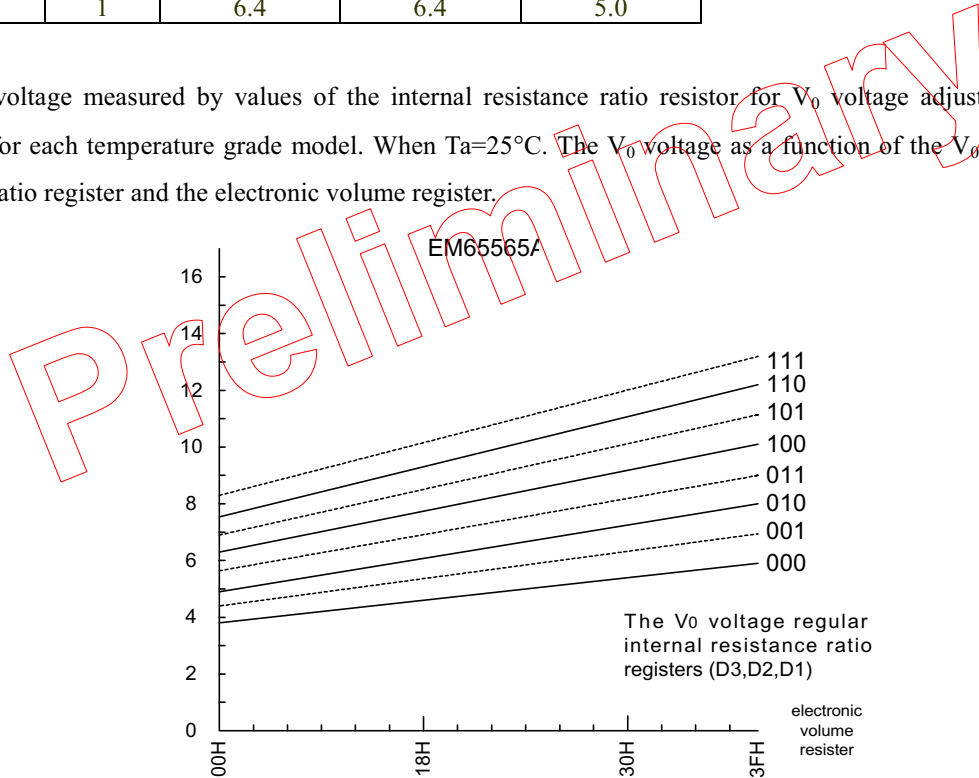


Fig. 10 Where the Thermal Gradient= -0.05%/°C and -0.2%/°C

(b) When an External Resistance is Used

The liquid crystal power supply voltage  $V_0$  can also be set without using the  $V_0$  voltage regulator internal resistors by adding resistors  $R_a'$  and  $R_b'$ . When this is done, the use of the electronic volume function makes it possible to adjust the brightness of the LCD by controlling the LCD power supply voltage  $V_0$  through commands. In the range where  $V_0 < V_{OUT}$ , the  $V_0$  voltage can be calculated using equation B based on the external resistances  $R_a'$  and  $R_b'$ .

$$V_5 = \left(1 + \frac{R_b'}{R_a'}\right)V_{EV} = \left(1 + \frac{R_b'}{R_a'}\right)\left(1 - \frac{\alpha}{162}\right)V_{REG} \text{ -----(B)}$$

$$\therefore V_{EV} = \left(1 - \frac{\alpha}{162}\right)V_{REG}$$

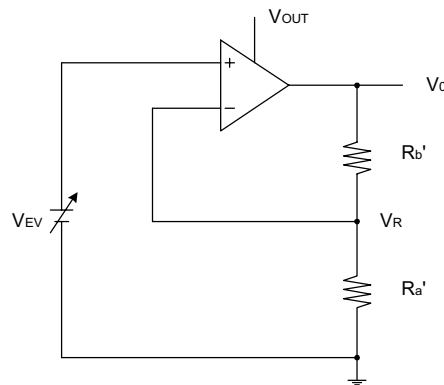


Fig. 11

### The Liquid Crystal Voltage Generator Circuit

The  $V_0$  voltage is produced by a resistive voltage divider within the IC, and can be produced at the  $V_1$ ,  $V_2$ ,  $V_3$  and  $V_4$  voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides  $V_1$ ,  $V_2$ ,  $V_3$ , and  $V_4$  to the liquid crystal drive circuit. 1/9 bias or 1/7 bias for EM65565A can be selected.

### The Power Supply Control Circuit

The power supply circuit equipped in the EM65565A Series chip has very power consumption (normal mode: /PCT = "H"). However, for LCDs or panels with large loads, this low-power power supply may cause display quality to degrade. When this occurs, setting the /PCT terminal to "L" (high power mode) can improve the quality of the display. We recommend that the display be checked on actual equipment to determine whether or not to use this mode.

Moreover, if the improvement to the display is inadequate even after high power mode has been set, then it is necessary to add a liquid crystal drive power supply externally.

### The Internal Power Supply Shutdown Command Sequence

The sequence is recommended for shutting down the internal power supply, first placing the power supply in power saver mode and then turning the power supply OFF.

Step1: display OFF.

Step2: display all point ON.

Step3: internal power supply OFF.

### Reference Circuit Example

Figure 21 shows reference circuit examples.

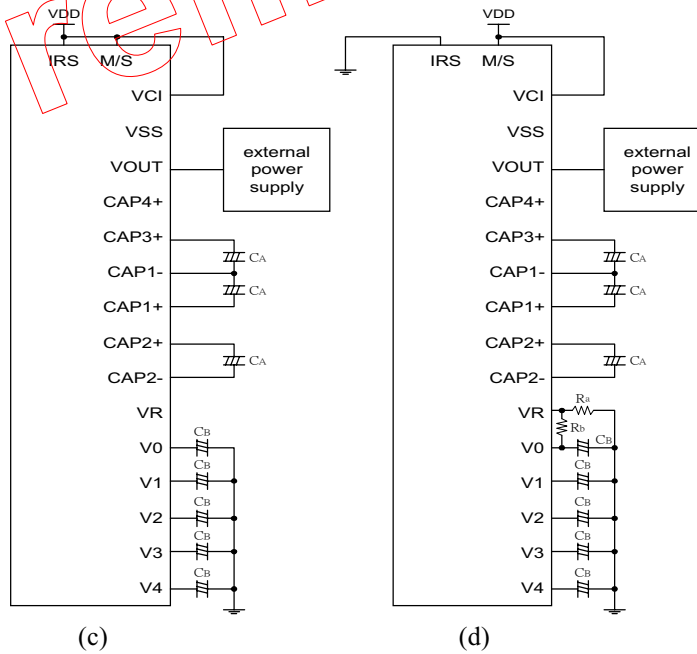
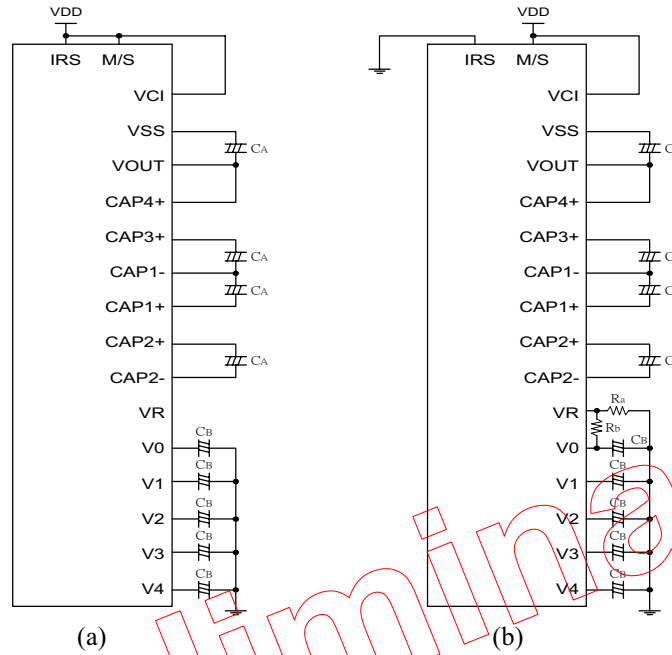
1. When used all of the step-up circuit, voltage regulating circuit and V/F circuit, and the voltage regulator internal resistor is used. Fig 12-(a)
2. When used all of the step-up circuit, voltage regulating circuit and V/F circuit, and the voltage regulator internal resistor is not used. Fig 12-(b).
3. When the voltage regulator circuit, V/F circuit and the  $V_0$  voltage regulator internal resistor are used. Fig 12-(c).
4. When the voltage regulator circuit and V/F circuit are used, and the  $V_0$  voltage regulator internal resistor is not used. Fig



12-(d).

5. When the V/F circuit is used. Fig 12-(e)

6. When not using any internal LCD power supply circuit. Fig 12-(f)



Preliminary

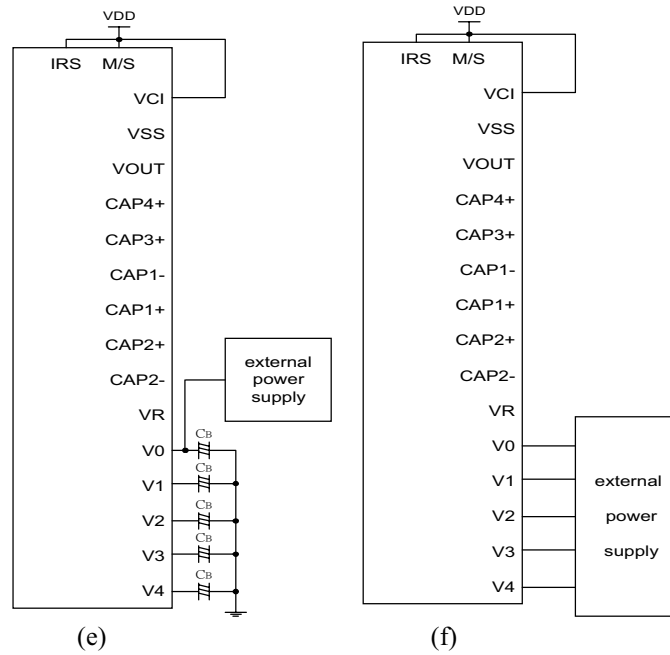


Fig. 12

Examples of shared reference settings. When  $V_0$  can vary between 8 and 12V

Item	Set value
$C_A$	1.0 – 4.7 $\mu$ F
$C_B$	0.47 – 1.0 $\mu$ F

Notes:

1. Because the  $V_R$  terminal input impedance is high, use short leads and shielded lines.
2.  $C_A$  and  $C_B$  are determined by the size of the LCD being driven. Select a value that will stabilize the liquid crystal drive voltage.

**The Reset Circuit**

When the /RST input falls to “L”, these LSI reenter their default state. The default settings are shown below:

1. Display OFF
2. Normal display
3. ADC select: normal (ADC command D0 = 0)
4. Power control resistor: (D2, D1, D0) = (0,0,0)
5. Serial interface internal register data clear
6. LCD power supply bias ratio: 1/9 bias
7. Read-modify-write OFF
8. Static indicator OFF: Static indicator register: (D1, D2) = (0,0)
9. Display start line set to first line
10. Column address set to address 0
11. Page address set to page 0

12. Common output status normal

13. V<sub>0</sub> voltage regulator internal power supply ratio set mode clear

V<sub>0</sub> voltage regulator internal resistor ratio register: (D2, D1, D0) = (1,0,0)

14. Electronic volume register set mode clear

Electronic volume register: (D5, D4, D3, D2, D1, D0) = (1,0,0,0,0,0)

15. Test mode clear

On the other hand, when the reset command is used only default settings 7 to 15 above are put into effect. The /RST terminal is connected to the MPU reset terminal, making the chip reinitialize simultaneously with the MPU. At the time of power up, it is necessary to reinitialize using the /RST terminal.

In the EM65565A, if the internal liquid crystal power supply circuit is not used, then it is necessary to apply an “L” signal to the /RST terminal when the external liquid crystal power supply is applied.

Even though the oscillator circuit operates while the /RST terminal is “L” the display timing generator circuit is stopped, and the DCLK, FR, FRS, and /BCT terminals are fixed to “H”. There is no influence on the D0 to D7 terminals.

## COMMANDS

Table 9

Command	Command Code											Functions	
	D/I	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0		
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	1	D	LCD display ON/OFF D=0:OFF, D=1:ON
Display start line set	0	1	0	0	1	Display start address					Sets the display RAM display start line address		
Page address set	0	1	0	1	0	1	1	Page address			Sets the display RAM page address		
Column address set upper bit	0	1	0	0	0	0	1	Most column address			Sets the most 4 bits of the display RAM column address.		
Column address set lower bit	0	1	0	0	0	0	0	Least column address			Sets the least 4 bits of the display RAM column address.		
Status read	0	0	1	Status				0	0	0	0	0	Reads the status data
Display data write	1	1	0	Write data								Writes to the display RAM	
Display data read	1	0	1	Read data								Reads from the display RAM	
ADC select	0	1	0	1	0	1	0	0	0	0	0	D	Sets the display RAM address SEG output correspondence D=0:normal, 1:reverse
Display normal/reverse	0	1	0	1	0	1	0	0	1	1	1	D	Sets the LCD display normal/reverse D=0:normal, 1:reverse
Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0	D	Display all points D=0: normal display D=1: all points ON
LCD bias set	0	1	0	1	0	1	0	0	0	1	1	D	Sets the LCD drive voltage bias ratio D=0: 1/9, D=1:1/7
Read-modify-write	0	1	0	1	1	1	0	0	0	0	0	0	Column address only increment at write: +1
End	0	1	0	1	1	1	0	1	1	1	1	0	Stop read-modify-write
Reset	0	1	0	1	1	1	0	0	0	1	0	0	Internal reset
Common output mode select	0	1	0	1	1	0	0	.	.	.	.	.	Select COM output scan direction D=0:normal direction D=1:reverse direction

(Continuous)

Command	Command Code										Functions	
	D/I	/RD	/WR	D7	D6	D5	D4	D3	D2	D1		D0
Power control set	0	1	0	0	0	1	0	1	Operating mode		Select internal power Supply operating mode	
V <sub>0</sub> voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio		Select internal resistor ratio mode	
Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	Set the V <sub>0</sub> output voltage electronic volume register	
Electronic volume Register set	0	1	0	.	.	Electronic volume value						
Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	D	D=0:OFF, D=1:ON
Static indicator register set	1	0	1	.	.	.	.	.	.	Mode		Set the flashing mode
Power saver	0	1	0	1	0	1	0	1	1	1	0	Display OFF and display all points ON compound command
				1	0	1	0	0	1	0	1	
NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
Test	0	1	0	1	1	1	1	.	.	.	.	Command for IC test. Don't use this command

#### Display ON/OFF

This command turns the display on and off. When the display OFF command is executed when in display all point ON mode, power saver mode is entered.

(AEH, AFH)

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

D=0:Display turn OFF

D=1:Display turn ON

#### Set Display start line

This command specifies a line address thus marking the display line that corresponds to C0.

(40H to 7FH)

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

A5	A4	A3	A2	A1	A0	Line Address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
↓	↓	↓	↓	↓	↓	↓
1	1	1	1	1	0	62
1	1	1	1	1	1	63

#### Set Column address

This command specifies a *DDRAM* column address. The column address is split into two parts (the upper 4-bits and the lower 4-bits) when it set. The column address is automatically incremented by 1 each time the MPU accesses from the set address to the *DDRAM*. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 131 (83H), and the page address is not changed continuously.



**Upper bits (10H to 18H), Lower bits (00H to 0FH)**

D/I	/RD	/WR(R/W)		D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	Upper bits	0	0	0	1	A7	A6	A5	A4
			Lower bits	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
↓	↓	↓	↓	↓	↓	↓	↓	↓
1	0	0	0	0	0	0	1	129
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

**Set Page address**

This command is used to specify a page address equivalent to a row address for MPU access to the *DDRAM*.

**(B0H to B8H)**

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Page number
0	0	0	0	0
0	0	0	1	1
↓	↓	↓	↓	↓
0	1	1	1	7
1	0	0	0	8

**Select ADC**

This command specifies a segment driver direction. The column address is automatically incremented by 1 each time when the read or write the display data.

**(A0H, A1H)**

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

D=0 clockwise output (forward) S0(00H)→S131(83H)

D=1 counterclockwise output (reverse) S0(83H)→S131(00H)

**Write display data**

Write data from data bus into *DDRAM*. Since the column address is automatically incremented by “1” after write.

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

**Read display data**

Read data from *DDRAM* onto data bus. Since the column address is automatically incremented by “1” after read. When the serial interface is used, reading of the display data becomes invalid.

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

**Read status**

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	Busy	ADC	ON/OFF	Reset	0	0	0	0

**Busy:** the busy bit indicated whether the driver accept instruction or not.

Busy=0: the driver will be accepted new instruction

Busy=1: no new instruction will be accepted.

**ADC:**

ADC=0: reverse (column address 131-n ↔ segment driver n)

ADC=1: Normal (column address n ↔ segment driver n)

**ON/OFF:** indicated the current status of the display

ON/OFF=0: display ON

ON/OFF=1: display OFF

**Reset:** indicates whether the driver is executing a hardware or software reset or if it is in normal operating mode.

Reset=0: Normal operation

Reset=1: currently executing reset instruction

**Read-modify-write**

This instruction defeats column address register auto-increment after data reads. The current contents of the column address register are saved. This mode remains active until an “End” instruction is received.

When the “End” instruction is entered, the column address returned to the one used during input of Read-modify-Write instruction. This function can reduce the load of MPU when data change is repeated at a specific display area (such as cursor blinking). Any instruction can be used in this instruction. However, the column address set instruction cannot be used.

**(E0H)**

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

**End**

This instruction cancels the read modify write instruction, returning the column address to the initial mode address.

**(EEH)**

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

**Reset**

This instruction initialization the display data line register, the column address, the page address counter, the V<sub>0</sub> voltage regulator internal resistor ratio, the electronic volume, and the static indicator are reset, and read-modify-write mode and test mode are released. It does not affect the contents of the *DDRAM*. When the power supply is turned on, a reset signal is entered in the /RST pin. The reset instruction cannot be used instead of this reset signal.

**(E2H)**

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

### Display all point ON

This command makes it possible to force all display points ON regardless of the content of the *DDRAM*. The contents of the *DDRAM* are maintained when this is done.

(A4H, A5H)

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	<b>D</b>	D=0: Normal display D=1: Display all point ON

### Display Normal /Reverse

This command can reverse the lit and unlit display without overwriting the contents of the *DDRAM*. When this is done the *DDRAM* contents are maintained.

(A6H, A7H)

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	<b>D</b>	D=0: Normal (RAM data "H" LCD ON) D=1: Reverse (RAM data "L" LCD ON)

### LCD Bias Set

This command specifies the voltage Bias ratio for *LCD*

(A2H, A3H)

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	1	<b>D</b>	D=0: 1/9 Bias D=1: 1/7 Bias

### Common Output Mode Select

This command can select the scan direction of the common output terminal

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	1	0	0	<b>D</b>	.	.	.	D=0: Normal COM0→COM63 D=1: Reverse COM63→COM0

### Power Controller Set

This command set the function of power supply circuit

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	0	0	1	0	1	<b>D2</b>	<b>D1</b>	<b>D0</b>	Voltage Follower Circuit D0=0: OFF, D0=1: ON Voltage Regular Circuit D1=0: OFF, D1=1: ON Booster Circuit D2=0: OFF, D2=1: ON

### V<sub>0</sub> Voltage Regulator Internal Resistor Ratio Set

This command set the V<sub>0</sub> voltage regulator internal resistor ratio

(20H, 27H)

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0	1+Rb/Ra ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								↓	↓	↓	↓
								1	1	1	Large

### The Electronic Volume

This command is used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other

*The Electronic Volume Mode Set:*

When this command is input, the electronic volume register set command enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used.

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

*Electronic Volume Register Set:*

This command specifies LCD drive voltage V<sub>0</sub> assumes one of the 64 Voltage level. When the electronic volume function is not used, set this to (1,0,0,0,0,0).

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0	V <sub>0</sub>
0	1	0	1	0	0	0	0	0	0	1	Small
					↓	↓	↓	↓	↓	↓	
					1	1	1	1	1	1	Large

### Static Indicator

This command controls the static drive system indicator display. This is used when one of the static indicator LCD drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal.

*Static Indicator ON/OFF:*

When the static indicator ON command is entered. The static indicator register set command is enabled.

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0	Static Indicator
0	1	0	1	0	1	0	1	1	0	<b>D</b>	D=0: OFF D=1: ON

*Static Indicator Register Set:*

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0	Indicator display state
0	1	0	.	.	..	.	.	.	0	0	OFF
									0	1	Blinking at approximately 0.5 second
									1	0	Blinking at approximately one second
									1	1	Constantly on



**Power Save**

The power save mode is entered when the display all point ON is performed while display OFF mode. The power save mode has the sleep mode and the standby mode. The sleep mode is entered when the static indicator is OFF, and the standby mode is entered when the static indicator is ON. This mode is cleared by the display all point OFF.

The sleep mode operation stops all operations in the LCD display system, and as long as there are no accesses from the MPU. In sleep mode operation, the oscillator circuit, the LCD power supply circuit, and all LCD driver circuits are halted.

The standby mode operation, the duty LCD display system operations are halted and only the static driver system for the indicator continues to operate, providing the minimum required consumption current for the static driver. In sleep mode operation, the LCD power supply circuit and the duty system LCD drive circuits are halted. The static drive system does not operate and the oscillator circuit continues to operate.

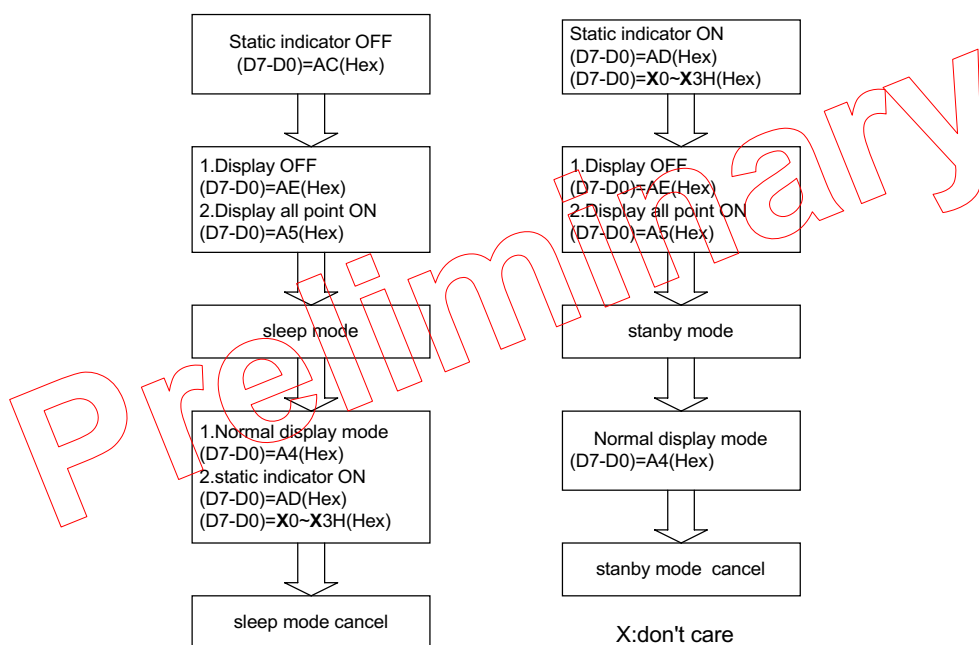


Fig. 13

**NOP**

Non-operation command

**(E3H)**

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

**Test**

This command is for IC chip testing. It can be cleared by applying a “L” signal to /RST input by the reset command or by using a NOP

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	.	.	.	.

**Initialization:**

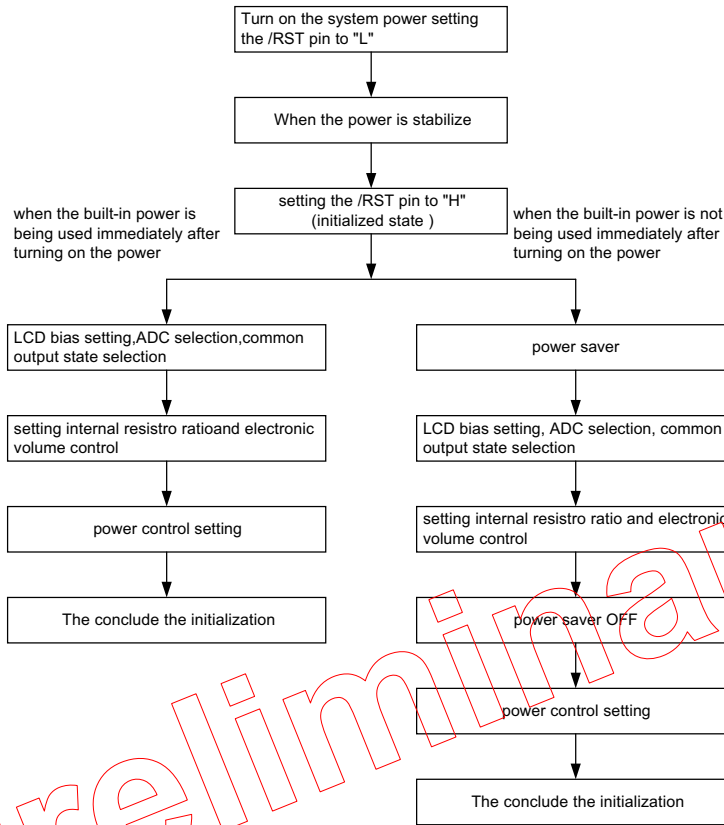


Fig. 14

**The Relationship between oscillator frequency  $f_{OSC}$ , display clock frequency  $f_{CL}$  and the LCD frame rate frequency  $f_{FR}$**

Table 10

Oscillator circuit	$f_{CL}$	$f_{FR}$
When the internal oscillator circuit is used (DCLKS="H")	$F_{OSC}/4$	$f_{CL}/65=f_{OSC}/(4*65)$
When the internal oscillator circuit is not used (DCLKS="L")	External input	$f_{CL}/(4*65)$

## ABSOLUTE MAXIMUM RATINGS

*Table 11 Absolute Maximum Ratings*

Unless otherwise noted,  $V_{SS} = 0\text{ V}$

Parameter		Symbol	Conditions	Unit
Power Supply Voltage		$V_{DD}$	-0.3 to +4.0	V
Power supply voltage		$V_{OUT}, V_0$	-0.3 to 12	V
Power supply voltage		$V_1, V_2, V_3, V_4$	-0.3 to $V_0$	V
Input voltage		$V_{IN}$	-0.3 to $V_{DD} + 0.3$	V
Output voltage		$V_O$	-0.3 to $V_{DD} + 0.3$	V
Operating temperature		$T_{OPR}$	-30 to +85	°C
Storage temperature	TCP	$T_{STR}$	-55 to +100	°C
	COG		-55 to +125	

### Notes and Cautions

1. Insure that the voltage levels of  $V_1, V_2, V_3,$  and  $V_4$  are always such that  $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$ .
2. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

Preliminary

## DC CHARACTERISTICS

Table 12 DC characteristics

Item		Symbol	Condition & Application Pin	Rating			Units
				Min.	Typ.	Max.	
Operating voltage (1)	Recommended voltage	$V_{DD}$	Pin $V_{DD}$	2.7		3.3	V
	Possible operating voltage		Pin $V_{DD}$	2.4		3.3	
Operating voltage (2)	Possible operating voltage	$V_0$		4.5		12	
		$V_1, V_2$		$0.6V_0$		$V_0$	
		$V_3, V_4$		$V_{SS}$		$0.4V_0$	
High-level input voltage		$V_{IHC}$	Pin D/I, D0-D7, /RD, /WR, /CS1, CS2, DCLKS, DCLK, FR, M/S, MPUS, P/S, /BCT, /RST, IRS, /PCT	$0.8V_{DD}$		$V_{DD}$	
Low-level input voltage		$V_{ILC}$		$V_{SS}$		$0.2V_{DD}$	
High-level output voltage		$V_{OHC}$	$I_{OH}=-0.5mA$	Pin D0-D7, FR, FRS, /BCT, DCLK	$0.8V_{DD}$	$V_{DD}$	
Low-level output voltage		$V_{OLC}$	$I_{OL}=-0.5mA$		$V_{SS}$	$0.2V_{DD}$	
Input leakage current		$I_{LI}$	$V_{IN}=V_{DD}$ or $V_{SS}$ Pin D/I, /RD, /WR, /CS1, CS2, DCLKS, M/S, MPUS, P/S, /RST, IRS, /PCT	-1.0		1.0	
Output leakage current		$I_{LO}$	Pin D0-D7, FR, FRS, /BCT, DCLK	-3.0		3.0	
LCD driver ON resistor		$R_{ON}$	$T_a=25^\circ C$ , Pin COMn & SEGn $V_0=8V,  \Delta V =0.1V$		3.2	5.4	$k\Omega$
Static consumption current		$I_{SSO}$	Pin $V_{SS}, V_{SS2}$		0.01	5	$\mu A$
Output leakage current		$I_{OQ}$	$V_0=16V$ , Pin $V_0$		0.01	15	
Sleep mode consumption current		$I_{DD1}$			0.01	5	
Standby mode consumption current		$I_{DD2}$			4	8	
Input terminal capacitance		$C_{IN}$	$T_a=25^\circ C, f=1MHz$		5.0	8.0	$pF$
Oscillator Frequency	Internal oscillator	$f_{OSC}$	$T_a=25^\circ C$	18	22	26	$kHz$
	External input	$f_{DCLK}$	Pin DCLK	18	22	26	
Input voltage		$V_{CI}$	With double	2.4		3.5	V
			With triple	2.4		3.5	
			With quad	2.4		3	
			With five times			2.4	
Supply step-up output voltage		$V_{OUT}$	Pin $V_{OUT}$			12	
Voltage follower circuit operating voltage		$V_{OUT}$	Pin $V_{OUT}$	6		12	
Voltage follower circuit operating voltage		$V_0$	Pin $V_0$	4.5		12	
Base voltage		$V_{REG}$	$T_a=25^\circ C, -0.2\%/^\circ C$ or $-0.05\%/^\circ C$	2.17	2.1	2.03	

Notes:

1. Insure that the voltage levels of  $V_1, V_2, V_3,$  and  $V_4$  are always such that  $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$ .
2. Unless otherwise specified,  $V_{SS} = 0V, V_{DD} = 3.0V \pm 10\%, T_a = -30$  to  $85^\circ C$
3. Dynamic Consumption Current (1), During Display, with the Internal Power Supply OFF Current consumed by total ICs when an external power supply is used.

**Display Pattern OFF**

Item	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Dynamic Consumption Current	$I_{DD} (1)$	$V_{DD} = 3.0 \text{ V}, V_0 = 11.0 \text{ V}$	--	16	27	$\mu\text{A}$

**Display Pattern Checker**

Item	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Dynamic Consumption Current	$I_{DD} (1)$	$V_{DD} = 3.0 \text{ V}, V_0 = 11.0 \text{ V}$	--	21	35	$\mu\text{A}$

Dynamic Consumption Current (2), During Display, with the Internal Power Supply ON

**Display Pattern ON**

Item	Symbol	Condition	Rating			Unit	
			Min.	Typ.	Max.		
Dynamic Consumption Current	$I_{DD} (2)$	$V_{DD} = 3.0 \text{ V}$ , Quad step-up voltage. $V_0 = 11.0 \text{ V}$	Normal Mode	--	81	135	$\mu\text{A}$
			High-Power Mode	--	138	230	

**TIMING DIAGRAM**

System Bus Read/Write timing L (80-Series MPU)

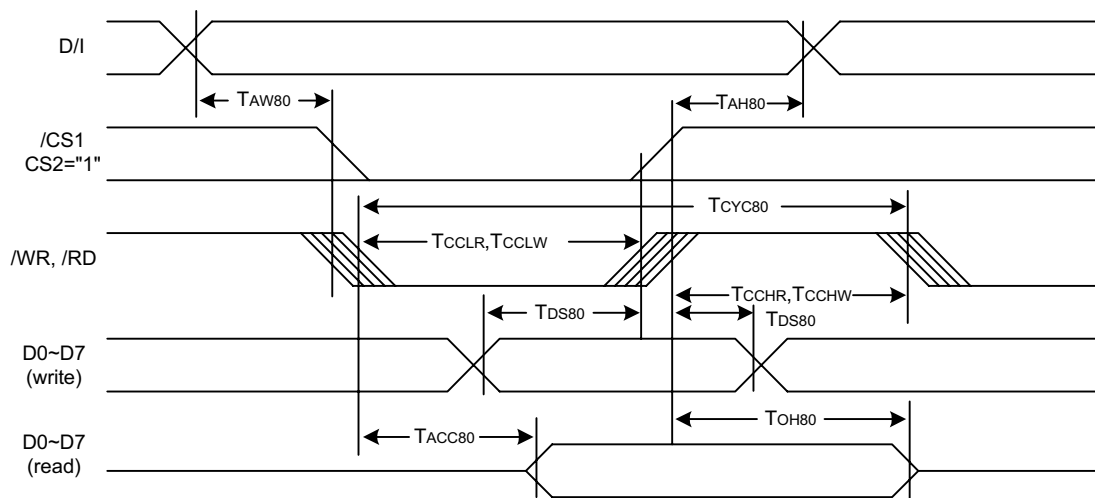


Fig. 15

Table 13 (V<sub>DD</sub>=2.4V to 3.3V, T<sub>a</sub>=-30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	D/I	T <sub>AH80</sub>		0	--	ns
Address setup time		T <sub>AW80</sub>		0	--	ns
System cycle time	D/I	T <sub>CYC80</sub>		300	--	ns
Control L pulse width (/WR)	/WR	T <sub>CCLW</sub>		60	--	ns
Control L pulse width (/RD)	/RD	T <sub>CCLR</sub>		120	--	ns
Control H pulse width (/WR)	/WR	T <sub>CCHW</sub>		60	--	ns
Control H pulse width (/RD)	/RD	T <sub>CCHR</sub>		60	--	ns
Data setup time	D0 to D7	T <sub>DS80</sub>		40	--	ns
Address hold time		T <sub>DH80</sub>		15	--	ns
/RD access time		T <sub>ACC80</sub>	C <sub>L</sub> =100pF	--	140	ns
Output disable time	T <sub>OH80</sub>	10		100	ns	

Notes:

1. The input signal rise time and fall time (T<sub>R</sub>, T<sub>F</sub>) is specified at 15 ns or less. When the system cycle time is extremely fast, (T<sub>R</sub>+T<sub>F</sub>) ≤ (T<sub>CYC80</sub>-T<sub>CCLW</sub>-T<sub>CCHW</sub>) for (T<sub>R</sub>+T<sub>F</sub>) ≤ (T<sub>CYC80</sub>-T<sub>CCLR</sub>-T<sub>CCHR</sub>) are specified.
2. All timing is specified using 20% and 80% of V<sub>DD</sub> as the reference.
3. T<sub>CCLW</sub> and T<sub>CCLR</sub> are specified as the overlap between /CS1 being "L" (CS2="H") and /WR and /RD being at the "L" level.

**System Bus Read/Write Characteristics 2 (68-Series MPU)**

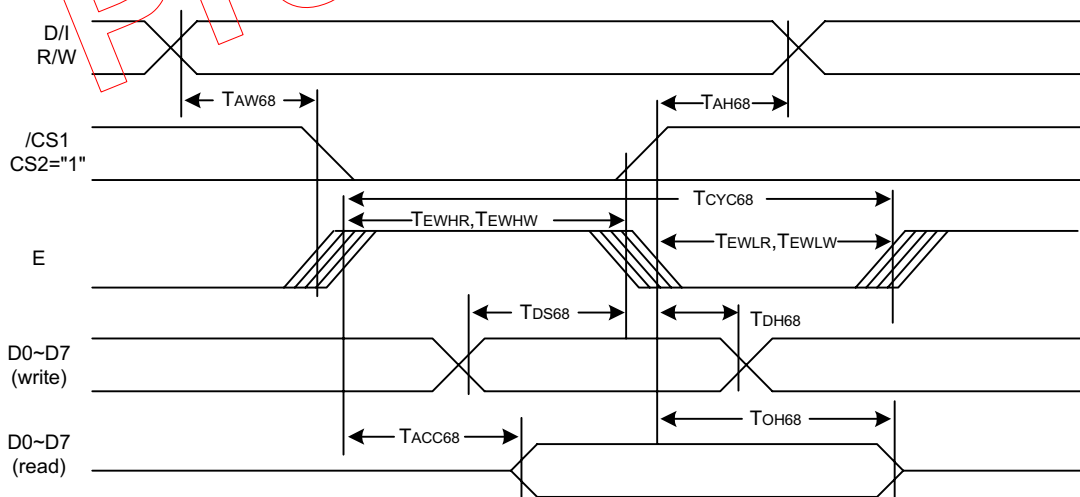


Fig. 16

Table 14 ( $V_{DD}=2.4V$  to  $3.3V, T_a=-30$  to  $85^{\circ}C$ )

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	D/I	$T_{AH68}$		0	--	ns
Address setup time		$T_{AW68}$		0	--	ns
System cycle time	D/I	$T_{CYC68}$		300	--	ns
Data setup time	D0 to D7	$T_{DS68}$		40	--	ns
Data hold time		$T_{DH68}$		15	--	ns
Access time		$T_{ACC68}$	$C_L=100pF$	--	140	ns
Output disable time		$T_{OH68}$		10	100	ns
Enable H pulse time	Read	E	$T_{EWHR}$	120	--	ns
	Write		$T_{EWHW}$	60	--	ns
Enable L pulse time	Read	E	$T_{EWLR}$	60	--	ns
	Write		$T_{EWLW}$	60	--	ns

Notes:

1. The input signal rise time and fall time ( $T_R, T_F$ ) is specified at 15 ns or less. When the system cycle time is extremely fast,  $(T_R+T_F) \leq (T_{CYC68}-T_{EWLW}-T_{EWHW})$  for  $(T_R+T_F) \leq (T_{CYC68}-T_{EWLR}-T_{EWHR})$  are specified.
2. All timing is specified using 20% and 80% of  $V_{DD}$  as the reference.
3.  $T_{EWLW}$  and  $T_{EWLR}$  are specified as the overlap between /CS1 being "L" (CS2="H") and E.

**The Serial Interface**

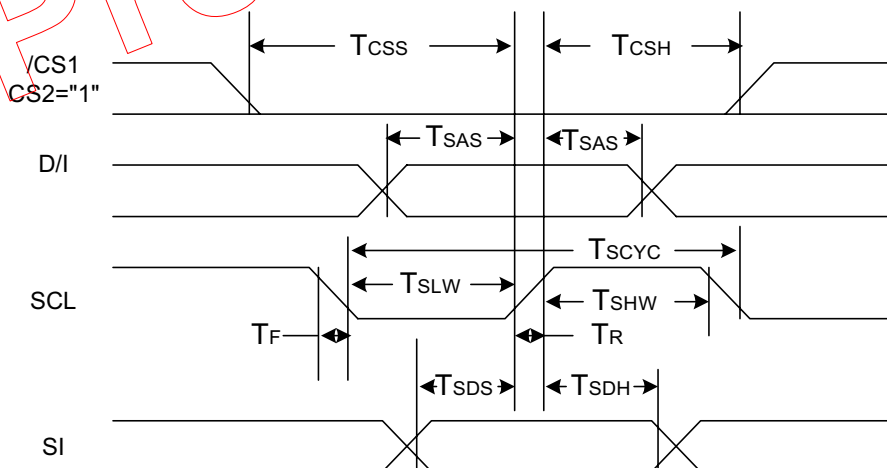


Fig. 17

Table 15 ( $V_{DD}=2.4V$  to  $3.3V$ ,  $T_a=-30$  to  $85^{\circ}C$ )

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Serial Clock Period	SCL	$T_{SCYC}$		250	--	ns
SDCLK "H" pulse width		$T_{SHW}$		100	--	ns
SDCLK "L" pulse width		$T_{SLW}$		100	--	ns
Address setup time	D/I	$T_{SAS}$		150	--	ns
Address hold time		$T_{SHA}$		150	--	ns
Data setup time	SI	$T_{SDS}$		100	--	ns
Data hold time		$T_{SDH}$		100	--	ns
CS-SDCLK time	CS	$T_{CSS}$		150	--	ns
		$T_{CSH}$		150	--	ns

1. The input signal rise and fall time ( $T_R$ ,  $T_F$ ) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of  $V_{DD}$  as the standard.

**Display Control Output Timing**

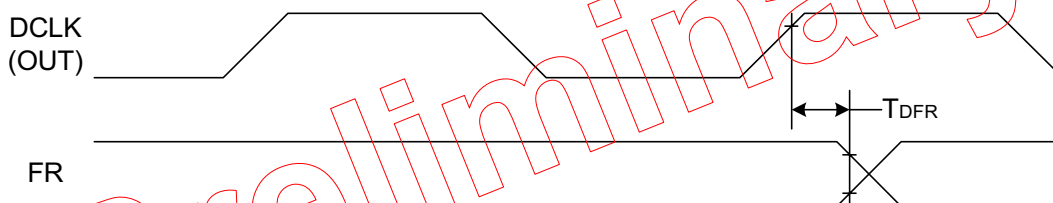


Fig. 18

Table 16 ( $V_{DD}=2.4V$  to  $3.3V$ ,  $T_a=-30$  to  $85^{\circ}C$ )

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
FR delay time	FR	$T_{DFR}$	$C_L=50pF$	--	20	80	ns

**Reset Timing**

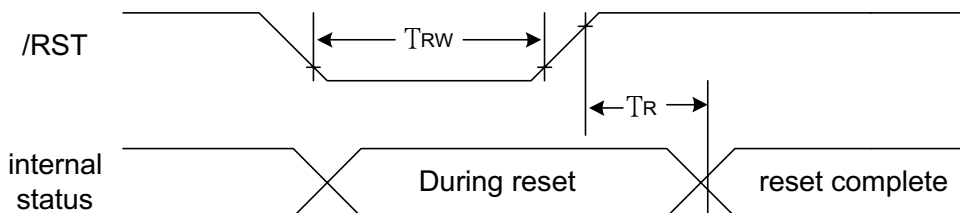


Fig. 19

Table 17 ( $V_{DD}=2.4V$  to  $3.3V$ ,  $T_a=-30$  to  $85^{\circ}C$ )

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		$T_R$		--	--	1	$\mu s$
Reset "L" pulse width	/RST	$T_{RW}$		1	--	--	$\mu s$

\*All timing is specified with 20% and 80% of  $V_{DD}$  as the standard.



**APPLICATION CIRCUIT**

**The MPU Interface (Reference example)**

The EM65565A can be connected to either 80-Series MPU or 68-Series MPU. Moreover, using the serial interface it is possible to operate the EM65565A series chips with fewer signal lines. The display area can be enlarged by use plural EM65565A Series chips. When this is done, the chip select signal can be used to select the individual ICs to access.

(1) 80-Series MPU

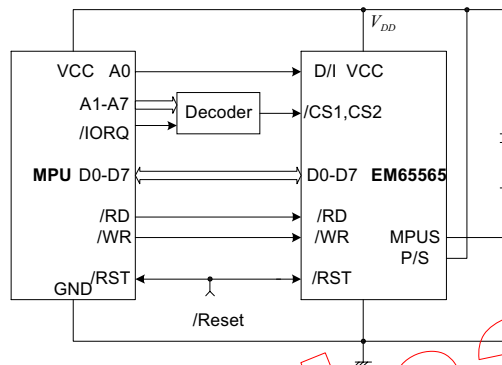


Fig. 20

(2) 68-Series MPU

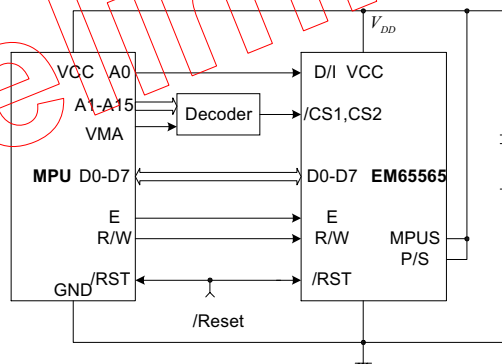


Fig. 21

(3) Using the Serial Interface

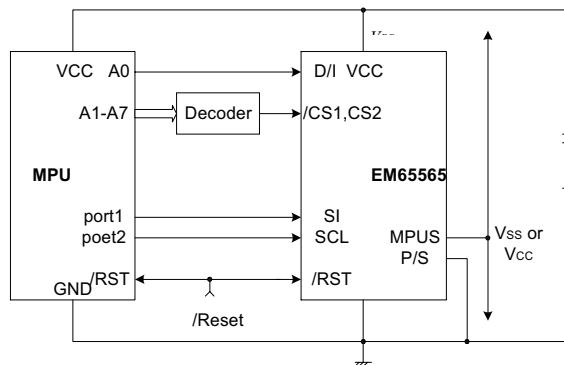
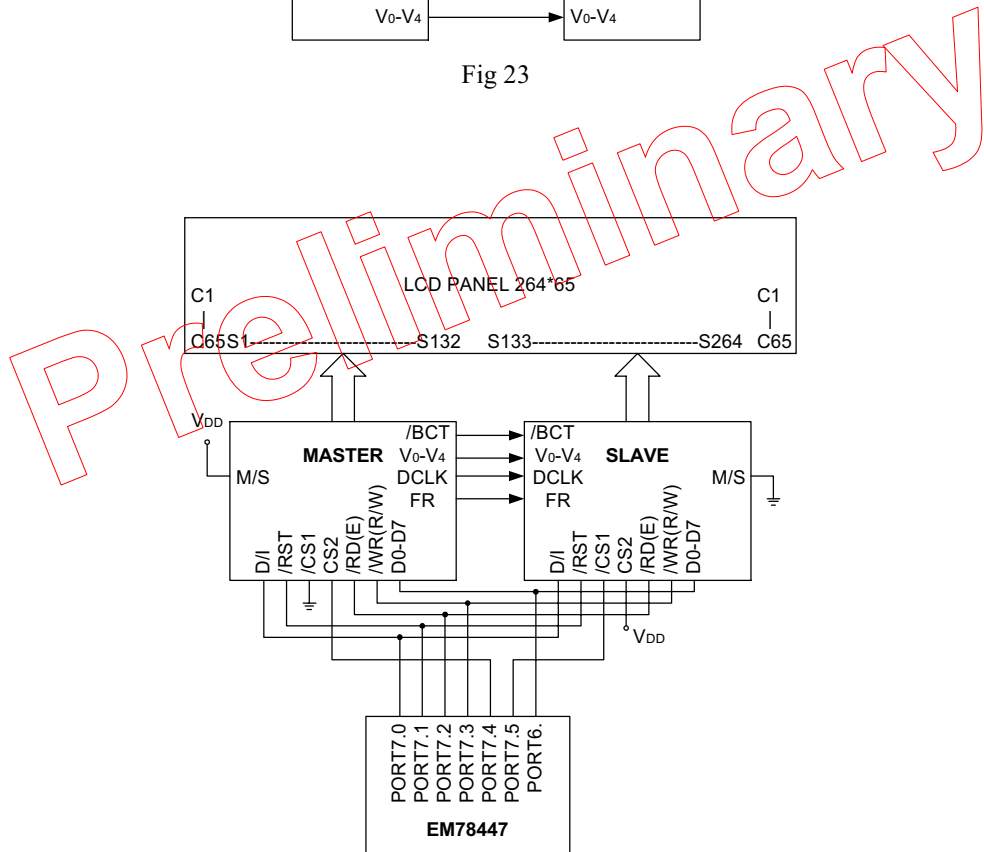
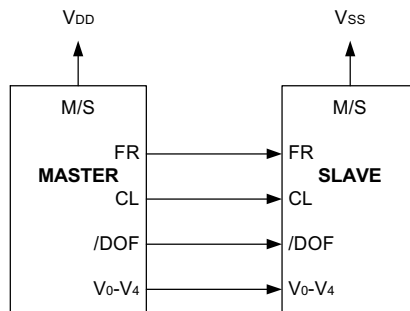


Fig. 22

**CONNECTIONS BETWEEN LCD DRIVERS (REFERENCE EXAMPLE)**

The LCD area can be enlarged with ease through the use of multiple EM65565A chips. Use a same equipment type.

EM65565A (master) → EM65565A(slave)



**RECOMMENDED COG ITO TRACES RESISTOR**

Interface	ITO Traces resistance ( $\Omega$ )
$V_0 \sim V_4$	Max = 300 $\Omega$
CAP1+, CAP1-, CAP2+, CAP2-, CAP3+, CAP4+, $V_{OUT}$	Max = 100 $\Omega$
$V_{DD}$	Max = 100 $\Omega$
$V_{SS}$	Max = 50 $\Omega$
/WR, /RD, /CS1, CS2, .., D7 ~ D0	Max = 3K $\Omega$

Preliminary