

#### **GENERAL DESCRIPTION**

The EM65160 is a 160-channel output common and segment driver LSI for driving large scale STN dot matrix LCD (liquid crystal display) panel using as PDA, computers and workstation. Since this product can be used as segment or common driver, a LCD panel can be configured only with this product. Through the use of SST (super slim TCP) technology, it is deal for substantially decreasing the size of LCD module frame.

In common driver mode, it can be selected in single mode and dual mode by a mode pin (MD), data input/output pins are bi-directional, four data shift direction are pin selectable.

In segment driver mode, it can be selected 4-bit parallel input mode or 8-bit parallel input mode by a mode pin (MD).

#### **FEATURES**

#### Both common mode and segment mode

- Display duty application: up to 1/480 duty
- Supply voltage for the logic system: +2.5 to +5.5V
- Supply voltage for LCD driver: +15 to +42V
- Number of LCD driver outputs: 160
- Low output impedance
- Low power consumption
- CMOS silicon process (P-type Silicon substrate)
- 186 pin TCP (tape carrier package) package
- Built-in display-off function: when /DSPOF is "L", all LCD drive output remain at the V<sub>SS</sub> level.

#### Common Mode

- Shift clock frequency: 4.0MHz (Max.)
- Built-in 160 bits bi-directional shift register (divisible into 80bits\*2)
- Available in a single mode or in a dual mode
- Data input/output pins are bi-directional, four data shift direction are pin selectable.
- Shift register circuit reset function when /DSPOF active

#### Segment mode

- Shift clock frequency: 14MHz(Max.) (V<sub>DD</sub>=+5V ± 10%)

#### $8MHz(Max.) (V_{DD} = +2.5V \text{ to } +4.5V)$

- Adopts a data bus system
- 4-bits/8-bits parallel input mode are selected by mode pin (MD)
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip select, causes the internal clock to be stopped by automatically counting 160 of input data
- Line latch circuit reset function when /DSPOF active



#### PIN ARRANGEMENT





**BLOCK DIAGRAM** 



Figure-2 Block Diagram



#### **PIN DESCRIPTION**

#### Table-1 Pin Arrangement

| Pin NO.       | Symbol                            | <i>I/O</i> | Description   |
|---------------|-----------------------------------|------------|---|
| 1 to 160      | $Y_1 - Y_{160}$                   | 0          | LCD driver output                                       |
| 161,186       | V <sub>OL</sub> , V <sub>OR</sub> | -          | Power supply for LCD driver                             |
| 162,185       | $V_{12L}, V_{12R}$                | -          | Power supply for LCD driver                             |
| 163,184       | $V_{43L}, V_{43R}$                | -          | Power supply for LCD driver                             |
| 165           | DIR                               | Ι          | Display data shift direction selection                  |
| 166           | $V_{DD}$                          | -          | Power supply for logic system                           |
| 167           | S/C                               | Ι          | Segment/common mode selection                           |
| 168           | EIO <sub>2</sub>                  | L/O        | Innut /tout for this sale to a data of thit societar    |
| 180           | EIO <sub>1</sub>                  | 1/0        | Input /output for chip select or data of shift register |
| $160 \pm 176$ | $\mathrm{DI}_0-\mathrm{DI}_7$     | т          | Display data input for segment mode                     |
| 109 10 170    | $DI_7$                            | 1          | Dual mode data input for common mode                    |
| 177           | XCK                               | Ι          | Display data shift clock input for segment mode         |
| 178           | /DSPOF                            | Ι          | Control input for deselect output level                 |
| 179           | LP                                | Ι          | Latch pulse input/shift clock input for shift register  |
| 181           | FR                                | Ι          | AC-converting signal input for LCD driver waveform      |
| 182           | MD                                | Ι          | Mode selection input                                    |
| 164,183       | V <sub>ss</sub>                   | -          | Ground (0 V)  |

#### Segment Mode

#### Table-2 Pin Functions Of Segment Mode

| Symbol   | <i>I/O</i> | Connected to                     | Functions  |  |  |  |  |
|--|------------|----------------------------------|--|--|--|--|--|
| V <sub>DD</sub>  | Ι          | Power Supply                     | Power supply for internal logic connects to +2.5 to +5.5V  |  |  |  |  |
| V <sub>SS</sub>  | Ι          | GND                              | Connect to Ground  |  |  |  |  |
| $\begin{array}{c} V_{0R} \ , \ V_{0L} \\ V_{12R} \ , \ V_{12L} \\ V_{43R} \ , \ V_{43L} \end{array}$ | Ι          | Power Supply                     | wer supply for LCD driver level<br>Normally , the bias voltage used is set by resistor divider<br>Ensure that the voltage are set such that $V_{ss} < V_{43} < V_{12} < V_0$<br>To further reduce the difference between the output waveforms of LCD driver output pin<br>$Y_1$ and $Y_{160}$ , externally connect $V_{iR}$ and $V_{iL}$ (i=0,12,43) |  |  |  |  |
| $DI_0 - DI_7$  | Ι          | Controller                       | Input for display data<br>• In 4-bit parallel input mode , input data into $DI_0 - DI_3$ , connect $DI_4 - DI_7$ to $V_{SS}$ or $V_{DD}$<br>• In 8-bit parallel input mode , input data into $DI_0 - DI_7$   |  |  |  |  |
| ХСК  | Ι          | Controller                       | Clock signal for taking display data<br>Data is read on the falling of the clock pulse   |  |  |  |  |
| LP   | Ι          | Controller                       | Latch signal for display data<br>• Data is latched on the falling edge of the clock pulse  |  |  |  |  |
| S/C  | Ι          | $V_{SS}/V_{DD}$                  | Selection of segment mode/common mode         S/C       Mode selection         H       Segment mode         L       Common mode  |  |  |  |  |
| DIR  | Ι          | V <sub>SS</sub> /V <sub>DD</sub> | Directional selection for reading display data $DIR$ Data read directionL $Y_{160}$ to $Y_1$ H $Y_1$ to $Y_{160}$  |  |  |  |  |



#### Segment mode (continuous)

| Symbol                              | <i>I/O</i> | Connected to                     |  | Functions   |
|-------------------------------------|------------|----------------------------------|--|---|
| /DSPOF                              | Ι          | Controller                       | <ul> <li>Control signal for output deselect level</li> <li>The input signal is level-shifted from controls LCD drive circuit</li> <li>When the signal is low , the output contents of line latch are reset , but condition of /DSPOF</li> <li>When this signal is high, the operation</li> </ul> | logic voltage level to LCD driver voltage level $\rightarrow$ and<br>$(Y_1 - Y_{160})$ of LCD drive be set to level $V_{SS}$ , the<br>read the display data in the data latch regardless of<br>on returns to the normal status. |
| FR                                  | Ι          | Controller                       | AC signal for LCD drive<br>• Input a frame inversion signal<br>• The LCD driver output voltage level   | can be set by line latch output signal and FR signal  |
| MD                                  | Ι          | V <sub>SS</sub> /V <sub>DD</sub> | Mode selection           MD         Mode           H         8-bit par           L         4-bit par   | selection<br>rallel input<br>rallel input   |
| EIO <sub>1</sub> , EIO <sub>2</sub> | Ι          |                                  | Input/output for chip selection <ul> <li>In output state , after 160-bit of data</li> <li>In input state , the chip is selected view read, the chip is deselected</li> </ul> <li>DIR EIO<sub>1</sub> <ul> <li>H Input</li> <li>L Output</li> </ul></li>  | have been read , set to "L" then set to "H"<br>when EI is set to "L", then 160-bit of data have been<br><u>EIO<sub>2</sub></u><br>Output<br>Input   |
| Y <sub>1</sub> -Y <sub>160</sub>    | 0          | LCD Panel                        | LCD driver output.<br>One of four levels is output according to  | o the combination of the FR signal and display data   |

#### **Common Mode**

#### Table-3 Pin Functions Of Common Mode

| Symbol   | <i>I/O</i> | Connected to |   |   | Functions   |  |  |  |  |
|--|------------|--------------|---|---|---|--|--|--|--|
| $V_{DD}$   | Ι          | Power supply | Power supply for internal logic connects to +2.5 to +5.5V   |   |   |  |  |  |  |
| V <sub>SS</sub>  | Ι          | GND          | Connect to Ground   | connect to Ground   |   |  |  |  |  |
| $V_{0R}, V_{0L} \\ V_{12R}, V_{12L} \\ V_{34R}, V_{34L}$ | I          | Power supply | Power supply for I<br>• Normally • the I<br>• Ensure that the v<br>• To further reduc<br>Y <sub>1</sub> and Y <sub>160</sub> ,ext | CD driver level<br>bias voltage used is so<br>voltage are set such th<br>the the difference betw<br>ernally connect V <sub>iR</sub> a   | et by resistor divider<br>hat $V_{ss} < V_{43} < V_{12}$<br>ween the output wavef<br>hd V <sub>iL</sub> (i=0,12,34) | < V <sub>0</sub><br>forms of LCD driver output pin |  |  |  |
| EIO <sub>1</sub> , EIO <sub>2</sub>                      | I          |              | Data input/output s<br>• When EIO <sub>1</sub> (EIC<br>• When EIO <sub>1</sub> (EIC<br><u>DIR</u><br>H<br>L                       | shift for bi-directiona<br>$p_2$ ) is input , it will be<br>$p_2$ ) is output , it will n<br><i>EIO</i> <sub>1</sub><br>Input<br>Output | l shift register<br>e pull-down<br>not be pull-down<br><u>EIO2</u><br>Output<br>Input                               |  |  |  |  |
| LP   | Ι          | Controller   | Shift clock for bi-d<br>• Data is shifted o   | lirectional shift regist<br>n the falling edge of   | er<br>the clock   |  |  |  |  |



#### Common Mode (Continuous)

| Symbol                           | <i>I/O</i> | Connected to                     | Functions  |
|----------------------------------|------------|----------------------------------|--|
|                                  |            |                                  | Directional selection of bi-directional shift register   |
| DIR                              | Ι          | Controller                       | $\begin{tabular}{ c c c c c } \hline DIR & Data read direction \\ \hline L & Y_{160} to Y_1 \\ \hline H & Y_1 to Y_{160} \\ \hline \end{tabular}$  |
| /DSPOF                           | Ι          | Controller                       | <ul> <li>Control signal for output deselect level</li> <li>The input signal is level-shifted from logic voltage level to LCD driver voltage level , and controls LCD drive circuit</li> <li>When the signal is low, the output (Y<sub>1</sub> - Y<sub>160</sub>) of LCD drive be set to level V<sub>SS</sub>, the contents of shift register are reset not read</li> <li>When this signal return to high, the operation returns to the normal status.</li> </ul> |
| FR                               | Ι          | Controller                       | <ul><li>AC signal for LCD drive</li><li>Input a frame inversion signal</li><li>The LCD driver output voltage level can be set by line latch output signal and FR signal</li></ul>  |
| MD                               | Ι          | $V_{ss}/V_{DD}$                  | Mode selectionMDMode selectionHDual modeLSingle mode   |
| S/C                              | Ι          | V <sub>ss</sub> /V <sub>DD</sub> | Selection of segment mode/common mode         S/C       Mode selection         H       Segment mode         L       Common mode  |
| DI <sub>7</sub>                  | Ι          | Controller                       | Dual mode data input<br>• In dual mode , data can input from 81 <sub>st</sub> bit  |
| DI <sub>0</sub> -DI <sub>6</sub> | Ι          | $V_{SS}$ or $V_{DD}$             | Not used, avoiding floating.   |
| XCK                              | Ι          | V <sub>SS</sub> or open          | Not used   |
| Y <sub>1</sub> -Y <sub>160</sub> | 0          | LCD Panel                        | LCD driver output.<br>• One of four voltage levels is output according to FR signal and the data of shift register   |

#### FUNCTIONAL DESCRIPTIONS

#### **Active Control**

In case of segment mode, controls the selection or de-selection of the chip. Following a LP signal, and after the chip select signal is input, a select signal is generated internally until 160bits of data have been read in. Once data input has been completed, a select signal for cascade connection is output, and the chip is deselected. In case of common mode, controls the input/output data of bi-directional pins.

#### SP Conversion & Data Control

In case of segment mode, keep input data which are 2 clocks of XCK at 4-bit parallel mode into latch circuit, or keep input data which are 1 clock of XCK at 8-bits parallel mode into latch circuit, after that they are put on the internal data bus 8 bits at a time.

#### **Data Latch Control**

In case of segment mode, selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic, for every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.



#### Data Latch

In case of segment mode, latches the data on the data bus. The latched state of each LCD driver output pin is controlled by the control logic and the data latch control, 160 bits of data are read in 20 sets of 8 bits.

#### Line Latch / Shift Register

In case of segment mode, all 160 bits, which have been read into the data latch block are simultaneously latched on the falling edge of the LP signal, and output to the level shifter block.

In case of common mode, shifts data from the data input pin on the falling edge of the LP signal.

#### Level Shifter

The logic voltage signal is boost to the LCD driver voltage level, and output to the driver block.

#### **4-level Driver**

Drive the LCD driver output pins from the line latch/shift register data, selecting one of 4 levels ( $V_0$ ,  $V_{12}$ ,  $V_{43}$ ,  $V_{SS}$ ) based on the S/C, FR and /DSPOF

#### **Clock control Logic**

Controls the operation of each block. In case of segment mode, when a LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block.

Once the selection signal has been output, operation of the data latch and data transmission are controlled, 160 bits of data are read in, and the chip is deselected. In case of common mode, controls the direction of data shift.

#### Relation between FR, data input and Liquid crystal display driver output voltage level, Explain as following table 4:

#### Table-4 Liquid Crystal Display Driver Output Voltage Level (Segment Mode)

(a) Segment Mode

| FR | Latch data | /DSPOF | Driver output voltage level |
|----|------------|--------|-----------------------------|
| Н  | Н          | Н      | $V_0$                       |
| Н  | L          | Н      | $V_2$                       |
| L  | Н          | Н      | V <sub>SS</sub>             |
| L  | L          | Н      | V <sub>3</sub>              |
| X  | X          | L      | V <sub>SS</sub>             |

 $V_{SS} < V_{43} < V_{12} < V_0$  H:  $V_{DD}$  L:  $V_{SS}$  X: Don't care

(b) Common Mode

| FR | Latch data | /DSPOF | Driver output voltage level |
|----|------------|--------|-----------------------------|
| Н  | Н          | Н      | $V_{SS}$                    |
| Н  | L          | Н      | V1                          |
| L  | Н          | Н      | $V_0$                       |
| L  | L          | Н      | $V_4$                       |
| Х  | Х          | L      | V <sub>SS</sub>             |

 $V_{SS} < V_{43} < V_{12} < V_0$  H:  $V_{DD}$ , L:  $V_{SS}$ , X: Don't care



#### Relationship between the display data and driver output pin

Table-5 Relationship Between The Display Data And Driver Output Pin

(a) Segment Mode (4-bit Parallel Mode)

|     |        | FIO     |                 | Data Figure of clock |                  |                  |                  |                 |                  |                  |                  |
|-----|--------|---------|-----------------|----------------------|------------------|------------------|------------------|-----------------|------------------|------------------|------------------|
| MD  | DIK    | $EIO_1$ | $EIO_2$         | Input                | $1_{st}$         | $2_{nd}$         | $3_{rd}$         |                 | 38 <sub>th</sub> | 39 <sub>th</sub> | 40 <sub>th</sub> |
|     |        |         |                 | $DI_0$               | Y <sub>157</sub> | Y <sub>153</sub> | Y <sub>149</sub> | •••             | Y <sub>9</sub>   | Y <sub>5</sub>   | Y <sub>1</sub>   |
| т   | т      | Output  | Ŧ,              | DI <sub>1</sub>      | Y <sub>158</sub> | Y <sub>154</sub> | Y <sub>150</sub> | •••             | Y <sub>10</sub>  | Y <sub>6</sub>   | Y <sub>2</sub>   |
|     | Output | Input   | DI <sub>2</sub> | Y <sub>159</sub>     | Y <sub>155</sub> | Y <sub>151</sub> | •••              | Y <sub>11</sub> | Y <sub>7</sub>   | Y <sub>3</sub>   |                  |
|     |        |         |                 | DI <sub>3</sub>      | Y <sub>160</sub> | Y <sub>156</sub> | Y <sub>152</sub> | •••             | Y <sub>12</sub>  | Y <sub>8</sub>   | Y <sub>4</sub>   |
|     |        |         |                 | $DI_0$               | $Y_4$            | Y <sub>8</sub>   | Y <sub>12</sub>  | •••             | Y <sub>152</sub> | Y <sub>156</sub> | Y <sub>160</sub> |
| L H | 11     | Turnet  | t Output        | DI <sub>1</sub>      | Y <sub>3</sub>   | Y <sub>7</sub>   | Y <sub>11</sub>  | •••             | Y <sub>151</sub> | Y <sub>155</sub> | Y <sub>159</sub> |
|     | п      | Input   |                 | DI <sub>2</sub>      | Y <sub>2</sub>   | Y <sub>6</sub>   | Y <sub>10</sub>  | •••             | Y <sub>150</sub> | Y <sub>154</sub> | Y <sub>158</sub> |
|     |        |         |                 | DI <sub>3</sub>      | Y <sub>1</sub>   | Y <sub>5</sub>   | Y <sub>9</sub>   | •••             | Y <sub>149</sub> | Y <sub>153</sub> | Y <sub>157</sub> |

#### (b) Segment Mode (8-bit Parallel Mode)

| MD |     | EIO    | FIO     | Data            |                  |                  | Fig              | ure of cl | lock             |                  |                  |
|----|-----|--------|---------|-----------------|------------------|------------------|------------------|-----------|------------------|------------------|------------------|
| MD | DIK | Output | $EIO_2$ | Input           | $1_{st}$         | $2_{nd}$         | $3_{rd}$         | •••       | 18 <sub>th</sub> | 19 <sub>th</sub> | $20_{th}$        |
|    |     |        |         | DI <sub>0</sub> | Y <sub>153</sub> | Y <sub>145</sub> | Y <sub>137</sub> | •••       | Y <sub>17</sub>  | Y <sub>9</sub>   | Y <sub>1</sub>   |
|    |     |        |         | $DI_1$          | Y <sub>154</sub> | Y <sub>146</sub> | Y <sub>138</sub> | •••       | Y <sub>18</sub>  | Y <sub>10</sub>  | Y <sub>2</sub>   |
|    |     |        |         | DI <sub>2</sub> | Y <sub>155</sub> | Y <sub>147</sub> | Y <sub>139</sub> | •••       | Y <sub>19</sub>  | Y <sub>11</sub>  | Y <sub>3</sub>   |
| 11 | т   | Output | Innut   | DI <sub>3</sub> | Y <sub>156</sub> | Y <sub>148</sub> | Y <sub>140</sub> | •••       | Y <sub>20</sub>  | Y <sub>12</sub>  | Y <sub>4</sub>   |
| п  | L   | Output | Input   | DI <sub>4</sub> | Y <sub>157</sub> | Y <sub>149</sub> | Y <sub>141</sub> | •••       | Y <sub>21</sub>  | Y <sub>13</sub>  | Y <sub>5</sub>   |
|    |     |        |         | DI <sub>5</sub> | Y <sub>158</sub> | Y <sub>150</sub> | Y <sub>142</sub> | •••       | Y <sub>22</sub>  | Y <sub>14</sub>  | Y <sub>6</sub>   |
|    |     |        |         | DI <sub>6</sub> | Y <sub>159</sub> | Y <sub>151</sub> | Y <sub>143</sub> | •••       | Y <sub>23</sub>  | Y <sub>15</sub>  | Y <sub>7</sub>   |
|    |     |        |         | DI <sub>7</sub> | Y <sub>160</sub> | Y <sub>152</sub> | Y <sub>144</sub> | •••       | Y <sub>24</sub>  | Y <sub>16</sub>  | Y <sub>8</sub>   |
|    |     |        |         | DI <sub>0</sub> | Y <sub>8</sub>   | Y <sub>16</sub>  | Y <sub>24</sub>  | •••       | Y <sub>144</sub> | Y <sub>152</sub> | Y <sub>160</sub> |
|    |     |        | Output  | $DI_1$          | Y <sub>7</sub>   | Y <sub>15</sub>  | Y <sub>23</sub>  | •••       | Y <sub>143</sub> | Y <sub>151</sub> | Y <sub>159</sub> |
|    |     |        |         | DI <sub>2</sub> | Y <sub>6</sub>   | Y <sub>14</sub>  | Y <sub>22</sub>  | •••       | Y <sub>142</sub> | Y <sub>150</sub> | Y <sub>158</sub> |
| 11 | 11  | Input  |         | DI <sub>3</sub> | Y <sub>5</sub>   | Y <sub>13</sub>  | Y <sub>21</sub>  | •••       | Y <sub>141</sub> | Y <sub>149</sub> | Y <sub>157</sub> |
| нн | п   |        |         | $DI_4$          | Y <sub>4</sub>   | Y <sub>12</sub>  | Y <sub>20</sub>  | •••       | Y <sub>140</sub> | Y <sub>148</sub> | Y <sub>156</sub> |
|    |     |        |         | DI <sub>5</sub> | Y <sub>3</sub>   | Y <sub>11</sub>  | Y <sub>19</sub>  | •••       | Y <sub>139</sub> | Y <sub>147</sub> | Y <sub>155</sub> |
|    |     |        |         | DI <sub>6</sub> | Y <sub>2</sub>   | Y <sub>10</sub>  | Y <sub>18</sub>  | •••       | Y <sub>138</sub> | Y <sub>146</sub> | Y <sub>154</sub> |
|    |     |        |         | DI <sub>7</sub> | Y <sub>1</sub>   | Y <sub>9</sub>   | Y <sub>17</sub>  |           | Y <sub>137</sub> | Y <sub>145</sub> | Y <sub>153</sub> |

#### (c) Common Mode

| MD       | DIR | Data transfer direction      | EIO <sub>1</sub> | EIO <sub>2</sub> | $DI_7$ |
|----------|-----|------------------------------|------------------|------------------|--------|
| L        | Н   | $Y_1 \rightarrow Y_{160}$    | Input            | Output           | X      |
| (Single) | L   | $Y_{160} \rightarrow Y_1$    | Output           | Input            | X      |
|          | II  | $Y_1 \rightarrow Y_{80}$     | Tamat            | Outrout          | Turnet |
| Н        | П   | $Y_{81} \rightarrow Y_{160}$ | Input            | Output           | Input  |
| (Dual)   | т   | $Y_{160} \rightarrow Y_{81}$ | Outrust          | Transit          | Innet  |
|          | L   | $Y_{80} \rightarrow Y_1$     | Output           | Input            | Input  |

 $H{:}V_{DD},\,L{:}V_{SS}\,, \textbf{X: Don't} \quad \textbf{care}$ 



#### Connection example of plural segment driver

Case of DIR = "L"



*Figure-3. Connection Example Of Plural Segment Driver (DIR="L")* 

Case of DIR = "H"



Figure-4. Connection Example Of Plural Segment Driver (DIR="H")

#### Timing chart of 4-Device cascade Connection of Segment Drivers







#### Connection of plural common driver of single mode

Single mode case of DIR="L"



Figure-6. Connection Of Plural Common Driver Of Single Mode (DIR="L")

Single mode case of DIR="H"



Figure-7. Connection Of Plural Common Driver Of Single Mode (DIR="H")

#### Connection of plural common driver of dual mode

Dual mode case of DIR="L"



Figure-8. Connection Of Plural Common Driver Of Dual Mode (DIR="L")



#### Dual mode case of DIR="H"



Figure-9. Connection Of Plural Common Driver Of Dual Mode (DIR="H")

#### Power Supply Circuit for LCD drive

#### **Resistive dividing**

Driving bias voltage is generally generated by a resistive divider.(Figure 17)

#### Precaution when connecting or disconnecting the power.

This LSI has a high voltage LCD driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LCD driver power supply while the logic system power supply is floating.

We recommend you connecting the serial resistor (50~100 $\Omega$ ) or fuse to the LCD drive power V<sub>0</sub> of the system as a current limiter. And set up the suitable value of the resistor in consideration of LCD display grade.

When connecting or disconnecting the power supply, show the following recommend sequence.



Figure-10. Sequence For Connecting Or Disconnecting The Power Supply



#### **Drive by Operation Amplifier**

In graphic display, the size of the LCD becomes larger and the display duty ratio becomes smaller, so the stability of LCD drive voltage level is more important than in small display system.

Since the LCD for graphic display is large and has many picture elements, the load capacitance becomes large. The high impedance of the power supply for LCD drive produces distortion in the drive waveforms, and degrades display quality. For this reason, the LCD drive voltage level impedance should be reduced with operational amplifier. (Figure 17)

#### **Range of Operating Voltage: V0**

It is necessary to set the voltage for V0 within the VDD operating voltage range shown in the diagram below.



Figure-11 Operating Voltage Range (VDD-VO)

#### Absolute Maximum ratings

Table-6 Absolute Maximum Ratings

| Parameter           | Symbol           | Conditions               | Applicable pins  | Ratings                            | Unit |
|---------------------|------------------|--------------------------|--|------------------------------------|------|
| Supply voltage (1)  | V <sub>DD</sub>  |                          | V <sub>DD</sub>  | -0.3 to +7.0                       | V    |
|                     | $V_0$            | T 25°0                   | $V_{0L}, V_{0R}$   | -0.3 to +45.0                      | V    |
| Supply voltage (2)  | V <sub>12</sub>  | $I_a=25$ (               | V <sub>12L</sub> , V <sub>12R</sub>  | -0.3 to $V_0$ +0.3                 | V    |
|                     | V <sub>43</sub>  | Referenced to $V_{}(0V)$ | $V_{43L}$ , $V_{43R}$  | -0.3 to $V_0$ +0.3                 | V    |
| Input voltage       | VI               | V SS (0 V )              | DI <sub>0-7</sub> , XCK, LP, DIR, FR, MD, S/C, EIO <sub>1</sub> ,<br>EIO <sub>2</sub> , /DSPOF | -0.3 to $V_{\text{DD}}\text{+}0.3$ | V    |
| Storage temperature | T <sub>stg</sub> |                          |  | -45 to +125                        | °C   |



#### **Recommended Operation Conditions**

Table-7 Recommended Operation Conditions

| Parameter             | Symbol           | Conditions    | Applicable pins                   | Min. | Туре | Max. | Unit |
|-----------------------|------------------|---------------|-----------------------------------|------|------|------|------|
| Supply voltage (1)    | $V_{DD}$         | Referenced to | V <sub>DD</sub>                   | +2.5 |      | +5.5 | V    |
| Supply voltage (2)    | $V_0$            | $V_{SS}(0V)$  | V <sub>0L</sub> , V <sub>0R</sub> | +15  |      | +42  | V    |
| Operating temperature | T <sub>opr</sub> |               |                                   | -20  |      | +85  | °C   |

Note: Ensure that voltages are set such that  $V_{ss} < V_{43} < V_{12} < V_0$ 

#### **DC** Characteristics

#### Segment Mode

#### Table-8 DC Characteristics Of Segment Mode

|   |                  | (                                     | $(V_{SS} == 0V, V_{DD} = +2.5 \text{ to } +5.5V, V_0 = +15 \text{ to } +42V, T_a = -20 \approx +85^{\circ}C)$ |                      |      |             |      |  |
|---|------------------|---------------------------------------|---|----------------------|------|-------------|------|--|
| Parameter                                 | Symbol           | Conditions                            | Applicable pins   | Min.                 | Тур. | Max.        | Unit |  |
| Input voltago                             | $V_{IH}$         |                                       | DI <sub>0</sub> -DI <sub>7</sub> , XCK, LP, DIR, FR, MD,  | $0.8V_{DD}$          |      |             | V    |  |
| Input voltage                             | V <sub>IL</sub>  |                                       | S/C, EIO <sub>1</sub> , EIO <sub>2</sub> , /DSPOF   |                      |      | $0.2V_{DD}$ | V    |  |
| Output Voltage                            | V <sub>OH</sub>  | I <sub>OH</sub> =-0.4mA               | FIO FIO   | V <sub>DD</sub> -0.4 |      |             | V    |  |
|   | V <sub>OL</sub>  | $I_{OL}$ =+0.4mA                      | $EIO_1, EIO_2$  |                      |      | +0.4        | V    |  |
| Input leakage                             | $I_{LIH}$        | V <sub>I</sub> =V <sub>DD</sub>       | DI <sub>0</sub> -DI <sub>7</sub> , XCK, LP, DIR, FR, MD,  |                      |      | +10         | μΑ   |  |
| current                                   | $I_{LIL}$        | V <sub>I</sub> =V <sub>SS</sub>       | S/C, EIO <sub>1</sub> , EIO <sub>2</sub> , /DSPOF   |                      |      | -10         | μΑ   |  |
|   | R <sub>ON</sub>  | V <sub>0</sub> =+40V                  |   |                      | 0.7  | 1.0         |      |  |
| Output resistance                         |                  | $ \Delta V_{ON}  = 0.5 V V_0 = +30 V$ | Y <sub>1</sub> - Y <sub>160</sub>   |                      | 1.0  | 1.5         | kΩ   |  |
|   |                  | V <sub>0</sub> =+20V                  |   |                      | 1.5  | 2.0         |      |  |
| Stand-by current                          | I <sub>STB</sub> | *1                                    | V <sub>SS</sub>   |                      |      | 50.0        | μΑ   |  |
| Consumed current                          | т                | *2                                    | V   |                      |      | 2.0         | mA   |  |
| (Deselection)                             | I <sub>DD1</sub> | - 2                                   | V DD  |                      |      | 2.0         | IIIA |  |
| Consumed current                          | I                | *3                                    | V   |                      |      | 8.0         | mΔ   |  |
| (Selection) <sup>1</sup> DD2 <sup>5</sup> |                  | 5                                     | * DD  |                      |      | 0.0         | шA   |  |
| Consumed current                          | I <sub>0</sub>   | *4                                    | $V_0$   |                      |      | 1.0         | mA   |  |

Note:

1.  $V_{DD}$ =+5.0V,  $V_0$ =+42.0V,  $V_I$ = $V_{SS}$ 

2.  $V_{DD}$ =+5.0V,  $V_0$ =+42.0V,  $V_I$ = $V_{SS}$ ,  $f_{XCK}$ =14MHz, No-load, EI= $V_{DD}$ 

3.  $V_{DD}$ =+5.0V,  $V_0$ =+42.0V,  $V_I$ = $V_{SS}$ ,  $f_{XCK}$ =14MHz, No-load, EI= $V_{SS}$ 

4.  $V_{DD}$ =+5.0V,  $V_0$ =+42.0V,  $V_I$ = $V_{SS}$ ,  $f_{XCK}$ =14MHz,  $f_{FR}$ =80Hz, No-load, EI= $V_{SS}$ 

(The input data is turned over by data taking clock (4-bit parallel input mode)



#### Common mode

| $(V_{SS} = 0V, V_{DD} = +2.5 \text{ to } 5.5V, V_0 = +15 \text{ to } +42V, Ta = -20 \approx 85^{\circ}\text{C})$ |  |  |                      |  |                      |      |             |           |
|--|--|--|----------------------|--|----------------------|------|-------------|-----------|
| Parameter  | Symbol   | Conditions                               |                      | Applicable pins  | Min.                 | Тур. | Max.        | Unit      |
| Investore litera   | V <sub>IH</sub>  |  |                      | DI <sub>0</sub> -DI <sub>7</sub> , XCK, LP, DIR, FR, MD, | $0.8V_{DD}$          |      |             | V         |
| input voltage  | V <sub>IL</sub>  |  |                      | S/C, EIO <sub>1</sub> , EIO <sub>2</sub> , /DSPOF        |                      |      | $0.2V_{DD}$ | V         |
| Output welte as  | V <sub>OH</sub>  | $I_{OH} = -0.4$                          | 4mA                  |  | V <sub>DD</sub> -0.4 |      |             | V         |
| Output voltage   | V <sub>OL</sub>  | $I_{OL} = +0.4$                          | 4mA                  | $EIO_1, EIO_2$   |                      |      | +0.4        | V         |
| Input leakage current  | I <sub>LIH</sub>   | V <sub>I</sub> =V <sub>I</sub>           | DD                   | DI <sub>0</sub> -DI <sub>7</sub> , XCK, LP, DIR, FR, MD, |                      |      | +10         | μΑ        |
|  | I <sub>LIL</sub>   | V <sub>I</sub> =V <sub>2</sub>           | SS                   | S/C, EIO <sub>1</sub> , EIO <sub>2</sub> , /DSPOF        |                      |      | -10         | μΑ        |
|  |  |  | V <sub>0</sub> =+40V |  |                      | 0.7  | 1.0         |           |
| Output resistance  | $\mathbf{R}_{\mathrm{ON}} \mid \Delta \mathbf{V}_{\mathrm{O}}$ | $\left  \Delta V_{ON} \right  {=} 0.5 V$ | V <sub>0</sub> =+30V | Y <sub>1</sub> - Y <sub>160</sub>                        |                      | 1.0  | 1.5         | $k\Omega$ |
|  |  |  | V <sub>0</sub> =+20V |  |                      | 1.5  | 2.0         |           |
| Input pull-down current  | $I_{PD}$   | V <sub>I</sub> =V <sub>DD</sub>          |                      | XCK, $EIO_1$ , $EIO_2$                                   |                      |      | 100.0       | μΑ        |
| Stand-by current   | I <sub>STB</sub>   | *1                                       |                      | V <sub>SS</sub>  |                      |      | 50.0        | μΑ        |
| Consumed current (1)   | I <sub>DD</sub>  | *2                                       |                      | V <sub>DD</sub>  |                      |      | 80.0        | μĀ        |
| Consumed current (2)   | I <sub>0</sub>   | *2                                       |                      | $V_0$  |                      |      | 160.0       | μA        |

Table-9 DC Characteristics Of Common Mode

NOTE:

1.  $V_{DD} = +5V$ ,  $V_0 = +42V$ ,  $V_I = V_{SS}$ 

2.  $V_{DD}$  = +5V,  $V_0$  = +42V,  $f_{LP}$  = 41.6kHz,  $f_{FR}$  = 80Hz, case of 1/480 duty operation, No-load

#### AC Electrical characteristic

#### Segment mode 1

#### Table-10 AC Electrical Characteristics Of Segment Mode 1

|   | $(V_{SS} = 0V, V_{DD} = +4.5 \text{ to } +5.5V, V_0 = +15 \text{ to } +42V, T_a = -20 \sim 85^{\circ}C)$ |                      |      |      |      |      |
|---|--|----------------------|------|------|------|------|
| Parameter                                 | Symbol   | Condition            | Min. | Туре | Max. | Unit |
| Shift clock period *1                     | T <sub>WCK</sub>   | $T_R, T_F \leq 10ns$ | 71   |      |      | ns   |
| Shift clock "H" pulse width               | Т <sub>WCKH</sub>  |                      | 23   |      |      | ns   |
| Shift clock "L" pulse width               | T <sub>WCKL</sub>  |                      | 23   |      |      | ns   |
| Data setup time                           | T <sub>DS</sub>  |                      | 10   |      |      | ns   |
| Data hold time                            | T <sub>DH</sub>  |                      | 20   |      |      | ns   |
| Latch pulse "H" pulse width               | T <sub>WLPH</sub>  |                      | 23   |      |      | ns   |
| Shift clock rise to latch pulse rise time | T <sub>LD</sub>  |                      | 0    |      |      | ns   |
| Shift clock fall to latch pulse fall time | T <sub>SL</sub>  |                      | 25   |      |      | ns   |
| Latch pulse rise to shift clock rise time | T <sub>LS</sub>  |                      | 25   |      |      | ns   |
| Latch pulse fall to shift clock fall time | T <sub>LH</sub>  |                      | 25   |      |      | ns   |
| Input signal rise time *2                 | T <sub>R</sub>   |                      |      |      | 50   | ns   |
| Input signal fall time *2                 | T <sub>F</sub>   |                      |      |      | 50   | ns   |
| Enable setup time                         | Ts   |                      | 21   |      |      | ns   |
| /DSPOF removal time                       | T <sub>SD</sub>  |                      | 100  |      |      | ns   |
| /DSPOF "L" pulse time                     | T <sub>WDL</sub>   |                      | 1.2  |      |      | μs   |
| Output delay time (1)                     | T <sub>D</sub>   | C <sub>L</sub> =15pF |      |      | 40   | ns   |
| Output delay time (2)                     | T <sub>PD1</sub> , T <sub>PD2</sub>  | C <sub>L</sub> =15pF |      |      | 1.2  | μs   |
| Output delay time (3)                     | T <sub>PD3</sub>   | C <sub>L</sub> =15pF |      |      | 1.2  | μs   |

#### NOTES:

1. Take the cascade connection into consideration.

2.  $(T_{WCK} - T_{WCKH} - T_{WCKL}) / 2$  is maximum in the case of high-speed operation.



#### Segment mode 2

Table-11 AC Electrical Characteristics Of Segment Mode 2

 $(V_{SS} = 0V, V_{DD} = +2.5 \text{ to } +4.5V, V_0 = +15 \text{ to } +42V, T_a = -20 \sim 85^{\circ}\text{C})$ 

| Parameter                                 | Symbol             | Condition            | Min. | Туре | Max. | Unit |
|---|--------------------|----------------------|------|------|------|------|
| Shift clock period *1                     | T <sub>WCK</sub>   | $T_R, T_F \leq 10ns$ | 125  |      |      | ns   |
| Shift clock "H" pulse width               | Т <sub>WCKH</sub>  |                      | 51   |      |      | ns   |
| Shift clock "L" pulse width               | T <sub>WCKL</sub>  |                      | 51   |      |      | ns   |
| Data setup time                           | T <sub>DS</sub>    |                      | 30   |      |      | ns   |
| Data hold time                            | T <sub>DH</sub>    |                      | 40   |      |      | ns   |
| Latch pulse "H" pulse width               | T <sub>WLPH</sub>  |                      | 51   |      |      | ns   |
| Shift clock rise to latch pulse rise time | T <sub>LD</sub>    |                      | 0    |      |      | ns   |
| Shift clock fall to latch pulse fall time | T <sub>SL</sub>    |                      | 51   |      |      | ns   |
| Latch pulse rise to shift clock rise time | T <sub>LS</sub>    |                      | 51   |      |      | ns   |
| Latch pulse fall to shift clock fall time | T <sub>LH</sub>    |                      | 51   |      |      | ns   |
| Input signal rise time *2                 | T <sub>R</sub>     |                      |      |      | 50   | ns   |
| Input signal fall time *2                 | T <sub>F</sub>     |                      |      |      | 50   | ns   |
| Enable setup time                         | Ts                 |                      | 36   |      |      | ns   |
| /DSPOF removal time                       | T <sub>SD</sub>    |                      | 100  |      |      | ns   |
| /DSPOF "L" pulse time                     | T <sub>WDL</sub>   |                      | 1.2  |      |      | μs   |
| Output delay time (1)                     | T <sub>D</sub>     | C <sub>L</sub> =15pF |      |      | 78   | ns   |
| Output delay time (2)                     | $T_{PD1}, T_{PD2}$ | C <sub>L</sub> =15pF |      |      | 1.2  | μs   |
| Output delay time (3)                     | T <sub>PD3</sub>   | C <sub>L</sub> =15pF |      |      | 1.2  | μs   |

NOTES:

1. Take the cascade connection into consideration.

2.  $(T_{WCK} - T_{WCKH} - T_{WCKL}) / 2$  is maximum in the case of high-speed operation.

#### Common mode

|                               | $(V_{SS}$          | = 0V, V <sub>DD</sub> $= +2.5$ to $-$ | +5.5V, V <sub>0</sub> | = +15  to  +2 | $2V, T_a = -2$ | 20~85°C) |
|-------------------------------|--------------------|---------------------------------------|-----------------------|---------------|----------------|----------|
| Parameter                     | Symbol             | Condition                             | Min.                  | Туре          | Max.           | Unit     |
| Shift clock period            | T <sub>WLP</sub>   | $T_R, T_F \leq 20ns$                  | 250                   |               |                | ns       |
| Shift aloale "II" pulsa width | т                  | V <sub>DD</sub> =+5.0V±10%            | 15                    |               |                | ns       |
| Shift clock H pulse width     | I WLPH             | V <sub>DD</sub> =+2.5V~+4.5V          | 30                    |               |                | ns       |
| Data setup time               | T <sub>SU</sub>    |                                       | 30                    |               |                | ns       |
| Data hold time                | T <sub>H</sub>     |                                       | 30                    |               |                | ns       |
| Input signal rise time        | T <sub>R</sub>     |                                       |                       |               | 50             | ns       |
| Input signal fall time        | T <sub>F</sub>     |                                       |                       |               | 50             | ns       |
| /DSPOF removal time           | T <sub>SD</sub>    |                                       | 100                   |               |                | ns       |
| /DSPOF "L" pulse time         | T <sub>WDL</sub>   |                                       | 1.2                   |               |                | μs       |
| Output delay time (1)         | T <sub>DL</sub>    | C <sub>L</sub> =15pF                  |                       |               | 200            | ns       |
| Output delay time (2)         | $T_{PD1}, T_{PD2}$ | C <sub>L</sub> =15pF                  |                       |               | 1.2            | μs       |
| Output delay time (3)         | T <sub>PD3</sub>   | C <sub>L</sub> =15pF                  |                       |               | 1.2            | μs       |



#### **Timing diagram**

#### Timing characteristics of segment mode



Figure-12 Timing Characteristics Of Segment Mode (1)











#### Timing characteristics of common mode



Figure-15 Timing Characteristics Of Common Mode (1)



DIR="L"

Figure-16. Timing Characteristics Of Common Mode (2)



### **Application circuit**



Figure-17. Application Circuit Of 640\*480 LCD Panel



| ¢1.40<br>¢1.00<br>ont ma<br>3/1  | 0(Cu)<br>00(SR)   |   |   |  |  |   |             |
|--|---|---|---|--|--|---|-------------|
|  | -0.600±<br>0.100±0.(  | 0.02<br>)2<br>r   |   | P0.060<br>80.034<br>4.056<br>0.026             | Bump)<br>0.039(Bump<br>Scale 10/1                      | 30  |             |
|  | 4/1   |   |   |  |  |   | 0.018 typ.  |
|  |   | Lipe<br>Lipe<br>Lipe<br>Lipe<br>Lipe<br>Lipe  | r Dibalio<br>Jac<br>Callas<br>Inter<br>Deceler      |  | Laper 10<br>Laper 11<br>Laper 13<br>Super 13           | Baid <mark>, Jam</mark><br>Bib. Jao<br>Carle Jao<br>Carle Jao       |             |
| De Materia<br>Tape Mati<br>El Size<br>e<br>Resist<br>Resist Tola<br>IFER IS R<br>CET HOLE<br>ctor >2 5 | arial<br>arial<br>arance, ±(<br>0,200mm<br>S (48W) 1<br>for all p | Mate<br>Polyeste<br>405mm<br>UPILEX-<br>#7100<br>FQ-VLP<br>Sn<br>AR-710<br>0.200mm<br>5<br>FQR 1TAPE<br>attern. | rial Desc<br>er(PET)<br>de(PI)<br>-S<br>DD<br>ESITE | 75±6 1<br>12±3 1<br>18±5 1<br>0.21±0<br>26 ±14 | um (<br>um 1)<br>um 7<br>um 1)<br>0.05 um 1)<br>4 um 7 | Dalnichi<br>JBE<br>Gald<br>JBE<br>Toray<br>Mitsul<br>MUS<br>Ajinomo | Kosei<br>to |
|  |   | Drawing   | Modifica  | tion   |  |   | Date        |
| .ea (EST)  | _PAU WIT  | n GNUA&   | vo pad  |  | by Je  | uny. (3)  | /8/01'      |
|  |   |   |   |  |  |   |             |
|  |   |   |   |  |  |   |             |
| ierwise  | Identifier  | d. Seniced.   | olor Technol  | ir III.  | Scale  | Proj  | •           |
| mm<br>ice  |   |   |   |  |  | +   | _           |
| ±0.05<br>±1  | EM65  | 5160 Out  | line Dro  | iwing  | Ma   | PI  |             |
| Checked  | REVIEW  | REVIEW  | REVIEW  | Approved                                       | Drawing  | No  | Rev         |
|  |   |   |   |  | Sheet 1 Df 1   | Size  | 1<br>       |
|  |   | 1   | I   |  | www.ch.or.i  | 1 3.26  |             |



