

Fast Switching Thyristor

 \mathbf{V}_{DRM}

I_{T(RMS)}

I_{TSM} dV/dt

dl/dt

tq

Replaces March 1998 version, DS4274-2.2

DS4274-3.0 January 2000

KEY PARAMETERS

1400V

700A

9000A

300V/μs

500A/μs **20**μs

APPLICATIONS

- High Power Inverters And Choppers
- **■** UPS
- Railway Traction
- Induction Heating
- AC Motor Drives
- Cycloconverters

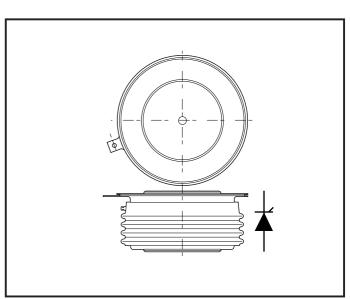
FEATURES

- Double Side Cooling
- High Surge Capability
- High Voltage

VOLTAGE RATINGS

Type Number	Repetitive Peak Voltages V _{DRM} V _{RRM}	Conditions
TF666 14A	1400	$V_{RSM} = V_{RRM} + 100V$
TF666 12A	1200	
TF666 10A	1000	$I_{DRM} = I_{RRM} = 35 \text{mA}$
TF666 08A	800	DIW KKW
TF666 06A	600	at V _{RRM} or V _{DRM} & T _{vj}

Lower voltage grades available.



Outline type code: MU171.
See Package Details for further information.

CURRENT RATINGS

Symbol	Parameter	Conditions	Max.	Units
I _{T(AV)}	Mean on-state current	Half sinewave, 50Hz, T _{case} = 80°C	446	Α
I _{T(RMS)}	RMS value	Half sinewave, 50Hz, T _{case} = 80°C	700	А

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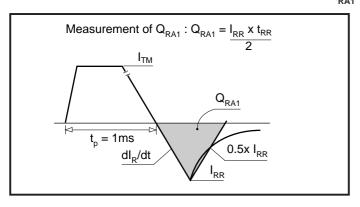
SURGE RATINGS

Symbol	Parameter	Conditions	Max.	Units
I _{TSM}	Surge (non-repetitive) on-state current	10ms half sine; $V_R = 0\% V_{RRM}$, $T_j = 125$ °C	9.0	kA
l ² t	I ² t for fusing	10ms half sine; $V_R = 0\% V_{RRM}$, $T_j = 125$ °C	405.0 x 10 ³	A ² s

THERMAL AND MECHANICAL DATA

Symbol	Parameter	Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	dc	-	0.05	°C/W
		Single side cooled	Anode dc	-	0.095	°C/W
			Cathode dc	-	0.11	°C/W
R _{th(c-h)}	Thermal resistance - case to heatsink	Clamping force 10.0kN with mounting compound	Double side	-	0.01	°C/W
			Single side	-	0.02	°C/W
T _{vj}	Virtual junction temperature	On-state (conducting)	On-state (conducting)		125	°C
		Reverse (blocking)		-	125	°C
T _{stg}	Storage temperature range			-40	150	°C
-	Clamping force			9.5	10.5	kN

MEASUREMENT OF RECOVERED CHARGE - \mathbf{Q}_{RA1}



DYNAMIC CHARACTERISTICS

Symbol	Parameter	Conditions		Min.	Max.	Units
V _{TM}	Maximum on-state voltage	At 1500A peak, T _{case} = 25°C		-	2.1	V
I _{RRM} /I _{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM} , $T_{case} = 125^{\circ}C$		-	35	mA
dV/dt	Maximum linear rate of rise of off-state voltage	Linear to 60% V_{DRM} $T_j = 125$ °C,	Gate open circuit	-	300	V/µs
dI/dt	Data of vice of an etate ourself	Gate source 20V, 20Ω	Repetitive 50Hz	-	500	A/μs
di/dt	Rate of rise of on-state current	t _r ≤ 0.5μs, T _j = 125°C	Non-repetitive	-	800	A/μs
V _{T(TO)}	Threshold voltage	At T _{vj} = 125°C		-	1.24	V
r _T	On-state slope resistance	At T _{vj} = 125°C		-	0.57	mΩ
t _{gd}	Delay time	$T_{j} = 25^{\circ}C, I_{T} = 50A,$ $V_{D} = 300V, I_{G} = 1A,$ $dI/dt = 50A/\mu s, dI_{G}/dt = 1A/\mu s$		-	1.5*	μs
t _{(ON)TOT}	Total turn-on time			-	3*	μs
I _H	Holding current	$T_{j} = 25^{\circ}C, I_{TM} = 1A, V_{D} = 12V$		-	80*	mA
IL	Latching current	$T_j = 25^{\circ}\text{C}, I_G = 0.5\text{A}, V_D = 12\text{V}$		-	500*	mA
t _q	Turn-off time	$T_j = 125^{\circ}\text{C}$, $I_T = 250\text{A}$, $V_R = 50\text{V}$ dV/dt = 20V/ μ s (Linear to 60% dI _R /dt = 50A/ μ s, Gate open circ	V_{DRM}), $ q $	-	20	μs

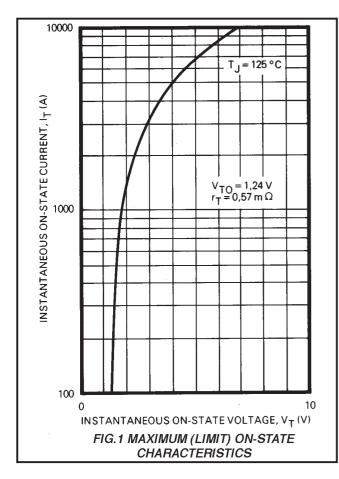
^{*}Typical value.

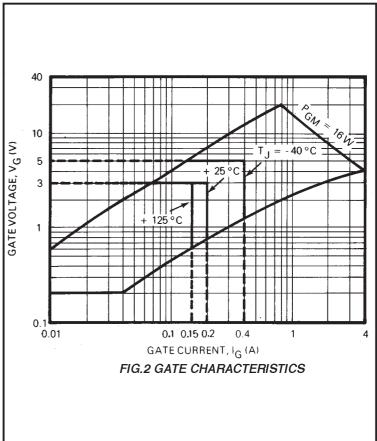
GATE TRIGGER CHARACTERISTICS AND RATINGS

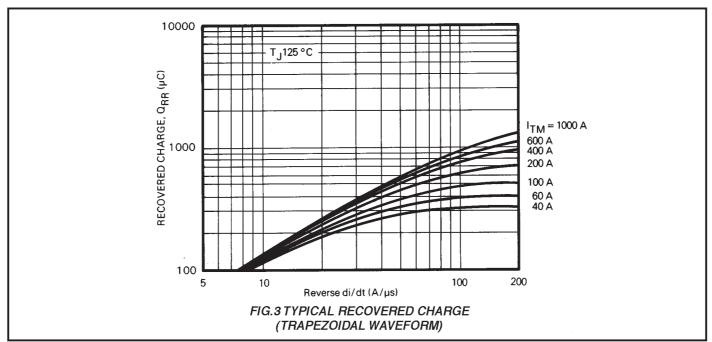
Symbol	Parameter	Conditions	Тур.	Max.	Units
V_{GT}	Gate trigger voltage	$V_{DRM} = 12V, T_{case} = 25^{\circ}C, R_{L} = 6\Omega$	-	3.0	V
I _{GT}	Gate trigger current	$V_{DRM} = 12V, T_{case} = 25^{\circ}C, R_{L} = 6\Omega$	-	200	mA
V _{GD}	Gate non-trigger voltage	At $V_{DRM} T_{case} = 125^{\circ}C$, $R_{L} = 1k\Omega$	-	0.2	V
V _{RGM}	Peak reverse gate voltage		-	5.0	V
I _{FGM}	Peak forward gate current	Anode positive with respect to cathode	-	4	А
P _{GM}	Peak gate power		-	16	W
P _{G(AV)}	Mean gate power		-	3	W

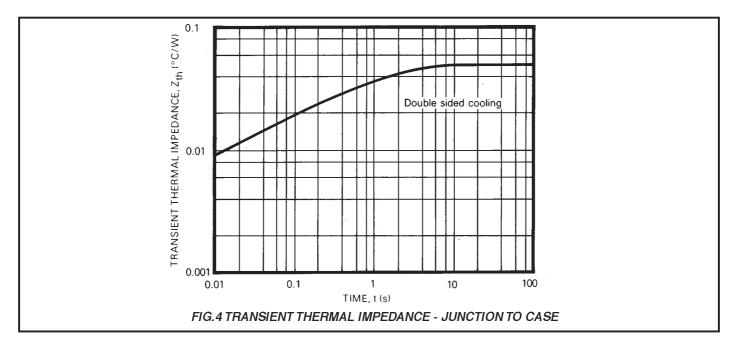
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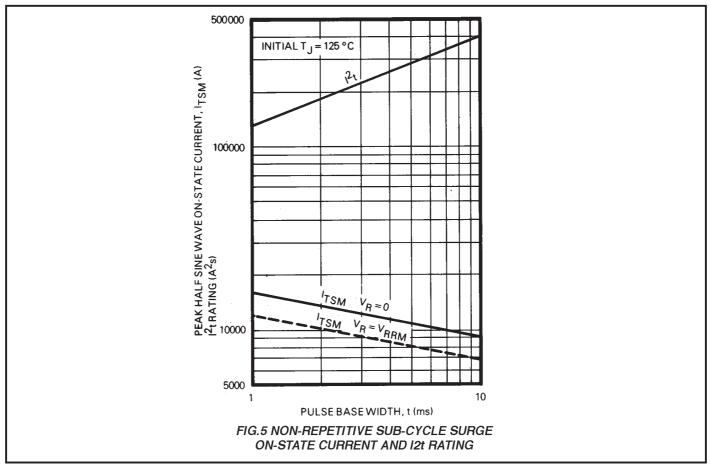
CURVES

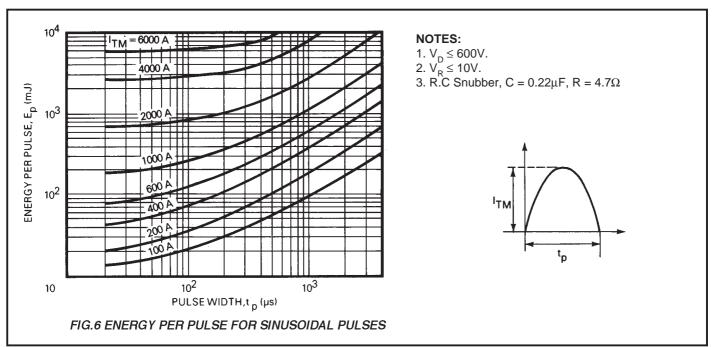


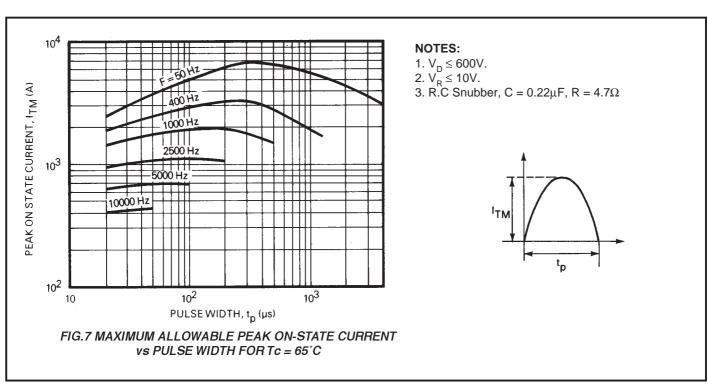


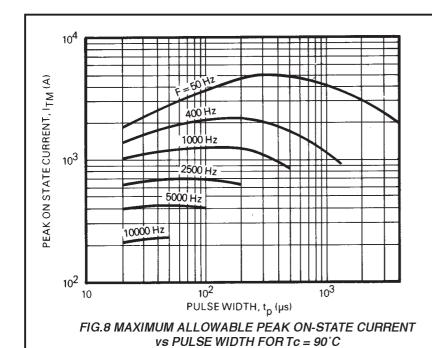






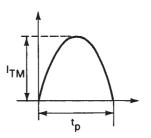


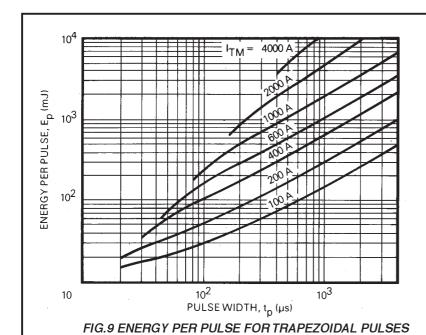




NOTES:

- 1. $V_D \le 600V$. 2. $V_R \le 10V$. 3. R.C Snubber, $C = 0.22\mu F$, $R = 4.7\Omega$

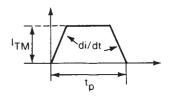




NOTES:

- 1. $dI/dt = 25A/\mu s$

- 2. $V_D \le 600V$. 3. $V_R \le 10V$. 4. R.C Snubber, $C = 0.22\mu F$, $R = 4.7\Omega$



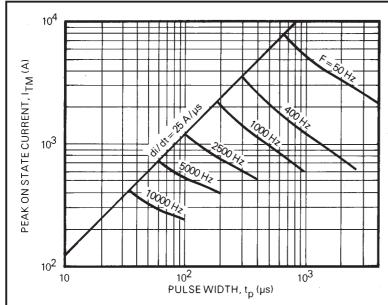
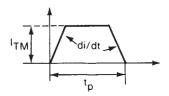


FIG. 10 MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT vs PULSE WIDTH FOR Tc = 65°C

NOTES:

- 1. $dI/dt = 25A/\mu s$

- 2. $V_D \le 600V$. 3. $V_R \le 10V$. 4. R.C Snubber, $C = 0.22\mu F$, $R = 4.7\Omega$



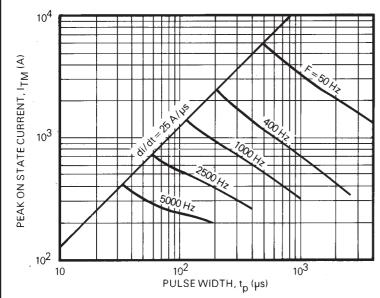
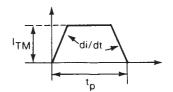


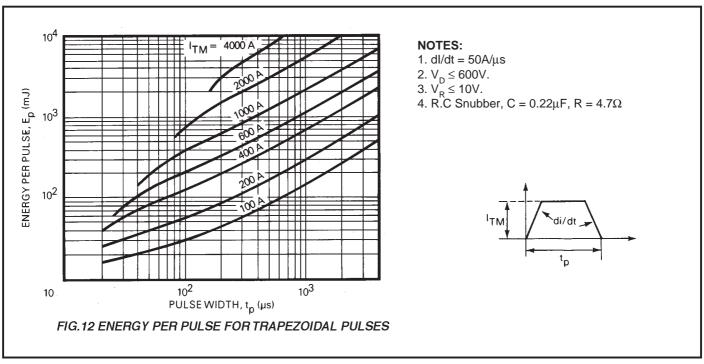
FIG.11 MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT vs PULSE WIDTH FOR Tc = 90°C

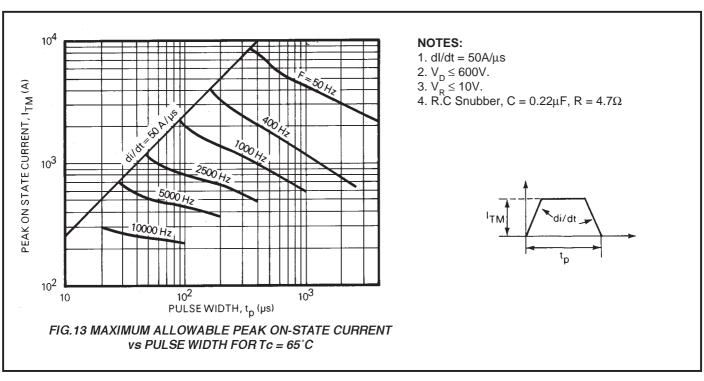
NOTES:

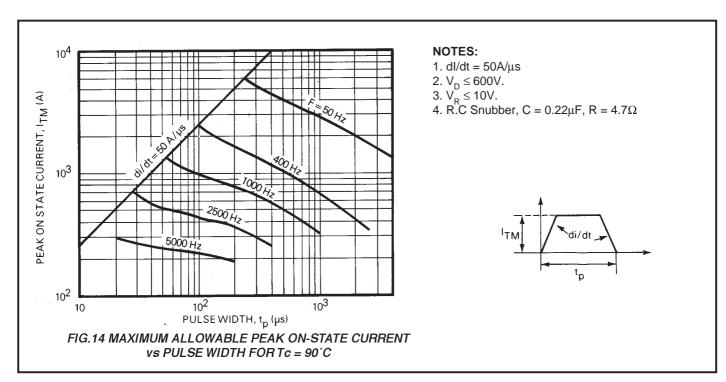
- 1. $dI/dt = 25A/\mu s$

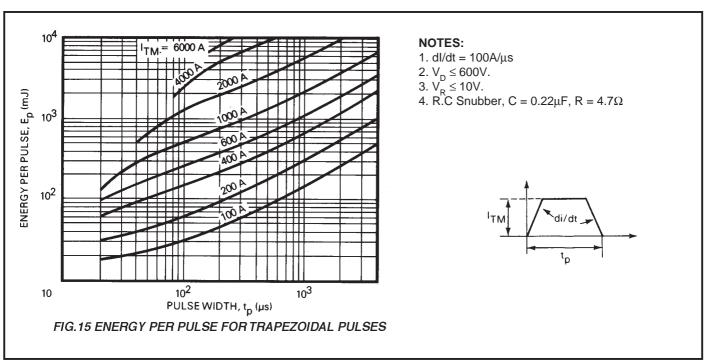
- 1. Givet = 257 vpc 2. $V_D \le 600V$. 3. $V_R \le 10V$. 4. R.C Snubber, $C = 0.22\mu F$, $R = 4.7\Omega$

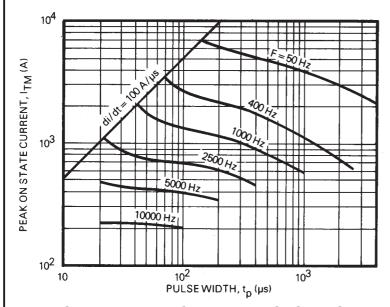












NOTES:

- 1. $dI/dt = 100A/\mu s$

- 2. $V_D \le 600V$. 3. $V_R \le 10V$. 4. R.C Snubber, $C = 0.22\mu F$, $R = 4.7\Omega$

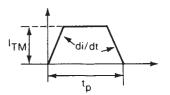
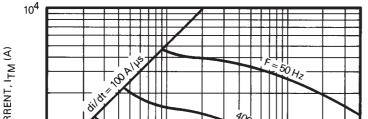


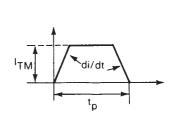
FIG.16 MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT vs PULSE WIDTH FOR Tc = 65°C



NOTES:

- 1. $dI/dt = 100A/\mu s$

- 2. $V_D \le 600V$. 3. $V_R \le 10V$. 4. R.C Snubber, $C = 0.22\mu F$, $R = 4.7\Omega$



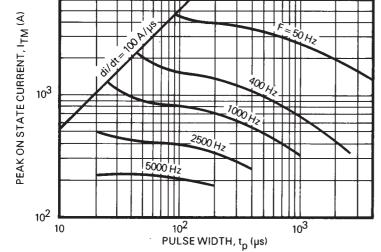
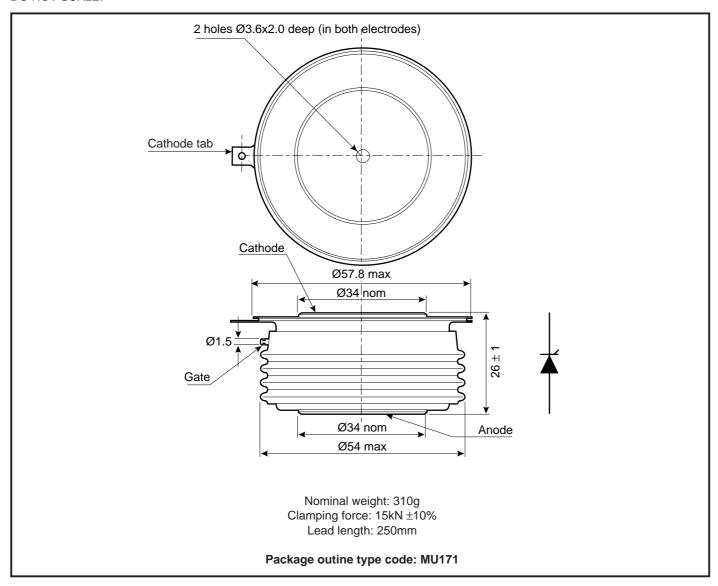


FIG.17 MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT vs PULSE WIDTH FOR Tc = 90°C

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PACKAGE DETAILS

For further package information, please contact your local Customer Service Centre. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



ASSOCIATED PUBLICATIONS

Title	Application Note	
	Number	
Calculating the junction temperature or power semiconductors	AN4506	
Gate triggering and the use of gate characteristics	AN4840	
Recommendations for clamping power semiconductors	AN4839	
The effect of temperature on thyristor performance	AN4870	
Thyristor and diode measurement with a multi-meter	AN4853	
Turn-on performance of thyristors in parallel	AN4999	
Use of V _{TO} , r _T on-state characteristic	AN5001	

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink / clamping systems in line with advances in device types and the voltage and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group continues to offer high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the up to date CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete solution (PACs).

DEVICE CLAMPS

Disc devices require the correct clamping force to ensure their safe operation. The PACs range offers a varied selection of preloaded clamps to suit all of our manufactured devices. This include cube clamps for single side cooling of 'T' 22mm

Clamps are available for single or double side cooling, with high insulation versions for high voltage assemblies.

Please refer to our application note on device clamping, AN4839

HEATSINKS

Power Assembly has it's own proprietary range of extruded aluminium heatsinks. They have been designed to optimise the performance or our semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest Sales Representative or the factory.



http://www.dynexsemi.com

e-mail: power_solutions@dynexsemi.com

HEADQUARTERS OPERATIONS DYNEX SEMICONDUCTOR LTD

Doddington Road, Lincoln. Lincolnshire. LN6 3LF. United Kingdom. Tel: 00-44-(0)1522-500500 Fax: 00-44-(0)1522-500550

DYNEX POWER INC.

Unit 7 - 58 Antares Drive, Nepean, Ontario, Canada K2E 7W6. Tel: 613.723.7035 Fax: 613.723.1518

Toll Free: 1.888.33.DYNEX (39639)

CUSTOMER SERVICE CENTRES

France, Benelux, Italy and Spain Tel: +33 (0)1 69 18 90 00. Fax: +33 (0)1 64 46 54 50

North America Tel: 011-800-5554-5554. Fax: 011-800-5444-5444

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Target Information: This is the most tentative form of information and represents a very preliminary specification. No actual design work on the product has been started.

Preliminary Information: The product is in design and development. The datasheet represents the product as it is understood but details may change.

Advance Information: The product design is complete and final characterisation for volume production is well in hand.

No Annotation: The product parameters are fixed and the product is available to datasheet specification

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