DENSE-PAC
M I C R O S Y S T E M S

256 Megabit Synchronous DRAM
## DPSD16ME16TKY5

ADVANCED INFORMATION

DESCRIPTION:

The PL-Stack series is a family of interchangeable memory modules. The 256 Megabit SDRAM is a member of this family which utilizes the new and innovative space saving TSOP stacking technology. The modules are constructed with 8 Meg x 16 SDRAMs.
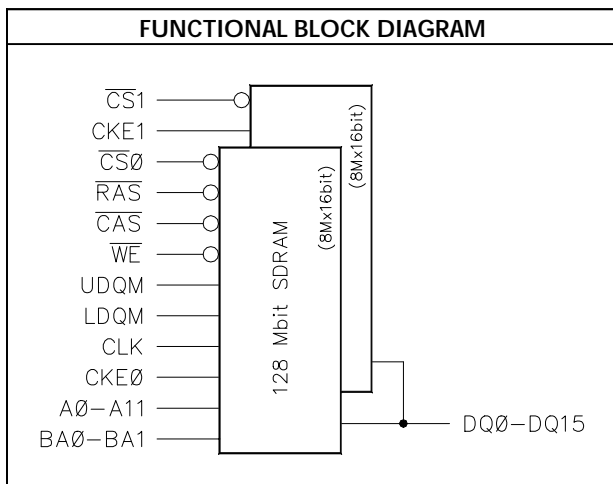
This 128 Megabit based PL-Stack module, the DPSD16ME16TKY5 has been designed to fit in the same footprint as the 8 Meg x 16 SDRAM TSOP monolithic and 128 Megabit SDRAM based family of PL-Stack modules. This allows the memory board designer to upgrade the memory in their products without redesigning the memory board, thus saving time and money.

FEATURES:
- Configuration Available:
    16 Meg x 16 bit
    (with two Chip Selects & two Clock Enables)
- Clock Frequency:
    66, 83, 100, 125, 133MHz (max.)[2]
- PC100 and PC133 Compatable
- 3.3V Supply
- LVTTL Compatible I/O
- Four Bank Operation
- Programmable Burst Type, Burst Length, and CAS Latency
- 4096 Cycles / 64 ms
- Auto and Self Refresh
- Package: TSOP Leadless Stack with Transposer
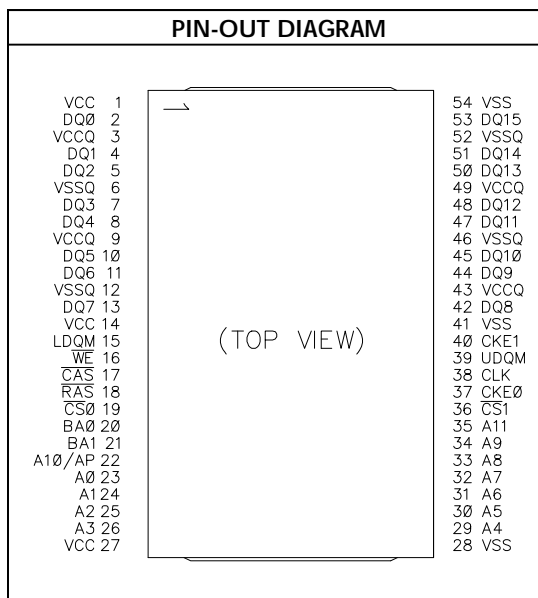
NOTES: [1] Available in Military and Industrial Temperature Ranges Only.
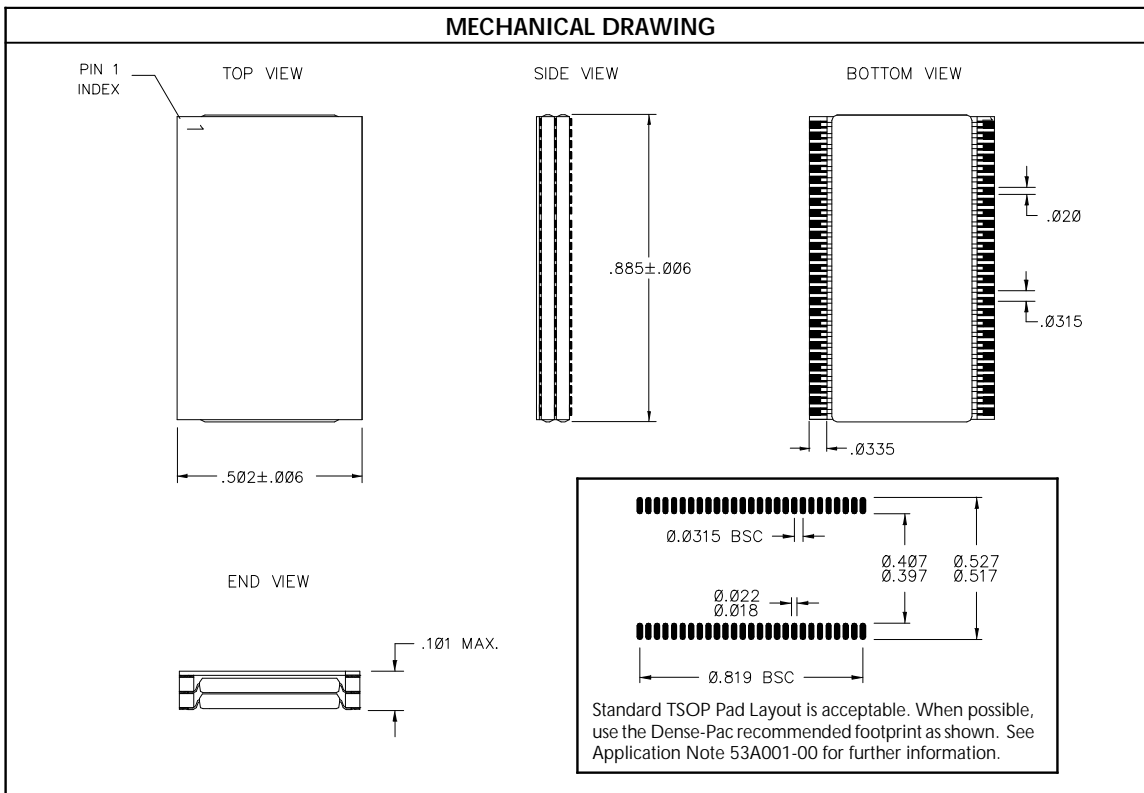   [2] Available in Commercial Temperature Range Only.

PIN-OUT DIAGRAM

VCC 1	54 VSS
DQØ 2	53 DQ15
VCCQ 3	52 VSSQ
DQ1 4	51 DQ14
DQ2 5	5Ø DQ13
VSSQ 6	49 VCCQ
DQ3 7	48 DQ12
DQ4 8	47 DQ11
VCCQ 9	46 VSSQ
DQ5 1Ø	45 DQ1Ø
DQ6 11	44 DQ9
VSSQ 12	43 VCCQ
DQ7 13	42 DQ8
VCC 14	41 VSS
LDQM 15	4Ø CKE1
$\overline{WE}$ 16	39 UDQM
$\overline{CAS}$ 17	38 CLK
$\overline{RAS}$ 18	37 CKEØ
$\overline{CS}$Ø 19	36 $\overline{CS}$1
BAØ 2Ø	35 A11
BA1 21	34 A9
A1Ø/AP 22	33 A8
AØ 23	32 A7
A1 24	31 A6
A2 25	3Ø A5
A3 26	29 A4
VCC 27	28 VSS

(TOP VIEW)

FUNCTIONAL BLOCK DIAGRAM

PIN NAMES

A0 - A11	Row Address: A0 - A11 Column Address: A0 - A7
BA0, BA1	Bank Select Address
DQ0 - DQ15	Data In / Data Out
$\overline{CAS}$	Column Address Strobes
$\overline{RAS}$	Row Address Enables
$\overline{WE}$	Data Write Enable
UDQM, LDQM	Upper & Lower Data Input/Output Mask
CKE0, CKE1	Clock Enables
CLK	System Clock
$\overline{CS}$0-$\overline{CS}$1	Chip Selects
V_{CC}/V_{SS}	Power Supply/Ground
V_{CCQ}/V_{SSQ}	Data Output Power/Ground

ADVANCED INFORMATION

PART NUMBER DESCRIPTION

DP SD 16M E 16 T KY5 — DP — XX XX X X

PREFIX TYPE MEMORY DESIG MEMORY DESIG PACKAGE SUPPLIER MEMORY SPEED CL GRADE
              DEPTH   WIDTH

Blank   Commercial Temperature
I   Industrial Temperature
M   Military Temperature

2   CAS LATENCY 2

15 [2]   15ns (66MHz) [2]
12 [2]   12ns (83MHz) [2]
10 [2]   10ns (100MHz) [2]
08 [2]   8ns (125MHz) [2]
75 [2]   7.5ns (133MHz) [2]
P1   PC100

MANUFACTURER CODE [3]
SUPPLIER CODE [3]
STACKABLE TSOP WITH TRANSPOSER
128 MEGABIT LVTTL BASED
DUAL CLOCK ENABLES
SYNCHRONOUS DRAM

NOTES: [1] Available in Military and Industrial Temperature Ranges Only.
       [2] Available in Commercial Temperature Range Only.
       [3] Contact your sales representative for supplier and manufacturer codes.

MECHANICAL DRAWING

PIN 1
INDEX

TOP VIEW   SIDE VIEW   BOTTOM VIEW

.885±.006

.502±.006

END VIEW

.101 MAX.

.020

.0315

.0335

Ø.0315 BSC

Ø.022
Ø.018

Ø.407   Ø.527
Ø.397   Ø.517

Ø.819 BSC

Standard TSOP Pad Layout is acceptable. When possible, use the Dense-Pac recommended footprint as shown. See Application Note 53A001-00 for further information.