

## 1 Gigabit Synchronous DRAM DPSD128MX8XKY5

## **DESCRIPTION:**

The Memory Stack<sup>M</sup> series is a family of interchangeable memory modules. The 1 Gigabit SDRAM is a member of this family which utilizes the space saving LP-Stack<sup>M</sup> TSOP stacking technology. The modules are constructed with two 64 Meg x 8 SDRAMs.

This 1 Gigabit LP-Stack<sup>™</sup> module, DPSD128MX8XKY5, has been designed to fit the same footprint as the 64 Meg x 8 SDRAM TSOP monolithics and 512 Megabit based family of LP-Stack.<sup>™</sup> modules. This allows system upgrade without electrical or mechanical redesign, providing an immediate and low cost memory solution.

## FEATURES:

- Configuration: 128 Meg x 8 bit (2 Banks x 16M x 4 Bit x 8 Banks)
- JEDEC Approved Footprint and Pinout
- · IPC-A-610 Manufacturing Standards
- Assemble per DPAC Application Note 53A001-00
- Package: 54-Pin LP-Stack™

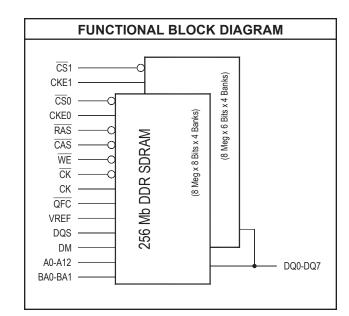
The Following Features are not affected by LP Stack<sup>™</sup> and are provided as reference only. Refer to memory OEM Device specification for details:

- Clock Frequency is determined by OEM memory device used.
- 3.3 Volt DQ Supply
- LVTTL Compatible I/O
- Four Bank Operation
- Programmable Burst Type, Burst Length, and CAS Latency

**PIN NAMES** 

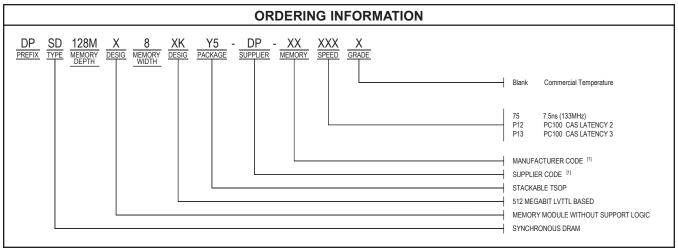
- Refresh: 8192 Cycles / 64ms
- · Refresh Types: Auto and Self

PINOUT DIAGRAM		
VCC 1 DQ0 2 VCCQ 3 N.C. 4 DQ1 5 VSSQ 6 N.C. 7 DQ2 8 VCCQ 9 N.C. 10 DQ3 111 VSSQ 12 N.C. 13 VCC 14 CS1 15 WE 16 CAS 17 RAS 18 CS0 19 BA1 21 A10 22 A0 23 A1 24 A2 25 A3 26 VCC 27	54 VSS   53 DQ7   52 VSSQ   51 N.C.   50 DQ6   49 VCCQ   48 N.C.   47 DQ5   46 VSSQ   45 N.C.   44 DQ4   43 VCCQ   42 N.C.   41 VSS   40 N.C.   39 DQM   38 CLK   37 CKE   36 A11   34 A9   33 A8   32 A7   31 A6   30 A5   29 A4   28 VSS	

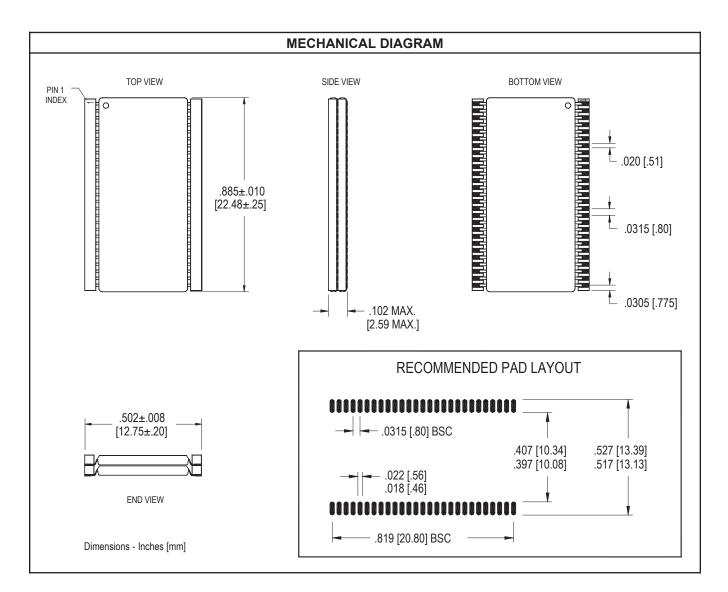


A0-A12	Row Address:	RA0-RA12
	Column Address:	CA0-CA9, A11, A12
BA0, BA1	Bank Select Address	
DQ0-DQ7	Data In/Data Out	
CAS	Column Address Strobe	
RAS	Row Address Strobe	
WE	Data Write Enable	
DQM	Data Input/Output Mask	
CKE	Clock Enables	
CLK	System Clock	
$\overline{CS}0 - \overline{CS}1$	Chip Selects	
VDD/VSS	Power Supply/Ground	
VDDQ/VSSQ	Data Output Power/Ground	
N.C.	No Connect	

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DPAC Technologies Products & Services for the Integration Age 7321 Lincoln Way, Garden Grove, CA 92841 **Tel** 714 898 0007 **Fax** 714 897 1772 www.dpactech.com Nasdaq: DPAC

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