## 1 Megabit CMOS EEPROM

DPE32X32XJ3

#### ADVANCED INFORMATION

#### **DESCRIPTION:**

The DPE32X32XJ3 is a high-performance Electrically Erasable and Programmable Read Only Memory (EEPROM) module and may be organized as 32K x 32, 64K X 16 or 128K x 8.

The module is built with four low-power CMOS 32K x 8 EEPROMs. The four chip enables are used for individual BWDW\* selection. The DPE32X32XJ3 is ideally suited for those computer systems having 16-bit or 32-bit architectures.

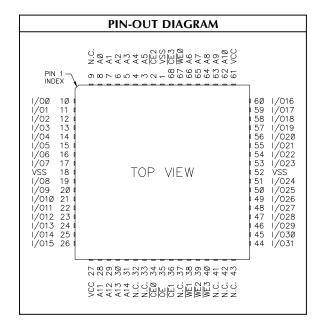
The DPE32X32XJ3 contains a 64-BWDW page register to allow writing of up to 64 BWDWs simultaneously. During a write cycle, the address and 1 to 64 BWDWs of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the module will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA Polling of the most significant data bit in each byte. Once the end of a write cycle has been detected, a new access for a read or write can begin.

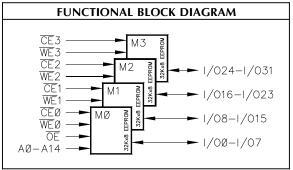
#### **FEATURES:**

- Fast Access Times:
   55, 70, 90, 120, 150, 200, 250ns
- Automatic Page Write Operation Internal Address and Data Latches Internal Control Timer
- Fast Write Cycle Times
   Page Write Cycle Time: 10ms maximum
   1 to 128 BWDW\* Page Write Operation
- DATA Polling for END of Write Detection
- High Reliability CMOS Technology Endurance: 10<sup>4</sup> Cycles Data Retention: 10 years
- Single +5V Power Supply, ±10% Tolerance
- CMOS and TTL Compatible Inputs and Outputs
- 68-Pin "J" Leaded Surface Mount Module

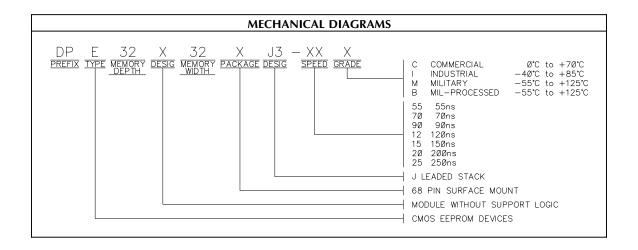
<sup>\*</sup> Byte, Word or Double Word (BWDW)

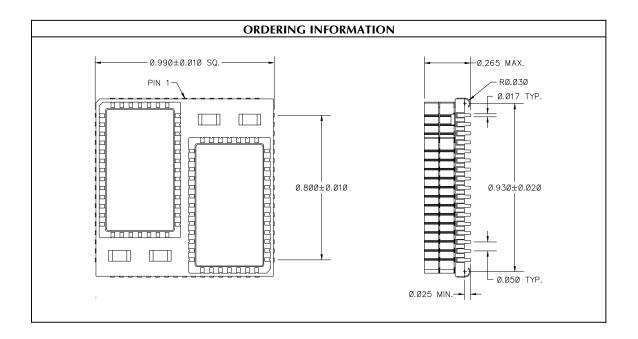
PIN NAMES	
A0 - A14	Address Inputs
I/O0 - I/O31	Data In/Out
CE0 - CE3	Chip Enables
WE0 - WE3	Write Enables
ŌĒ	Output Enable
$V_{DD}$	Power (+5V)
Vss	Ground
N.C.	No Connect





### ADVANCED INFORMATION





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