ADVANCED COMPONENTS PACKAGING

256 Megabit CMOS DDR SDRAM

DPDD16MX16TSBY5

ADVANCED INFORMATION

DESCRIPTION:

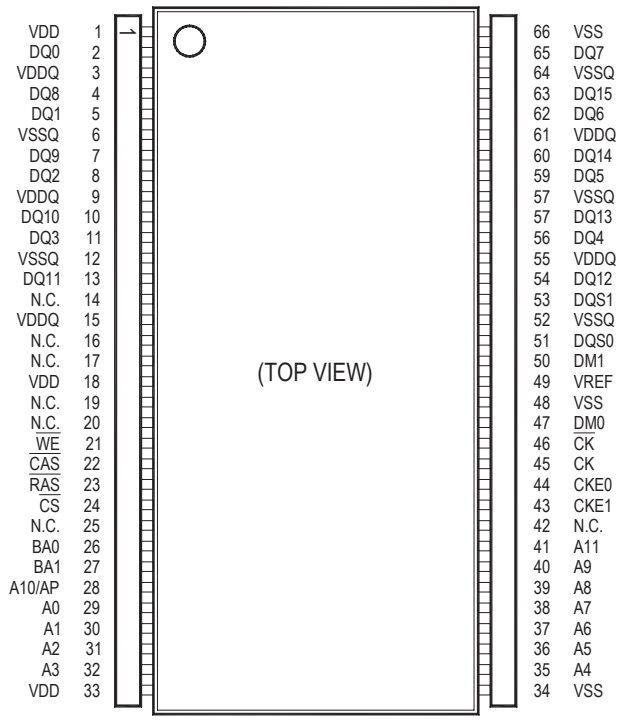
The LP-Stack™ series is a family of interchangeable memory devices. The 256 Megabit Double Data Rate Synchronous DRAM is a member of this family which utilizes the new and innovative space saving TSOP stacking technology. The devices are constructed with two 16 Meg x 8 DDR SDRAM's.

This 256 Megabit based LP-Stack™ module DPDD16MX16TSBY5, based on 128 Megabit devices, has been designed to fit in the same footprint as the 16 Meg x 8 DDR SDRAM TSOP monolithic and 512 Megabit SDRAM based family of LP-Stack™. This allows for system upgrade without electrical or mechanical redesign. Providing an immediate and low cost memory solution.

FEATURES:

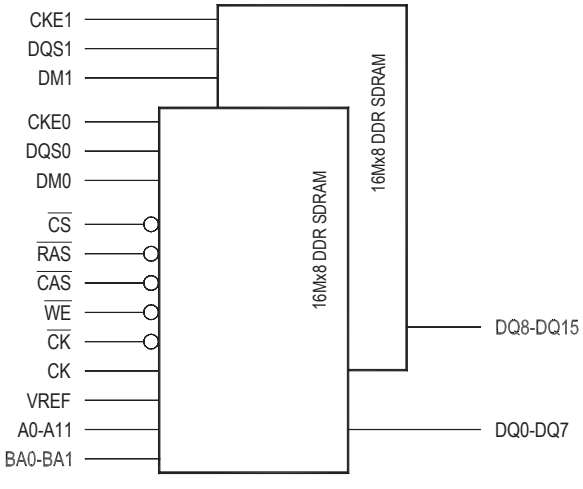
- Configuration Available:
  16 Meg x 16 bit (2 Banks of 4 Meg x 8 bits x 4)
- Clock Frequency: 100, 125, 133, 143 MHz
- 2.5 Volt DQ Supply
- JEDEC Standard SSTL_2 Interface for all Inputs/Outputs
- Four Bank Operation
- Programmable Burst Type:
  Burst Length and Read Latency
- Refresh: 4096 Cycles/64ms
- Refresh Types: Auto and Self
- JEDEC Approved Footprint and Pinout
- Package: 66-Pin Leadless TSOP Stack

PIN-OUT DIAGRAM



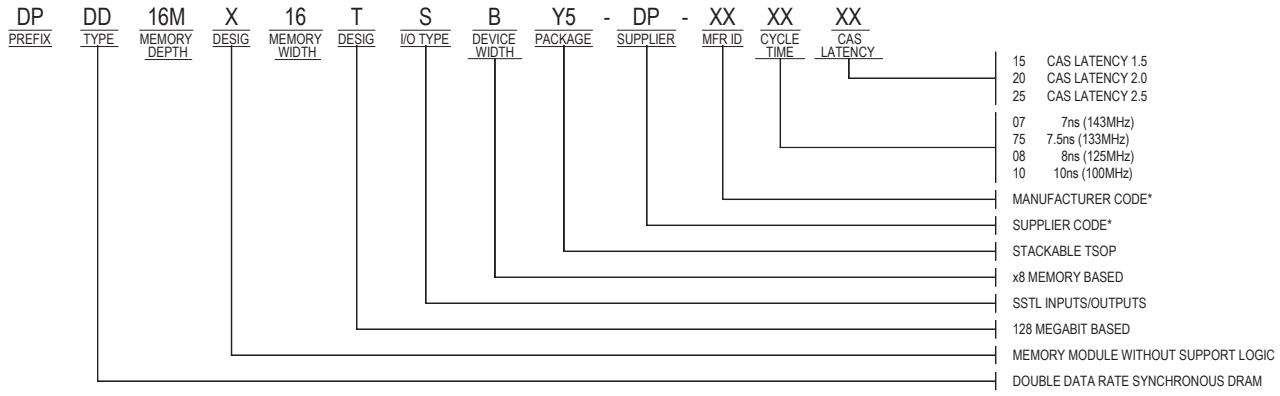
PIN NAMES	
A0-A11	Row Address: A0-A11 Column Address: A0-A9
BA0,BA1	Bank Select Address
A10/AP	Auto Precharge
DQ0-DQ15	Data In/Data Out
$\overline{CAS}$	Column Address Strobes
$\overline{CS}$	Chip Selects
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Data Write Enables
CK, $\overline{CK}$	Differential Clock Inputs
CKE0, CKE1	Clock Enables
DQS0, DQS1	Data Strode
DM0, DM1	Data Mask
V_{DD}	Power Supply (+2.5V)
Vss	Ground
V_{DDQ}	DQ Power Supply (+2.5V)
V_{SSQ}	DQ Ground
V_{REF}	Reference Voltage for inputs
N.C.	No Connect
NU	Not Used

FUNCTIONAL BLOCK DIAGRAM



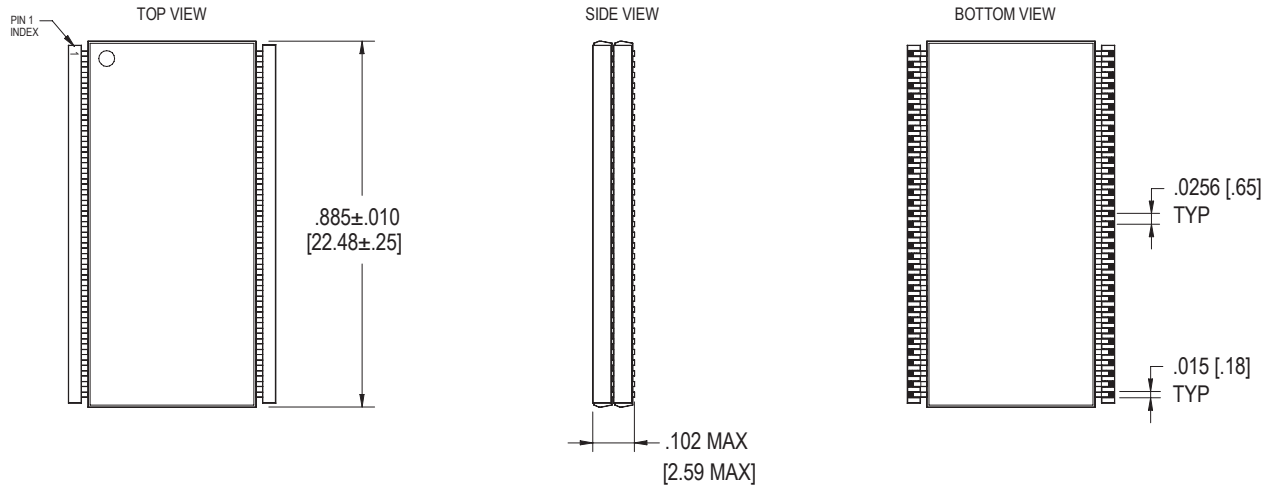
ADVANCED INFORMATION

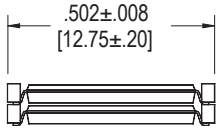
PART NUMBER DESCRIPTION



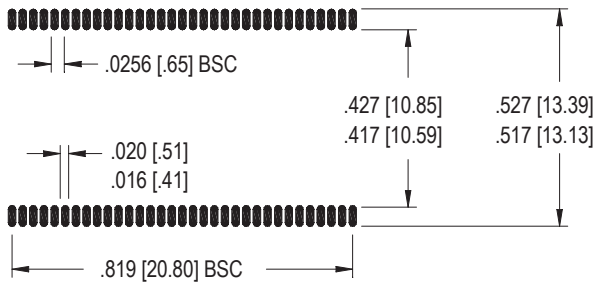
* Contact your sales representative for manufacturer and supplier codes.

MECHANICAL DRAWING





Standard TSOP pad layout is acceptable, however, when possible, the following pad layout is recommended for optimal manufacture and inspection. See Application Note 53A001-00 for further information.



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