ADVANCED COMPONENTS PACKAGING

1 Gigabit CMOS DDR SDRAM

DPDD128MX8XSBY5

PRELIMINARY

DESCRIPTION:

The Memory Stack™ series is a family of interchangeable memory modules. The 1 Gigabit Double Data Rate Synchronous DRAM module is a member of this family which utilizes the space saving LP-Stack™ TSOP stacking technology. The devices are constructed with two 64 Meg x 8 DDR SDRAMs.

This 512 Megabit based LP-Stack™ module, DPDD128MX8XSBY5, has been designed to fit in the same footprint as the 64 Meg x 8 DDR SDRAM TSOP monolithic. This allows system upgrade without electrical or mechanical redesign, providing an immediate and low cost memory solution.

FEATURES:

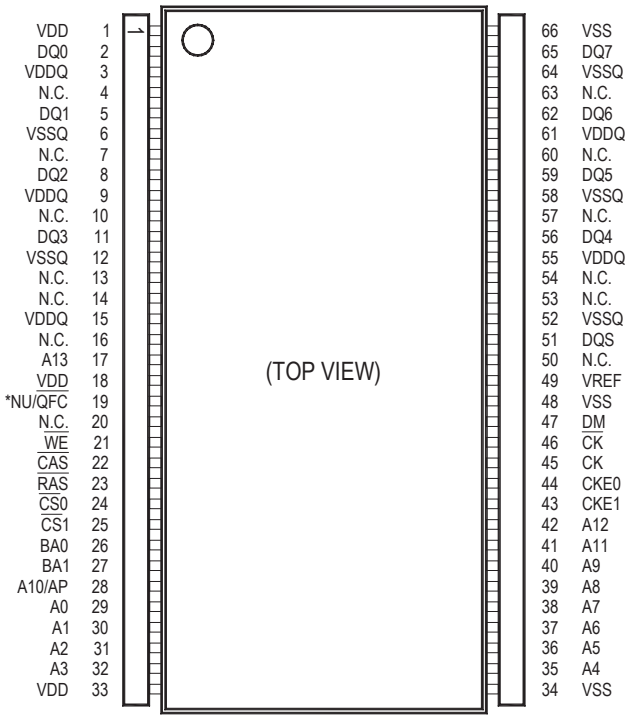
- Configuration:
  128 Meg x 8 (2 Banks of 16 Meg x 8 Bits x 4 Banks)
- JEDEC Approved Footprint and Pinout
- IPC-A-610 Manufacturing Standards
- Package: 66-Pin Leadless TSOP Stack

The Following Features are not affected by LP-Stack™ and are provided as reference only. Refer to memory OEM device specification for details:

- Clock Frequency is determined by OEM memory device used.
- 2.5 Volt DQ Supply
- JEDEC Standard SSTL_2 Interface for all Inputs/Outputs
- Four Bank Operation
- Programmable Burst Length and Read Latency
- Refresh: 8192 Cycles/64ms
- Refresh Types: Auto and Self

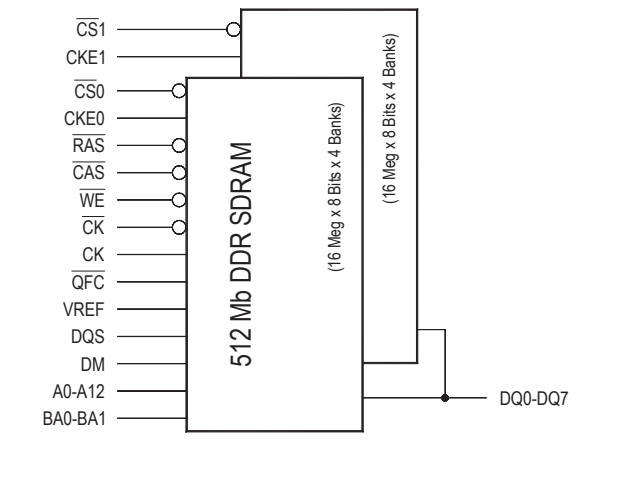
PIN NAMES	
A0-A12	Row Address: A0-A12 Column Address: A0-A9, A11, A12
BA0,BA1	Bank Select Address
A10/AP	Auto Precharge
DQ0-DQ7	Data In/Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{CS0}$,$\overline{CS1}$	Chip Selects
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Data Write Enable
CK, $\overline{CK}$	Differential Clock Inputs
CKE0, CKE1	Clock Enables
DQS	Data Strobe
DM	Data Masks
$\overline{QFC}$	DQ FET Switch Control
V_{DD}	Power Supply (+2.5V)
V_{SS}	Ground
V_{DDQ}	DQ Power Supply (+2.5V)
V_{SSQ}	DQ Ground
V_{REF}	Reference Voltage for inputs
N.C.	No Connect
NU*	Not used, Electrical Connect is Present

PIN-OUT DIAGRAM



* This pin is a No Connect for Some Manufacturers.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

DP	DD	128M	X	8	X	S	B	Y5	-	DP	-	XX	XX	XX
PREFIX	TYPE	MEMORY DEPTH	DESIG	MEMORY WIDTH	DESIG	I/O TYPE	DEVICE WIDTH	PACKAGE		SUPPLIER		MFR ID	CYCLE TIME	CAS LATENCY

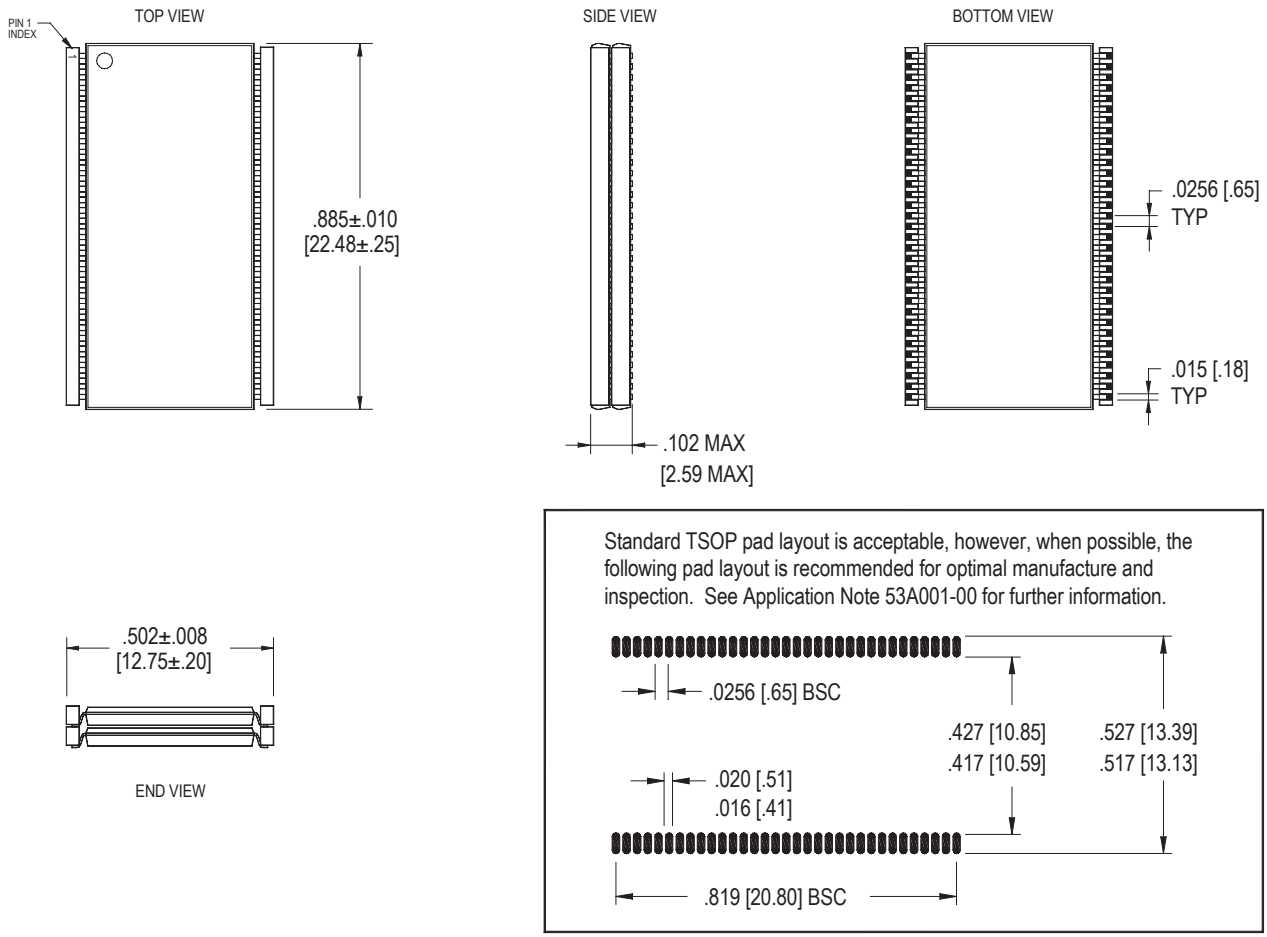
- CAS LATENCY
  - 20 CAS LATENCY 2.0
  - 25 CAS LATENCY 2.5
- CYCLE TIME
  - 60 6ns (166MHz)
  - 70 7ns (143MHz)
  - 75 7.5ns (133MHz)
  - 08 8ns (125MHz)
  - 10 10ns (100MHz)
- MFR ID: MANUFACTURER CODE *
- SUPPLIER: SUPPLIER CODE *
- PACKAGE: STACKABLE TSOP
- DEVICE WIDTH: x8 MEMORY BASED
- I/O TYPE: SSTL INPUTS/OUTPUTS
- DESIG: 512 MEGABIT BASED
- MEMORY WIDTH: MEMORY MODULE WITHOUT SUPPORT LOGIC
- TYPE: DOUBLE DATA RATE SYNCHRONOUS DRAM

* Contact your sales representative for supplier and manufacturer codes.

NOTE:

1. AC Parameters of base memory are unchanged from device manufacturers' specifications.
2. DC Parameters may be affected by stacking. Please refer to Application Note 53A004-00 for further information.

MECHANICAL DRAWING



PRELIMINARY

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