Ces, inc.

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5-TAP, TTL-INTERFACED FIXED DELAY LINE (SERIES DDU8F)

FEATURES

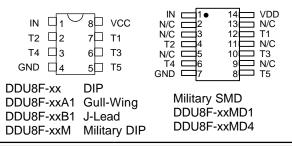
- Five equally spaced outputs
- Fits standard 8-pin DIP socket
- Low profile
- Auto-insertable
- Input & outputs fully TTL interfaced & buffered
- 10 T²L fan-out capability

FUNCTIONAL DESCRIPTION

The DDU8F-series device is a 5-tap digitally buffered delay line. The signal input (IN) is reproduced at the outputs (T1-T5), shifted in time by an amount determined by the device dash number (See Table). For dash numbers less than 5025, the total delay of the line is measured from T1 to T5. The nominal tap-to-tap delay increment is given by one-fourth of the

PACKAGES

data



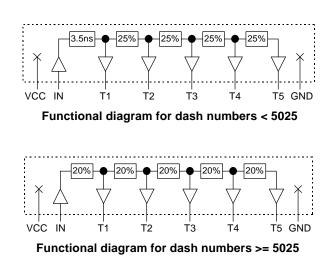
PIN DESCRIPTIONS

Signal Input Tap Outputs
+5 Volts
Ground

total delay, and the inherent delay from IN to T1 is nominally 3.5ns. For dash numbers greater than or equal to 5025, the total delay of the line is measured from IN to T5. The nominal tap-to-tap delay increment is given by one-fifth of this number.

SERIES SPECIFICATIONS

- Minimum input pulse width: 40% of total delay
- Output rise time: 2ns typical
- Supply voltage: $5VDC \pm 5\%$
- Supply current: I_{CCL} = 32ma typical
- Operating temperature: 0° to 70° C
- Temp. coefficient of total delay: 100 PPM/°C



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DASH NUMBER SPECIFICATIONS

Part	Total	Delay Per
Number	Delay (ns)	Tap (ns)
DDU8F-5004	4 ± 1.0 *	1.0 ± 0.5
DDU8F-5006	6 ± 1.0 *	1.5 ± 0.5
DDU8F-5008	8 ± 2.0 *	2.0 ± 1.0
DDU8F-5010	10 ± 2.0 *	2.5 ± 1.0
DDU8F-5012	12 ± 2.0 *	3.0 ± 1.0
DDU8F-5016	16 ± 2.0 *	4.0 ± 1.5
DDU8F-5020	20 ± 3.0 *	5.0 ± 2.0
DDU8F-5025	25 ± 3.0	5.0 ± 2.0
DDU8F-5030	30 ± 3.0	6.0 ± 2.0
DDU8F-5035	35 ± 3.0	7.0 ± 2.0
DDU8F-5040	40 ± 3.0	8.0 ± 2.0
DDU8F-5045	45 ± 3.0	9.0 ± 3.0
DDU8F-5050	50 ± 3.0	10.0 ± 3.0
DDU8F-5060	60 ± 3.0	12.0 ± 3.0
DDU8F-5075	75 ± 4.0	15.0 ± 3.0
DDU8F-5100	100 ± 5.0	20.0 ± 3.0
DDU8F-5125	125 ± 6.5	25.0 ± 3.0
DDU8F-5150	150 ± 7.5	30.0 ± 3.0
DDU8F-5175	175 ± 8.0	35.0 ± 4.0
DDU8F-5200	200 ± 10.0	40.0 ± 4.0
DDU8F-5250	250 ± 12.5	50.0 ± 5.0

* Total delay is referenced to first tap output Input to first tap = $3.5ns \pm 1ns$

NOTE: Any dash number between 5004 and 5250 not shown is also available.

APPLICATION NOTES

HIGH FREQUENCY RESPONSE

The DDU8F tolerances are guaranteed for input pulse widths and periods greater than those specified in the test conditions. Although the device will function properly for pulse widths as small as 40% of the total delay and periods as small as 80% of the total delay (for a symmetric input), the delays may deviate from their values at low frequency. However, for a given input condition, the deviation will be repeatable from pulse to pulse. Contact technical support at Data Delay Devices if your application requires device testing at a specific input condition.

POWER SUPPLY BYPASSING

The DDU8F relies on a stable power supply to produce repeatable delays within the stated tolerances. A 0.1uf capacitor from VCC to GND, located as close as possible to the VCC pin, is recommended. A wide VCC trace and a clean ground plane should be used.

DEVICE SPECIFICATIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V _{cc}	-0.3	7.0	V	
Input Pin Voltage	V _{IN}	-0.3	V _{DD} +0.3	V	
Storage Temperature	T _{STRG}	-55	150	С	
Lead Temperature	T _{LEAD}		300	С	10 sec

TABLE 1: ABSOLUTE MAXIMUM RATINGS

TABLE 2: DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
High Level Output Voltage	V _{OH}	2.5	3.4		V	$V_{CC} = MIN, I_{OH} = MAX$
						$V_{IH} = MIN, V_{IL} = MAX$
Low Level Output Voltage	V _{OL}		0.35	0.5	V	$V_{CC} = MIN, I_{OL} = MAX$
						$V_{IH} = MIN, V_{IL} = MAX$
High Level Output Current	I _{OH}			-1.0	mA	
Low Level Output Current	I _{OL}			20.0	mA	
High Level Input Voltage	V _{IH}	2.0			V	
Low Level Input Voltage	V _{IL}			0.8	V	
Input Clamp Voltage	VIK			-1.2	V	$V_{CC} = MIN, I_I = I_{IK}$
Input Current at Maximum	I _{IHH}			0.1	mA	$V_{CC} = MAX, V_1 = 7.0V$
Input Voltage						
High Level Input Current	Iн			20	μA	$V_{CC} = MAX, V_I = 2.7V$
Low Level Input Current	١ _{١L}			-0.6	mA	$V_{CC} = MAX, V_1 = 0.5V$
Short-circuit Output Current	I _{OS}	-60		-150	mA	$V_{CC} = MAX$
Output High Fan-out				25	Unit	
Output Low Fan-out				12.5	Load	

(0C to 70C, 4.75V to 5.25V)

.010 TYP.

.300

TYP.

.050 TYP.-

.350

MAX.

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.050

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.008

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.065 TYP.

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MAX.

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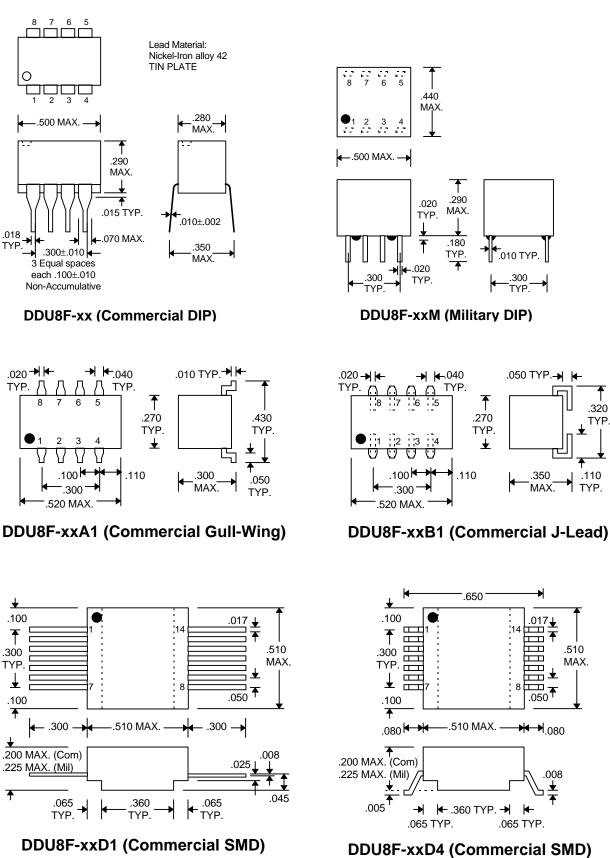
.320

TYP.

.110

TYP.

PACKAGE DIMENSIONS



DDU8F-xxMD4 (Military SMD)

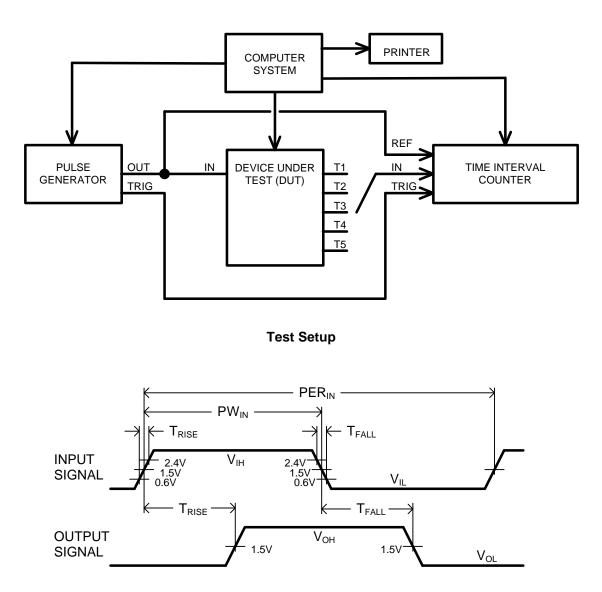
DDU8F-xxMD1 (Military SMD)

DELAY LINE AUTOMATED TESTING

TEST CONDITIONS

INPUT: Ambient Temperature:	$25^{\circ}C \pm 3^{\circ}C$	OUTPUT: Load:	1 FAST-TTL Gate
Supply Voltage (Vcc):		C _{load} :	5pf ± 10%
Input Pulse:	High = $3.0V \pm 0.1V$	Threshold:	1.5V (Rising & Falling)
	$Low = 0.0V \pm 0.1V$		
Source Impedance:	50Ω Max.		
Rise/Fall Time:	3.0 ns Max. (measured		
	between 0.6V and 2.4V)		
Pulse Width:	PW _{IN} = 1.5 x Total Delay		
Period:	$PER_{IN} = 10 \text{ x}$ Total Delay		

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.



Timing Diagram For Testing