DS2434
Battery Identification Chip

www.dalsemi.com

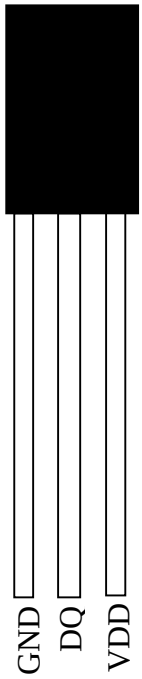
FEATURES

- Provides unique ID number to battery packs
- Eliminates thermistors by sensing battery temperature on-chip
- 256-bit nonvolatile user memory available for storage of user data such as gas gauge and manufacturing information
- Operating range of -40°C to +85°C
- Applications include portable computers, portable/cellular phones, consumer electronics, and handheld instrumentation.
- Surface-mount package (209-mil SSOP16) available

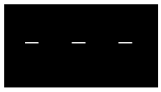
PIN DESCRIPTION

GND	- Ground
DQ	- Data In/Out
V_{DD}	- Supply Voltage
NC	- No Connect

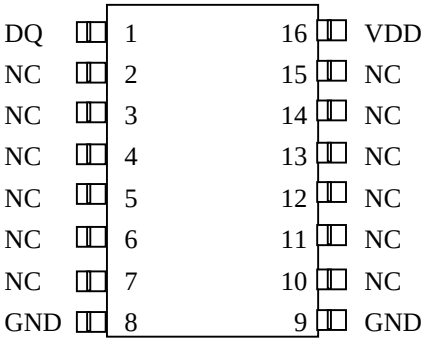
PACKAGE OUTLINE



DS2434
PR-35 PACKAGE
See Mech. Drawings
Section



BOTTOM VIEW



DS2434 16-Pin SSOP
See Mech. Drawings
Section

DESCRIPTION

The DS2434 Battery Identification Chip provides a convenient method of tagging and identifying battery packs by manufacturer, chemistry, or other identifying parameters. The DS2434 allows the battery pack to be coded with a unique identification number, and also store information regarding the battery life and charge/discharge characteristics in its nonvolatile memory.

The DS2434 also performs the essential function of monitoring battery temperature, without the need for a thermistor in the battery pack.

Information is sent to/from the DS2434 over a 1-Wire interface, so that battery packs need only have three output connectors; power, ground, and the 1-Wire interface.

DETAILED PIN DESCRIPTION

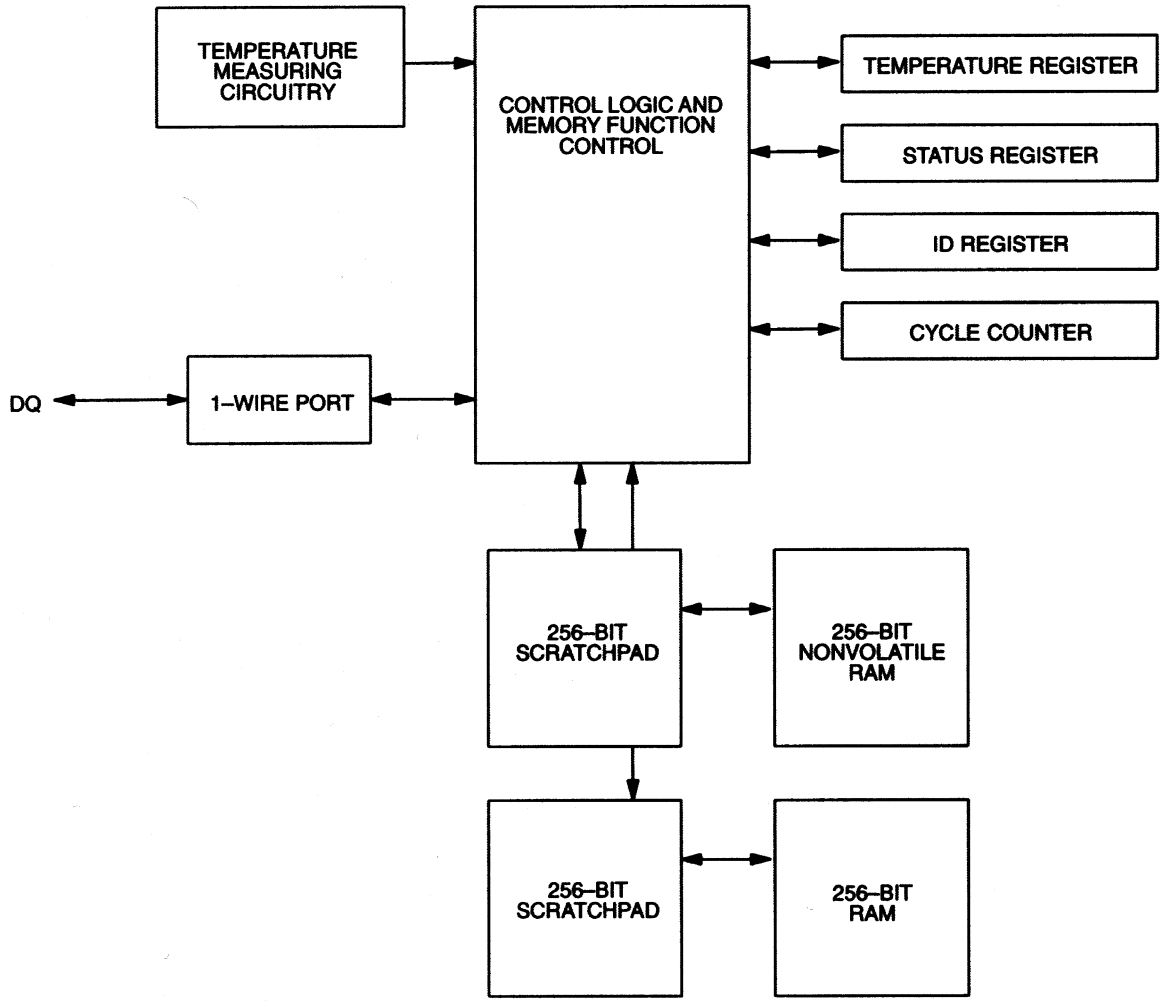
PIN 14-PIN SOIC	PIN PR35	SYMBOL	DESCRIPTION
1	1	GND	**Ground pin**
14	2	DQ	**Data Input/Output pin**- for 1Wire communication port
13	3	VDD	**Supply pin**- input power supply

OVERVIEW

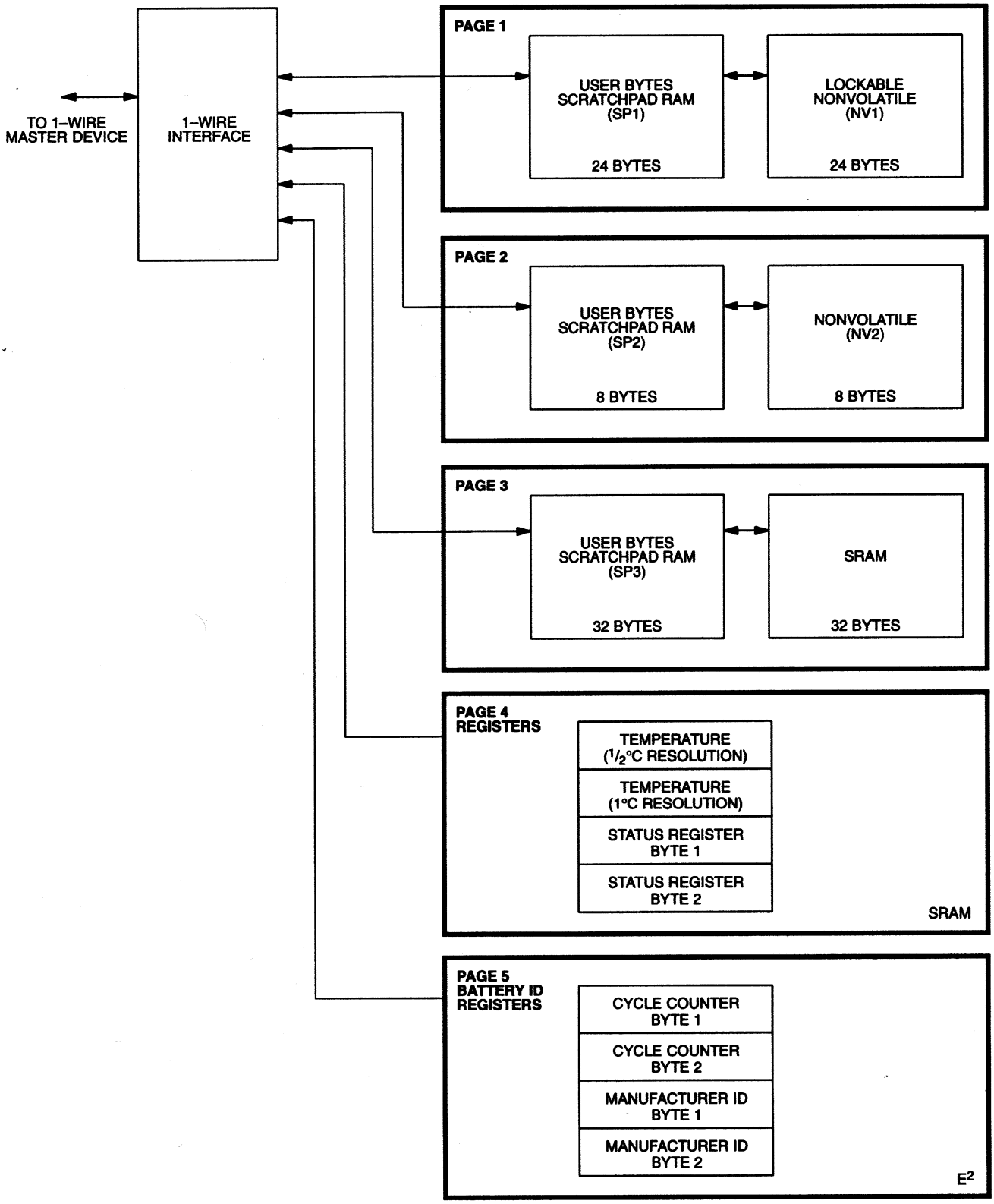
The DS2434 has five major components: 1) Scratchpad Memory, 2) Nonvolatile Memory, 3) On-board SRAM, 4) Temperature Sensor, and 5) ID Register. All data is read and written least significant bit first.

Access to the DS2434 is over a 1-Wire interface. Charging parameters and other data such as battery chemistry, gas gauge information, and other user data would be stored in the DS2434, allowing this information to be permanently stored in the battery pack. Nonvolatile (E^2) RAM holds information even if the battery goes dead; as long as the battery remains within typical charge/discharge operating range, the SRAM provides battery-backed storage of information.

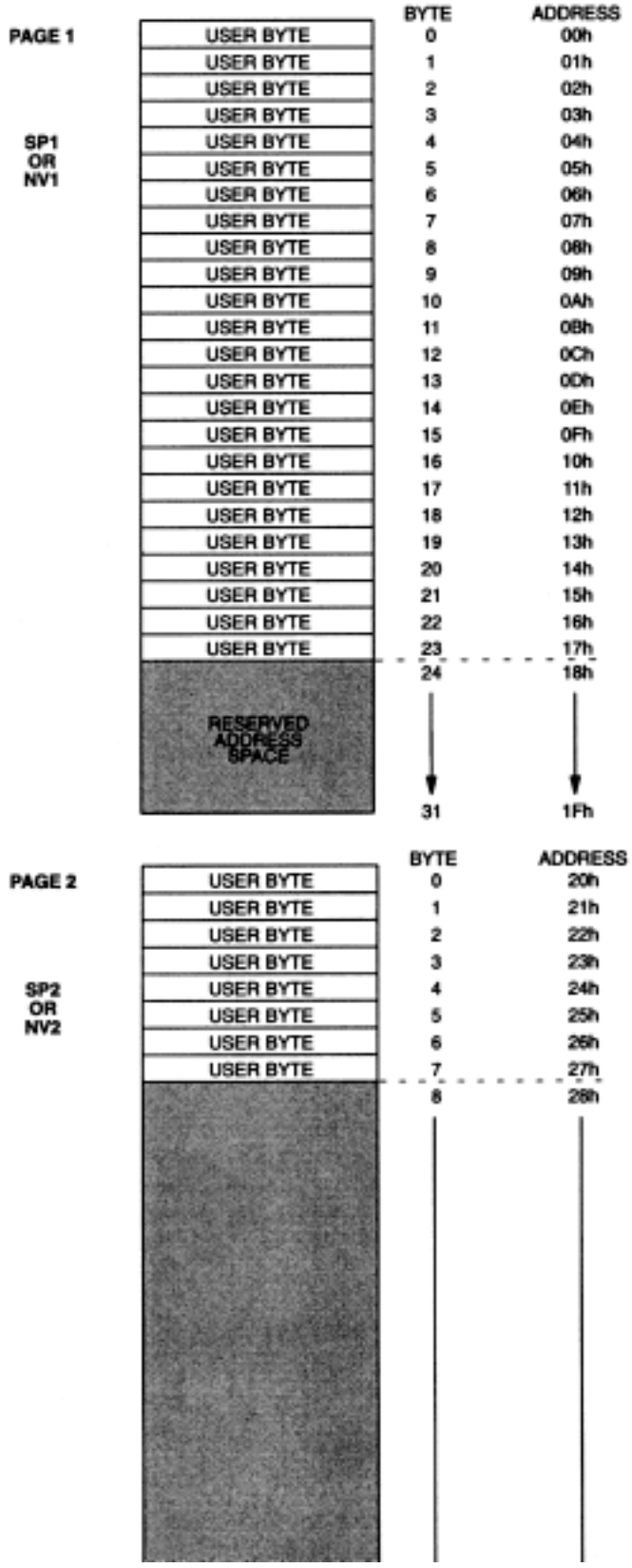
DS2434 BLOCK DIAGRAM Figure 1



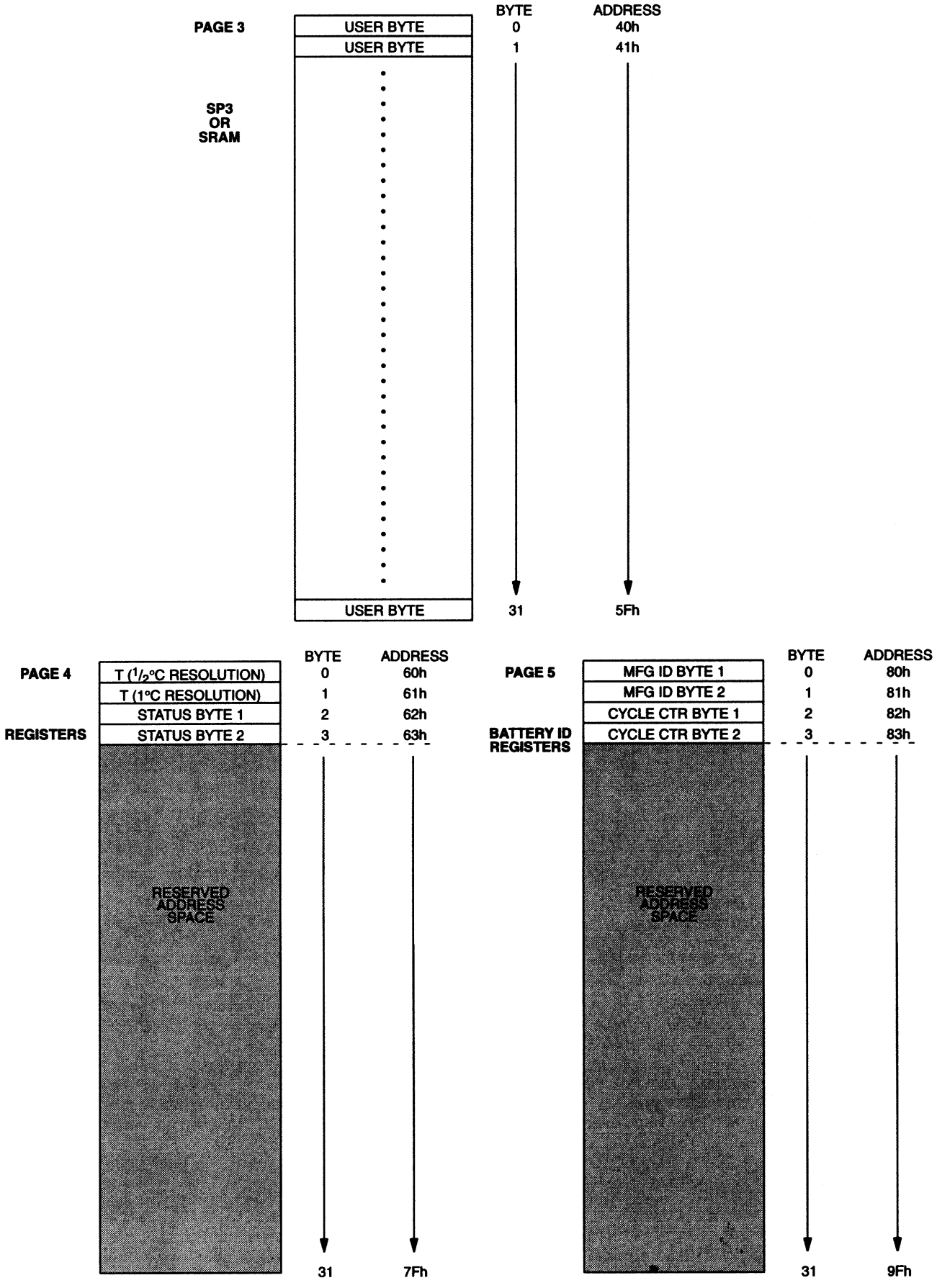
DS2434 MEMORY PARTITIONING Figure 2



DS2434 ADDRESSABLE RAM MEMORY MAP Figure 3



DS2434 ADDRESSABLE RAM MEMORY MAP (cont'd) Figure 3



MEMORY

The DS2434's memory is divided into five pages, each page filling 32 bytes of address space. Not all of the available addresses are used, however. Refer to the memory map of Figure 3 to see actual addresses which are available for use.

The first three pages of memory consist of a scratchpad RAM and then either a nonvolatile RAM (pages 1 and 2) or SRAM (page 3). The scratchpads help insure data integrity when communicating over the 1-Wire bus. Data is first written to the scratchpad where it can be read back. After the data has been verified, a Copy Scratchpad command will transfer the data to the RAM (NV or SRAM). This process insures data integrity when modifying the memory.

The fourth page of memory consists of registers which contain the measured temperature value and status registers for the device; these registers are made from SRAM cells.

The fifth page of memory holds the ID number for the device and the cycle count registers in E^2 RAM, making these registers nonvolatile under all power conditions.

PAGE 1

The first page of memory has 24 bytes. It consists of a scratchpad RAM and a nonvolatile (E^2) RAM. These 24 bytes may be used to store any data the user wishes; such as battery chemistry descriptors, manufacturing lot codes, gas gauge information, etc.

The nonvolatile portion of this page may be locked to prevent data stored here from being changed inadvertently.

Both the nonvolatile and the scratchpad portions are organized identically, as shown in the memory map of Figure 3. In this page, these two portions are referred to as NV1 and SP1, respectively.

PAGE 2

The second page of memory has 8 bytes. It consists of a scratchpad RAM and a nonvolatile (E^2) RAM. These eight bytes may be used to store any data the user wishes, such as battery chemistry descriptors, manufacturing lot codes, gas gauge information, etc.

PAGE 3

The third page of memory has a full 32 bytes. It consists of a scratchpad RAM and an SRAM. This address space may be used to store any data the user wishes, provided that, should the battery go dead and power to the DS2434 is lost, this data may also be lost without serious repercussions. Data which must remain even if power to the DS2434 is lost should be placed in either Page 1 or Page 2.

This section of memory may be used to store gas gauge and self-discharge information. If the battery dies and this information is lost, it is moot because the user can easily determine that the battery is dead.

PAGE 4

The fourth page of memory is used by the DS2434 to store the converted value of battery temperature. A 2-byte status register is also provided.

TEMPERATURE REGISTERS (60h-61h)

The DS2434 can measure temperature without external components. The resulting temperature measurement is placed into two temperature registers. These registers are SRAM, and therefore will hold the values placed in them until the battery voltage falls below the minimum V_{DD} specified. The first

register, at address 60h, provides 1/2°C resolution for temperatures between 0°C and 127 1/2°C, formatted as follows:

64°C	32°C	16°C	8°C	4°C	2°C	1°C	1/2°C

The second register, at address 61h, provides 1°C resolution over the -40°C to +85°C range, formatted as follows in the binary two's complement coding.

7-BIT BINARY TEMP READING,
SHOWS 1°C INCREMENTS

SIGN BIT -0 FOR POSITIVE,
1 FOR NEGATIVE

STATUS/CONTROL REGISTER (62h-63h)

The status register is a 2-byte register at addresses 62h and 63h (consisting of SRAM). Address 62h is the least significant byte of the status register, and is currently the only address with defined status bits; the other byte at address 63h is reserved for future use. The status register is formatted as follows:

STATUS REGISTER

							LSB	
X	X	X	X	X	LOCK	NVB	TB	62h
X	X	X	X	X	X	X	X	63h

where

X = Don't Care

TB = Temperature Busy flag. 1 = temperature conversion in progress; 0 = temperature conversion complete, valid data in temperature register.

NVB = nonvolatile memory busy flag. 1 = Copy from scratchpad to NV RAM in progress, 0 = nonvolatile memory is not busy. A copy to NV RAM may take from 2 ms to 10 ms (taking longer at lower supply voltages).

LOCK = NV1 Locked flag. 1 indicates that NV1 is locked; 0 indicates that NV1 is unlocked.

MSB BYTE 2

32768	16384	8192	4096	2048	1024	512	256

83h

BYTE 1 LSB

128	64	32	16	8	4	2	1

82h

PAGE 5

The fifth page of memory holds the battery manufacturer ID number as well as a 2-byte counter for counting the number of battery charge/discharge cycles.

ID REGISTER (80h and 81h)

The ID Register is a 16-bit ROM register that can contain a unique identification code, if purchased from Dallas Semiconductor. This ID number is programmed by Dallas Semiconductor, is unchangeable, and is unique to each customer. This ID number may be used to assure that batteries containing a DS2434 have the same manufacturer ID number as a charger configured to operate with that battery pack. This feature may be used to prevent charging of batteries for which the charging circuit has not been designed.

CYCLE COUNTER (82h and 83h)

The cycle counter register gives an indication of the number of charge/discharge cycles the battery pack has been through. This nonvolatile (E 2) register is incremented by the user through the use of a protocol to the DS2434 and is reset by another protocol. The counter is a straight binary counter, formatted as follows:

MEMORY FUNCTION COMMANDS

The protocols necessary for accessing the DS2434 are described in this section. Only these protocols may be written to the DS2434. Writing other protocols to the device may result in permanent damage to the part. These are summarized in Table 1, and examples of memory functions are provided in Tables 2 and 3.

PAGE 1 THROUGH PAGE 3 COMMANDS

Read Scratchpad [11h]

This command reads the contents of the scratchpad RAM on the DS2434. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin reading the data. The user may read data through the end of the scratchpad space (address 5Fh), with any reserved data bits reading all logic 1s and after which the data read will be all logic 1s.

Write Scratchpad [17h]

This command writes to the scratchpad RAM on the DS2434. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin writing data to the DS2434 scratchpad at the starting byte address.

Copy SP1 to NV1 [22h]

This command copies the entire contents (24 bytes) of Scratchpad 1 (SP1) to its corresponding nonvolatile memory (NV1). The nonvolatile RAM memory of the DS2434 cannot be written to directly by the bus master; however, the scratchpad RAM may be copied to the nonvolatile RAM. This prevents accidental overwriting of the nonvolatile RAM, and allows the data to be written first to the scratchpad, where it can be read back and verified before copying to the nonvolatile RAM. This command does not use a start address; the entire contents of the scratchpad will be copied to the nonvolatile RAM. The NVB bit will be set when the copy is in progress. NV1 is made with E^2 type memory cells that will accept at least 50000 changes.

Copy SP2 to NV2 [25h]

This command copies the entire contents (8 bytes) of SP2 (user bytes) to its corresponding nonvolatile memory (NV2). This command does not use a start address; the entire contents of SP2 will be copied to NV2. The NVB bit will be set when the copy is in progress. NV2 is made with E^2 type memory cells that will accept at least 50000 changes.

Copy SP3 to SRAM [28h]

This command copies the entire contents (32 bytes) of SP3 to its corresponding SRAM. This command does not use a start address; the entire contents of SP3 will be copied to the SRAM.

Copy NV1 to SP1 [71h]

This command copies the entire contents (24 bytes) of NV1 to its corresponding scratchpad RAM (SP1). This command does not use a start address; the entire contents of NV1 will be copied to SP1. The nonvolatile RAM memory of the DS2434 cannot be read directly by the bus master; however, the nonvolatile RAM may be copied to the scratchpad RAM.

Copy NV2 to SP2 [77h]

This command copies the entire contents (8 bytes) of NV2 (user bytes) to its corresponding scratchpad RAM (SP2). This command does not use a start address; the entire contents of NV2 will be copied to SP2. The nonvolatile RAM memory of the DS2434 cannot be read directly by the bus master; however, the nonvolatile RAM may be copied to the scratchpad RAM.

Copy SRAM to SP3 [7Ah]

This command copies the entire contents (32 bytes) of SRAM to its corresponding scratchpad RAM (SP3). This command does not use a start address; the entire contents of SRAM will be copied to SP3. The SRAM memory of the DS2434 cannot be read directly by the bus master; however, the SRAM may be copied to the scratchpad RAM.

Lock NV1 [43h]

This command prevents copying SP1 to NV1. This is done as an added measure of data security, preventing data from being changed inadvertently. NV1 may be copied up into SP1 while the part is locked. This allows NV1 to be read at any time. However, NV1 cannot be written to through a Copy SP1 to NV1 command without first unlocking the DS2434.

Unlock NV1 [44h]

This command unlocks NV1 to allow copying SP1 into NV1. This is done as an added measure of data security, preventing data from being changed inadvertently.

PAGE 4 AND 5 COMMANDS

Convert T [D2h]

This command instructs the DS2434 to initiate a temperature conversion cycle. This sets the TB flag. When the temperature conversion is done, the TB flag is reset and the current temperature value is placed in the temperature register. While a temperature conversion is taking place, all other memory functions are still available for use.

Read Registers [B2h]

This command reads the contents of the registers in Page 4 and 5. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin reading the data. The user may read data through the end of the register space (through address 63h in Page 4, address 83h in Page 5), after which the data read will be all logic 1s.

Increment Cycle [B5h]

This command increments the value in the cycle counter register. This command does not use a start address; no further data is required.

Reset Cycle Counter [B8h]

This command is used to reset the cycle counter register to 0, if desired.

DS2434 COMMAND SET Table 1

INSTRUCTION	DESCRIPTION	PROTOCOL	1-WIRE BUS MASTER STATUS AFTER ISSUING PROTOCOL	1-WIRE BUS DATA AFTER ISSUING PROTOCOL
Read Scratchpad	Reads bytes from DS2434 Scratchpad	11<addr (00h-05h)>	RX	<read data>
Write Scratchpad	Writes bytes to DS2434 Scratchpad	17h<addr 00h-5Fh)>	TX	<write data>
Copy SP1 to NV1	Copies entire contents of SP1 to NV1	22h	Idle	{NVB bit in Status Register=1 until copy complete(10 ms, typ)}
Copy to SP2 to NV2	Copies entire contents of SP2 to NV2	25h	Idle	{NVB bit in Status Register=1 until copy complete(10 ms, typ)}
Copy SP3 to SRAM	Copies entire contents to SP3 to SRAM	28h	Idle	Idle
Copy NV1 to SP1	Copies entire contents to NV1 to SP1	71h	Idle	Idle
Copy NV2 to SP2	Copies entire contents to NV2 to SP2	77h	Idle	Idle
Copy SRAM to SP3	Copies entire contents of SRAM to SP3	7Ah	Idle	Idle
Lock NV1	Locks 24 bytes of SP1 and NV1 from reading and writing.	43h	Idle	{NVB bit in Status Register=1 until copy complete(10 ms, typ)}
Unlock NV1	Unlocks 24 bytes of SP1 and NV1 for reading and writing	44h	Idle	{NVB bit in Status Register=1 until copy complete(10 ms, typ)}
Read Registers	Reads bytes from Temperature, Status and ID Registers	B2<addr (60h-63h, 80h-83h)>	RX	<read data>
Reset Cycle Counter	Resets cycle counter register to 0	B8h	Idle	{NVB bit in Status Register=1 until copy complete (10 ms, typ)}
Increment Cycle Counter	Increments the value in the cycle counter register	B5h	Idle	{NVB bit in Status Register= 1 until copy complete (10 ms, typ)}
Convert T	Initiates temperature conversion	D2h	Idle	{TB bit in Status Register = 1 until conversion complete}

MEMORY FUNCTION EXAMPLE Table 2

Example: Bus Master writes 24 bytes of data to DS2434 scratchpad, then copies to it to NV1.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480-960 µs)
RX	Presence	Presence pulse
TX	17h	Issue "write scratchpad" command
TX	00h	Start address
TX	<24 bytes>	Write 24 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	11h	Issue "read scratchpad" command
TX	00h	Start address
RX	<24 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	22h	Issue "copy SP1 to NV1" command
RX	<busy indicator>	Wait until NVB in status register=0 (10 ms typical)
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

MEMORY FUNCTION EXAMPLE Table 3

Example: Bus Master initiates temperature conversion, then reads temperature.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480-960 µs)
RX	Presence	Presence pulse
TX	D2h	Issue "convert T" command
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	B2h	Issue "read registers" command; begin loop
TX	62h	Status register address
RX	<1 data byte>	Read status register and loop until TB=0
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	B2h	Issue "read registers" command
TX	61h	Temperature register address
RX	<1 data byte>	Read temperature register
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

1-WIRE BUS SYSTEM

The DS2434 1-Wire bus is a system which has a single bus master and one slave. The DS2434 behaves as a slave. The DS2434 is not able to be multidropped, unlike other 1-Wire devices from Dallas Semiconductor.

The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing).

HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open drain or 3-state outputs. The 1-Wire port of the DS2434 is open drain with an internal circuit equivalent to that shown in Figure 5. The 1-Wire bus requires a pullup resistor of approximately 5 kΩ.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. Infinite recovery time can occur between bits so long as the bus is left in the idle (HIGH) state during the interrupt. If this does not occur and the bus is left low for more than 480 µs, all components on the bus will be reset.

TRANSACTION SEQUENCE

The protocol for accessing the DS2434 via the 1-Wire port is as follows:

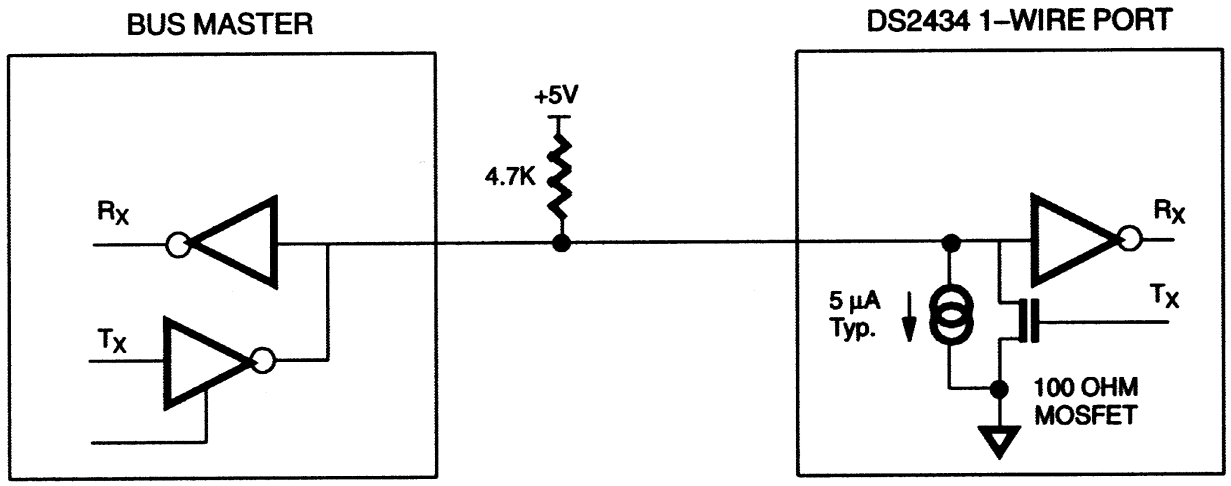
- Initialization
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS2434 is on the bus and is ready to operate. For more details, see the "1-Wire Signaling" section.

HARDWARE CONFIGURATION Figure 4



I/O SIGNALING

The DS2434 requires strict protocols to insure data integrity. The protocol consists of several types of signaling on one line: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. All of these signals, with the exception of the presence pulse, are initiated by the bus master.

The initialization sequence required to begin any communication with the DS2434 is shown in Figure 5. A reset pulse followed by a presence pulse indicates the DS2434 is ready to send or receive data given the correct memory function command.

The bus master transmits (TX) a reset pulse (a low signal for a minimum of 480 µs). The bus master then releases the line and goes into a receive mode (RX). The 1-Wire bus is pulled to a high state via the 5k pullup resistor. After detecting the rising edge on the I/O pin, the DS2434 waits 15-60 µs and then transmits the presence pulse (a low signal for 60-240 µs).

READ/WRITE TIME SLOTS

DS2434 data is read and written through the use of time slots to manipulate bits and a command word to specify the transaction.

Write Time Slots

A write time slot is initiated when the host pulls the data line from a high logic level to a low logic level. There are two types of write time slots: Write 1 time slots and Write 0 time slots. All write time slots must be a minimum of 60 µs in duration with a minimum of a 1 µs recovery time between individual write cycles.

The DS2434 samples the I/O line in a window of 15 µs to 60 µs after the I/O line falls. If the line is high, a Write 1 occurs. If the line is low, a Write 0 occurs (see Figure 6).

For the host to generate a Write 1 time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 µs after the start of the write time slot.

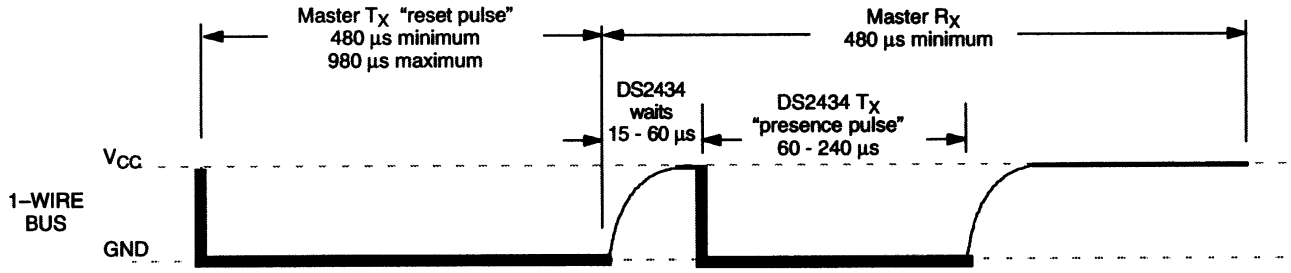
For the host to generate a Write 0 time slot, the data line must be pulled to a logic low level and remain low for the duration of the write time slot.

Read Time Slots

The host generates read time slots when data is to be read from the DS2434. A read time slot is initiated when the host pulls the data line from a logic high level to logic low level. The data line must remain at a low logic level for a minimum of 1 µs; output data from the DS2434 is then valid for the next 14 µs maximum. The host therefore must stop driving the I/O pin low in order to read its state 15 µs from the start of the read slot (see Figure 6). By the end of the read time slot, the I/O pin will pull back high via the external pullup resistor. All read time slots must be a minimum of 60 µs in duration with a minimum of a 1 µs recovery time between individual read slots.

Figure 7 shows that the sum of T_{INIT} , T_{RC} , and T_{SAMPLE} must be less than 15 µs. Figure 9 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as small as possible and by locating the master sample time towards the end of the 15 µs period.

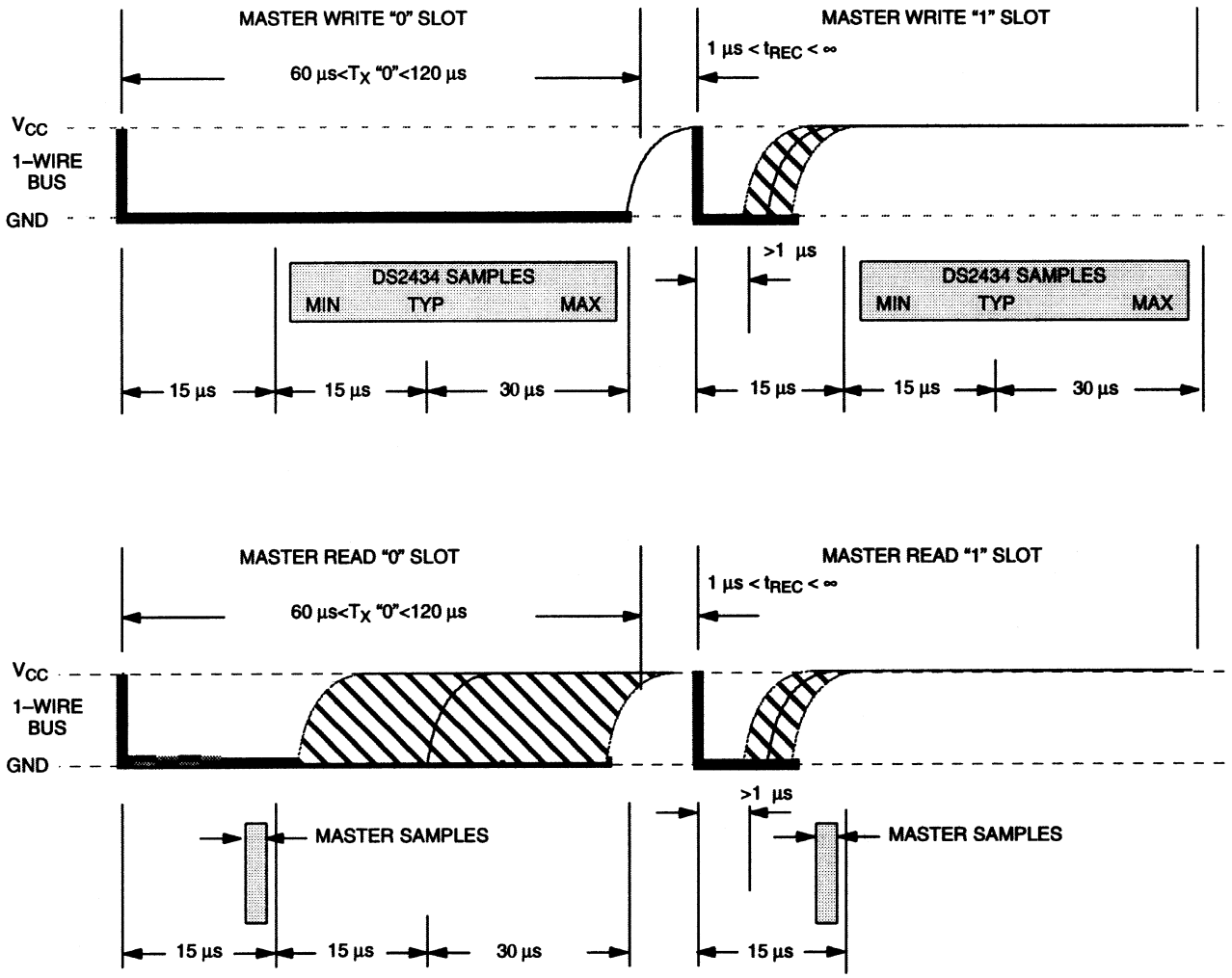
INITIALIZATION PROCEDURE “RESET AND PRESENCE PULSES” Figure 5



LINE TYPE LEGEND:

———	Bus master active low	———	DS2434 active low
- - - -	Both bus master and DS2434 active low	———	Resistor pullup

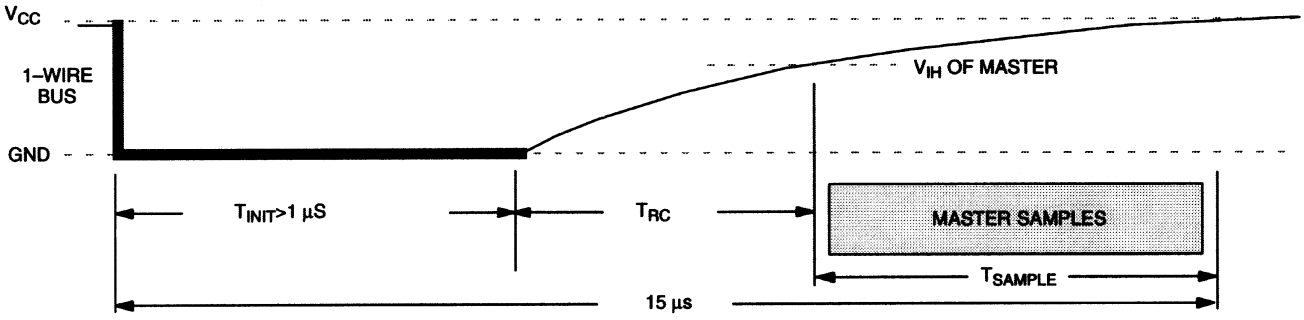
READ/WRITE TIMING DIAGRAM Figure 6



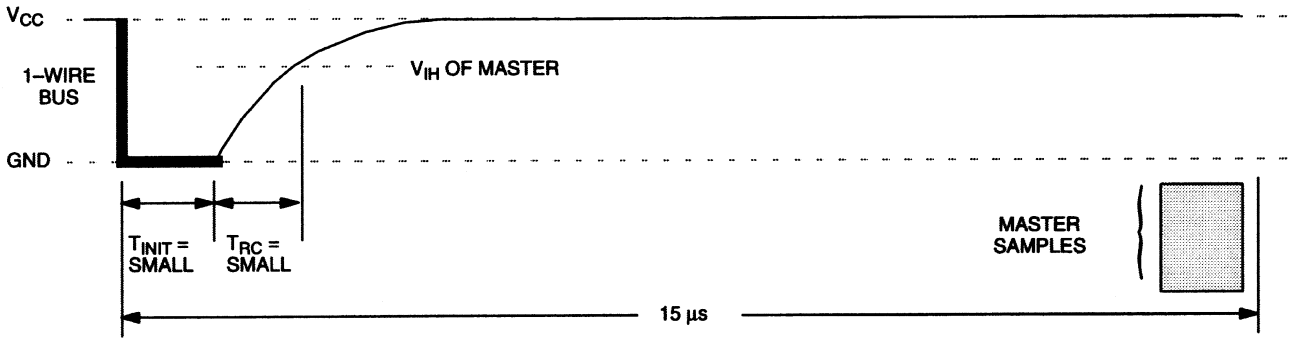
LINE TYPE LEGEND:

▬▬	Bus master active low	▬▬	DS2434 active low
▬ ▬ ▬	Both bus master and DS2434 active low	———	Resistor pullup

DETAILED MASTER READ "1" TIMING Figure 7



RECOMMENDED MASTER READ "1" TIMING Figure 8



LINE TYPE LEGEND:

▬▬	Bus master active low	▬▬	DS2434 active low
▬ ▬	Both bus master and DS2434 active low	———	Resistor pullup

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-40°C to +85°C; V_{DD} =3.6V to 6.4V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	I/O Functions	2.5		6.4	V	1
		NV Copy Functions	2.7		6.4		
		±½°C Accurate Temp. Conversions	3.6		6.4		
Data Pin	$V_{I/O}$		-0.3		V_{CC}+0.3	V	2

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{DD} =3.6V to 6.4V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Temperature Accuracy (=T_{ACTUAL} -$T_{MEASURED}$)		T_A =0°C to 70°C			±½	°C	3
		T_A =-40°C to 0°C and + 70°C to +85°C			±1		
Input Logic High	V_{IH}		2.2		V_{CC}+0.3	V	
Input Logic Low	V_{IL}		-0.3		+0.8	V	
Sink Current	I_L	$V_{I/O}$=0.4V	-4.0			mA	
Standby Current	I_Q				3	µA	
Active Current	I_{DD}				1.5	mA	4
Input Resistance	R_I			500		kΩ	4

NOTES:

1. Temperature conversion will work with ±2°C accuracy down to V_{DD} =2.7V.

2. The DQ terminal can withstand programming pulses up to 12V maximum. This maintains compatibility to MicroLAN devices.

3. Reflects sensor accuracy as tested during calibration.

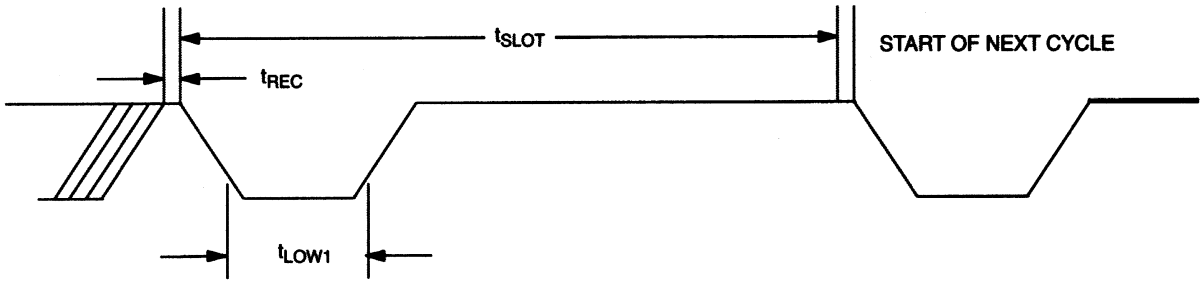
4. I/O line in "hi-Z" state and $I_{I/O}$ =0.

AC ELECTRICAL CHARACTERISTICS:
1-WIRE INTERFACE

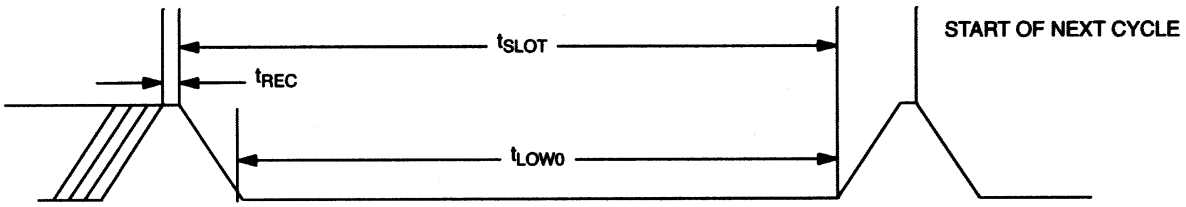
(-40°C to +85°C; V_{DD} =3.6V to 6.4V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	t_{CONV}		700	1000	ms	
Time Slot	t_{SLOT}	60		120	µs	
Recovery Time	t_{REC}	1			µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Read Data Valid	t_{RDV}			15	µs	
Reset Time High	t_{RSTH}	480			µs	
Reset Time Low	t_{RSTL}	480			µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	
Capacitance	$C_{IN/OUT}$			25	pF	
NV Write Cycle	t_{WR}		10	50	ms	

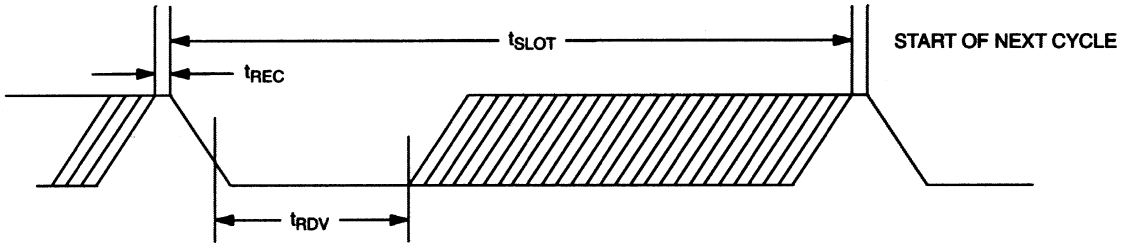
1-WIRE WRITE ONE TIME SLOT



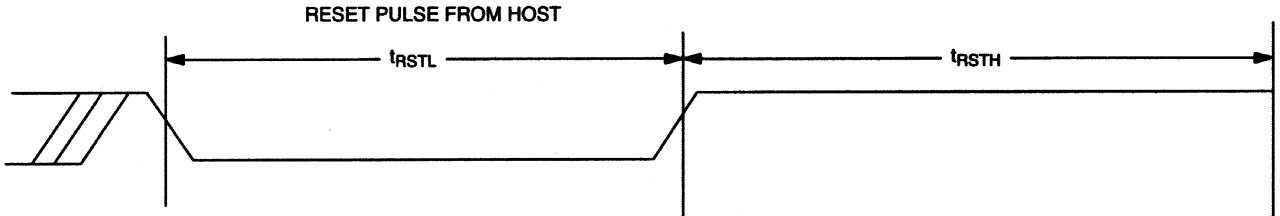
1-WIRE WRITE ZERO TIME SLOT



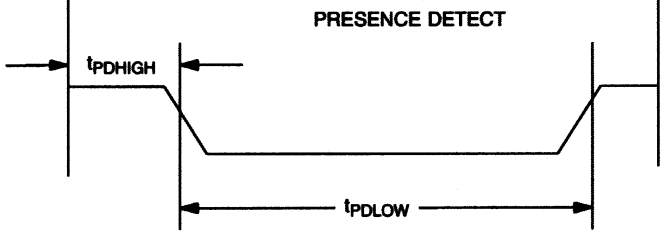
1-WIRE READ ZERO TIME SLOT



1-WIRE RESET PULSE



1-WIRE PRESENCE DETECT



DATA SHEET REVISION SUMMARY

The following represent the key differences between 04/24/97 and 07/31/97 version of the DS2434 data sheet. Please review this summary carefully.

1. Add surface mount package (16-pin SSOP); page 1.
2. Correct cycle counter LSB description; page 7.
3. Add supply voltage compatibility on DQ up to 12V; page 15.