133-MHz Spread Spectrum FTG for Mobile Pentium® III Platforms

Features

- **Maximized EMI suppression using Cypress's Spread Spectrum technology (–0.5% and ±0.5%)**
- **Single chip system FTG for Mobile Intel® Platforms**
- **Two CPU outputs**
- **Seven copies of PCI clock (one Free Running)**
- **Seven SDRAM clock (one DCLK for Memory Hub)**
- **Two copies of 48-MHz clock (non-spread spectrum) optimized for USB reference input and video DOT clock**
- **Three 3V66 Hublink/AGP outputs**
- **One VCH clock (48-MHz non-SSC or 66.67-MHz SSC)**
- **One APIC outputs**
- **One buffered reference output**
- **Supports frequencies up to 133 MHz**
- **SMBus interface for programming**
- **Power management control inputs**

Key Specifications

CPU, SDRAM Outputs Cycle-to-Cycle Jitter:..... 250 ps

APIC, 48-MHz, 3V66, PCI Outputs Cycle-to-Cycle Jitter: .....500 ps

CPU Output Skew: .....150 ps

3V66 Output Skew: .....175 ps

APIC, SDRAM Output Skew: .....250 ps

PCI Output Skew:.....500 ps

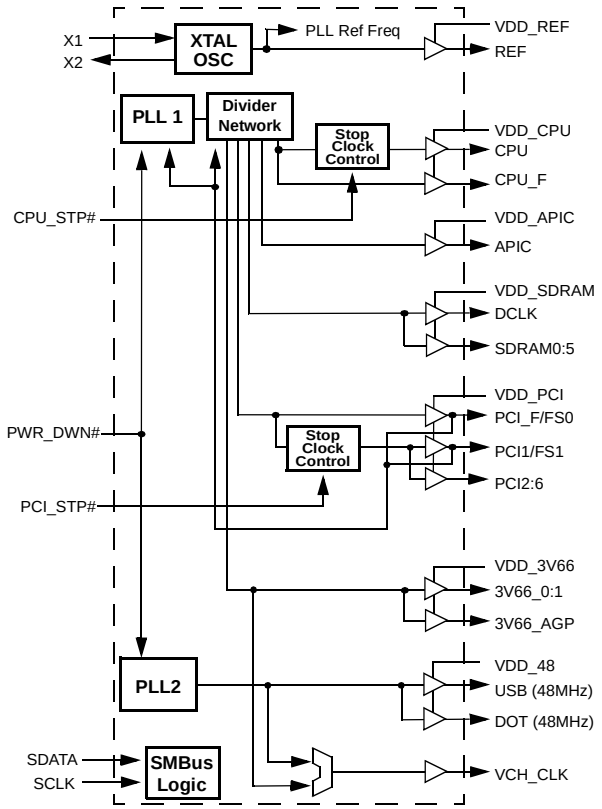
VDDQ3 (REF, PCI, 3V66, 48 MHz, SDRAM): .....3.3V±5%

VDDQ2 (CPU, APIC):..... 2.5V±5%in Selectable Frequency

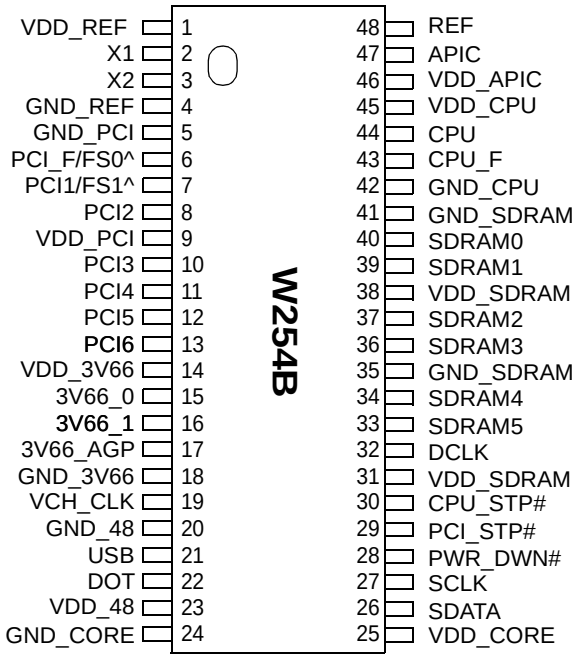
Table 1. Pin Selectable Frequency

Input Address		Output Frequencies						
FS1	FS0	CPU	SDRAM	48MHz	PCI	APIC	REF	3V66
0	0	66	100	48 MHz	33 MHz		14.318 MHz	66 MHz
0	1	100	100					
1	0	133	133					
1	1	133	100					

Block Diagram



Pin Configuration



Note:

1. Internal pull-down or pull-up resistors present on inputs marked with * or ^ respectively. Design should not rely solely on internal pull-up or pull-down resistor to set I/O pins HIGH or LOW respectively.

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU CPU_F	44, 43	O	***CPU Clock Outputs:*** Frequency is set by the FS0:1 inputs or through serial input interface. The CPU output is gated by the CLK_STOP# input.
PCI1:6, PCI_F/FS0, PCI1/FS1	8, 10, 11, 12, 13, 6, 7	I/O	***33-MHz PCI Outputs:*** Except for the PCI_F output, these outputs are gated by the PCI_STOP# input. Upon power up, FS0 and FS1 is configured momentarily as input latches allowing various output frequencies to be selected. See *Table 2*.
APIC	47	O	***APIC Output:*** 2.5V fixed 33.3-MHz clock. This output is synchronous to the CPU clock.
SDRAM0:5, DCLK	40, 39, 37, 36, 34, 33, 32	O	***SDRAM Output Clocks:*** 3.3V outputs running at either 100 MHz or 133 MHz depending on the setting of FS0:1 inputs. DCLK is a free-running clock.
3V66_0:1, 3V66_AGP	15, 16, 17	O	***66-MHz Clock Outputs:*** 3.3V fixed 66-MHz clock.
USB	21	O	***USB Clock Output:*** 3.3V fixed 48-MHz, non-spread spectrum USB clock output.
DOT	22	O	***Dot Clock Output:*** 3.3V fixed 48-MHz, non-spread spectrum signal.
REF	48	O	***Reference Clock:*** 3.3V 14.318-MHz clock output.
VCH_CLK	19	O	***Video Control Hub Clock Output:*** 3.3V selectable 48-MHz non-spread spectrum or 66.67-MHz spread spectrum clock output.
PWR_DWN#	28	I	***Power-Down Control:*** 3.3V LVTTL-compatible input that places the device in power-down mode when held LOW.
CPU_STP#	30	I	***CPU Output Control:*** 3.3V LVTTL-compatible input that stops only the CPU0 clock. Output remains in the LOW state.
PCI_STP#	29	I	***PCI Output Control:*** 3.3V LVTTL-compatible input that stops PCI1:6 clocks. Output remains in the LOW state.
SCLK	27	I	***SMBus Clock Input:*** Clock pin for SMBus circuitry.
SDATA	26	I/O	***SMBus Data Input:*** Data pin for SMBus circuitry.
X1	2	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.
X2	3	O	***Crystal Connection:*** Connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
VDD_REF, VDD_PCI, VDD _3V66, VDD_48, VDD_CORE, VDD_SDRAM, VDD_SDRAM	1, 9, 14, 23, 25, 31, 38	P	***3.3V Power Connection:*** Power supply for core logic, PLL circuitry, SDRAM outputs buffers, PCI output buffers, reference output buffers and 48-MHz output buffers. Connect to 3.3V.
VDD_APIC, VDD_CPU	45, 46	P	***2.5V Power Connection:*** Power for APIC and CPU output buffers. Connect to 2.5V.
GND_REF, GND_PCI, GND_3V66, GND_48, GND_CORE GND_SDRAM, GND_SDRAM, GND_CPU	4, 5, 18, 20, 24, 35, 41, 42	G	***Ground Connection:*** Connect all ground pins to the common system ground plane.

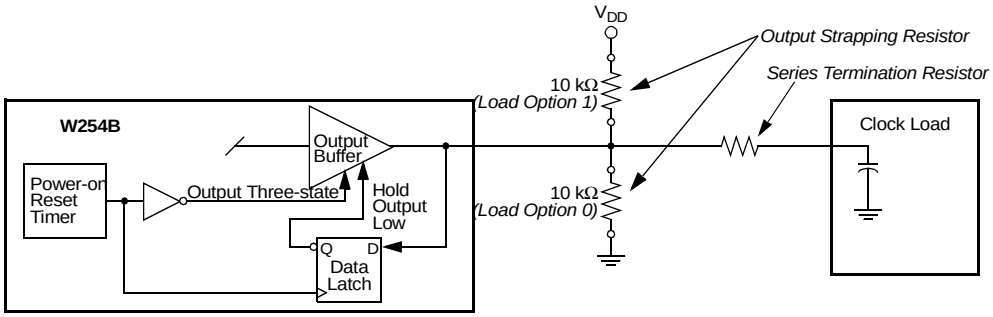


Figure 1. Input Logic Selection Through Resistor Load Option

Overview

The W254B is a highly integrated frequency timing generator, supplying all the required clock sources for an Intel® architecture platform using graphics-integrated core logic.

Functional Description

I/O Pin Operation

Pins 6 and 7 are dual-purpose I/O pins. Upon power-up these pins act as logic inputs, allowing the determination of assigned device functions. A short time after power-up, the logic state of each pin is latched and the pins then become clock outputs. This feature reduces device pin count by combining clock outputs with input select pins.

An external 10-kΩ "strapping" resistor is connected between each I/O pin and ground or VDDQ3. Connection to ground sets a latch to "0", connection to VDDQ3 sets a latch to "1". *Figure 1* shows one suggested method for strapping resistor connection.

Upon W254B power-up, the first 2 ms of operation is used for input logic selection. During this period, the PCI_F and PCI1 clock output buffers are three-stated, allowing the output strapping resistor on each I/O pin to pull the pin and its associated capacitive clock load to either a logic HIGH or logic LOW state. At the end of the 2-ms period, the established logic 0 or 1 condition of each I/O is pin is latched. Next the output buffers are enabled, converting all I/O pins into operating clock outputs. The 2-ms timer starts when VDDQ3 reaches 2.0V. The input bits can only be reset by turning VDDQ3 off and then back on again.

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of the clock output is 40Ω (nominal), which is minimally affected by the 10-kΩ strap to ground or VDDQ3. As with the series termination resistor, the output strapping resistor should be placed as close to the I/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or VDDQ3 should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

When the clock outputs are enabled following the 2-ms input period, target (normal) output frequency is delivered, assuming that VDDQ3 has stabilized. If VDDQ3 has not yet reached full value, output frequency initially may be below target but will increase to target once VDDQ3 voltage has stabilized. In either case, a short output clock cycle may be produced from the CPU clock outputs when the outputs are enabled.

CPU/ SDRAM Frequency Selection

CPU output frequency is selected with I/O pins 6 and 7. For CPU/SDRAM frequency programming information refer to *Table 2*. Alternatively, frequency selections are available through the serial data interface.

Table 2. Frequency Select Truth Table[2]

Input Address		Output Frequencies						
FS1	**FS0**	**CPU**	**SDRAM**	**48 MHz**[3]	**PCI**	**APIC**	**REF**	**3V66**
0	0	66	100	48 MHz	33 MHz		14.318 MHz	66 MHz
0	1	100	100					
1	0	133	133					
1	1	133	100					

Notes:
2. Range of reference frequency allowed is min. = 14.316 MHz, nominal = 14.31818 MHz, max. = 14.32 MHz.
3. Frequency accuracy of 48 MHz must be +167 PPM to match USB default.

Offsets Among Clock Signal Groups

Figure 2 and *Figure 3* represent the phase relationship among the different groups of clock outputs from W254B when it is providing a 66-MHz CPU clock and a 100-MHz CPU clock, respectively. It should be noted that when CPU clock is operating at 100 MHz, CPU clock output is 180 degrees out of phase with SDRAM clock outputs.

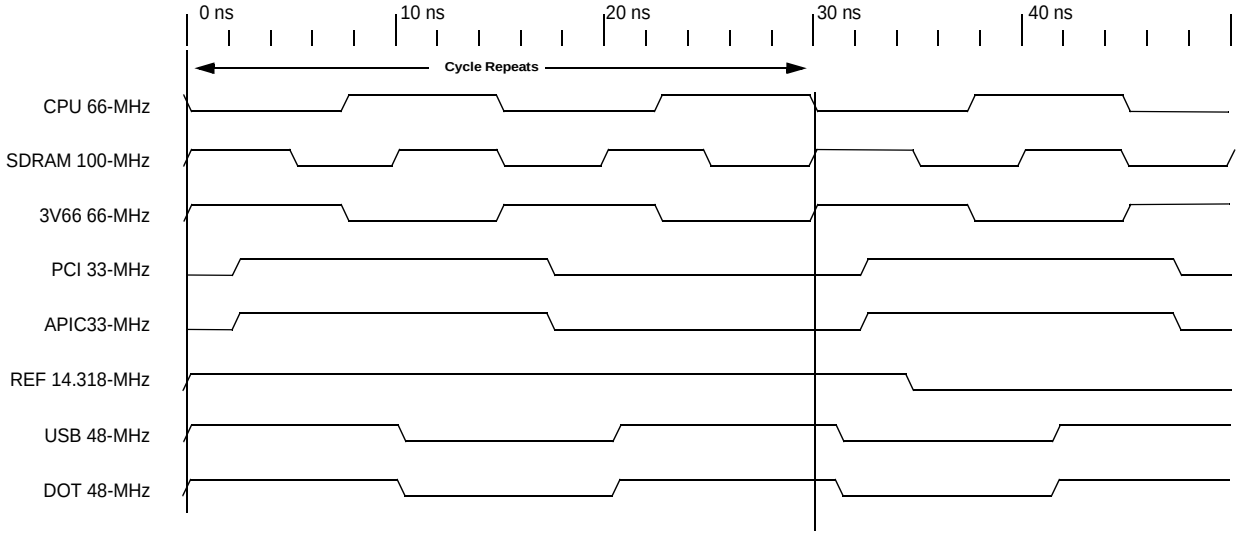


Figure 2. Group Offset Waveforms (66 Mhz CPU/100 MHz SDRAM Clock)

Table 3. 66 MHz Group Timing Relationships and Tolerances

	CPU to SDRAM	CPU to 3V66	SDRAM to 3V66	3V66 to PCI	PCI to APIC	USB & DOT
Offset	–2.5 ns	7.5 ns	0.0 ns	1.5-3.5 ns	0.0 ns	Async
Tolerance	500 ps	500 ps	500 ps	500 ps	1.0 ns	N/A

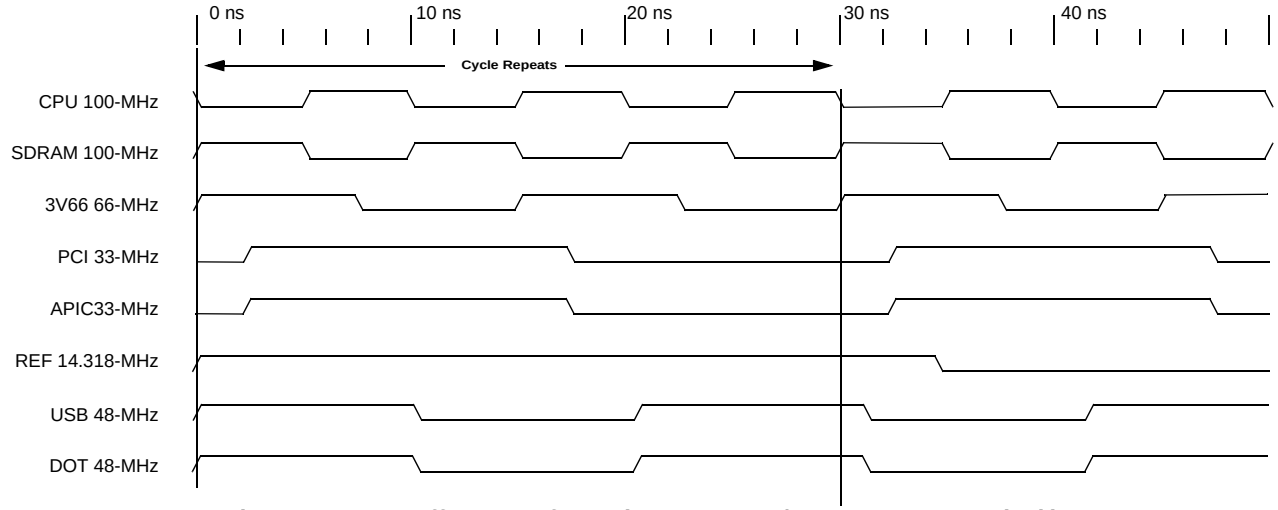


Figure 3. Group Offset Waveforms (100 MHz CPU/100 MHz SDRAM Clock)

Table 4. 100 MHz Group Timing Relationships and Tolerances

	CPU to SDRAM	CPU to 3V66	SDRAM to 3V66	3V66 to PCI	PCI to APIC	USB & DOT
Offset	5.0 ns	5.0ns	0.0 ns	1.5-3.5 ns	0.0 ns	Async
Tolerance	500 ps	500 ps	500 ps	500 ps	1.0 ns	N/A

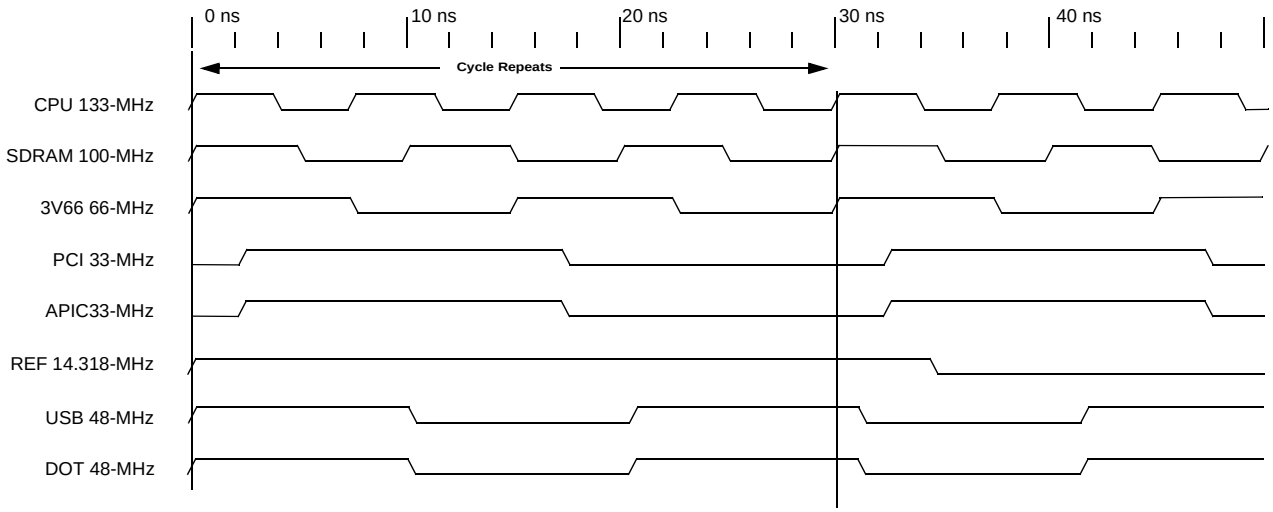


Figure 4. Group Offset Waveforms (133-MHz CPU/100-MHz SDRAM Clock)

Table 5. 133 MHz/SDRAM 100 MHz Group Timing Relationships and Tolerances

	CPU to SDRAM	CPU to 3V66	SDRAM to 3V66	3V66 to PCI	PCI to APIC	USB & DOT
Offset	0.0 ns	0.0 ns	0.0 ns	1.5-3.5 ns	0.0 ns	Async
Tolerance	500 ps	500 ps	500 ps	500 ps	1.0 ns	N/A

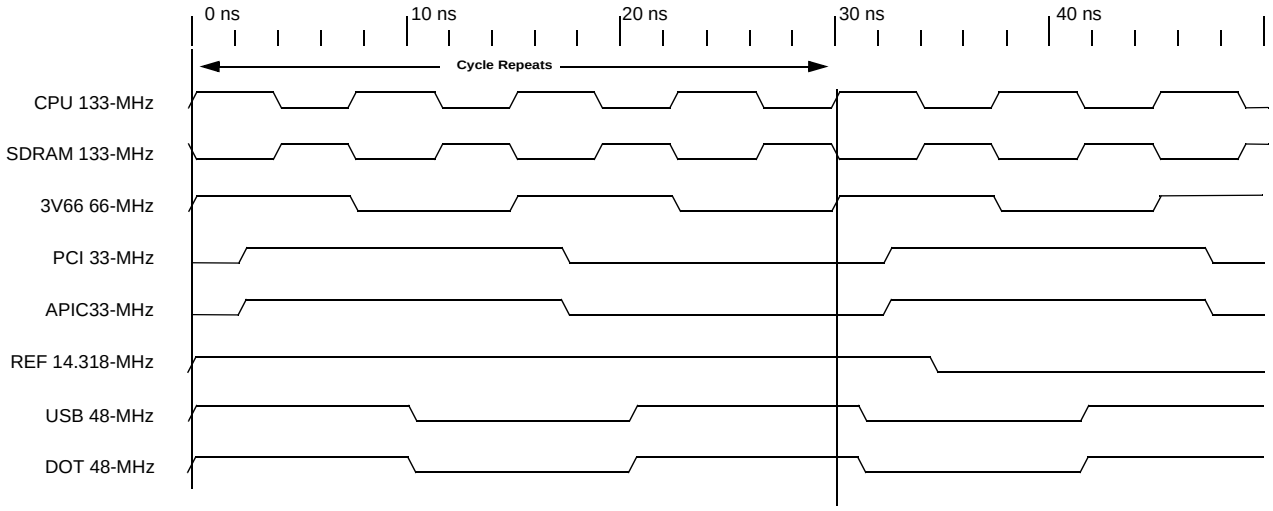


Figure 5. Group Offset Waveforms (133-MHz CPU/133-MHz SDRAM Clock)

Table 6. 133 MHz/SDRAM Test Mode Group Timing Relationships and Tolerance

	CPU to SDRAM	CPU to 3V66	SDRAM to 3V66	3V66 to PCI	PCI to APIC	USB& DOT
Offset	3.75 ns	0.0 ns	3.75 ns	1.5-3.5 ns	0.0 ns	Async
Tolerance	500 ps	500 ps	500 ps	500 ps	1.0 ns	N/A

Power-Down Control

W254B provides one PWR_DWN# signal to place the device in low-power mode. In low-power mode, the PLLs are turned off and all clock outputs are driven LOW.

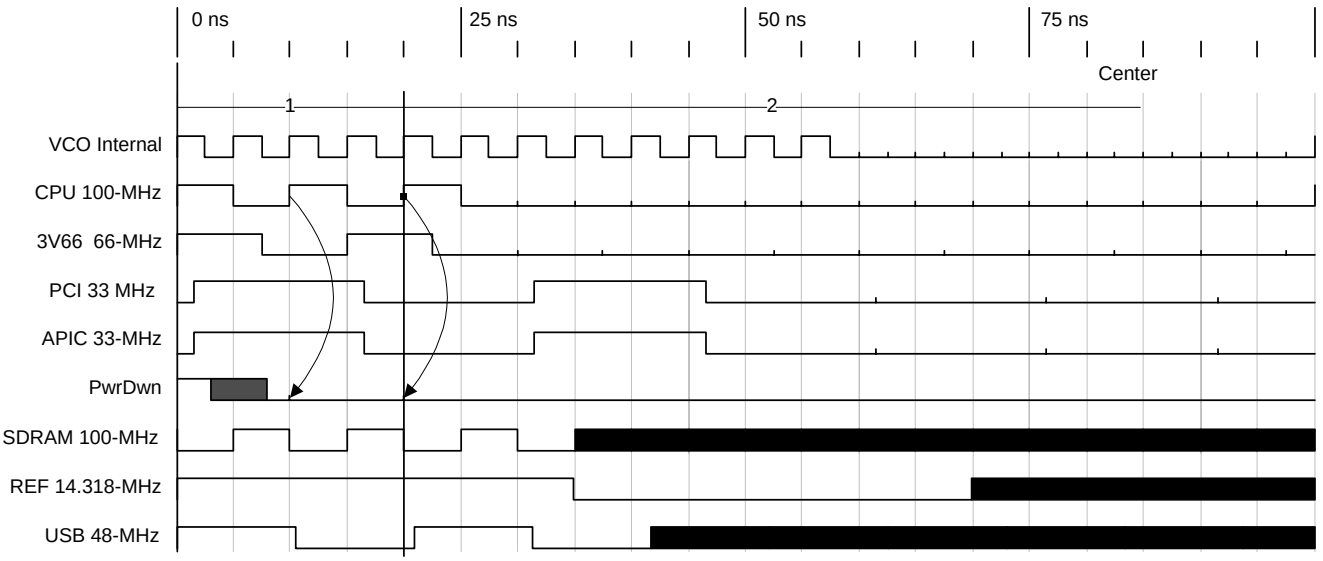


Figure 6. W254B PWR_DWN# Timing Diagram[4, 5, 6, 7]

Table 7. W254B Maximum Allowed Current

W254B Condition	Max. 2.5V supply consumption Max. discrete cap loads, V_{DDQ2} = 2.625V All static inputs = V_{DDQ3} or V_{SS}	Max. 3.3V supply consumption Max. discrete cap loads V_{DDQ3} = 3.465V All static inputs = V_{DDQ3} or V_{SS}
Powerdown Mode (PWR_DWN# = 0)	$\leq$ 1 mA	$\leq$ 1 mA
Full Active 66 MHz FS1:0 = 00 (PWR_DWN# =1)	70 mA	280 mA
Full Active 100 MHz FS1:0 = 01 (PWR_DWN# =1)	100 mA	280 mA
Full Active 133 MHz FS1:0 = 11 (PWR_DWN# =1)	100 mA	280 mA

Notes:

4. Once the PWR_DWN# signal is sampled LOW for two consecutive rising edges of CPU, clocks of interest will be held LOW on the next HIGH-to-LOW transition.
5. PWR_DWN# is an asynchronous input and metastable conditions could exist. This signal is synchronized inside W254B.
6. The shaded sections on the SDRAM, REF, and USB clocks indicate “Don’t Care” states.
7. Diagrams shown with respect to 100 MHz. Similar operation when CPU is 66 MHz.

Spread Spectrum Frequency Timing Generation

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 7*.

As shown in *Figure 7*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is:

$$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$$

Where *P* is the percentage of deviation and *F* is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 8*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin, produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is ±0.5% or –0.5% of the selected frequency. *Figure 8* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

Spread Spectrum clocking is activated or deactivated by selecting the appropriate value for bit 3 in data byte 0 of the SMBus data stream. Refer to page 9 for more details.

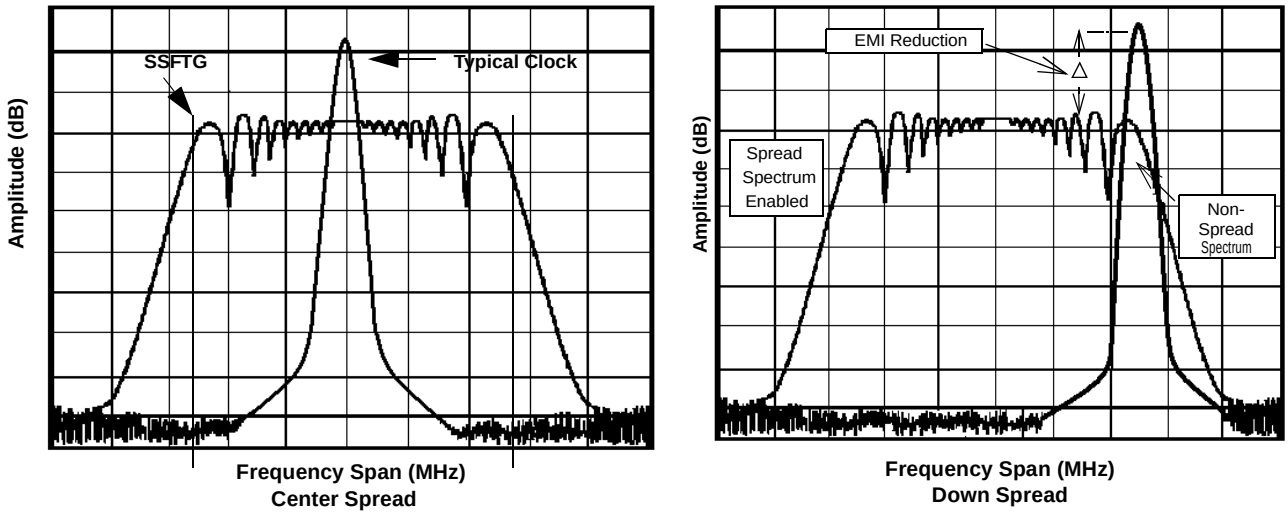


Figure 7. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation

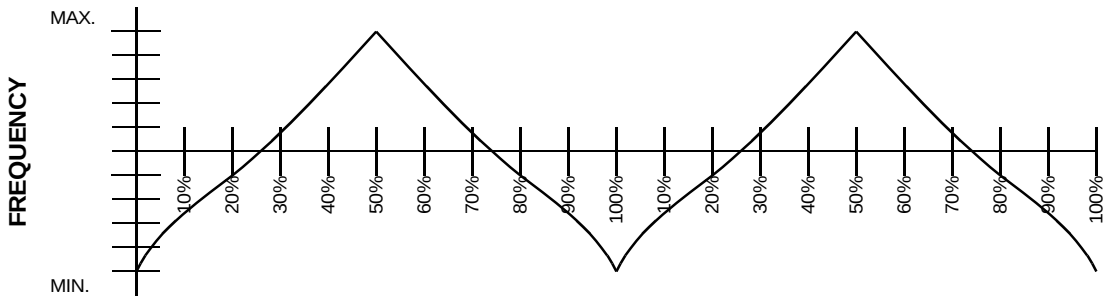


Figure 8. Typical Modulation Profile

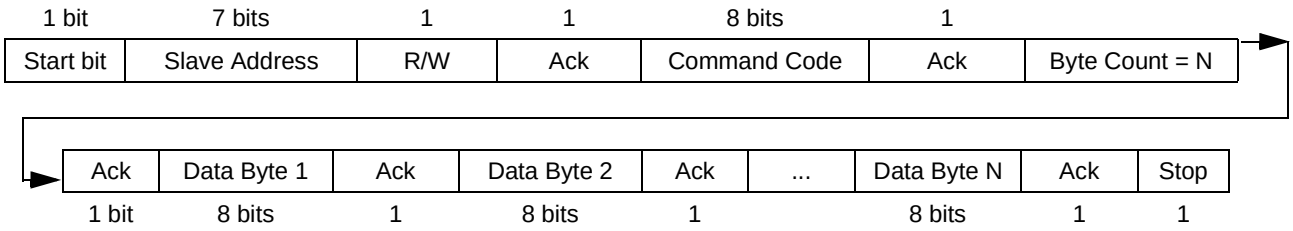


Figure 9. An Example of a Block Write[8]

Serial Data Interface

The W254B features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions.

Data Protocol

The clock driver serial protocol accepts only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. Indexed bytes are not allowed.

A block write begins with a slave address and a write condition. After the command code the core logic issues a byte count which describes how many more bytes will follow in the message. If the host had 20 bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count may not be 0. A block write command is allowed to transfer a maximum of 32 data bytes. The slave receiver address for W254B is 11010010. *Figure 9* shows an example of a block write.

The command code and the byte count bytes are required as the first two bytes of any transfer. W254B expects a command code of 0000 0000. The byte count byte is the number of additional bytes required for the transfer, not counting the command code and byte count bytes. Additionally, the byte count byte is required to be a minimum of 1 byte and a maximum of 32 bytes to satisfy the above requirement. *Table 8* shows an example of a possible byte count value.

A transfer is considered valid after the acknowledge bit corresponding to the byte count is read by the controller. The command code and byte count bytes are ignored by the W254B. However, these bytes must be included in the data write sequence to maintain proper byte allocation.

Table 8. Example of Possible Byte Count Value

Byte Count Byte		Notes
MSB	LSB	
0000	0000	Not allowed. Must have at least one byte
0000	0001	Data for functional and frequency select register (currently byte 0 in spec)
0000	0010	Writes first two bytes of data (byte 0 then byte 1)
0000	0011	Writes first three bytes (byte 0, 1, 2 in order)
0000	0100	Writes first four bytes (byte 0, 1, 2, 3 in order)
0000	0101	Writes first five bytes (byte 0, 1, 2, 3, 4 in order)
0000	0110	Writes first six bytes (byte 0, 1, 2, 3, 4, 5 in order)
0000	0111	Writes first seven bytes (byte 0, 1, 2, 3, 4, 5, 6 in order)
0010	0000	Max. byte count supported = 32

Note:
8. The acknowledgment bit is returned by the slave/receiver (W254B).

W254B Serial Configuration Map

1. The serial bits will be read by the clock driver in the following order:

   Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

   Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

   Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

2. All unused register bits (reserved and N/A) should be written to a “0” level.
3. All register bits labeled “Initialize to 0" must be written to zero during initialization. Failure to do so may result in higher than normal operating current.

Byte 0: Control Register (1 = Enable, 0 = Disable)[9]

Bit	Pin#	Name	Pin Description
Bit 7	19	VCH_CLK	(Active/Inactive)
Bit 6	--	Reserved Drive to ’0’	(Active/Inactive)
Bit 5	43	CPU_F	(Disabled/Enabled)
Bit 4	44	CPU	(Disabled/Enabled)
Bit 3	--	Spread Spectrum (1 = On; 0 = Off)	(Active/Inactive)
Bit 2	22	DOT (48 MHz)	(Disabled/Enabled)
Bit 1	21	USB (48 MHz)	(Disabled/Enabled)
Bit 0	--	Reserved Drive to ’0’	(Active/Inactive)

Byte 1: Control Register (1 = Enable, 0 = Disable)[9]

Bit	Pin#	Name	Pin Description
Bit 7	--	Reserved Drive to ’0’	(Active/Inactive)
Bit 6	--	Reserved Drive to ’0’	(Active/Inactive)
Bit 5	33	SDRAM5	(Disabled/Enabled)
Bit 4	34	SDRAM4	(Disabled/Enabled)
Bit 3	36	SDRAM3	(Disabled/Enabled)
Bit 2	37	SDRAM2	(Disabled/Enabled)
Bit 1	39	SDRAM1	(Disabled/Enabled)
Bit 0	40	SDRAM0	(Disabled/Enabled)

Byte 2: Control Register (1 = Enable, 0 = Disable)[9]

Bit	Pin#	Name	Pin Description
Bit 7	17	3V66_AGP	(Disabled/Enabled)
Bit 6	16	3V66_1	(Disabled/Enabled)
Bit 5	15	3V66_0	(Disabled/Enabled)
Bit 4	--	Reserved Drive to ’0’	(Active/Inactive)
Bit 3	--	Reserved Drive to ’0’	(Active/Inactive)
Bit 2	--	Reserved Drive to ’0’	(Active/Inactive)
Bit 1	--	Reserved Drive to ’0’	(Active/Inactive)
Bit 0	--	Reserved Drive to ’0’	(Active/Inactive)

Note:

9. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.

Byte 3: Control Register (1 = Enable, 0 = Disable)

Bit	Pin#	Name	Pin Description
Bit 7	-	Reserved Drive to ’0’	(Active/Inactive)
Bit 6	13	PCI6	(Disabled/Enabled)
Bit 5	12	PCI5	(Disabled/Enabled)
Bit 4	11	PCI4	(Disabled/Enabled)
Bit 3	10	PCI3	(Disabled/Enabled)
Bit 2	8	PCI2	(Disabled/Enabled)
Bit 1	7	PCI1/FS1	(Disabled/Enabled)
Bit 0	--	SDRAM 133-MHz Mode Enable	Default is Disabled = ‘0’, Enabled = ’1’

Byte 4: Control Register (1 = Enable, 0 = Disable)

Bit	Pin#	Name	Pin Description
Bit 7	19	VCH_CLK SSC Mode 0 = 48 MHz non-SSC (default) 1 = 66 MHz SSC	(Disabled/Enabled)
Bit 6	-	Reserved Drive to ’0’	(Active/Inactive)
Bit 5	-	Reserved Drive to ’0’	(Active/Inactive)
Bit 4	-	Reserved Drive to ’0’	(Active/Inactive)
Bit 3	-	Reserved Drive to ’0’	(Active/Inactive)
Bit 2	-	Reserved Drive to ’0’	(Active/Inactive)
Bit 1		Reserved Drive to ’0’	(Active/Inactive)
Bit 0	-	Reserved Drive to ’0’	(Active/Inactive)

Byte 5: Control Register (1 = Enable, 0 = Disable)

Bit	Pin#	Name	Pin Description
Bit 7	-	Reserved Drive to ‘0’	(Active/Inactive)
Bit 6	-	Spread Spectrum and Overclocking Mode Select. See *Table 9*	(Active/Inactive)
Bit 5	-		(Active/Inactive)
Bit 4	-	Reserved Drive to ’0’	(Active/Inactive)
Bit 3	-	Reserved Drive to ’0’	(Active/Inactive)
Bit 2	-	Reserved Drive to ’0’	(Active/Inactive)
Bit 1		Reserved Drive to ‘0’	(Active/Inactive)
Bit 0	-	Reserved Drive to ‘0’	(Active/Inactive)

Byte 5 has been provided as an optional register to enable a greater degree of spread spectrum and overclocking performance for all PLL1 outputs. (CPU, SDRAM, DCLK, APIC, PCI, 3V66 and VCH_CLK)

By enabling Byte 5, (bits 5 and 6) spread spectrum can be increased to $\pm$0.5% and /or overclocking of either 5%, 10% or 15% can be enabled.

It is not necessary to access Byte 5 if these additional features are not implemented. All outputs will default to 0% overclocking upon power up, with either 0% or –0.5% spread spectrum.

Table 9. Spread Spectrum and Overclocking Mode Select

Byte 0	Byte 5				
Bit 3	**Bit 5**	**Bit 6**	**SS %**	**Overclock %**	**Description and Comments**
Spread Spectrum ON	0	0	–0.5%	0%	No overclocking (Default)
	0	1	±0.5%	0%	No overclocking
	1	0	–0.5%	5% [10]	
	1	1	±0.5%	5% [10]	
Spread Spectrum OFF	0	0	-	0%	No overclocking
	0	1	-	10% [10]	
	1	0	-	5% [10]	
	1	1	-	15% [10]	

Note:
10. Overclocking not tested; characterized at room temperature only. Base Frequency determined through hardware select pins, FS0 & FS1.

DC Electrical Characteristics

Absolute Maximum DC Power Supply

Parameter	Description	Min.	Max.	Unit
V_{DD3}	3.3V Core Supply Voltage	–0.5	4.6	V
V_{DDQ2}	2.5V I/O Supply Voltage	–0.5	3.6	V
V_{DDQ3}	3.3V Supply Voltage	–0.5	4.6	V
T_S	Storage Temperature	–65	150	°C

Absolute Maximum DC I/O

Parameter	Description	Min.	Max.	Unit
V_{ih3}	3.3V Input High Voltage	–0.5	4.6	V
V_{il3}	3.3V Input Low Voltage	–0.5		V
ESD prot.	Input ESD Protection	2000		V

DC Operating Requirements

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD3}	3.3V Core Supply Voltage	3.3V±5%	3.135	3.465	V
V_{DDQ3}	3.3V I/O Supply Voltage	3.3V±5%	3.135	3.465	V
V_{DDQ2}	2.5V I/O Supply Voltage	2.5V±5%	2.375	2.625	V
V_{DD3} = 3.3V±5%					
V_{ih3}	3.3V Input High Voltage	V_{DD3}	2.0	V_{DD} + 0.3	V
V_{il3}	3.3V Input Low Voltage		V_{SS} – 0.3	0.8	V
I_{il}	Input Leakage Current[11]	$0<V_{in}<V_{DD3}$	–5	+5	µA
V_{DDQ2} = 2.5V±5%					
V_{oh2}	2.5V Output High Voltage	I_{oh} = (–1 mA)	2.0		V
V_{ol2}	2.5V Output Low Voltage	I_{ol} = (1 mA)		0.4	V
V_{DDQ3} = 3.3V±5%					
V_{oh3}	3.3V Output High Voltage	I_{oh} = (–1 mA)	2.4		V
V_{ol3}	3.3V Output Low Voltage	I_{ol} = (1 mA)		0.4	V
V_{DDQ3} = 3.3V±5%					
V_{poh3}	PCI Bus Output High Voltage	I_{oh} = (–1 mA)	2.4		V
V_{pol3}	PCI Bus Output Low Voltage	I_{ol} = (1 mA)		0.55	V
C_{in}	Input Pin Capacitance			5	pF
C_{xtal}	Xtal Pin Capacitance		13.5	22.5	pF
C_{out}	Output Pin Capacitance			6	pF
L_{pin}	Pin Inductance		0	7	nH
T_a	Ambient Temperature	No Airflow	0	70	°C

Note:
11. Input Leakage Current does not include inputs with pull-up or pull-down resistors.

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2}= 2.5V±5% f_{XTL} = 14.31818 MHz Spread Spectrum Function Turned Off

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.[12]

AC Electrical Characteristics

Parameter	Description	66.6-MHz Host		100-MHz Host		133-MHz Host		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
T_{Period}	Host/CPUCLK Period	15.0	15.5	10.0	10.5	7.5	8.0	ns	12
T_{HIGH}	Host/CPUCLK High Time	5.2	N/A	3.0	N/A	1.87	N/A	ns	13
T_{LOW}	Host/CPUCLK Low Time	5.0	N/A	2.8	N/A	1.67	N/A	ns	14
T_{RISE}	Host/CPUCLK Rise Time	0.4	1.6	0.4	1.6	0.4	1.6	ns	
T_{FALL}	Host/CPUCLK Fall Time	0.4	1.6	0.4	1.6	0.4	1.6	ns	
T_{Period}	SDRAM CLK Period (100-MHz)	10.0	10.5	10.0	10.5	10.0	10.5	ns	12
T_{HIGH}	SDRAM CLK High Time (100-MHz)	3.0	N/A	3.0	N/A	3.0	N/A	ns	13
T_{LOW}	SDRAM CLK Low Time (100-MHz)	2.8	N/A	2.8	N/A	2.8	N/A	ns	14
T_{RISE}	SDRAM CLK Rise Time (100-MHz)	0.4	1.6	0.4	1.6	0.4	1.6	ns	
T_{FALL}	SDRAM CLK Fall Time (100-MHz)	0.4	1.6	0.4	1.6	0.4	1.6	ns	
T_{Period}	APIC 33-MHz CLK Period	30.0	N/A	30.0	N/A	30.0	N/A	ns	12, 15
T_{HIGH}	APIC 33-MHz CLK High Time	12.0	N/A	12.0	N/A	12.0	N/A	ns	13
T_{LOW}	APIC 33-MHz CLK Low Time	12.0	N/A	12.0	N/A	12.0	N/A	ns	14
T_{RISE}	APIC CLK Rise Time	0.4	1.6	0.4	1.6	0.4	1.6	ns	
T_{FALL}	APIC CLK Fall Time	0.4	1.6	0.4	1.6	0.4	1.6	ns	
T_{Period}	3V66 CLK Period	15.0	16.0	15.0	16.0	15.0	16.0	ns	12, 16
T_{HIGH}	3V66 CLK High Time	5.25	N/A	5.25	N/A	5.25	N/A	ns	13
T_{LOW}	3V66 CLK Low Time	5.05	N/A	5.05	N/A	5.05	N/A	ns	14
T_{RISE}	3V66 CLK Rise Time	0.5	2.0	0.5	2.0	0.5	2.0	ns	
T_{FALL}	3V66 CLK Fall Time	0.5	2.0	0.5	2.0	0.5	2.0	ns	
T_{Period}	PCI CLK Period	30.0	N/A	30.0	N/A	30.0	N/A		12, 16
T_{HIGH}	PCI CLK High Time	12.0	N/A	12.0	N/A	12.0	N/A		13
T_{LOW}	PCI CLK Low Time	12.0	N/A	12.0	N/A	12.0	N/A		14
T_{RISE}	PCI CLK Rise Time	0.5	2.0	0.5	2.0	0.5	2.0		
T_{FALL}	PCI CLK Fall Time	0.5	2.0	0.5	2.0	0.5	2.0		
tp_{ZL}, tp_{ZH}	Output Enable Delay (All outputs)	30.0	N/A	30.0	N/A	30.0	N/A	ns	
tp_{LZ}, tp_{ZH}	Output Disable Delay (All outputs)	12.0	N/A	12.0	N/A	12.0	N/A	ns	
t_{stable}	All Clock Stabilization from Power-Up	12.0	N/A	12.0	N/A	12.0	N/A	ms	

Notes:

12. Period, jitter, offset, and skew measured on rising edge at 1.25 for 2.5V clocks and at 1.5V for 3.3V clocks.
13. The time specified is measured from when V_{DDQ3} achieves its nominal operating level (typical condition V_{DDQ3} = 3.3V) until the frequency output is stable and operating within specification.
14. T_{RISE} and T_{FALL} are measured as a transition through the threshold region V_{ol} = 0.4V and V_{oh} = 2.0V (1 mA) JEDEC specification.
15. T_{LOW} is measured at 0.4V for all outputs.
16. T_{HIGH} is measured at 2.0V for 2.5V outputs, 2.4V for 3.3V outputs.

Group Skew and Jitter Limits

Output Group	Pin-Pin Skew Max.	Cycle-Cycle Jitter	Duty Cycle	Nom Vdd	Skew, Jitter Measure Point
CPU	150 ps	250 ps	45/55	2.5V	1.25V
SDRAM	250 ps	250 ps	45/55	3.3V	1.5V
APIC	250 ps	500 ps	45/55	2.5V	1.25V
48MHz	N/A	500 ps	45/55	3.3V	1.5V
3V66	175 ps	500 ps	45/55	3.3V	1.5V
PCI	500 ps	500 ps	45/55	3.3V	1.5V
REF	N/A	1000 ps	45/55	3.3V	1.5V
VCH_CLK	N/A	250 ps	45/55	3.3V	1.5V

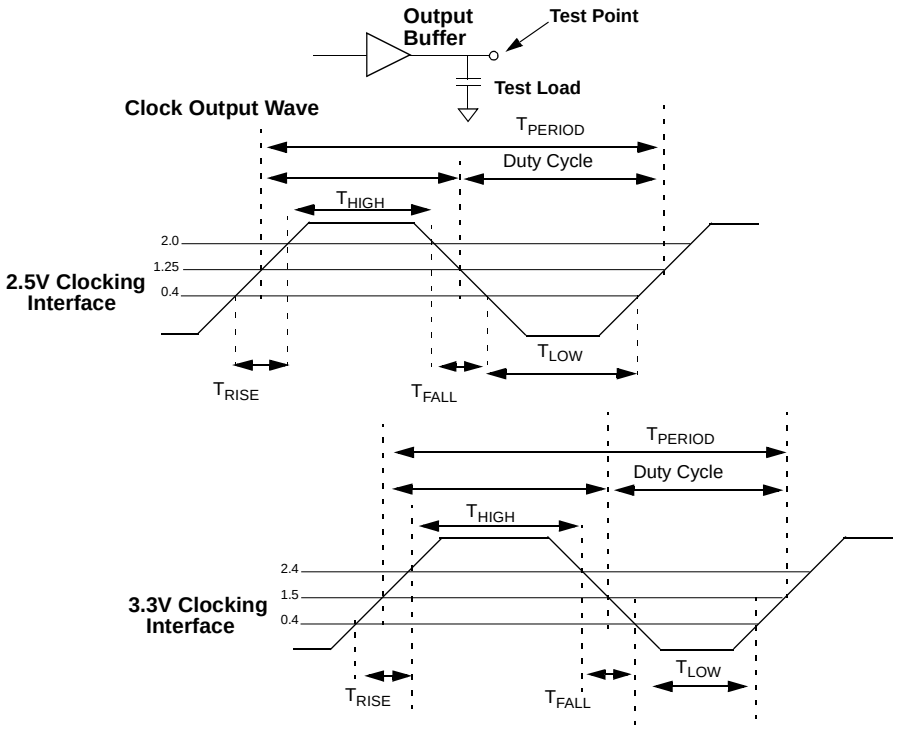
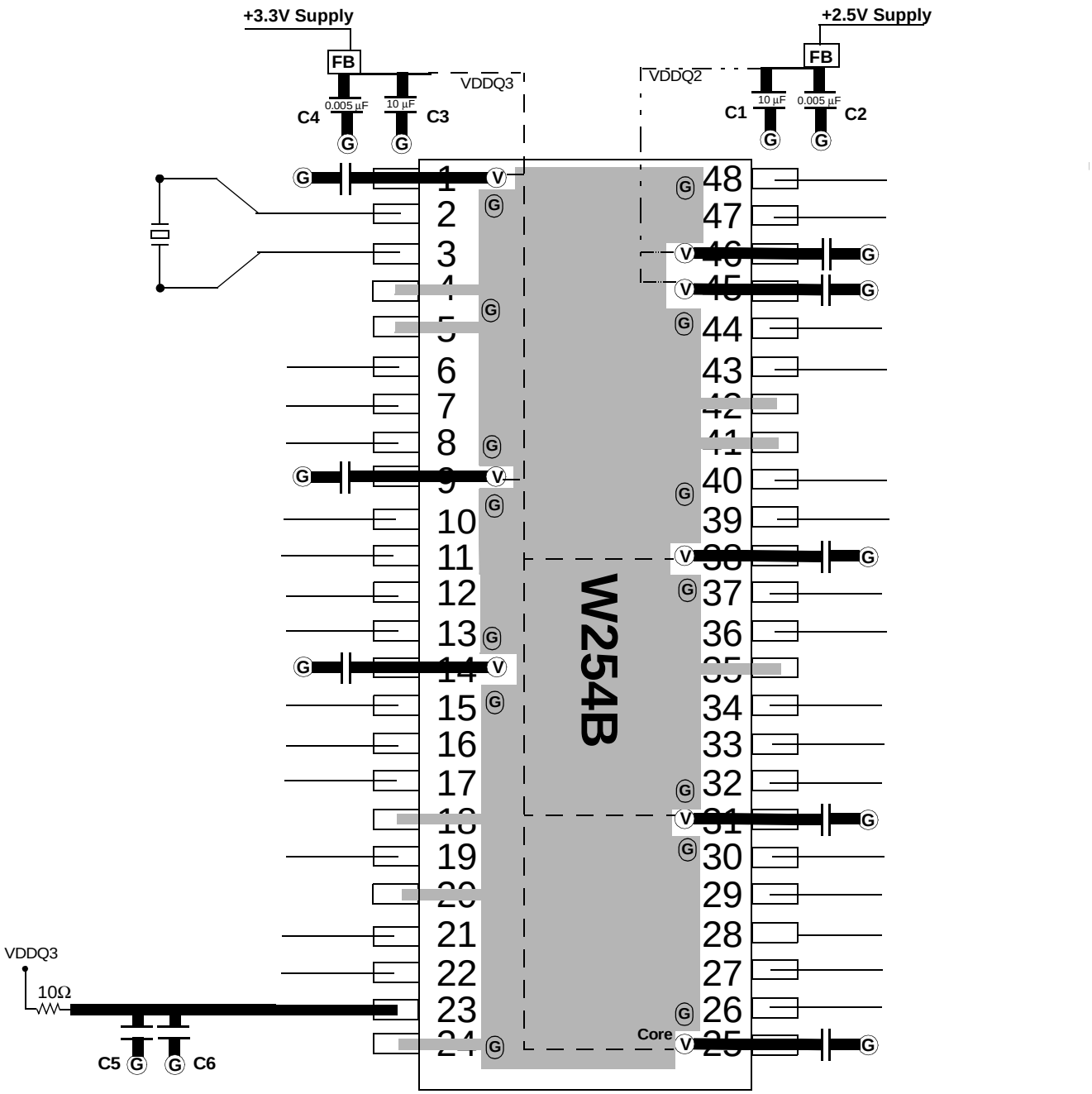


Figure 10. Output Buffer

Ordering Information

Ordering Code	Package Name	Package Type
W254B	X	48-pin TSSOP (6.1 mm)

Layout Diagram



FB = Dale ILB1206 - 300 (300Ω @ 100 MHz)

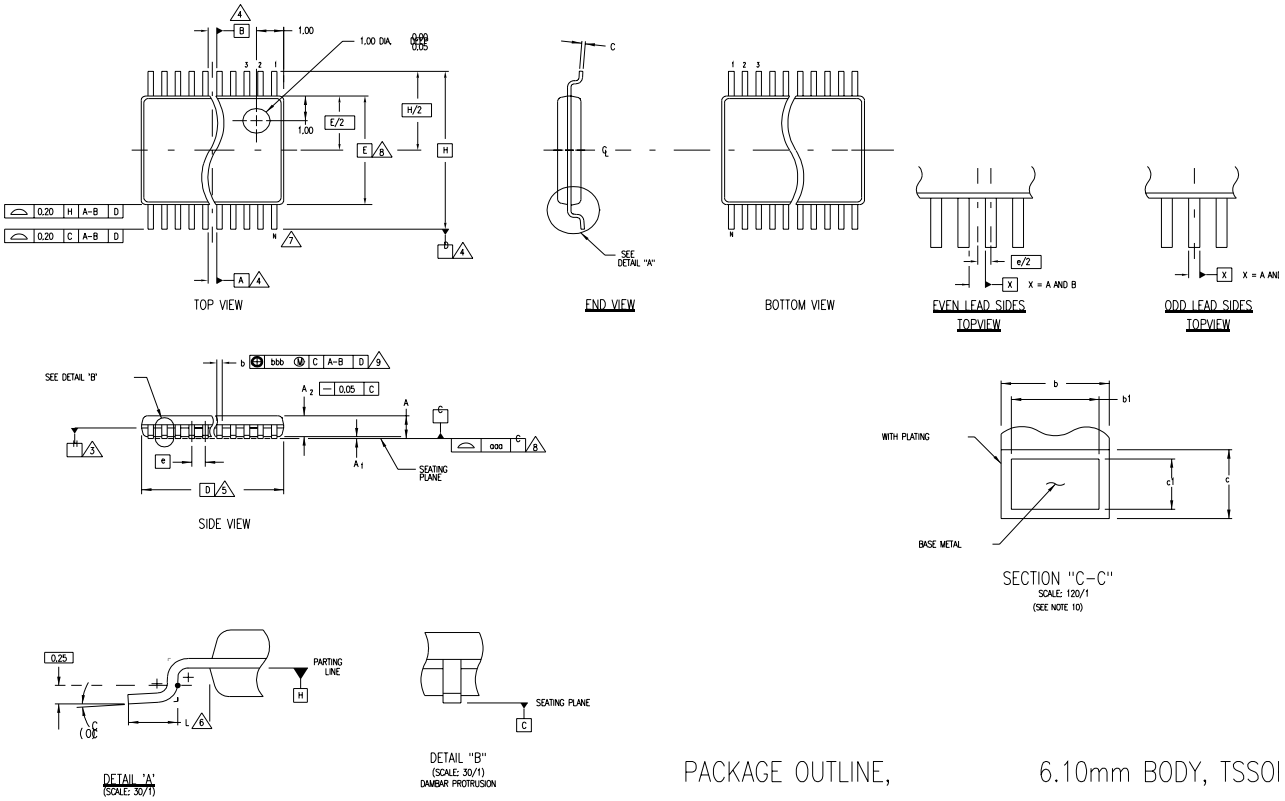
Ceramic Caps C1, C3 & C5 = 10–22 µF C2 & C4 = 0.005 µF C6 = 0.1 µF

G = VIA to GND plane layer V =VIA to respective supply plane layer

Note: Each supply plane or strip should have a ferrite bead and capacitors

Package Diagram

48-Pin Thin Shrink Small Outline Package (TSSOP, 6.1 mm)



PACKAGE OUTLINE, 6.10mm BODY, TSSOI

THIS TABLE FOR 0.50mm PITCH

SYMBOL	COMMON DIMENSIONS			NOTE	VARIATIONS	D			N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	——	——	1.10		ED	12.40	12.50	12.60	48
A_1	0.05	——	0.15		EE	13.90	14.00	14.10	56
A_2	0.80	1.00	1.05		EF*	16.90	17.00	17.10	64
aaa		0.10							
b	0.17	-	0.27	9					
b1	0.17	0.20	0.23						
bbb		0.08							
c	0.09	-	0.20						
c1	0.09	0.127	0.16						
D	SEE VARIATIONS			5					
E	6.00	6.10	6.20	5					
e	0.50 BSC								
H	8.10 BSC								
L	0.50	0.60	0.75	6					
N	SEE VARIATIONS			7					
α	0	——	8						

*DESIGNED BUT NOT TOOLED

ALL DIMENSIONS IN MILLIMETERS

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.279±0.127 (.011)DIE THICKNESS ALLOWABLE IS 0.279±0.005 INCHES)
2. DIMENSIONING & TOLERANCES PER ASME. Y14.5M-1994.
3. DATUM PLANE H LOCATED AT MOLD PARTING LINE AND CONCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
4. DATUMS A-B AND D TO BE DETERMINED WHERE CENTERLINE BETWEEN LEADS EXITS PLASTIC BODY AT DATUM PLANE H.
5. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE BOTTOM PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm ON D AND 0.25mm ON E PER SIDE.
6. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.076mm AT SEATING PLANE.
9. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND AN ADJACENT LEAD TO BE 0.10MM FOR 0.65MM PITCH, 0.08MM FOR 0.50MM PITCH AND 0.07MM FOR 0.40MM PITCH PACKAGES.
10. SEE DETAIL 'B' AND SECTION "C-C". SECTION "C-C" TO BE DETERMINED AT 0.10 TO 0.25 MM FROM THE LEAD TIP.
11. CONTROLLING DIMENSION: MILLIMETERS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-153, VARIATIONS DB, DC, DE, ED, EE, AND FE.

Document Title: W254B 133-MHz Spread Spectrum FTG for Mobile Pentium® III Platforms Document Number: 38-07233				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110498	11/07/01	SZV	Change from Spec number: 38-00927 to 38-07233