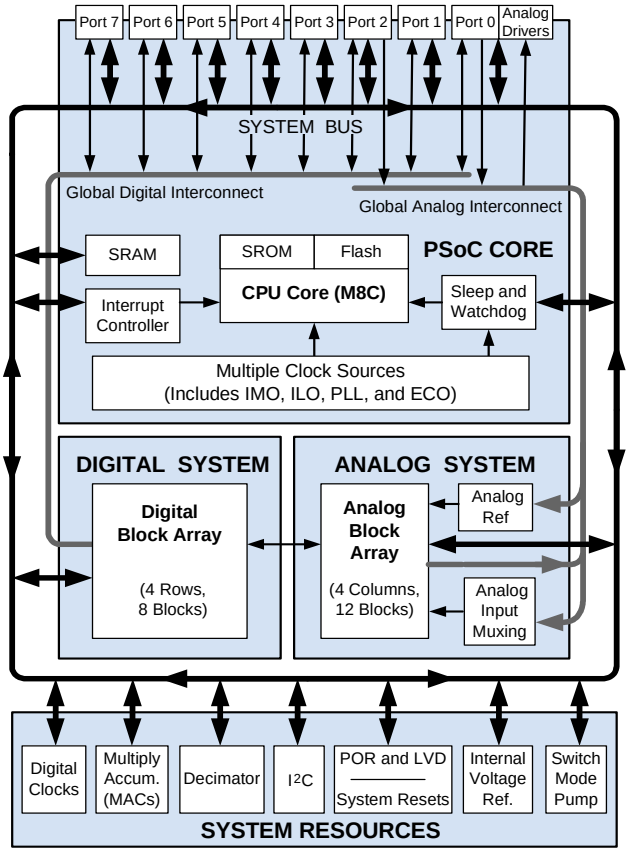
CY8C27466, CY8C27566, CY8C27666, and CY8C27866

Features

- **Powerful Harvard Architecture Processor**
  - M8C Processor Speeds to 24 MHz
  - 8x8 Multiply, 32-Bit Accumulate
  - Low Power at High Speed
  - 3.0 to 5.25 V Operating Voltage
  - Operating Voltages Down to 1.0V Using On-Chip Switch Mode Pump (SMP)
  - Industrial Temperature Range: -40°C to +85°C
- **Advanced Peripherals (PSoC Blocks)**
  - 12 Rail-to-Rail Analog PSoC Blocks Provide:
    - Up to 14-Bit ADCs
    - Up to 9-Bit DACs
    - Programmable Gain Amplifiers
    - Programmable Filters and Comparators
  - 8 Digital PSoC Blocks Provide:
    - 8- to 32-Bit Timers, Counters, and PWMs
    - CRC and PRS Modules
    - Up to 4 Full-Duplex UARTs
    - Multiple SPI™ Masters or Slaves
    - Connectable to all GPIO Pins
  - Complex Peripherals by Combining Blocks
- **Precision, Programmable Clocking**
  - Internal ±2.5% 24/48 MHz Oscillator
  - 24/48 MHz with Optional 32 kHz Crystal
  - Optional External Oscillator, up to 24 MHz
  - Internal Oscillator for Watchdog and Sleep
- **Flexible On-Chip Memory**
  - 32K Bytes Flash Program Storage 50,000 Erase/Write Cycles
  - 2K Bytes SRAM Data Storage
  - In-System Serial Programming (ISSP™)
  - Partial Flash Updates
  - Flexible Protection Modes
  - EEPROM Emulation in Flash
- **Programmable Pin Configurations**
  - 25 mA Sink on all GPIO
  - Pull up, Pull down, High Z, Strong, or Open Drain Drive Modes on all GPIO
  - Up to 12 Analog Inputs on GPIO
  - Four 40 mA Analog Outputs on GPIO
  - Configurable Interrupt on all GPIO
- **Additional System Resources**
  - I²C™ Slave, Master, and Multi-Master to 400 kHz
  - Watchdog and Sleep Timers
  - User-Configurable Low Voltage Detection
  - Integrated Supervisory Circuit
  - On-Chip Precision Voltage Reference
- **Complete Development Tools**
  - Free Development Software (PSoC™ Designer)
  - Full-Featured, In-Circuit Emulator and Programmer
  - Full Speed Emulation
  - Complex Breakpoint Structure
  - 128K Bytes Trace Memory
  - Complex Events
  - C Compilers, Assembler, and Linker



PSoC™ Functional Overview

The PSoC™ family consists of many *Mixed Signal Array with On-Chip Controller* devices. These devices are designed to replace multiple traditional MCU-based system components with one, low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, as well as programmable interconnects. This architecture allows the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts and packages.

The PSoC architecture, as illustrated on the left, is comprised of four main areas: PSoC Core, Digital System, Analog System, and System Resources. Configurable global busing allows all the device resources to be combined into a complete custom system. The PSoC CY8C27x66 family can have up to eight IO ports that connect to the global digital and analog interconnects, providing access to 16 digital blocks and 12 analog blocks.

The PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose I/O).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU utilizes an interrupt controller with 25 vec-

tors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

Memory encompasses 32k of Flash for program storage, 2k of SRAM for data storage, and up to 2k of EEPROM emulated using the Flash. Program Flash utilizes four protection levels on blocks of 64 bytes, allowing customized software IP protection.

The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to 2.5% over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

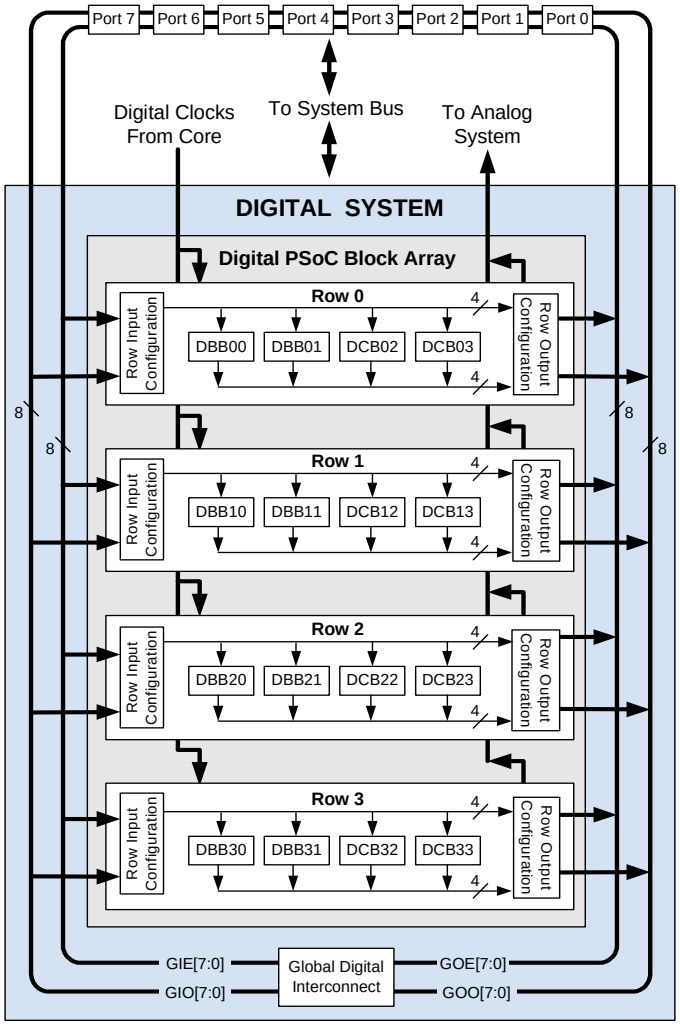
The Digital System

The Digital System is composed of 8 digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references. Digital peripheral configurations include those listed below.

- PWMs (8- to 32-bit)
- PWMs with Dead band (8- to 16-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- UART 8-bit with selectable parity (up to 2)
- SPI master and slave (up to 2 each)
- I2C slave and master (1 available as a System Resource)
- Cyclical Redundancy Checker/Generator (8- to 16-bit)
- IrDA (up to 4)
- Pseudo Random Sequence Generators (8- to 16-bit)

The digital blocks can be connected to any GPIO through a series of global busses that can route any signal to any pin. The busses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows you the optimum choice of system resources for your application. Family resources are shown in the table titled "PSoC Configurations" on page 3.



Digital System Block Diagram

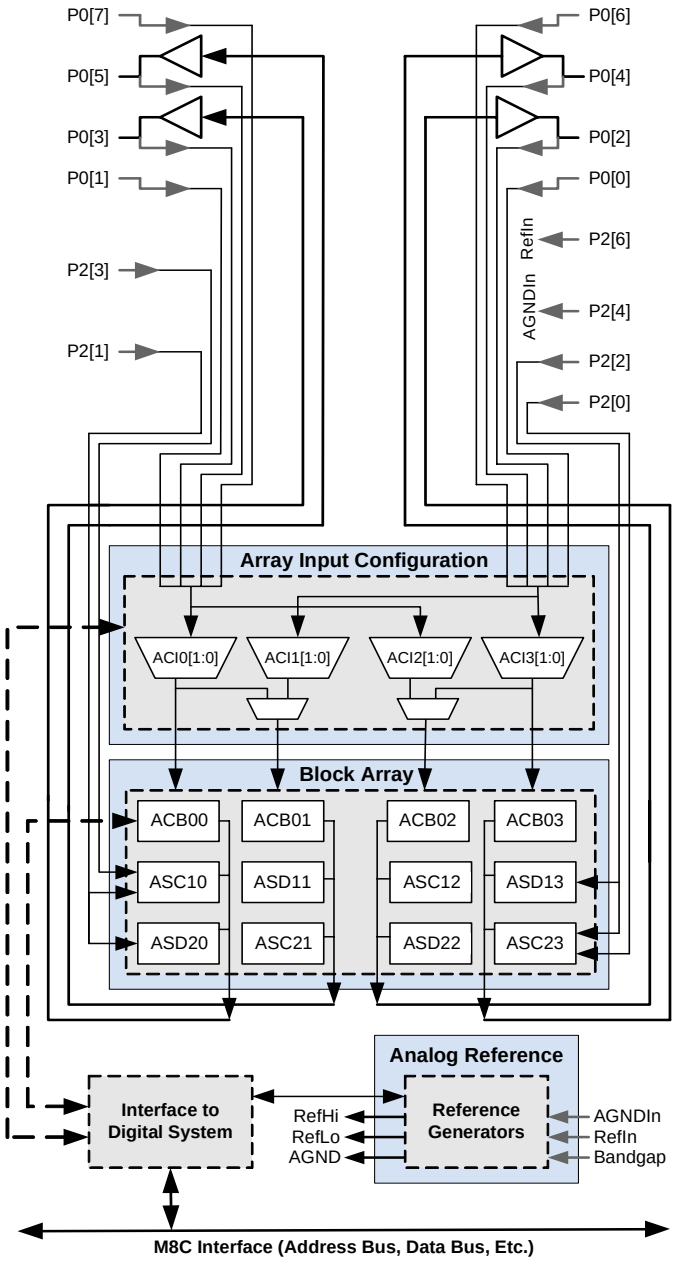
The Analog System

The Analog System is composed of 12 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are listed below.

- Analog to digital converters (up to 4, with 6 to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (2, 4, and 6 pole band-pass, low-pass, and notch)
- Amplifiers (up to 4, with selectable gain to 48x)
- Instrumentation amplifiers (up to 2, with selectable gain to 93x)
- Comparators (up to 4, with 16 selectable thresholds)
- DACs (up to 4, with 6- to 9-bit resolution)
- Multiplying DACs (up to 4, with 6- to 9-bit resolution)
- High current output drivers (four with 40 mA drive as a Core Resource)

- 1.3V, 1% voltage reference (as a System Resource)
- DTMF dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks. The number of blocks is dependant on the device family which is detailed in the table titled "PSoC Configurations" on page 3.



Analog System Block Diagram

Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, switch mode pump, low voltage detection, and power on reset. Brief statements describing the merits of each system resource are presented below.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math as well as digital filters.
- The decimator provides a custom hardware filter for digital signal, processing applications including the creation of Delta Sigma ADCs.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3V voltage reference provides an absolute reference for the analog system, including ADCs and DACs. The reference's 1% resolution over voltage and temperature satisfies most system requirements.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.2V battery cell, providing a low cost boost converter.

Configuration Options

Depending on your PSoC device configuration, the digital and analog systems can have 16, 12, 8, or 4 digital blocks and 12, 6, or 3 analog blocks. The following table lists the resources available for specific PSoC device groups.

PSoC Configurations

PSoC Part Number	Digital IO	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks
CY8C29x66	up to 64	4	16	12	4	4	12
CY8C27x66	**up to 64**	**4**	**8**	**12**	**4**	**4**	**12**
CY8C27x43	up to 44	2	8	12	4	4	12
CY8C24x23	up to 24	1	4	12	2	2	6
CY8C22x13	up to 16	1	4	8	1	1	3

Getting Started

The quickest path to understanding the PSoC silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications for the CY8C27x66 PSoC device family. For in-depth information, along with detailed programming information, reference the *PSoC™ Mixed Signal Array Technical Reference Manual*.

For up-to-date Ordering, Packaging, and Electrical Specification information, reference the latest PSoC device data sheets on the web at http://www.cypress.com.

Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store at http://www.onfulfillment.com/cypressstore/ contains development kits, C compilers, and all accessories for PSoC development. Click on *PSoC (Programmable System-on-Chip)* to view a current list of available items.

Tele-Training

Free PSoC "Tele-training" is available for beginners and taught by a live marketing or application engineer over the phone. Five training classes are available to accelerate the learning curve including introduction, designing, debugging, advanced design, advanced analog, as well as application-specific classes covering topics like PSoC and the LIN bus. For days and times of the tele-training, see http://www.cypress.com/support/training.cfm.

Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant, go to the following Cypress support web site: http://www.cypress.com/support/cypros.cfm.

Technical Support

PSoC application engineers take pride in fast and accurate response. They can be reached with a 4-hour guaranteed response at http://www.cypress.com/support/login.cfm.

Application Notes

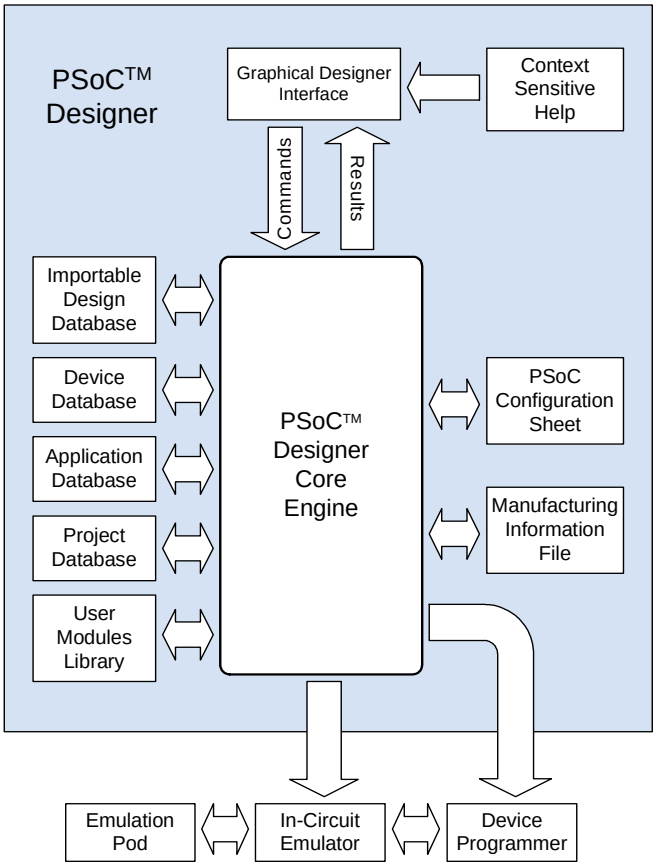
A long list of application notes will assist you in every aspect of your design effort. To locate the PSoC application notes, go to http://www.cypress.com/design/results.cfm.

Development Tools

The Cypress MicroSystems PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows 98, Windows NT 4.0, Windows 2000, Windows Millennium (Me), or Windows XP. (Reference the PSoC Designer Functional Flow diagram below.)

PSoC Designer helps the customer to select an operating configuration for the PSoC, write application code that uses the PSoC, and debug the application. This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and the CYASM macro assembler for the CPUs.

PSoC Designer also supports a high-level C language compiler developed specifically for the devices in the family.



PSoC Designer Subsystems

PSoC Designer Software Subsystems

Device Editor

PSoC Designer has several main functions. In the Design Editor you can easily configure a design and APIs are automatically generated for the user modules. The Device Editor subsystem allows the user to select different onboard analog and digital components called user modules using the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configuration at run time.

PSoC Designer sets up power-on initialization tables for selected PSoC block configurations and creates source code for an application framework. The framework contains software to operate the selected components and, if the project uses more than one operating configuration, contains routines to switch between different sets of PSoC block configurations at runtime. PSoC Designer can print out a configuration sheet for given project configuration for use during application programming in conjunction with the Device Data Sheet. Once the framework is generated, the user can add application-specific code to flesh out the framework. It's also possible to change the selected components and regenerate the framework.

Design Browser

The Design Browser allows users to select and import preconfigured designs into the user's project. Users can easily browse a catalog of preconfigured designs to facilitate time-to-design. Recent examples provided in the tools include a 300-baud modem, Lin Bus master and slave, fan controller, and magnetic card reader.

Application Editor

In the Application Editor you can edit your C language and Assembly language source code. You can also assemble, compile, link, and build.

Assembler. The macro assembler allows the assembly code to be merged seamlessly with C code. The link libraries automatically use absolute addressing or can be compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compiler. An ANSI C language compiler supports Cypress MicroSystems' PSoC family devices (except for 64-bit doubles). Even if you have never worked in the C language before, the product quickly allows you to create complete C programs for the PSoC family devices.

The embedded, optimizing C compiler provides all the features of C tailored to the PSoC architecture. It comes complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing the designer to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and write program and data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulation consists of a base unit that connects to the PC by way of the parallel or USB port. The base unit is universal and will operate with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

PSoC Development Tool Kit

User Modules and the PSoC Development Process

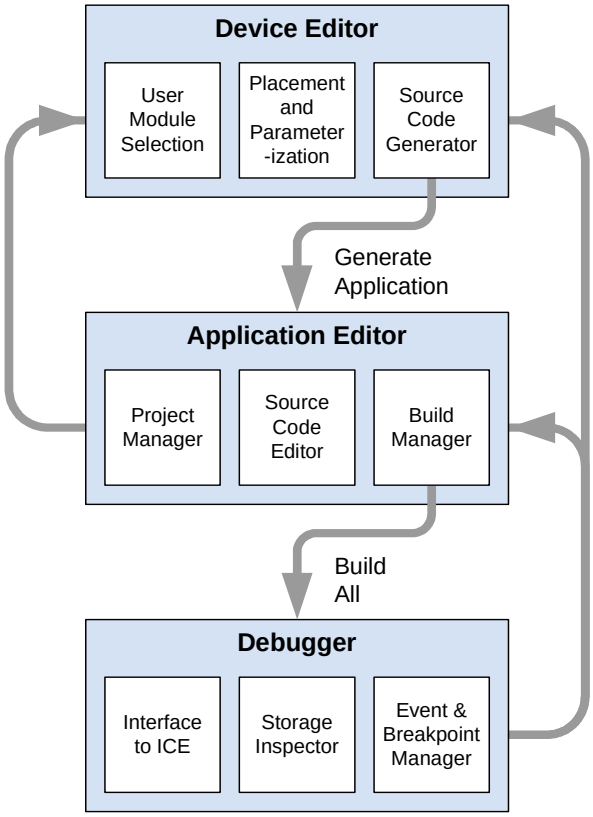
The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and later by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. Each block has several registers that determine its function and connectivity to other blocks, multiplexers, busses and, ultimately, to the IO pins. Iterative development cycles permit you to adapt the hardware as well as the software. This substantially lowers the risk that you will have to select a different part to meet the final design requirements.

To speed the development process, the PSoC Designer Integrated Development Environment (IDE) provides a library of pre-built, pre-tested hardware peripheral functions, called “User Modules.” User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties. The standard User Module library contains over 50 common peripherals such as ADCs, DACs Timers, Counters, UARTs, and other not-so common peripherals such as DTMF Generators and Bi-Quad analog filter sections.

Each user module establishes the basic register settings that implement the selected function. It also provides parameters that allow you to tailor its precise configuration to your particular application. For example, a Pulse Width Modulator User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution, to select the PWM function. The user module parameters permit you to establish the pulse width and duty cycle. User modules also provide tested software to cut your development time. The user module application programming interface (API) provides high-level functions to control and respond to hardware events at run-time. The API also provides optional interrupt service routines that you can adapt as needed.

The API functions are documented in user module data sheets that are viewed directly in the PSoC Designer IDE. These data sheets explain the internal operation of the user module and provide performance specifications. Each data sheet describes the use of each user module parameter and documents the setting of each register controlled by the user module.

The development process starts when you open a new project and bring up the Device Editor, a pictorial environment (GUI) for configuring the hardware. You pick the user modules you need for your project and map them onto the PSoC blocks with point-and-click simplicity. Next, you build signal chains by interconnecting user modules to each other and the IO pins. At this stage, you also configure the clock source connections and enter parameter values directly or by selecting values from drop-down menus. When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the high-level user module API functions.



User Module and Source Code Development Flows

The next step is to write your main program, and any sub-routines using PSoC Designer’s Application Editor subsystem. The Application Editor includes a Project Manager that allows you to open the project source code files (including all generated code files) from a hierarchal view. The source code editor provides syntax coloring and advanced edit features for both C and assembly language. File search capabilities include simple string searches and recursive “grep-style” patterns. A single mouse click invokes the Build Manager. It employs a professional-strength “makefile” system to automatically analyze all file dependencies and run the compiler and assembler as necessary. Project-level options control optimization strategies used by the compiler and linker. Syntax errors are displayed in a console window. Double clicking the error message takes you directly to the offending line of source code. When all is correct, the linker builds a ROM file image suitable for programming.

The last step in the development process takes place inside the PSoC Designer’s Debugger subsystem. The Debugger downloads the ROM image to the In-Circuit Emulator (ICE) where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description
AC	alternating current
API	application programming interface
APOR	analog power on reset
BC	broadcast clock
CPU	central processing unit
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
EEPROM	electrically erasable programmable read-only memory
FB	feedback
FSR	full scale range
GPIO	general purpose IO
IO	input/output
IOW	IO write
IPOR	imprecise power on reset
IRA	interrupt request acknowledge
IRQ	interrupt request
ISR	interrupt service routine
LSB	least-significant bit
LUT	lookup table
MSB	most-significant bit
PC	program counter
PD	power down
PGA	programmable gain amplifier
POR	power on reset
PPOR	precision power on reset
PSoC™	Programmable System-on-Chip
PSRR	power supply rejection ratio
PVT	process voltage temperature
PWM	pulse width modulator
RAM	random access memory
RAS	ROM access strobe
RI	row input
RO	row output
ROM	read only memory
SC	switched capacitor
SNR	signal-to-noise ratio
TC	terminal count
VCO	voltage controlled oscillator

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 3-1 on page 19 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexidecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexidecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (e.g., 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or 0x are decimal.

Table of Contents

For an in depth discussion and more information on your PSoC device, obtain the *PSoC Mixed Signal Array Technical Reference Manual*. This document encompasses and is organized into the following chapters and sections.

1. Pin Information

This chapter describes, lists, and illustrates the CY8C27x66 PSoC device pins and pinout configurations.

1.1 Pinouts

The CY8C27x66 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital IO. However, Vss, Vdd, SMP, and XRES are not capable of Digital IO.

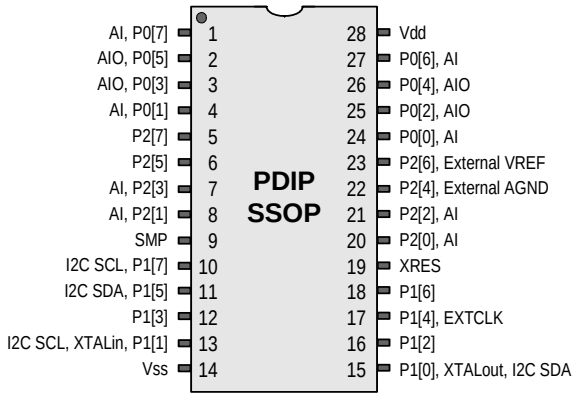
1.1.1 28-Pin Part Pinout

Table 1-1. 28-Pin Part Pinout (PDIP, SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I	P0[7]	Analog column mux input.
2	IO	IO	P0[5]	Analog column mux input and column output.
3	IO	IO	P0[3]	Analog column mux input and column output.
4	IO	I	P0[1]	Analog column mux input.
5	IO		P2[7]	
6	IO		P2[5]	
7	IO	I	P2[3]	Direct switched capacitor block input.
8	IO	I	P2[1]	Direct switched capacitor block input.
9	Power		SMP	Switch Mode Pump (SMP) connection to required external components.
10	IO		P1[7]	I2C Serial Clock (SCL)
11	IO		P1[5]	I2C Serial Data (SDA)
12	IO		P1[3]	
13	IO		P1[1]	Crystal (XTALin), I2C Serial Clock (SCL)
14	Power		Vss	Ground connection.
15	IO		P1[0]	Crystal (XTALout), I2C Serial Data (SDA)
16	IO		P1[2]	
17	IO		P1[4]	Optional External Clock Input (EXTCLK)
18	IO		P1[6]	
19	Input		XRES	Active high pin reset with internal pull down.
20	IO	I	P2[0]	Direct switched capacitor block input.
21	IO	I	P2[2]	Direct switched capacitor block input.
22	IO		P2[4]	External Analog Ground (AGND)
23	IO		P2[6]	External Voltage Reference (VREF)
24	IO	I	P0[0]	Analog column mux input.
25	IO	IO	P0[2]	Analog column mux input and column output.
26	IO	IO	P0[4]	Analog column mux input and column output.
27	IO	I	P0[6]	Analog column mux input.
28	Power		Vdd	Supply voltage.

LEGEND: D = Digital, A = Analog, I = Input, and O = Output.

CY8C27x66 28-Pin PSoC Device



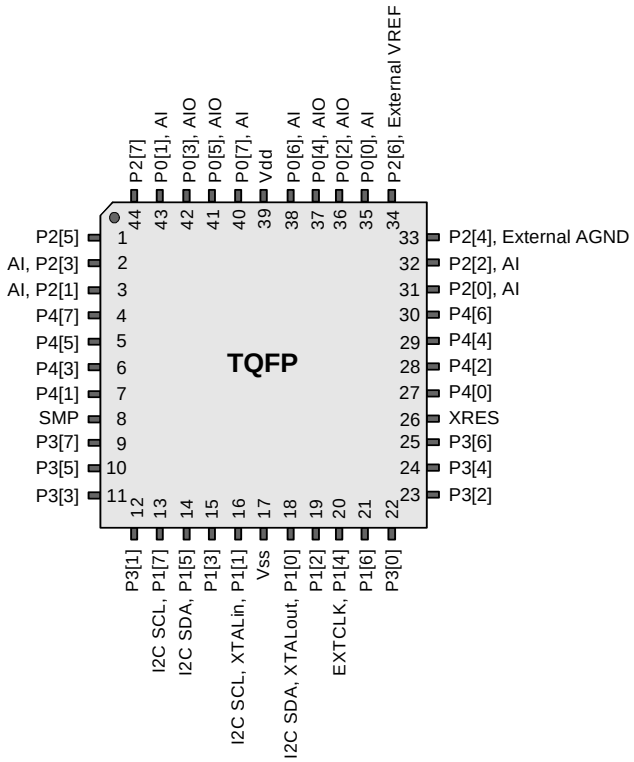
1.1.2 44-Pin Part Pinout

Table 1-2. 44-Pin Part Pinout (TQFP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO		P2[5]	
2	IO	I	P2[3]	Direct switched capacitor block input.
3	IO	I	P2[1]	Direct switched capacitor block input.
4	IO		P4[7]	
5	IO		P4[5]	
6	IO		P4[3]	
7	IO		P4[1]	
8	Power		SMP	Switch Mode Pump (SMP) connection to required external components.
9	IO		P3[7]	
10	IO		P3[5]	
11	IO		P3[3]	
12	IO		P3[1]	
13	IO		P1[7]	I2C Serial Clock (SCL)
14	IO		P1[5]	I2C Serial Data (SDA)
15	IO		P1[3]	
16	IO		P1[1]	Crystal (XTALin), I2C Serial Clock (SCL)
17	Power		Vss	Ground connection.
18	IO		P1[0]	Crystal (XTALout), I2C Serial Data (SDA)
19	IO		P1[2]	
20	IO		P1[4]	Optional External Clock Input (EXTCLK)
21	IO		P1[6]	
22	IO		P3[0]	
23	IO		P3[2]	
24	IO		P3[4]	
25	IO		P3[6]	
26	Input		XRES	Active high pin reset with internal pull down.
27	IO		P4[0]	
28	IO		P4[2]	
29	IO		P4[4]	
30	IO		P4[6]	
31	IO	I	P2[0]	Direct switched capacitor block input.
32	IO	I	P2[2]	Direct switched capacitor block input.
33	IO		P2[4]	External Analog Ground (AGND)
34	IO		P2[6]	External Voltage Reference (VREF)
35	IO	I	P0[0]	Analog column mux input.
36	IO	IO	P0[2]	Analog column mux input and column output.
37	IO	IO	P0[4]	Analog column mux input and column output.
38	IO	I	P0[6]	Analog column mux input.
39	Power		Vdd	Supply voltage.
40	IO	I	P0[7]	Analog column mux input.
41	IO	IO	P0[5]	Analog column mux input and column output.
42	IO	IO	P0[3]	Analog column mux input and column output.
43	IO	I	P0[1]	Analog column mux input.
44	IO		P2[7]	

LEGEND: D = Digital, A = Analog, I = Input, and O = Output.

CY8C27x66 44-Pin PSoC Device



1.1.3 48-Pin Part Pinouts

Table 1-3. 48-Pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I	P0[7]	Analog column mux input.
2	IO	IO	P0[5]	Analog column mux input and column output.
3	IO	IO	P0[3]	Analog column mux input and column output.
4	IO	I	P0[1]	Analog column mux input.
5	IO		P2[7]	
6	IO		P2[5]	
7	IO	I	P2[3]	Direct switched capacitor block input.
8	IO	I	P2[1]	Direct switched capacitor block input.
9	IO		P4[7]	
10	IO		P4[5]	
11	IO		P4[3]	
12	IO		P4[1]	
13	Power		SMP	Switch Mode Pump (SMP) connection to required external components.
14	IO		P3[7]	
15	IO		P3[5]	
16	IO		P3[3]	
17	IO		P3[1]	
18	IO		P5[3]	
19	IO		P5[1]	
20	IO		P1[7]	I2C Serial Clock (SCL)
21	IO		P1[5]	I2C Serial Data (SDA)
22	IO		P1[3]	
23	IO		P1[1]	Crystal (XTALin), I2C Serial Clock (SCL)
24	Power		Vss	Ground connection.
25	IO		P1[0]	Crystal (XTALout), I2C Serial Data (SDA)
26	IO		P1[2]	
27	IO		P1[4]	Optional External Clock Input (EXTCLK)
28	IO		P1[6]	
29	IO		P5[0]	
30	IO		P5[2]	
31	IO		P3[0]	
32	IO		P3[2]	
33	IO		P3[4]	
34	IO		P3[6]	
35	Input		XRES	Active high pin reset with internal pull down.
36	IO		P4[0]	
37	IO		P4[2]	
38	IO		P4[4]	
39	IO		P4[6]	
40	IO	I	P2[0]	Direct switched capacitor block input.
41	IO	I	P2[2]	Direct switched capacitor block input.
42	IO		P2[4]	External Analog Ground (AGND)
43	IO		P2[6]	External Voltage Reference (VREF)
44	IO	I	P0[0]	Analog column mux input.
45	IO	IO	P0[2]	Analog column mux input and column output.
46	IO	IO	P0[4]	Analog column mux input and column output.
47	IO	I	P0[6]	Analog column mux input.
48	Power		Vdd	Supply voltage.

LEGEND: D = Digital, A = Analog, I = Input, and O = Output.

CY8C27x66 48-Pin PSoC Device

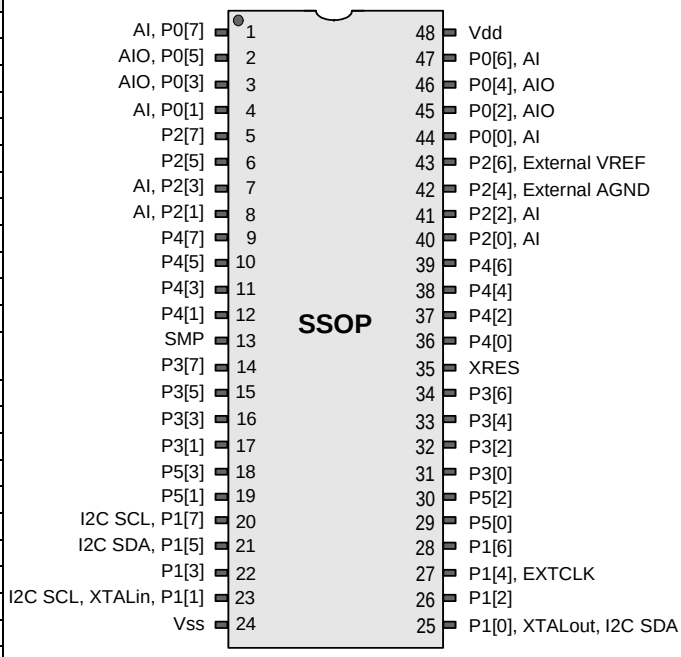


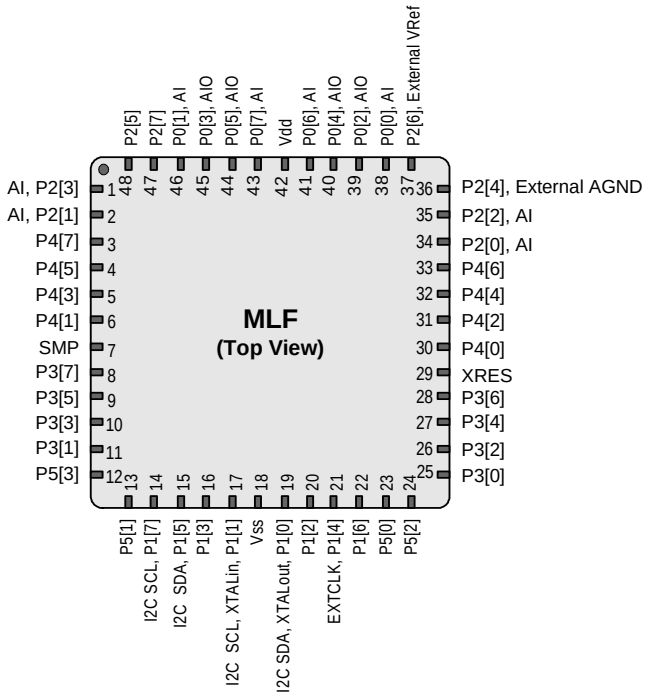
Table 1-4. 48-Pin Part Pinout (MLF*)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I	P2[3]	Analog column mux input and column output.
2	IO	I	P2[1]	Analog column mux input and column output.
3	IO		P4[7]	
4	IO		P4[5]	
5	IO		P4[3]	
6	IO		P4[1]	
7	Power		SMP	Switch Mode Pump (SMP) connection to required external components.
8	IO		P3[7]	
9	IO		P3[5]	
10	IO		P3[3]	
11	IO		P3[1]	
12	IO		P5[3]	
13	IO		P5[1]	
14	IO		P1[7]	I2C Serial Clock (SCL)
15	IO		P1[5]	I2C Serial Data (SDA)
16	IO		P1[3]	
17	IO		P1[1]	Crystal (XTALin), I2C Serial Clock (SCL)
18	Power		Vss	Ground connection.
19	IO		P1[0]	Crystal (XTALout), I2C Serial Data (SDA)
20	IO		P1[2]	
21	IO		P1[4]	Optional External Clock Input (EXTCLK)
22	IO		P1[6]	
23	IO		P5[0]	
24	IO		P5[2]	
25	IO		P3[0]	
26	IO		P3[2]	
27	IO		P3[4]	
28	IO		P3[6]	
29	Power		XRES	Active high pin reset with internal pull down.
30	IO		P4[0]	
31	IO		P4[2]	
32	IO		P4[4]	
33	IO		P4[6]	
34	IO	I	P2[0]	Direct switched capacitor block input.
35	IO	I	P2[2]	Direct switched capacitor block input.
36	IO		P2[4]	External Analog Ground (AGND)
37	IO		P2[6]	External Voltage Reference (VREF)
38	IO	I	P0[0]	Analog column mux input.
39	IO	IO	P0[2]	Analog column mux input and column output.
40	IO	IO	P0[4]	Analog column mux input and column output.
41	IO	I	P0[6]	Analog column mux input.
42	Power		Vdd	Supply voltage.
43	IO	I	P0[7]	Analog column mux input.
44	IO	IO	P0[5]	Analog column mux input and column output.
45	IO	IO	P0[3]	Analog column mux input and column output.
46	IO	I	P0[1]	Analog column mux input.
47	IO		P2[7]	
48	IO		P2[5]	

LEGEND: D = Digital, A = Analog, I = Input, and O = Output.

* The MLF package has a center pad that must be connected to the ground (Vss).

CY8C27x66 48-Pin PSoC Device



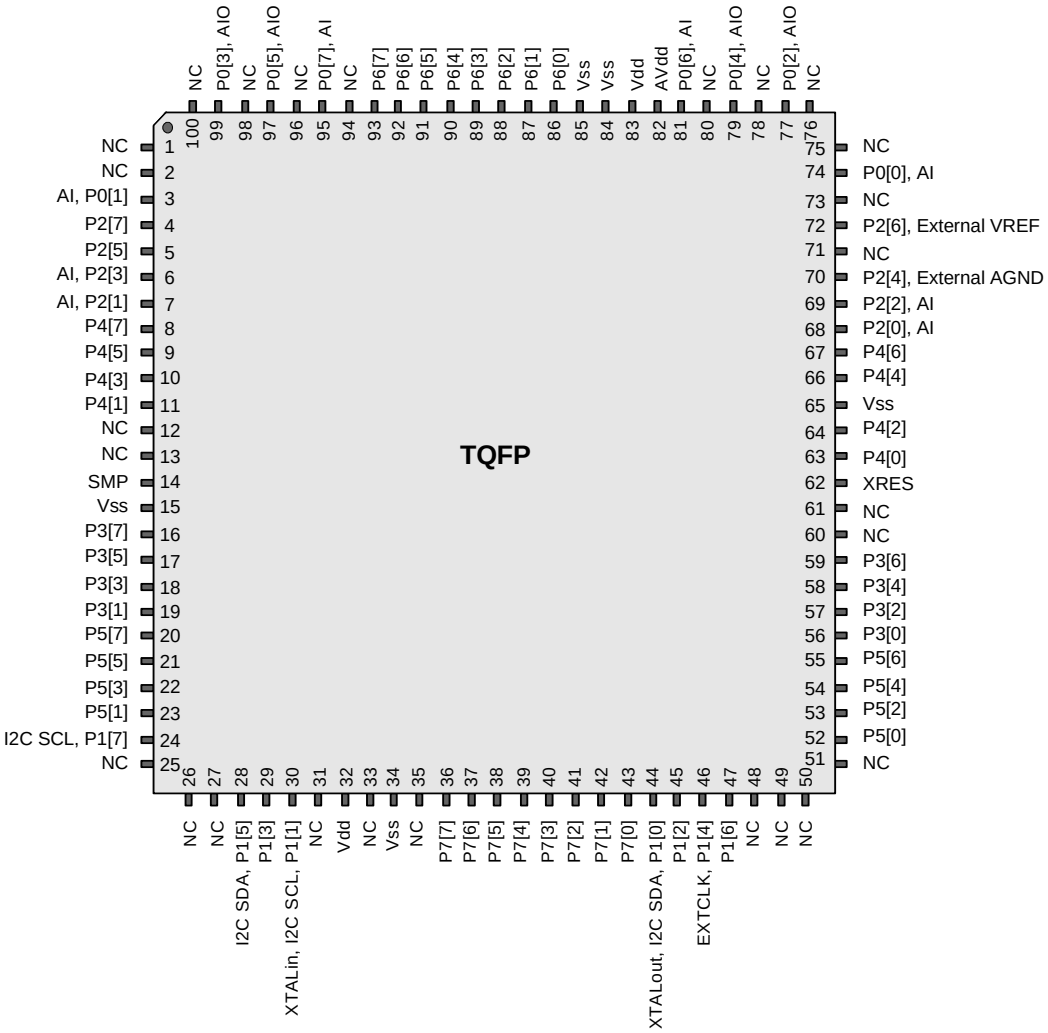
1.1.4 100-Pin Part Pinout

Table 1-5. 100-Pin Part Pinout (TQFP)

Pin No.	Type		Name	Description	Pin No.	Type		Name	Description
	Digital	Analog				Digital	Analog		
1			NC	No connection. Do not use.	51			NC	No connection. Do not use.
2			NC	No connection. Do not use.	52	IO		P5[0]	
3	IO	I	P0[1]	Analog column mux input.	53	IO		P5[2]	
4	IO		P2[7]		54	IO		P5[4]	
5	IO		P2[5]		55	IO		P5[6]	
6	IO	I	P2[3]	Direct switched capacitor block input.	56	IO		P3[0]	
7	IO	I	P2[1]	Direct switched capacitor block input.	57	IO		P3[2]	
8	IO		P4[7]		58	IO		P3[4]	
9	IO		P4[5]		59	IO		P3[6]	
10	IO		P4[3]		60			NC	No connection. Do not use.
11	IO		P4[1]		61			NC	No connection. Do not use.
12			NC	No connection. Do not use.	62	Input		XRES	Active high pin reset with internal pull down.
13			NC	No connection. Do not use.	63	IO		P4[0]	
14	Power		SMP	Switch Mode Pump (SMP) connection to required external components.	64	IO		P4[2]	
15	Power		Vss	Ground connection.	65	Power		Vss	Ground connection.
16	IO		P3[7]		66	IO		P4[4]	
17	IO		P3[5]		67	IO		P4[6]	
18	IO		P3[3]		68	IO	I	P2[0]	Direct switched capacitor block input.
19	IO		P3[1]		69	IO	I	P2[2]	Direct switched capacitor block input.
20	IO		P5[7]		70	IO		P2[4]	External Analog Ground (AGND)
21	IO		P5[5]		71			NC	No connection. Do not use.
22	IO		P5[3]		72	IO		P2[6]	External Voltage Reference (VREF)
23	IO		P5[1]		73			NC	No connection. Do not use.
24	IO		P1[7]	I2C Serial Clock (SCL)	74	IO	I	P0[0]	Analog column mux input.
25			NC	No connection. Do not use.	75			NC	No connection. Do not use.
26			NC	No connection. Do not use.	76			NC	No connection. Do not use.
27			NC	No connection. Do not use.	77	IO	IO	P0[2]	Analog column mux input and column output.
28	IO		P1[5]	I2C Serial Data (SDA)	78			NC	No connection. Do not use.
29	IO		P1[3]		79	IO	IO	P0[4]	Analog column mux input and column output.
30	IO		P1[1]	Crystal (XTALin), I2C Serial Clock (SCL)	80			NC	No connection. Do not use.
31			NC	No connection. Do not use.	81	IO	I	P0[6]	Analog column mux input.
32	Power		Vdd	Supply voltage.	82	Power		AVdd	Supply voltage for Analog System.
33			NC	No connection. Do not use.	83	Power		Vdd	Supply voltage.
34	Power		Vss	Ground connection.	84	Power		Vss	Ground connection.
35			NC	No connection. Do not use.	85	Power		Vss	Ground connection.
36	IO		P7[7]		86	IO		P6[0]	
37	IO		P7[6]		87	IO		P6[1]	
38	IO		P7[5]		88	IO		P6[2]	
39	IO		P7[4]		89	IO		P6[3]	
40	IO		P7[3]		90	IO		P6[4]	
41	IO		P7[2]		91	IO		P6[5]	
42	IO		P7[1]		92	IO		P6[6]	
43	IO		P7[0]		93	IO		P6[7]	
44	IO		P1[0]	Crystal (XTALout), I2C Serial Data (SDA)	94			NC	No connection. Do not use.
45	IO		P1[2]		95	IO	I	P0[7]	Analog column mux input.
46	IO		P1[4]	Optional External Clock Input (EXTCLK)	96			NC	No connection. Do not use.
47	IO		P1[6]		97	IO	IO	P0[5]	Analog column mux input and column output.
48			NC	No connection. Do not use.	98			NC	No connection. Do not use.
49			NC	No connection. Do not use.	99	IO	IO	P0[3]	Analog column mux input and column output.
50			NC	No connection. Do not use.	100			NC	No connection. Do not use.

LEGEND: D = Digital, A = Analog, I = Input, and O = Output.

CY8C27x66 100-Pin PSoC Device



2. Register Reference

This chapter lists the registers of the CY8C27x66 PSoC device by way of mapping tables, in offset order. For detailed register information, reference the *PSoC™ Mixed Signal Array Technical Reference Manual*.

2.1 Register Conventions

2.1.1 Abbreviations Used

The register conventions specific to this section are listed in the following table.

Convention	Description
RW	Read and write register or bit(s)
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

2.1.2 Naming Conventions

The register naming convention for arrays of PSoC blocks and their registers is:

<Prefix>mn<Suffix>
where m=row index, n=column index

Therefore, ASD13CR3 is a register for an analog PSoC block in row 1 column 3.

2.2 Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is also referred to as IO space and is broken into two parts. The XOI bit in the Flag register determines which bank the user is currently in. When the XOI bit is set, the user is said to be in the “extended” address space or the “configuration” registers.

Note In the following register mapping tables, blank fields are Reserved and should not be accessed.

Register Map 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0IE	01	RW		41		ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0GS	02	RW		42		ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0DM2	03	RW		43		ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DR	04	RW		44		ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1IE	05	RW		45		ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1GS	06	RW		46		ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48		ASC12CR0	88	RW	RDI3RI	C8	RW
PRT2IE	09	RW		49		ASC12CR1	89	RW	RDI3SYN	C9	RW
PRT2GS	0A	RW		4A		ASC12CR2	8A	RW	RDI3IS	CA	RW
PRT2DM2	0B	RW		4B		ASC12CR3	8B	RW	RDI3LT0	CB	RW
PRT3DR	0C	RW		4C		ASD13CR0	8C	RW	RDI3LT1	CC	RW
PRT3IE	0D	RW		4D		ASD13CR1	8D	RW	RDI3RO0	CD	RW
PRT3GS	0E	RW		4E		ASD13CR2	8E	RW	RDI3RO1	CE	RW
PRT3DM2	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW	PRV_PP	D2	RW
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C_SCR	D7	#
PRT6DR	18	RW		58		ASD22CR0	98	RW	I2C_DR	D8	RW
PRT6IE	19	RW		59		ASD22CR1	99	RW	I2C_MSCR	D9	#
PRT6GS	1A	RW		5A		ASD22CR2	9A	RW	INT_CLR0	DA	RW
PRT6DM2	1B	RW		5B		ASD22CR3	9B	RW	INT_CLR1	DB	RW
PRT7DR	1C	RW		5C		ASC23CR0	9C	RW	INT_CLR2	DC	RW
PRT7IE	1D	RW		5D		ASC23CR1	9D	RW	INT_CLR3	DD	RW
PRT7GS	1E	RW		5E		ASC23CR2	9E	RW	INT_MSK3	DE	RW
PRT7DM2	1F	RW		5F		ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCB02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCB02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCB02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCB03DR0	2C	#	TMP0_DR	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP1_DR	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP2_DR	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP3_DR	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBB10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBB10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11DR0	34	#	ACB01CR3	74	RW	RDIOLT1	B4	RW		F4	
DBB11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBB11CR0	37	#	ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCB12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCB13CR0	3F	#	ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

Register Map 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0DM1	01	RW		41		ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW		42		ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW		43		ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW		44		ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1DM1	05	RW		45		ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW		46		ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW		48		ASC12CR0	88	RW	RDI3RI	C8	RW
PRT2DM1	09	RW		49		ASC12CR1	89	RW	RDI3SYN	C9	RW
PRT2IC0	0A	RW		4A		ASC12CR2	8A	RW	RDI3IS	CA	RW
PRT2IC1	0B	RW		4B		ASC12CR3	8B	RW	RDI3LT0	CB	RW
PRT3DM0	0C	RW		4C		ASD13CR0	8C	RW	RDI3LT1	CC	RW
PRT3DM1	0D	RW		4D		ASD13CR1	8D	RW	RDI3RO0	CD	RW
PRT3IC0	0E	RW		4E		ASD13CR2	8E	RW	RDI3RO1	CE	RW
PRT3IC1	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DM0	10	RW		50		ASD20CR0	90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW		54		ASC21CR0	94	RW		D4	
PRT5DM1	15	RW		55		ASC21CR1	95	RW		D5	
PRT5IC0	16	RW		56		ASC21CR2	96	RW		D6	
PRT5IC1	17	RW		57		ASC21CR3	97	RW		D7	
PRT6DM0	18	RW		58		ASD22CR0	98	RW		D8	
PRT6DM1	19	RW		59		ASD22CR1	99	RW		D9	
PRT6IC0	1A	RW		5A		ASD22CR2	9A	RW		DA	
PRT6IC1	1B	RW		5B		ASD22CR3	9B	RW		DB	
PRT7DM0	1C	RW		5C		ASC23CR0	9C	RW		DC	
PRT7DM1	1D	RW		5D		ASC23CR1	9D	RW	OSC_GO_EN	DD	RW
PRT7IC0	1E	RW		5E		ASC23CR2	9E	RW	OSC_CR4	DE	RW
PRT7IC1	1F	RW		5F		ASC23CR3	9F	RW	OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	W
DCB02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP0_DR	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP1_DR	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP2_DR	6E	RW		AE			EE	
	2F		TMP3_DR	6F	RW		AF			EF	
DBB10FN	30	RW	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10IN	31	RW	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10OU	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11FN	34	RW	ACB01CR3	74	RW	RDIOLT1	B4	RW		F4	
DBB11IN	35	RW	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11OU	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12FN	38	RW	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12IN	39	RW	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12OU	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
	3B		ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13FN	3C	RW	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13IN	3D	RW	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13OU	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
	3F		ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

3. Electrical Specifications

This chapter presents the DC and AC electrical specifications of the CY8C27x66 PSoC device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com.

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C as specified, except where noted.

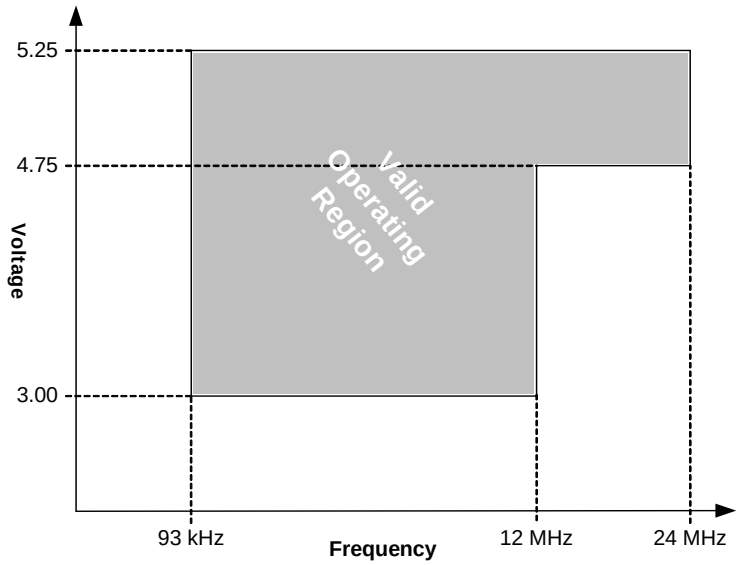


Figure 3-1. Voltage versus Operating Frequency

The following table lists the units of measure that are used in this chapter.

Table 3-1: Units of Measure

Symbol	Units of Measure	Symbol	Units of Measure
°C	degree Celsius	µV	microvolts
AC	alternating current	µVrms	microvolts root-mean-square
dB	decibels	mA	milliampere
DC	direct current	ms	millisecond
fF	femto Farad	mV	millivolts
Hz	hertz	ns	nanosecond
k	kilo, 1000	nV	nanovolts
K	2^{10}, 1024	Ω	ohm
KB	1024 bytes	pF	pico Farad
Kbit	1024 bits	pp	peak-to-peak
kHz	kilohertz	ppm	parts per million
kΩ	kilohm	ps	pico second
MHz	megahertz	sps	samples per second
MΩ	megaohm	σ	sigma: one standard deviation
µA	microampere	V	volts
µs	microsecond		

3.1 Absolute Maximum Ratings

Table 3-2. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-65	–	+100	°C	Higher storage temperatures will reduce data retention time.
T_A	Ambient Temperature with Power Applied	-40	–	+85	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss-0.5	–	Vdd+0.5	V	
–	DC Voltage Applied to Tri-state	Vss-0.5	–	Vdd+0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
I_{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	-50	–	+50	mA	
–	Static Discharge Voltage	2000	–	–	V	
–	Latch-up Current	–	–	200	mA	

3.2 Operating Temperature

Table 3-3. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+85	°C	
T_J	Junction Temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See “Thermal Impedances” on page 42. The user must limit the power consumption to comply with this requirement.

3.3 DC Electrical Characteristics

3.3.1 DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 3-4. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	3.00	–	5.25	V	
I_{DD}	Supply Current	–	5	8	mA	Conditions are 5.0V, 25 ^oC, 3 MHz, 48 MHz disabled. VC1=1.5 MHz, VC2=93.75 kHz, VC3=93.75 kHz.
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active. Lower 3/4 temperature range.	–	3	10	µA	Conditions are with internal slow speed oscillator, Vdd = 3.3 V, -40 ^oC <=T_A <= 55 ^oC.
I_{SBH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active. Higher 1/4 temperature range (hot).	–	4	25	µA	Conditions are with internal slow speed oscillator, Vdd = 3.3 V, 55 ^oC < T_A <= 85 ^oC.
I_{SBXTL}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, internal slow oscillator, and 32 kHz crystal oscillator active. Lower 3/4 temperature range.	–	4	12	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. Vdd = 3.3 V, -40 ^oC <= T_A <= 55 ^oC.
I_{SBXTLH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and 32 kHz crystal oscillator active. Higher 1/4 temperature range (hot).	–	5	27	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. Vdd = 3.3 V, 55 ^oC < T_A <= 85 ^oC.
V_{REF}	Reference Voltage (Bandgap)	1.28	1.3	1.32	V	Trimmed for appropriate Vdd.

3.3.2 DC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 3-5. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd - 1.0	–	–	V	IOH = 10 mA, Vdd = 4.75 to 5.25V (8 IO switching, 4 per side)
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, Vdd = 4.75 to 5.25V (8 IO switching, 4 per side)
V_{IL}	Input Low Level	–	–	0.8	V	Vdd = 3.0 to 5.5
V_{IH}	Input High Level	2.2	–		V	Vdd = 3.0 to 5.5
V_H	Input Hysterisis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 µA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25^oC.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25^oC.

3.3.3 DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 3-6. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Low Power	–	1.6	10	mV	
	Input Offset Voltage (absolute value) Mid Power	–	1.3	8	mV	
	Input Offset Voltage (absolute value) High Power	–	1.2	7.5	mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range. All Cases, except highest.	0.0	–	Vdd	V	
	Power = High, Opamp Bias = High	0.5	–	Vdd-0.5	V	
$CMRR_{OA}$	Common Mode Rejection Ratio	60	–	–	dB	
G_{OLOA}	Open Loop Gain	80	–	–	dB	
$V_{OHIGHOA}$	High Output Voltage Swing (worst case internal load)	Vdd-.01	–	–	V	
V_{OLOWOA}	Low Output Voltage Swing (worst case internal load)	–	–	0.1	V	
I_{SOA}	Supply Current (including associated AGND buffer)					
	Power=Low	–	150	200	µA	
	Power=Low, Opamp Bias=High	–	300	400	µA	
	Power=Medium	–	600	800	µA	
	Power=Medium, Opamp Bias=High	–	1200	1600	µA	
	Power=High	–	2400	3200	µA	
	Power=High, Opamp Bias=High	–	4600	6400	µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	60	–	–	dB	

Important Note Do not use the combination of Power = High and Opamp Bias = High for 3.3V operations.

Table 3-7. 3.3V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Low Power	–	1.65	10	mV	
	Input Offset Voltage (absolute value) Mid Power	–	1.32	8	mV	
	High Power is 5 Volt Only					
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range	0	–	Vdd	V	
$CMRR_{OA}$	Common Mode Rejection Ratio	60	–	–	dB	
G_{OLOA}	Open Loop Gain	80	–	–	dB	
$V_{OHIGHOA}$	High Output Voltage Swing (worst case internal load)	-.01	–	–	V	
V_{OLOWOA}	Low Output Voltage Swing (worst case internal load)	–	–	-1	V	
I_{SOA}	Supply Current (including associated AGND buffer)					
	Power=Low	–	150	200	µA	
	Power=Low, Opamp Bias=High	–	300	400	µA	
	Power=Medium	–	600	800	µA	
	Power=Medium, Opamp Bias=High	–	1200	1600	µA	
	Power=High	–	2400	3200	µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	50	–	–	dB	

3.3.4 DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 3-8. 5V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	.5	–	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance					
	Power = Low	–	–	1	Ω	
	Power = High	–	–	1	Ω	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 32 ohms to Vdd/2)					
	Power = Low	.5 x Vdd + 1.3	–	–	V	
	Power = High	.5 x Vdd + 1.3	–	–	V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 32 ohms to Vdd/2)					
	Power = Low	–	–	.5 x Vdd - 1.3	V	
	Power = High	–	–	.5 x Vdd - 1.3	V	
I_{SOB}	Supply Current Including Bias Cell (No Load)					
	Power = Low	–	1.1	2	mA	
	Power = High	–	2.6	5	mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	40	–	–	dB	

Table 3-9. 3.3V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	.5	-	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance					
	Power = Low	–	–	10	Ω	
	Power = High	–	–	10	Ω	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1K ohms to Vdd/2)					
	Power = Low	.5 x Vdd + 1.0	–	–	V	
	Power = High	.5 x Vdd + 1.0	–	–	V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 1K ohms to Vdd/2)					
	Power = Low	–	–	.5 x Vdd - 1.0	V	
	Power = High	–	–	.5 x Vdd - 1.0	V	
I_{SOB}	Supply Current Including Bias Cell (No Load)					
	Power = Low		0.8	1	mA	
	Power = High	–	2.0	8	mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	60	–	–	dB	

3.3.5 DC Switch Mode Pump Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 3-10. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PUMP} 5V	5V Output voltage	4.75	–	5.25	V	Average, neglecting ripple
V_{PUMP} 3V	3V Output voltage	3.00		3.60	V	Average, neglecting ripple
I_{PUMP}	Available Output Current vi= 1.5V, Vo= 3.25V vi= 1.5V, Vo= 5.0V	 8 5	 – –	 – –	 mA mA	For implementation, which includes 2 uH inductor, 1 uF cap, and Shottky diode.
I_{SHORT}	Short Circuit Current	–	12	–	mA	
V_{INPUMP} 5V	5V Input Voltage Range	1.8	–	3.3	V	
V_{INPUMP} 3V	3V Input Voltage Range	1.0	–	3.3	V	
$V_{IN-PUMP(MIN)}$	Minimum Input Voltage to Start Pump	1.1	–	–	V	
$V_{OUTPUMP}$	Output Voltage (over Vi range)	–	5	–	$\%V_O$	
$\Delta V_{OUTPUMP}$	Line Regulation (over Vi range)	–	5	–	$\%V_O$	
$\Delta V_{OUTPUMP}$	Load Regulation	–	5	–	$\%V_O$	
$\Delta V_{OUTPUMP}$	Output Voltage Ripple (depends on cap/load)	–	25	–	mVpp	Configuration of note 2, load is 5mA.
–	Efficiency	35	50	–	%	Configuration of note 2, load is 5mA, Vout is 3.25V.
F_{PUMP}	Switching Frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching Duty Cycle	–	50	–	%	

3.3.6 DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block.

Table 3-11. 5V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
–	AGND = Vdd/2[a] CT Block Power = High	Vdd/2 - 0.017	Vdd/2 - 0.0	Vdd/2 + 0.017	V
–	AGND = 2*BandGap[a] CT Block Power = High	2*BG - 0.034	2*BG - 0.0	2*BG + 0.034	V
–	AGND = P2[4] (P2[4] = Vdd/2)[a] CT Block Power = High	P2[4] - 0.013	P2[4] 0.0	P2[4] + 0.013	V
–	AGND = BandGap[a] CT Block Power = High	BG- 0.009	BG	BG+0.009	V
–	AGND = 1.6*BandGap[a] CT Block Power = High	1.6*BG- 0.018	1.6*BG	1.6*BG+0.018	V
–	AGND Column to Column Variation (AGND=Vdd/2)[a] CT Block Power = High	-0.034	0.000	0.034	V
–	RefHi = Vdd/2 + BandGap Ref Control Power = High	Vdd/2+BG - 0.062	Vdd/2+BG - 0.0	Vdd/2+BG + 0.062	V
–	RefHi = 3*BandGap Ref Control Power = High	3*BG - 0.084	3*BG - 0.0	3*BG + 0.084	V
–	RefHi = 2*BandGap + P2[6] (P2[6] = 1.3V) Ref Control Power = High	2*BG+P2[6] - 0.082	2*BG+P2[6] - 0.0	2*BG+P2[6] + 0.082	V
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2) Ref Control Power = High	P2[4]+BG - 0.062	P2[4]+BG - 0.0	P2[4]+BG + 0.062	V
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V) Ref Control Power = High	P2[4]+P2[6] - 0.058	P2[4]+P2[6] - 0.0	P2[4]+P2[6]+ 0.058	V
–	RefHi = 2*BandGap Ref Control Power = High	2*BG - 0.053	2*BG	2*BG + 0.053	V
–	RefHi = 3.2*BandGap Ref Control Power = High	3.2*BG - 0.068	3.2*BG	3.2*BG + 0.068	V
–	RefLo = Vdd/2 – BandGap Ref Control Power = High	Vdd/2-BG - 0.049	Vdd/2-BG + 0.0	Vdd/2-BG + 0.049	V
–	RefLo = BandGap Ref Control Power = High	BG - 0.074	BG + 0.0	BG + 0.074	V
–	RefLo = 2*BandGap - P2[6] (P2[6] = 1.3V) Ref Control Power = High	2*BG-P2[6] - 0.071	2*BG-P2[6] + 0.0	2*BG-P2[6] + 0.071	V
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2) Ref Control Power = High	P2[4]-BG - 0.048	P2[4]-BG + 0.0	P2[4]-BG + 0.048	V
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V) Ref Control Power = High	P2[4]-P2[6] - 0.042	P24-P26 + 0.0	P2[4]-P2[6] + 0.042	V

a. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 0.02V.

Table 3-12. 3.3V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
–	AGND = Vdd/2[a] CT Block Power = High	Vdd/2 - 0.017	Vdd/2 - 0.0	Vdd/2 + 0.017	V
–	AGND = 2*BandGap[a] CT Block Power = High	Not Allowed			
–	AGND = P2[4] (P2[4] = Vdd/2) CT Block Power = High	P24 - 0.009	P24 + 0.0	P24 + 0.009	V
–	AGND = BandGap[a] CT Block Power = High	BG- 0.009	BG	BG+0.009	V
–	AGND = 1.6*BandGap[a] CT Block Power = High	1.6*BG- 0.018	1.6*BG	1.6*BG+0.018	V
–	AGND Column to Column Variation (AGND=Vdd/2)[a] CT Block Power = High	-0.034	0.000	0.034	mV
–	RefHi = Vdd/2 + BandGap Ref Control Power = High	Not Allowed			
–	RefHi = 3*BandGap Ref Control Power = High	Not Allowed			
–	RefHi = 2*BandGap + P2[6] (P2[6] = 0.5V) Ref Control Power = High	Not Allowed			
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2) Ref Control Power = High	Not Allowed			
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V) Ref Control Power = High	P2[4]+P2[6] - 0.042	P2[4]+P2[6] - 0.0	P2[4]+P2[6]+ 0.042	V
–	RefHi = 2*BandGap Ref Control Power = High	2*BG - 0.053	2*BG	2*BG + 0.053	V
–	RefHi = 3.2*BandGap Ref Control Power = High	Not Allowed			
–	RefLo = Vdd/2 - BandGap Ref Control Power = High	Not Allowed			
–	RefLo = BandGap Ref Control Power = High	Not Allowed			
–	RefLo = 2*BandGap - P2[6] (P2[6] = 0.5V) Ref Control Power = High	Not Allowed			
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2) Ref Control Power = High	Not Allowed			
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V) Ref Control Power = High	P2[4]-P2[6] - 0.036	P24-P26 + 0.0	P2[4]-P2[6] + 0.036	V

a. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 0.02V.

3.3.7 DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 3-13. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.24	–	kΩ	
C_{SC}	Capacitor Unit Value (Switch Cap)	–	80	–	fF	

3.3.8 DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 3-14. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{IPOR}	Vdd Value for IPOR Trip	1.60	1.90	2.30	V	
	Vdd Value for PPOR Trip (positive ramp)					
V_{PPOR0R}	PORLEV[1:0]=00b		2.908		V	
V_{PPOR1R}	PORLEV[1:0]=01b	–	4.394	–	V	
V_{PPOR2R}	PORLEV[1:0]=10b		4.548		V	
	Vdd Value for PPOR Trip (negative ramp)					
V_{PPOR0}	PORLEV[1:0]=00b		2.816		V	
V_{PPOR1}	PORLEV[1:0]=01b	–	4.394	–	V	
V_{PPOR2}	PORLEV[1:0]=10b		4.548		V	
	PPOR Hysteresis					
V_{PH0}	PORLEV[1:0]=00b	–	92	–	mV	
V_{PH1}	PORLEV[1:0]=01b	–	0	–	mV	
V_{PH2}	PORLEV[1:0]=10b	–	0	–	mV	
	Vdd Value for LVD Trip					
V_{LVD0}	VM[2:0]=000b	2.863	2.921	2.979[a]	V	
V_{LVD1}	VM[2:0]=001b	2.963	3.023	3.083	V	
V_{LVD2}	VM[2:0]=010b	3.070	3.133	3.196	V	
V_{LVD3}	VM[2:0]=011b	3.920	4.00	4.080	V	
V_{LVD4}	VM[2:0]=100b	4.393	4.483	4.573	V	
V_{LVD5}	VM[2:0]=101b	4.550	4.643	4.736[b]	V	
V_{LVD6}	VM[2:0]=110b	4.632	4.727	4.822	V	
V_{LVD7}	VM[2:0]=111b	4.718	4.814	4.910	V	
	Vdd Value for PUMP Trip					
V_{PUMP0}	VM[2:0]=000b	2.963	3.023	3.083	V	
V_{PUMP1}	VM[2:0]=001b	3.033	3.095	3.157	V	
V_{PUMP2}	VM[2:0]=010b	3.185	3.250	3.315	V	
V_{PUMP3}	VM[2:0]=011b	4.110	4.194	4.278	V	
V_{PUMP4}	VM[2:0]=100b	4.550	4.643	4.736	V	
V_{PUMP5}	VM[2:0]=101b	4.632	4.727	4.822	V	
V_{PUMP6}	VM[2:0]=110b	4.719	4.815	4.911	V	
V_{PUMP7}	VM[2:0]=111b	4.900	5.000	5.100	V	

a. Always greater than 50 mV above PPOR (PORLEV=00) for falling supply.
b. Always greater than 50 mV above PPOR (PORLEV=10) for falling supply.

3.3.9 DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 3-15. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{CCP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss+0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[a]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

a. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (and so forth to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).

The PSoC devices use an adaptive algorithm to enhance endurance over the industrial temperature range (-40°C to +85°C ambient). Any temperature range within a 50°C span between 0°C and 85°C is considered constant with respect to endurance enhancements. For instance, if room temperature (25°C) is the nominal operating temperature, then the range from 0°C to 50°C can be approximated by the constant value 25 and a temperature sensor is not needed.

For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

3.4 AC Electrical Characteristics

3.4.1 AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 3-16. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO}	Internal Main Oscillator Frequency	23.4	24	24.6[a,c]	MHz	Trimmed. Utilizing factory trim values.
F_{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.6[a,b]	MHz	
F_{CPU2}	CPU Frequency (3.3V Nominal)	0.93	12	12.3[b,c]	MHz	
F_{48M}	Digital PSoC Block Frequency	0	48	49.2[a,b,d]	MHz	Refer to the AC Digital Block Specifications below.
F_{24M}	Digital PSoC Block Frequency	0	24	24.6[b,e,d]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{PLL}	PLL Frequency	–	23.986	–	MHz	Is a multiple (x732) of crystal frequency.
Jitter24M2	24 MHz Period Jitter (PLL)	600	–		ps	
$T_{PLLSLEW}$	PLL Lock Time	0.5	–	10	ms	
$T_{PLLSLEWLOW}$	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	
T_{OS}	External Crystal Oscillator Startup to 1%	–	250	500	ms	
T_{OSACC}	External Crystal Oscillator Startup to 100 ppm	–	300	600[f]	ms	
Jitter32k	32 kHz Period Jitter	–	100		ns	
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2[a,c]	MHz	Trimmed. Utilizing factory trim values.
Jitter24M1	24 MHz Period Jitter (IMO)	–	600		ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12	MHz	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	

a. 4.75V < Vdd < 5.25V.
b. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
c. 3.0V < Vdd < 3.6V.
d. See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on maximum frequency for User Modules.
e. 3.0V < 5.25V.
f. The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 uW maximum drive level 32.768 kHz crystal. 3.0V ≤ Vdd ≤ 5.5V, -40 ^{0}C ≤ T_A ≤ 85 ^{0}C.

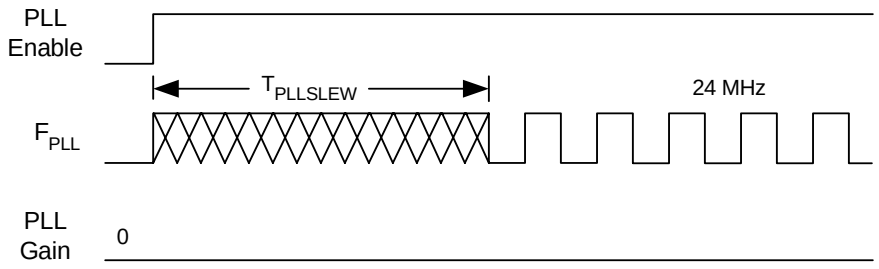


Figure 3-2. PLL Lock Timing Diagram

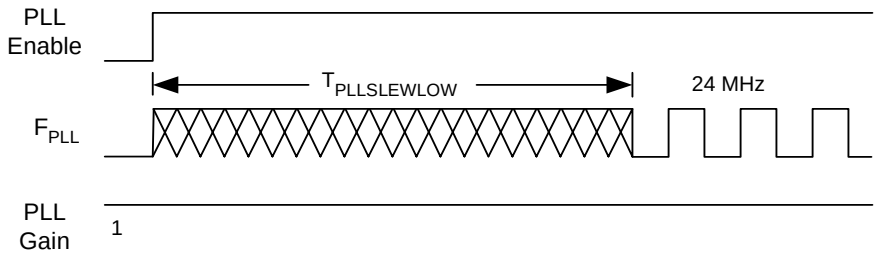


Figure 3-3. PLL Lock for Low Gain Setting Timing Diagram

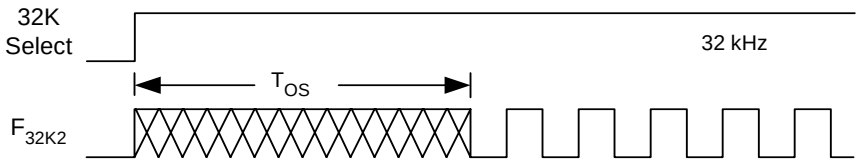


Figure 3-4. External Crystal Oscillator Startup Timing Diagram

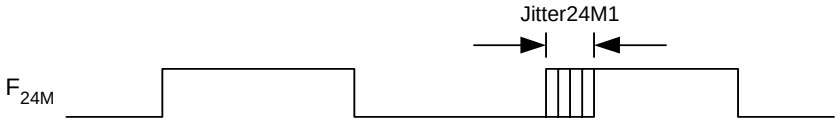


Figure 3-5. 24 MHz Period Jitter (IMO) Timing Diagram

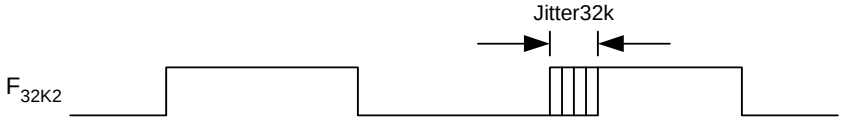


Figure 3-6. 32 kHz Period Jitter (ECO) Timing Diagram

3.4.2 AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 3-17. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12	MHz	
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.5V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.5V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	Vdd = 3 to 5.5V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	Vdd = 3 to 5.5V, 10% - 90%

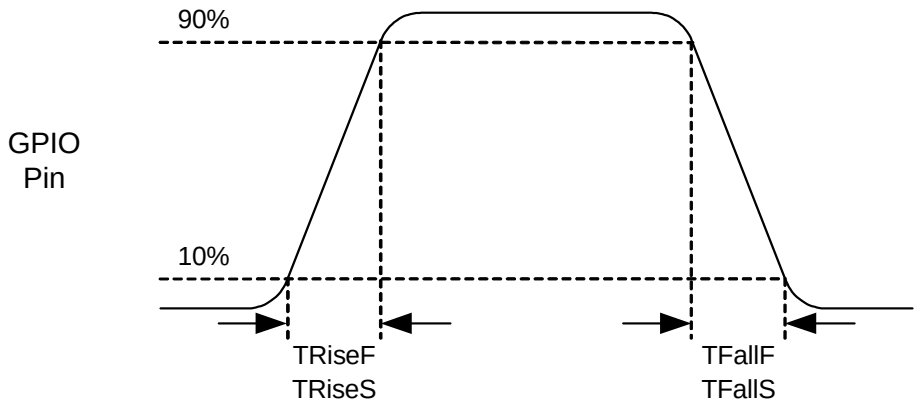


Figure 3-7. GPIO Timing Diagram

3.4.3 AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Table 3-18. 5V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time to 0.1% for a 1V Step (10 pF load, Unity Gain)					Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	–	–	3.9	µs	
	Power = Low, Opamp Bias = High	–			µs	
	Power = Medium	–			µs	
	Power = Medium, Opamp Bias = High	–	–	0.72	µs	
	Power = High	–			µs	
	Power = High, Opamp Bias = High	–	–	0.62	µs	
T_{SOA}	Falling Settling Time to 0.1% for a 1V Step (10 pF load, Unity Gain)					Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	–	–	5.9	µs	
	Power = Low, Opamp Bias = High	–			µs	
	Power = Medium	–			µs	
	Power = Medium, Opamp Bias = High	–	–	0.92	µs	
	Power = High	–			µs	
	Power = High, Opamp Bias = High	–	–	0.72	µs	
SR_{ROA}	Rising Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain)					Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	0.15	–		V/µs	
	Power = Low, Opamp Bias = High				V/µs	
	Power = Medium				V/µs	
	Power = Medium, Opamp Bias = High	1.7	–		V/µs	
	Power = High				V/µs	
	Power = High, Opamp Bias = High	6.5	–		V/µs	
SR_{FOA}	Falling Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain)					Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	0.01	–		V/µs	
	Power = Low, Opamp Bias = High				V/µs	
	Power = Medium				V/µs	
	Power = Medium, Opamp Bias = High	0.5	–		V/µs	
	Power = High				V/µs	
	Power = High, Opamp Bias = High	4.0	–		V/µs	
BW_{OA}	Gain Bandwidth Product					Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	0.75	–		MHz	
	Power = Low, Opamp Bias = High				MHz	
	Power = Medium				MHz	
	Power = Medium, Opamp Bias = High	3.1	–		MHz	
	Power = High				MHz	
	Power = High, Opamp Bias = High	5.4	–		MHz	
E_{NOA}	Noise at 1 kHz	–	200	–	nV/rt-Hz	

Table 3-19. 3.3V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time to 0.1% of a 1V Step (10 pF load, Unity Gain)					Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	–	–	3.92	µs	
	Power = Low, Opamp Bias = High	–			µs	
	Power = Medium	–			µs	
	Power = Medium, Opamp Bias = High	–	–	0.72	µs	
	Power = High (3.3 Volt High Bias Operation not supported)	–	–	–	µs	
	Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	–	–	–	µs	
T_{SOA}	Falling Settling Time to 0.1% of a 1V Step (10 pF load, Unity Gain)					Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	–	–	5.41	µs	
	Power = Low, Opamp Bias = High	–			µs	
	Power = Medium	–			µs	
	Power = Medium, Opamp Bias = High	–	–	0.72	µs	
	Power = High (3.3 Volt High Bias Operation not supported)	–	–	–	µs	
	Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	–	–	–	µs	
SR_{ROA}	Rising Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain)					Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	0.31	–		V/µs	
	Power = Low, Opamp Bias = High				V/µs	
	Power = Medium				V/µs	
	Power = Medium, Opamp Bias = High	2.7	–		V/µs	
	Power = High (3.3 Volt High Bias Operation not supported)	–	–	–	V/µs	
	Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	–	–	–	V/µs	
SR_{FOA}	Falling Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain)					Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	0.24	–		V/µs	
	Power = Low, Opamp Bias = High				V/µs	
	Power = Medium				V/µs	
	Power = Medium, Opamp Bias = High	1.8	–		V/µs	
	Power = High (3.3 Volt High Bias Operation not supported)	–	–	–	V/µs	
	Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	–	–	–	V/µs	
BW_{OA}	Gain Bandwidth Product					Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	0.67	–		MHz	
	Power = Low, Opamp Bias = High				MHz	
	Power = Medium				MHz	
	Power = Medium, Opamp Bias = High	2.8	–		MHz	
	Power = High (3.3 Volt High Bias Operation not supported)	–	–	–	MHz	
	Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	–	–	–	MHz	
E_{NOA}	Noise at 1 kHz (Turbo Medium)	–	200	–	nV/rt-Hz	

3.4.4 AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 3-20. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All Functions	Maximum Block Clocking Frequency (> 4.75V)			48		4.75V < Vdd < 5.25V.
	Maximum Block Clocking Frequency (< 4.75V)			24		3.0V < Vdd < 4.75V.
Timer	Capture Pulse Width	50[a]	–	–	ns	
	Maximum Frequency, No Capture	–	–	48	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, With Capture	–	–	24	MHz	
Counter	Enable Pulse Width	50[a]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	48	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, Enable Input	–	–	24	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[a]	–	–	ns	
	Disable Mode	50[a]	–	–	ns	
	Maximum Frequency	–	–	48	MHz	4.75V < Vdd < 5.25V.
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	48	MHz	4.75V < Vdd < 5.25V.
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8	MHz	
SPIS	Maximum Input Clock Frequency	–	–	4	ns	
	Width of SS_ Negated Between Transmissions	50[a]	–	–	ns	
Transmitter	Maximum Input Clock Frequency	–	–	16	MHz	
Receiver	Maximum Input Clock Frequency	–	16	48	MHz	4.75V < Vdd < 5.25V.

a. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

3.4.5 AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 3-21. 5V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	–	–	4	µs	
	Power = High	–	–	4	µs	
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	–	–	3.4	µs	
	Power = High	–	–	3.4	µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load					
	Power = Low	0.5	–	–	V/µs	
	Power = High	0.5	–	–	V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load					
	Power = Low	0.55	–	–	V/µs	
	Power = High	0.55	–	–	V/µs	
BW_{OB}	Small Signal Bandwidth, 20mV_{pp}, 3dB BW, 100pF Load					
	Power = Low	0.8	–	–	MHz	
	Power = High	0.8	–	–	MHz	
BW_{OB}	Large Signal Bandwidth, 1V_{pp}, 3dB BW, 100pF Load					
	Power = Low	300	–	–	kHz	
	Power = High	300	–	–	kHz	

Table 3-22. 3.3V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	–	–	4.7	µs	
	Power = High	–	–	4.7	µs	
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	–	–	4	µs	
	Power = High	–	–	4	µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load					
	Power = Low	.36	–	–	V/µs	
	Power = High	.36	–	–	V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load					
	Power = Low	.4	–	–	V/µs	
	Power = High	.4	–	–	V/µs	
BW_{OB}	Small Signal Bandwidth, 20mV_{pp}, 3dB BW, 100pF Load					
	Power = Low	0.7	–	–	MHz	
	Power = High	0.7	–	–	MHz	
BW_{OB}	Large Signal Bandwidth, 1V_{pp}, 3dB BW, 100pF Load					
	Power = Low	200	–	–	kHz	
	Power = High	200	–	–	kHz	

3.4.6 AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 3-23. 5V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0	–	24.24	MHz	
–	High Period	20.6	–	–	ns	
–	Low Period	20.6	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

Table 3-24. 3.3V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU Clock divide by 1[a]	0	–	12	MHz	
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater[b]	0	–	24	MHz	
–	High Period with CPU Clock divide by 1	41.7	–	–	ns	
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

a. Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
b. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider will ensure that the fifty percent duty cycle requirement is met.

3.4.7 AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 3-25. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	15	–	ms	
T_{WRITE}	Flash Block Write Time	–	30	–	ms	
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	

3.4.8 AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 3-26. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz	
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs	
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs	
$T_{SUSTAI2C}$	Set-up Time for a Repeated START Condition	4.7	–	0.6	–	µs	
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs	
$T_{SUDATI2C}$	Data Set-up Time	250	–	100[a]	–	ns	
$T_{SUSTOI2C}$	Set-up Time for STOP Condition	4.0	–	0.6	–	µs	
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs	
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns	

a. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

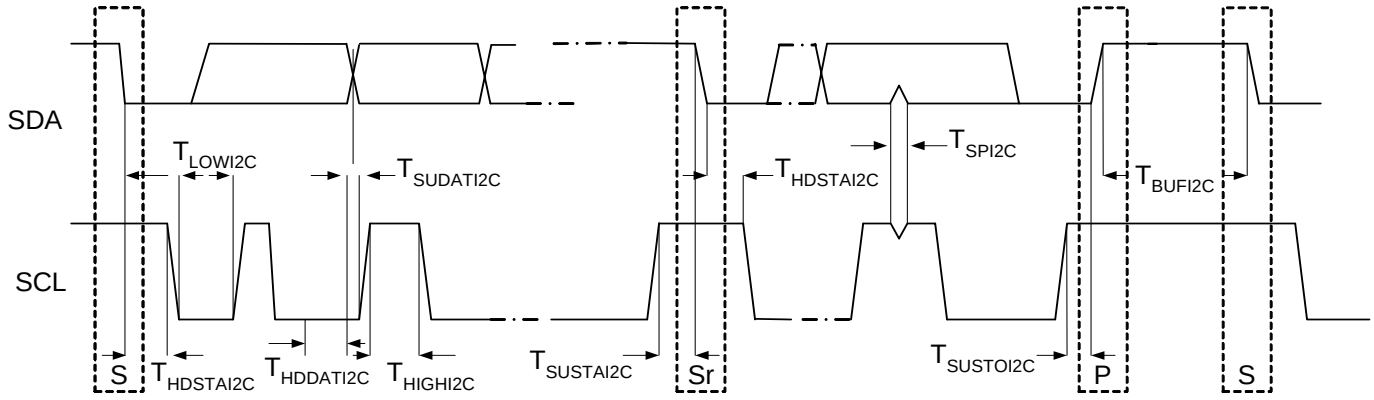


Figure 3-8. Definition for Timing for Fast/Standard Mode on the I²C Bus

4. Packaging Information

4.1 Packaging Dimensions

This chapter illustrates the packaging specifications for the CY8C27x66 PSoC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

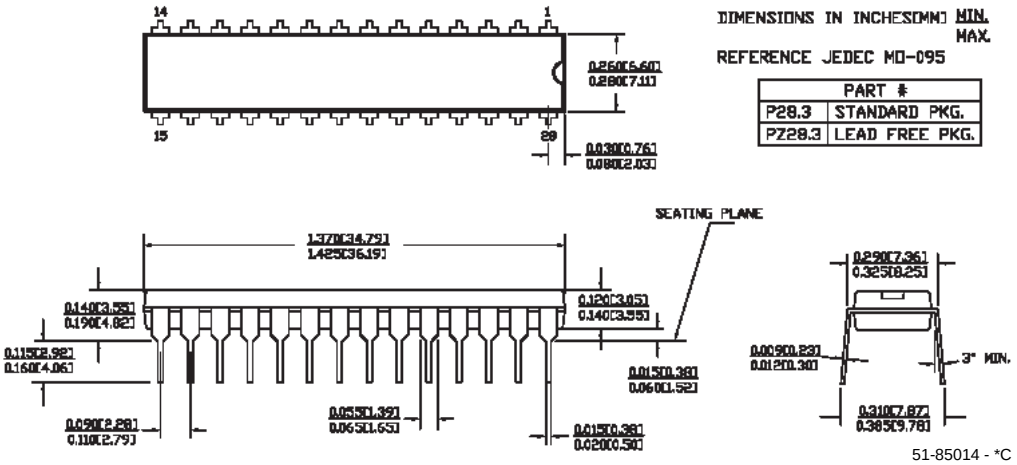


Figure 4-1. 28-Lead (300-Mil) Molded DIP

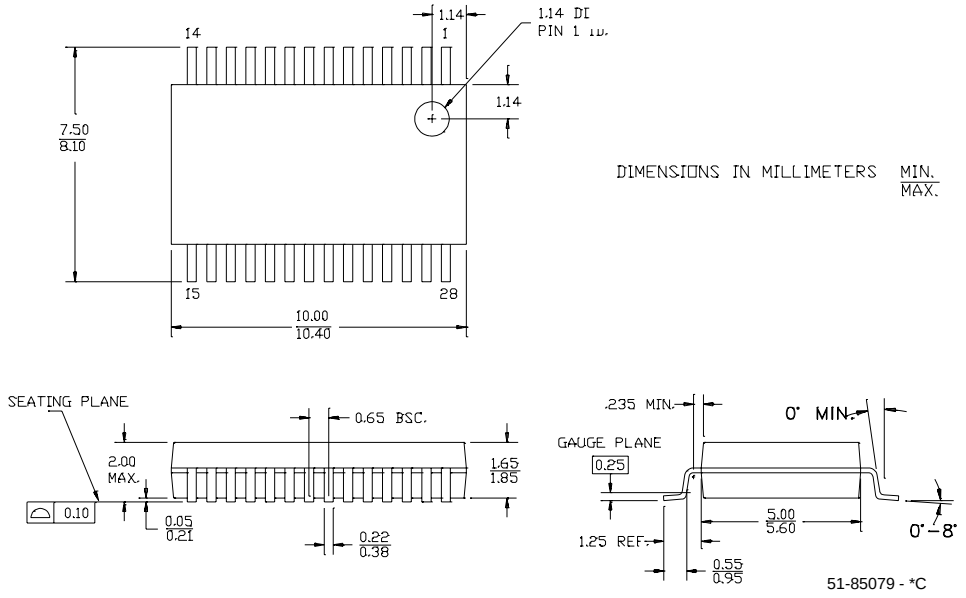


Figure 4-2. 28-Lead (210-Mil) SSOP

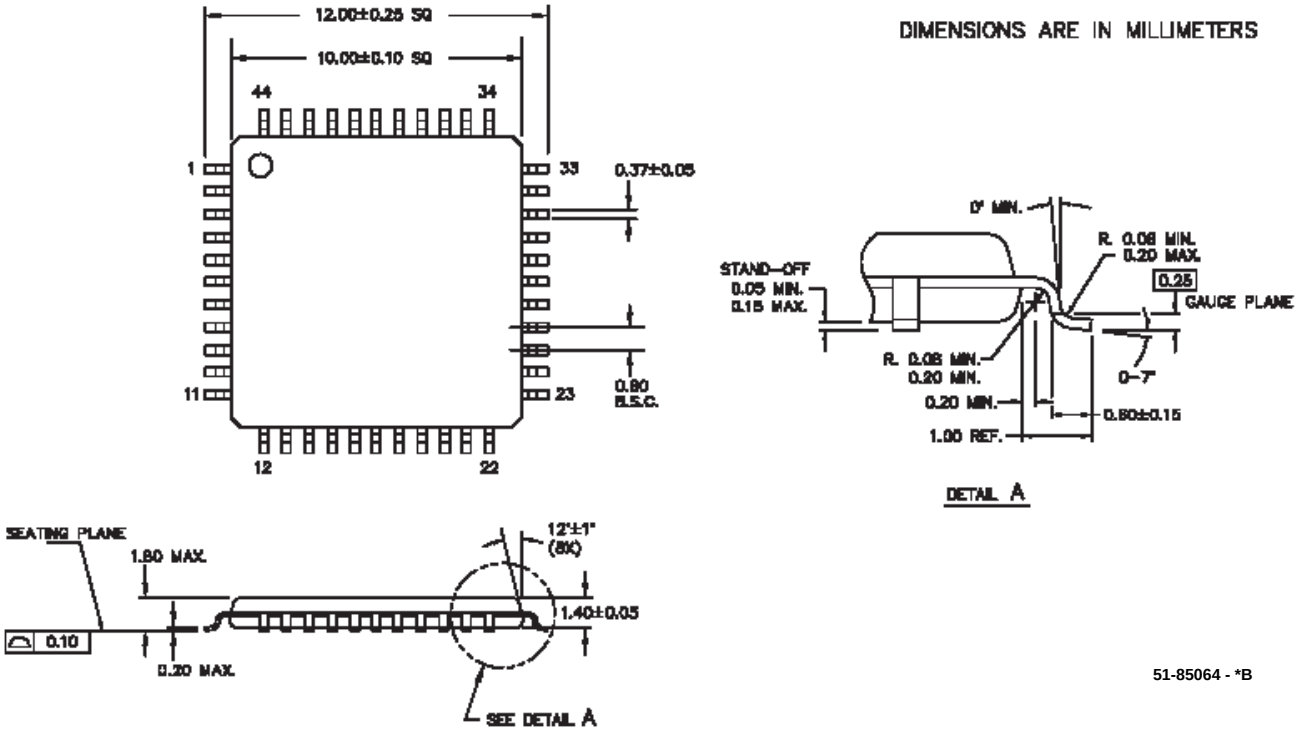


Figure 4-3. 44-Lead TQFP

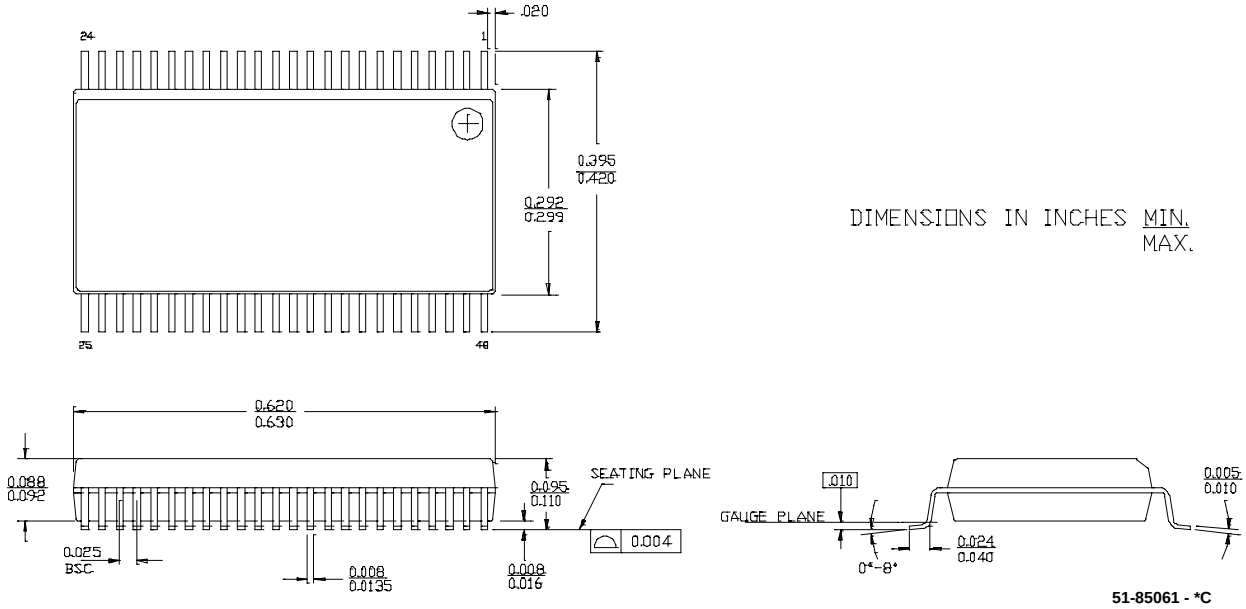


Figure 4-4. 48-Lead (300-Mil) SSOP

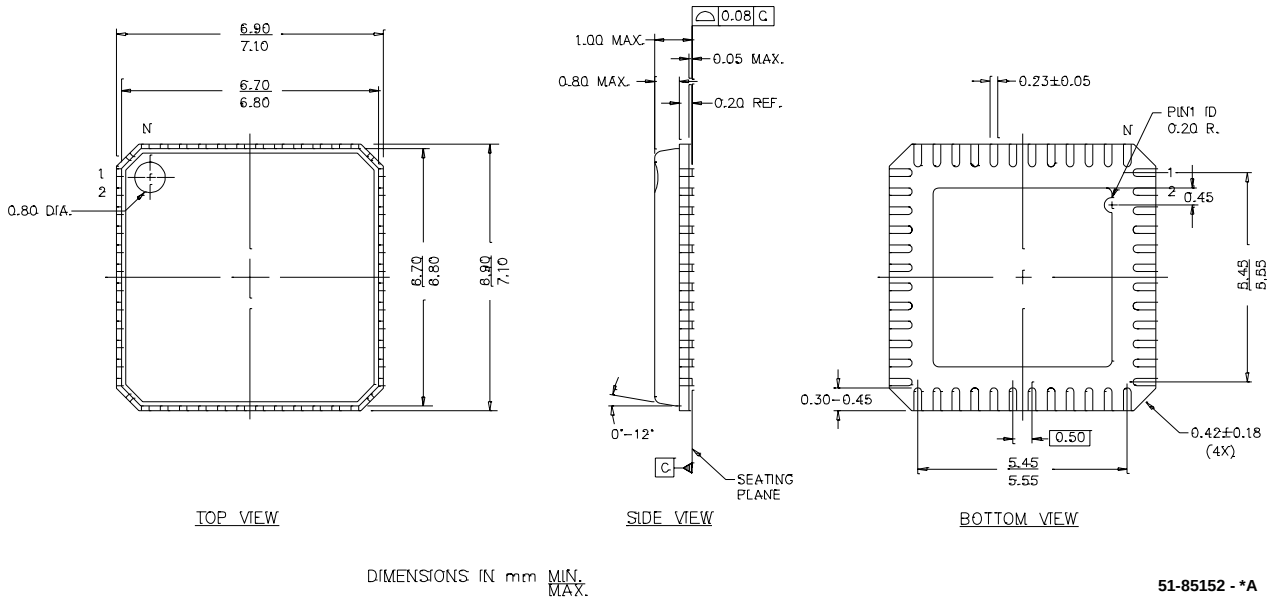


Figure 4-5. 48-Lead (7x7 mm) MLF

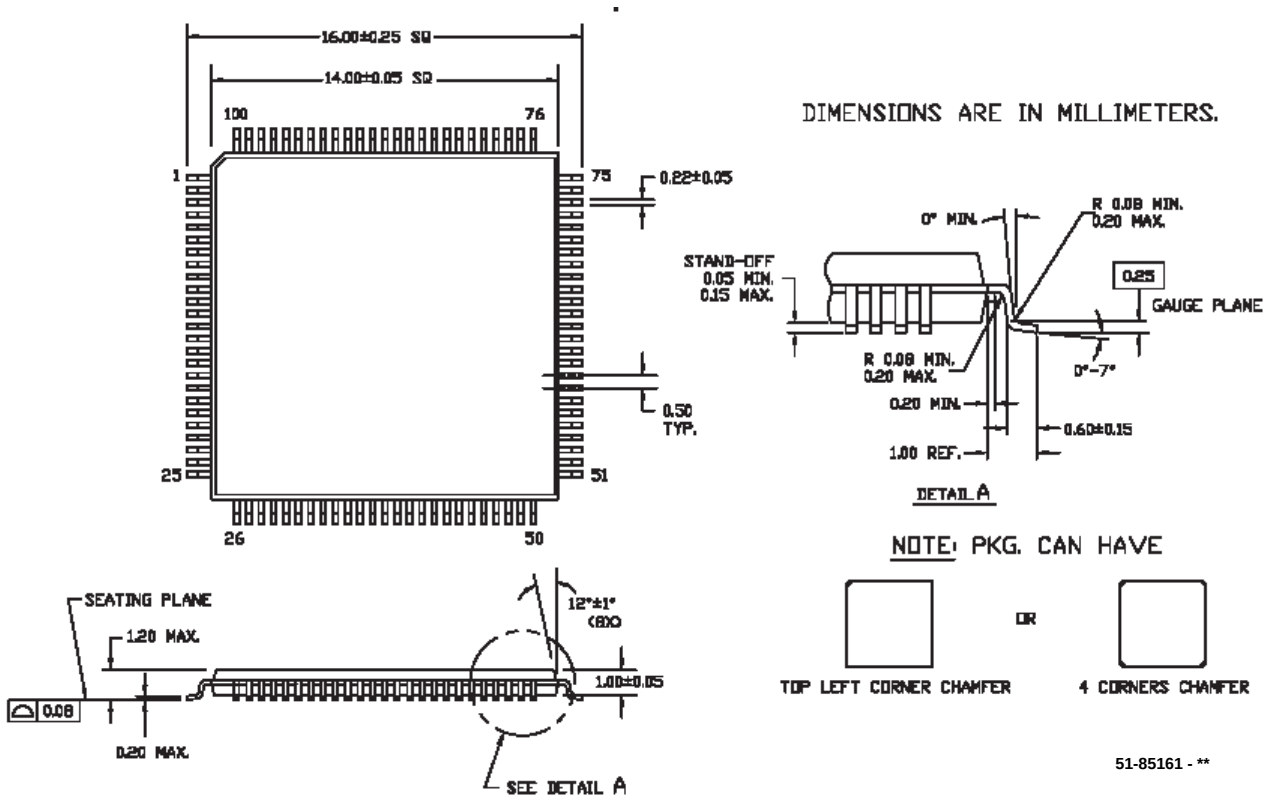


Figure 4-6. 100-Lead TQFP

4.2 Thermal Impedances

Table 4-1. Thermal Impedances per Package

Package	Typical θ
28 PDIP	69 °C/W
28 SSOP	96 °C/W
44 TQFP	60 °C/W
48 SSOP	69 °C/W
48 MLF	28 °C/W
100 TQFP	48 °C/W

4.3 Capacitance on Crystal Pins

Table 4-2: Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
28 PDIP	3.5 pF
28 SSOP	2.8 pF
44 TQFP	2.6 pF
48 SSOP	3.3 pF
48 MLF	1.8 pF
100 TQFP	3.1 pF

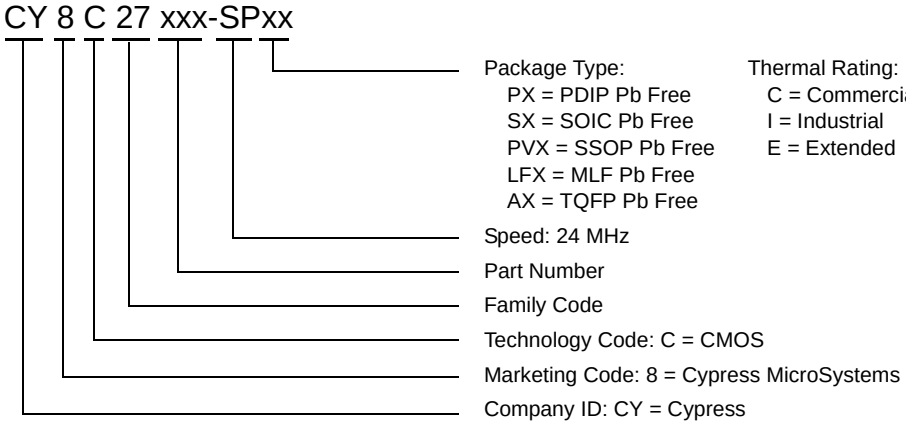
5. Ordering Information

The following table lists the CY8C27x66 PSoC Device family's key package features and ordering codes.

Table 5-1. CY8C27x66 PSoC Device Family Key Features and Ordering Information

Package	Ordering Code	Flash (Kbytes)	RAM (Bytes)	Switch Mode Pump	Temperature Range	Digital PSoC Blocks (Rows of 4)	Analog PSoC Blocks (Columns of 3)	Digital IO Pins	Analog Inputs	Analog Outputs	XRES Pin
28 Pin (300 Mil) DIP	CY8C27466-24PXI	32	2K	Yes	-40°C to +85°C	8	12	24	12	4	Yes
28 Pin (210 Mil) SSOP	CY8C27466-24PVXI	32	2K	Yes	-40°C to +85°C	8	12	24	12	4	Yes
28 Pin (210 Mil) SSOP (Tape and Reel)	CY8C27466-24PVXIT	32	2K	Yes	-40°C to +85°C	8	12	24	12	4	Yes
44 Pin TQFP	CY8C27566-24AXI	32	2K	Yes	-40°C to +85°C	8	12	40	12	4	Yes
44 Pin TQFP (Tape and Reel)	CY8C27566-24AXIT	32	2K	Yes	-40°C to +85°C	8	12	40	12	4	Yes
48 Pin (300 Mil) SSOP	CY8C27666-24PVXI	32	2K	Yes	-40°C to +85°C	8	12	44	12	4	Yes
48 Pin (300 Mil) SSOP (Tape and Reel)	CY8C27666-24PVXIT	32	2K	Yes	-40°C to +85°C	8	12	44	12	4	Yes
48 Pin MLF	CY8C27666-24LFXI	32	2K	Yes	-40°C to +85°C	8	12	44	12	4	Yes
100 Pin TQFP	CY8C27866-24AXI	32	2K	Yes	-40°C to +85°C	8	12	64	12	4	Yes

5.1 Ordering Code Definitions



6. Sales and Service Information

To obtain information about Cypress MicroSystems or PSoC sales and technical support, reference the following information or go to the section titled “Getting Started” on page 4 in this document.

Cypress MicroSystems
2700 162nd Street SW
Building D
Lynnwood, WA 98037

Phone: 800.669.0557
Facsimile: 425.787.4641

Web Sites: Company Information – http://www.cypress.com
Sales – http://www.cypress.com/aboutus/sales_locations.cfm
Technical Support – http://www.cypress.com/support/login.cfm

6.1 Revision History

Table 6-1. CY8C27x66 Data Sheet Revision History

Document Title: CY8C27466, CY8C27566, CY8C27666, and CY8C27866 PSoC™ Mixed Signal Array Preliminary Data Sheet Document Number: 38-12019				
Revision	**ECN #**	**Issue Date**	**Origin of Change**	**Description of Change**
**	133204	02/09/2004	SFV	New silicon and document (Revision **).
*A	209441	03/15/2004	SFV	Changed block diagram on first page to match feature set description.
Distribution: External/Public			**Posting**: None	

6.2 Copyrights