CY62157DV30
MoBL®

8-Mbit (512K x 16) MoBL® Static RAM

Features

- **Temperature Ranges**
  - **Industrial: –40°C to 85°C**
  - **Automotive: –40°C to 125°C (Preliminary)**
- **Very high speed: 45 ns, 55 ns and 70 ns**
- **Wide voltage range: 2.20V – 3.60V**
- **Pin-compatible with CY62157CV25, CY62157CV30, and CY62157CV33**
- **Ultra-low active power**
  - **Typical active current: 1.5 mA @ f = 1 MHz**
  - **Typical active current: 12 mA @ f = f_{max}**
- **Ultra-low standby power**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Packages offered: 48-ball BGA, 48-pin TSOPI, and 44-pin TSOPII**

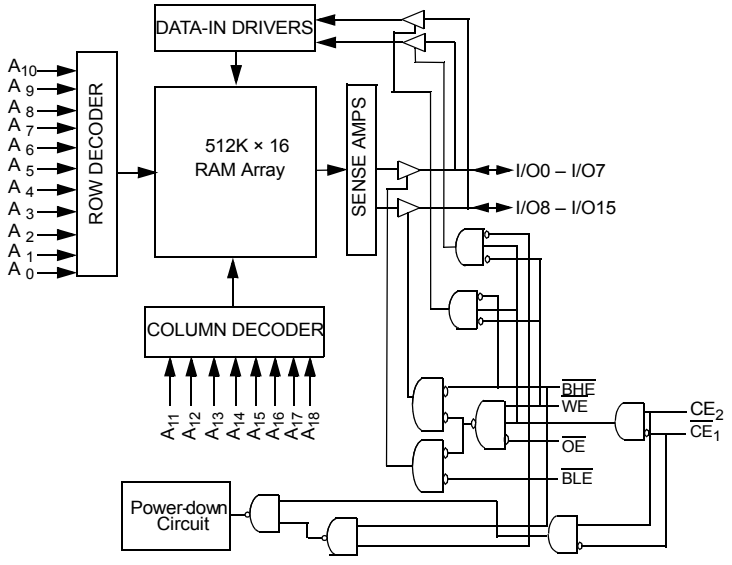
Functional Description[1]

The CY62157DV30 is a high-performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones.The device also has an automatic power-down feature that significantly reduces power consumption. The device can also be put into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE}_1$HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{18}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table for a complete description of read and write modes.

Logic Block Diagram



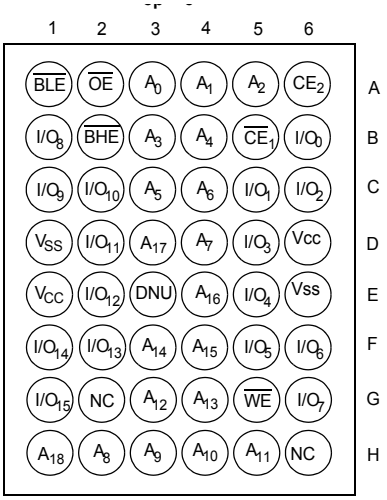
Notes:
1. For best practice recommendations, please refer to the Cypress application note entitled *System Design Guidelines*, which is available at http://www.cypress.com.

Product Portfolio

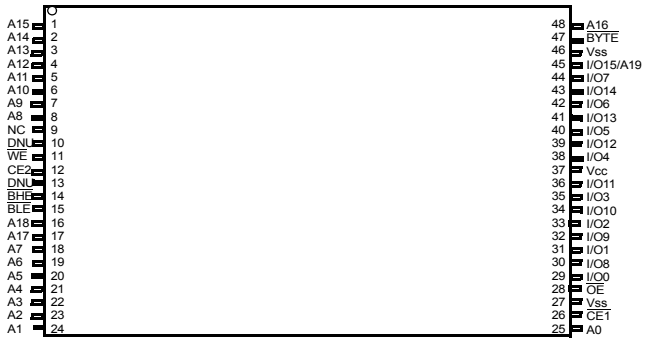
Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC}, (mA)				Standby I_{SB2}, (μA)	
						f = 1MHz		f = f_{max}			
		Min.	Typ.[2]	Max.		Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.
CY62157DV30L	Industrial	2.2	3.0	3.6	45, 55, 70	1.5	3	12	20	2	20
CY62157DV30LL	Industrial	2.2	3.0	3.6	45, 55, 70	1.5	3	12	15	2	8
CY62157DV30L	Automotive[3]	2.2	3.0	3.6	55	1.5	3	12	20	2	50

Pin Configuration[4, 5, 6, 7]

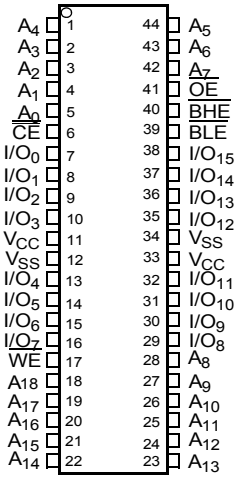
FBGA



48TSOPI
Top View



44 TSOP II
Top View



Notes:
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ.)}$, T_A = 25°C.
3. Automotive data is PRELIMINARY. Shaded areas of the datasheet contain PRELIMINARY information.
4. NC pins are not internally connected on the die.
5. DNU pins have to be left floating.
6. The BYTE pin in the 48-TSOPI package has to be tied HIGH to use the device as a 512K × 16 SRAM. The 48-TSOPI package can also be used as a 1M × 8 SRAM by tying the BYTE signal LOW. For 1M × 8 Functionality, please refer to the CY62158DV30 datasheet. In the 1M × 8 configuration, Pin 45 is A19.
7. The 44-TSOPII package device has only one chip enable pin (CE).

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to + 150°C

Ambient Temperature with Power Applied.....–55°C to + 125°C

Supply Voltage to Ground Potential .....–0.3V to + $V_{CC(max)}$ + 0.3V

DC Voltage Applied to Outputs in High-Z State[8, 9].....–0.3V to $V_{CC(max)}$ + 0.3V

DC Input Voltage[8, 9] .....–0.3V to $V_{CC(max)}$ + 0.3V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current.....>200 mA

Operating Range

Device	Range	Ambient Temperature (T_A)	V_{CC}[10]
CY62157DV30L	Industrial	–40°C to +85°C	2.20V to 3.60V
CY62157DV30LL			
CY62157DV30L	Automotive (Preliminary)	–40°C to +125°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			CY62157DV30 Min.	CY62157DV30 Typ.[2]	CY62157DV30 Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA	V_{CC} = 2.20V		2.0			V
		I_{OH} = –1.0 mA	V_{CC} = 2.70V		2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	V_{CC} = 2.20V				0.4	V
		I_{OL} = 2.1mA	V_{CC} = 2.70V				0.4	V
V_{IH}	Input HIGH Voltage	V_{CC} = 2.2V to 2.7V			1.8		V_{CC} + 0.3V	V
		V_{CC}= 2.7V to 3.6V			2.2		V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage	V_{CC} = 2.2V to 2.7V			–0.3		0.6	V
		V_{CC}= 2.7V to 3.6V			–0.3		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	Industrial		–1		+1	µA
			Automotive		-4		+4	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	Industrial		–1		+1	µA
			Automotive		-4		+4	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = 1/t_{RC}	V_{CC} = V_{CCmax} I_{OUT} = 0 mA CMOS levels	L		12	20	mA
				LL			15	mA
		f = 1 MHz		L		1.5	3	mA
				LL			3	mA
I_{SB1}	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE}_1$ ≥ V_{CC}–0.2V, CE_2≤ 0.2V V_{IN}≥V_{CC}–0.2V, V_{IN}≤0.2V) f = f_{MAX} (Address and Data Only), ___ f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$ and $\overline{BLE}$), V_{CC}=3.60V	Industrial	L		2	20	µA
				LL		2	8	
			Automotive	L			50	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE}_1$ ≥ V_{CC} – 0.2V or CE_2 ≤ 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = 3.60V	Industrial	L		2	20	µA
				LL		2	8	
			Automotive	L			50	

Notes:
8. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
9. $V_{IH(max)}$= V_{CC}+0.75V for pulse duration less than 20 ns.
10. Full device AC operation assumes a 100 µs ramp time from 0 to V_{cc}(min) and 200 µs wait time after V_{cc} stabilization.

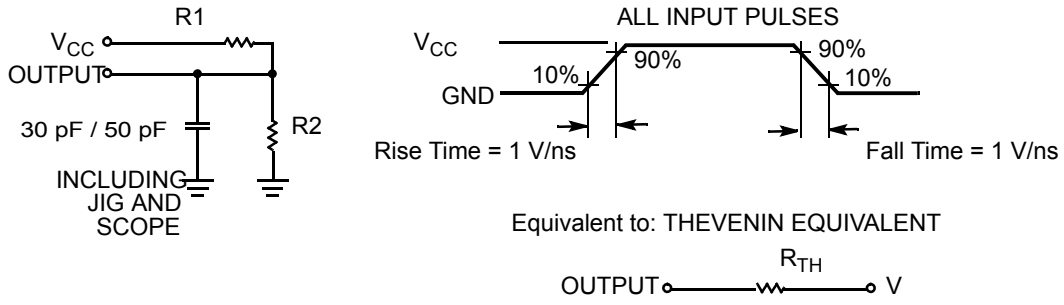
Capacitance[11, 12]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output Capacitance		10	pF

Thermal Resistance[11]

Parameter	Description	Test Conditions	BGA	TSOP II	TSOP I	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	72	75.13	74.88	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		8.86	8.95	8.6	°C/W

AC Test Loads and Waveforms[13]



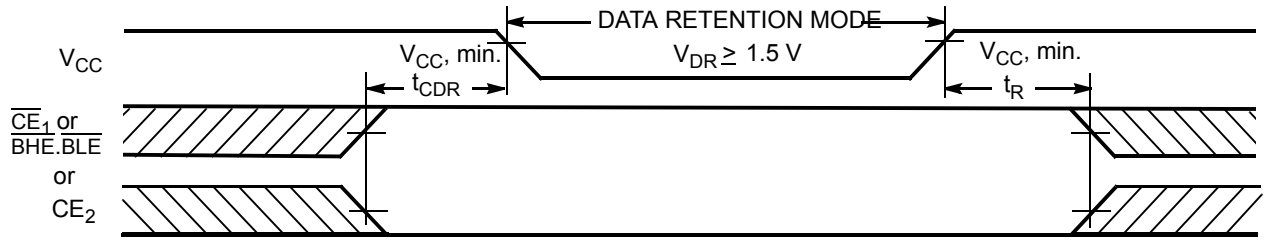
Parameters	2.50V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions		Min.	Typ.[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			1.5			V
I_{CCDR}	Data Retention Current	V_{CC}= 1.5V $\overline{CE_1} \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	Industrial (L)			10	µA
			Industrial (LL)			4	
			Automotive (L)			25	
t_{CDR}[11]	Chip Deselect to Data Retention Time			0			ns
t_R[14]	Operation Recovery Time			t_{RC}			ns

Notes:
11. Tested initially and after any design or process changes that may affect these parameters.
12. The input capacitance on the CE_2 pin of the FBGA and 48TSOPI packages and on the $\overline{BHE}$ pin of the 44TSOPII package is 15 pF.
13. Test condition for the 45 ns part is a load capacitance of 30 pF.
14. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ us or stable at $V_{CC(min.)} \geq 100$ us.

Data Retention Waveform[15]



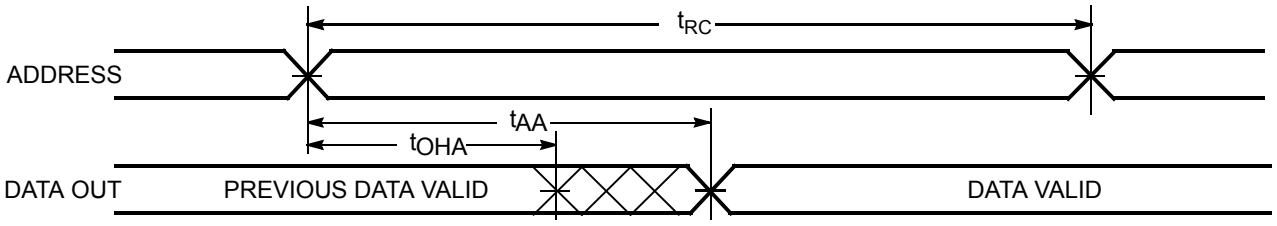
Switching Characteristics Over the Operating Range [16]

Parameter	Description	45 ns [13]		55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	45		55		70		ns
t_{AA}	Address to Data Valid		45		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		10		ns
t_{ACE}	$\overline{CE_1}$ LOW and CE_2 HIGH to Data Valid		45		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		25		35	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[17]	5		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[17, 18]		15		20		25	ns
t_{LZCE}	$\overline{CE_1}$ LOW and CE_2 HIGH to Low Z[17]	10		10		10		ns
t_{HZCE}	$\overline{CE_1}$ HIGH and CE_2 LOW to High Z[17, 18]		20		20		25	ns
t_{PU}	$\overline{CE_1}$ LOW and CE_2 HIGH to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE_1}$ HIGH and CE_2 LOW to Power-Down		45		55		70	ns
t_{DBE}	BLE / BHE LOW to Data Valid		45		55		70	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low Z[17]	10		10		10		ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to HIGH Z[17, 18]		15		20		25	ns
Write Cycle[19]								
t_{WC}	Write Cycle Time	45		55		70		ns
t_{SCE}	$\overline{CE_1}$ LOW and CE_2 HIGH to Write End	40		40		60		ns
t_{AW}	Address Set-up to Write End	40		40		60		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	35		40		45		ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Write End	40		40		60		ns
t_{SD}	Data Set-up to Write End	25		25		30		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[17, 18]		15		20		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[17]	10		10		10		ns

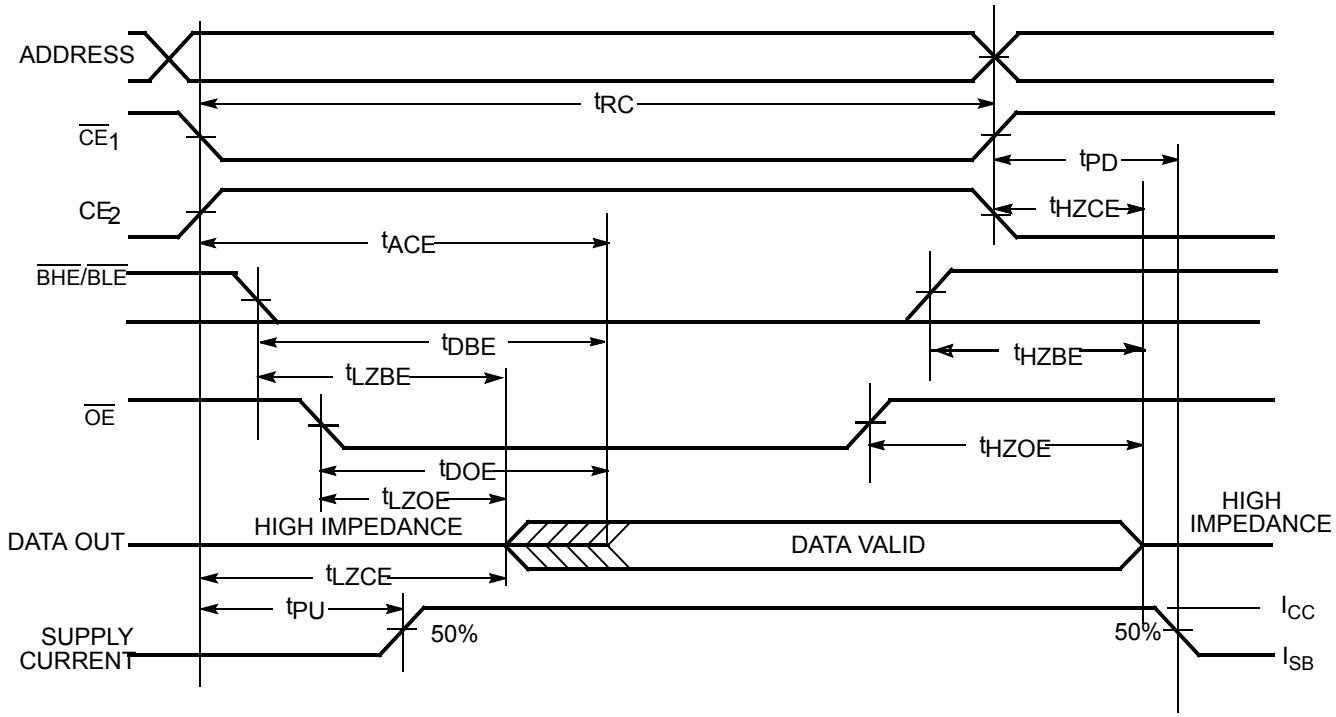
Notes:
15. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.
16. Test conditions for all parameters other than three-state parameters assume signal transition time of 3 ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
17. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
18. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedence state.
19. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE_1} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)[20, 21]



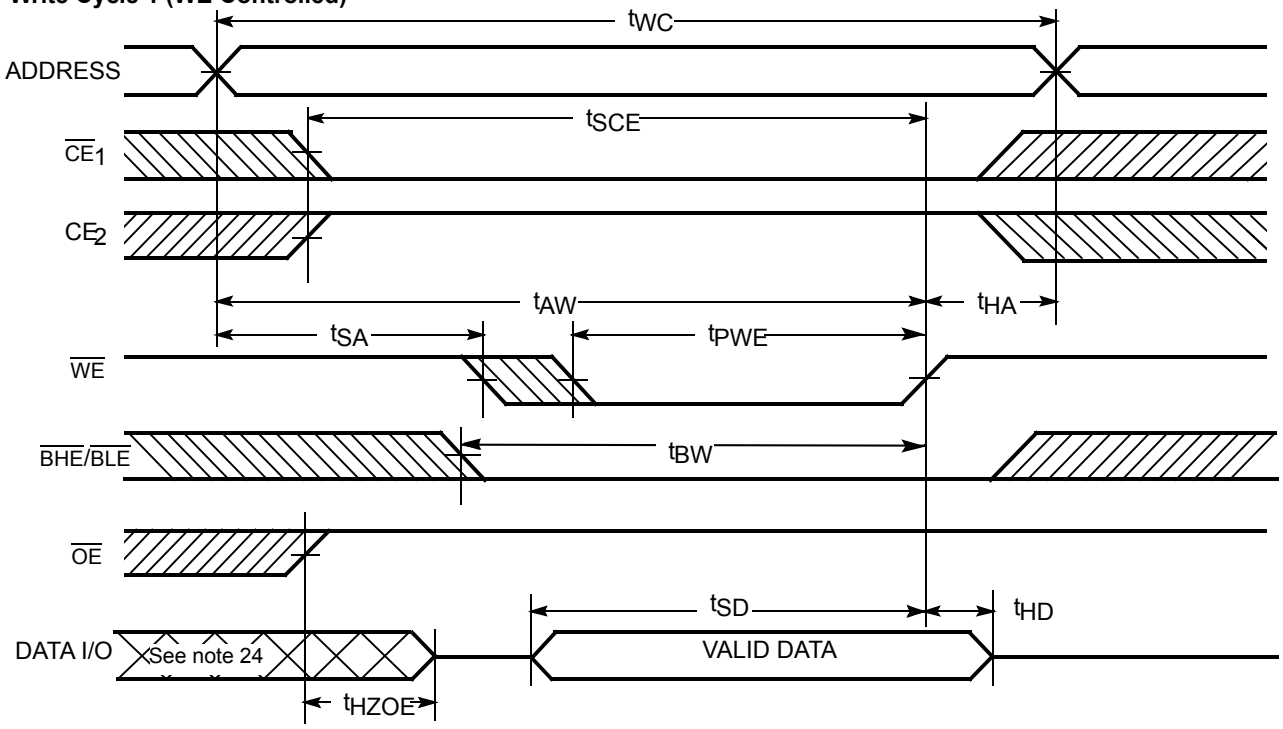
Read Cycle 2 ($\overline{OE}$ Controlled)[21, 22]



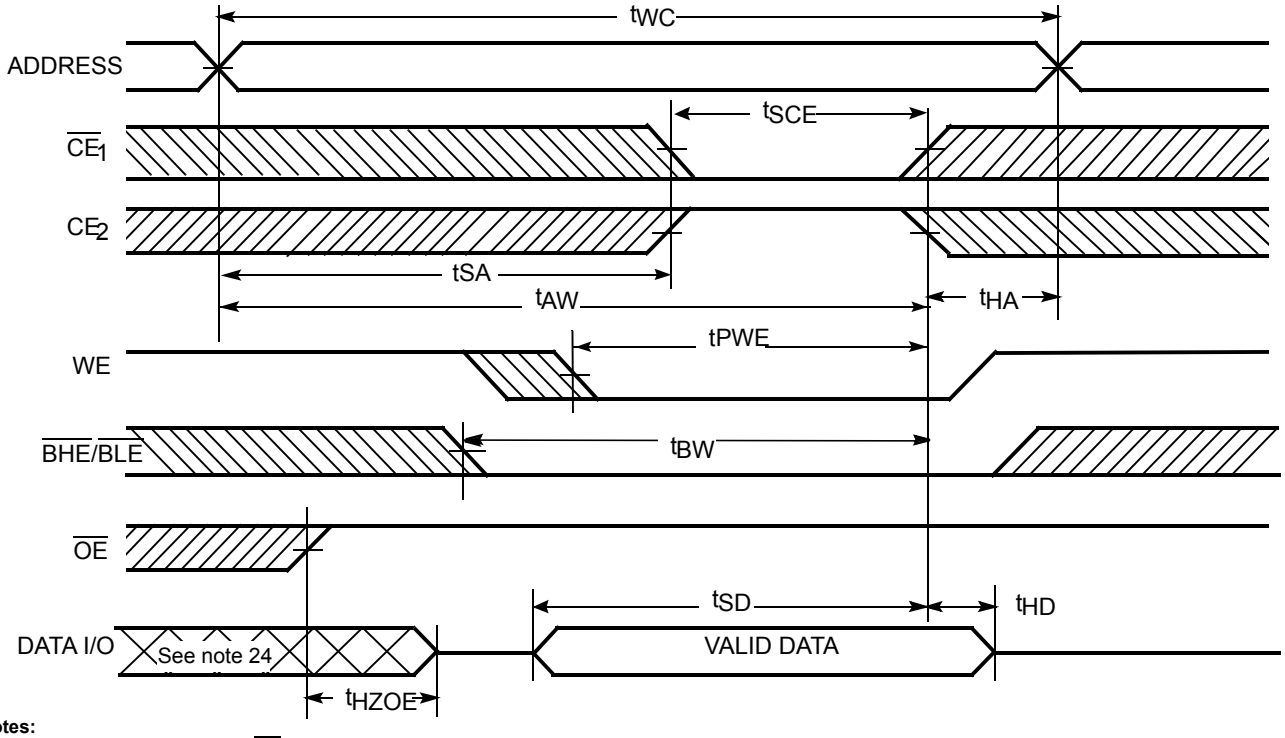
Notes:
20. The device is continuously selected. OE, $\overline{CE_1} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$.
21. $\overline{WE}$ is HIGH for read cycle.
22. Address valid prior to or coincident with $\overline{CE_1}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Write Cycle 1 ($\overline{WE}$ Controlled)[19, 23, 24, 25]



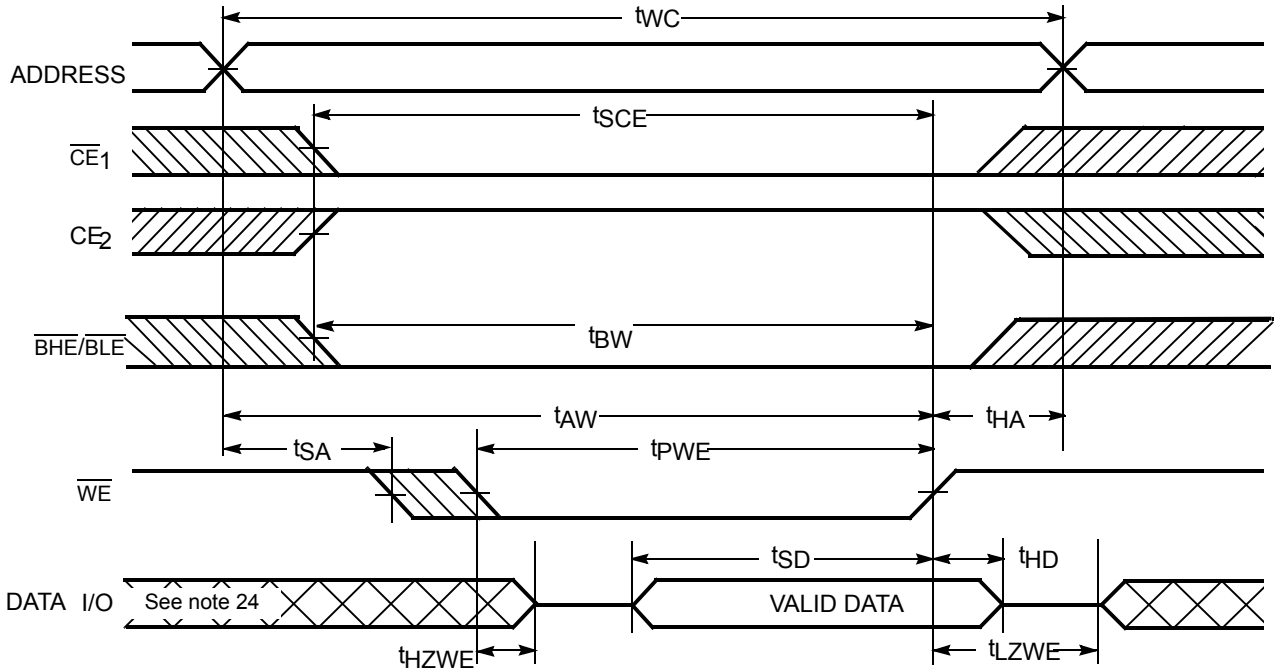
Write Cycle 2 ($\overline{CE_1}$ or CE_2 Controlled)[19, 23, 24, 25]



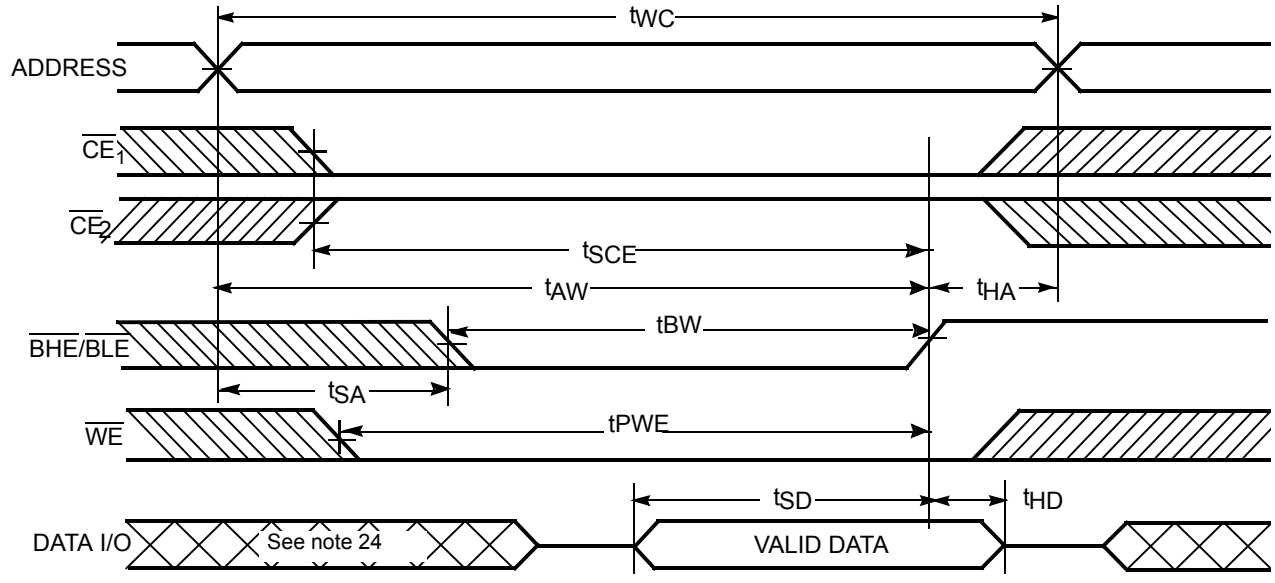
Notes:
23. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
24. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high-impedance state.
25. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[24, 25]



Write Cycle 4 ($\overline{BHE}$/$\overline{BLE}$ Controlled, $\overline{OE}$ LOW)[24, 25]



Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O0 – I/O15)	Read (Upper byte and Lower Byte)	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O0 – I/O7); High Z (I/O8 – I/O15)	Read (Lower Byte only)	Active (I_{CC})
L	H	H	L	L	H	High Z (I/O0 – I/O7); Data Out (I/O8 – I/O15)	Read (Upper Byte only)	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O0 – I/O15)	Write(Upper byte and Lower Byte)	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O0 – I/O7); High Z (I/O8 – I/O15)	Write (Lower Byte only)	Active (I_{CC})
L	H	L	X	L	H	High Z (I/O0 – I/O7); Data In (I/O8 – I/O15)	Write (Upper Byte only)	Active (I_{CC})

Ordering Information

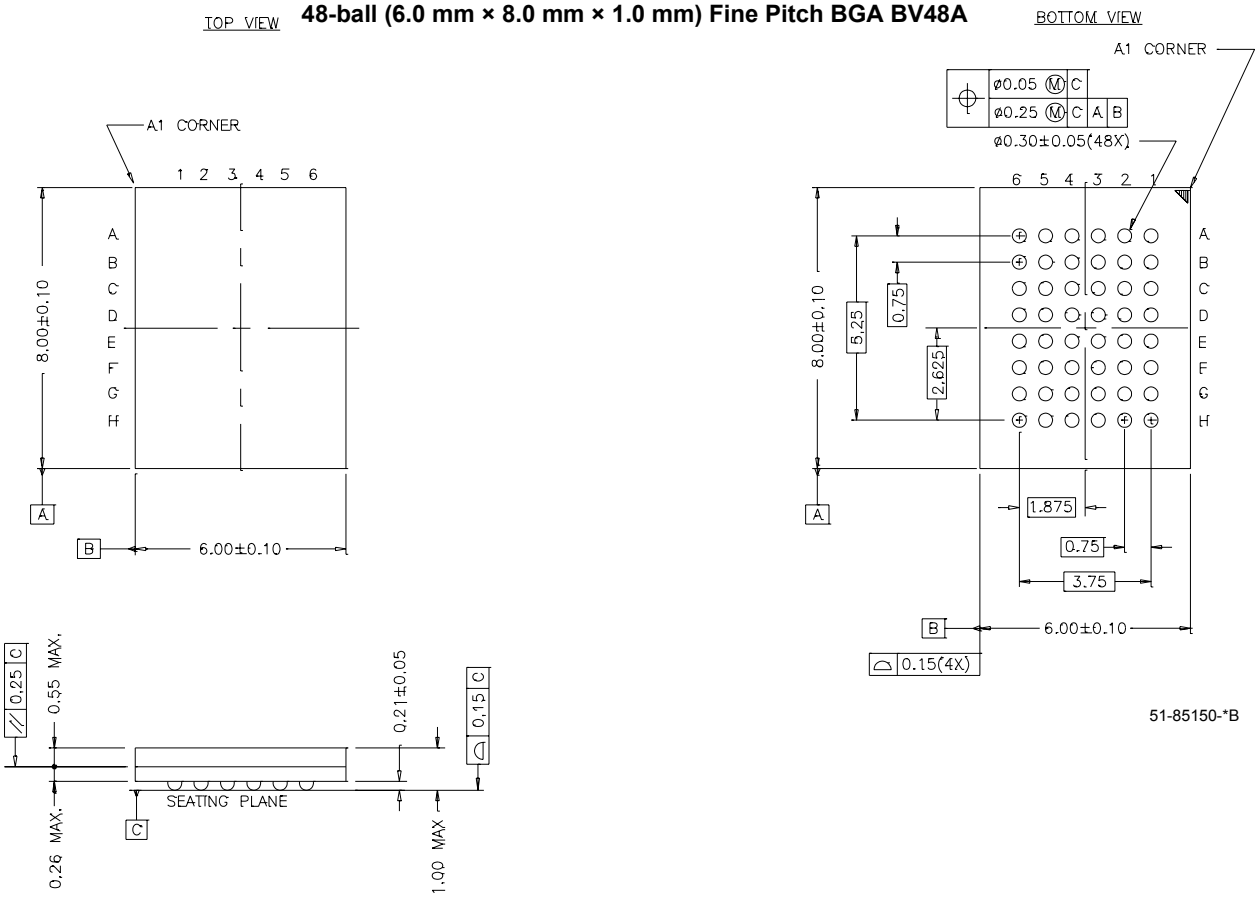
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY62157DV30L-45BVI	BV48A	48-ball Fine Pitch BGA (6 mm × 8 mm × 1 mm)	Industrial
	CY62157DV30LL-45BVI			
45	CY62157DV30L-45ZXI	Z-48	48-pin TSOP I (Pb-free)	Industrial
	CY62157DV30LL-45ZXI			
45	CY62157DV30L-45ZSXI	ZS-44	44-pin TSOP II (Pb-free)	Industrial
	CY62157DV30LL-45ZSXI			
55	CY62157DV30L-55BVI	BV48A	48-ball Fine Pitch BGA (6 mm × 8 mm × 1 mm)	Industrial
	CY62157DV30LL-55BVI			
55	CY62157DV30L-55BVXI	BV48A	48-ball Fine Pitch BGA (6 mm × 8 mm × 1 mm) (Pb-free)	Industrial
	CY62157DV30LL-55BVXI			
55	CY62157DV30L-55BVE	BV48A	48-ball Fine Pitch BGA (6 mm × 8 mm × 1 mm)	Automotive
55	CY62157DV30L-55ZXI	Z-48	48-pin TSOP I (Pb-free)	Industrial
	CY62157DV30LL-55ZXI			
55	CY62157DV30L-55ZXE	Z-48	48-pin TSOP I (Pb-free)	Automotive
55	CY62157DV30L-55ZSXI	ZS-44	44-pin TSOP II (Pb-free)	Industrial
	CY62157DV30LL-55ZSXI			
55	CY62157DV30L-55ZSXE	ZS-44	44-pin TSOP II (Pb-free)	Automotive
55	CY62157DV30L-55ZSI	ZS-44	44-pin TSOP II	Industrial
	CY62157DV30LL-55ZSI			
70	CY62157DV30L-70BVI	BV48A	48-ball Fine Pitch BGA (6 mm × 8 mm × 1 mm)	Industrial
	CY62157DV30LL-70BVI			
70	CY62157DV30L-70BVXI	BV48A	48-ball Fine Pitch BGA (6 mm × 8 mm × 1 mm) (Pb-free)	Industrial
	CY62157DV30LL-70BVXI			
70	CY62157DV30L-70ZXI	Z-48	48-pin TSOP I (Pb-free)	Industrial
	CY62157DV30LL-70ZXI			

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62157DV30L-70ZSXI	ZS-44	44-pin TSOP II (Pb-free)	Industrial
	CY62157DV30LL-70ZSXI			
70	CY62157DV30L-70ZSI	ZS-44	44-pin TSOP II	Industrial
	CY62157DV30LL-70ZSI			

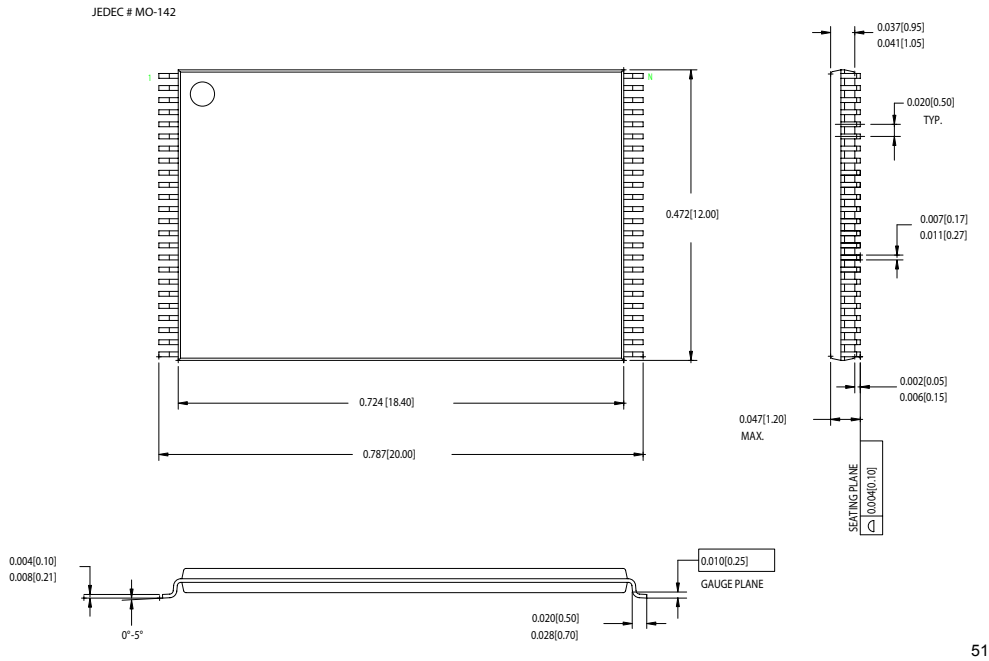
Package Diagrams

48-ball (6.0 mm × 8.0 mm × 1.0 mm) Fine Pitch BGA BV48A



Package Diagrams (continued)

48-Lead TSOP I (12 mm x 18.4 mm x 1.0 mm) Z48A



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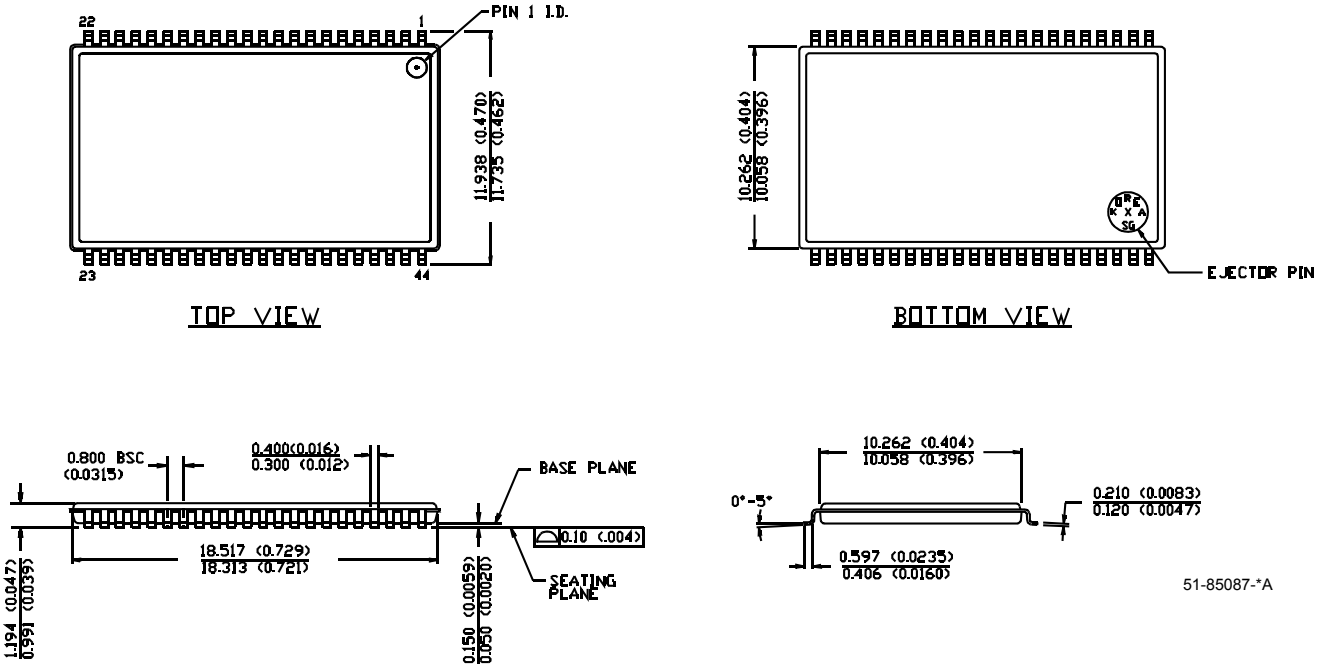
DIMENSION IN MM (INCH)
MAX
MIN.

44-Pin TSOP II ZS44



51-85087-*A

Document History Page

Document Title:CY62157DV30 MoBL® 8-Mbit (512K x 16) MoBL® Static RAM Document Number: 38-05392				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	126316	05/22/03	HRT	New Data Sheet
*A	131013	11/19/03	CBD/LDZ	Change from Advance to Preliminary
*B	133115	01/24/04	CBD	Minor Change: Change MPN and upload.
*C	211601	See ECN	AJU	Change from Preliminary to Final Changed Marketing part number from CY62157DV to CY62157DV30 in the title and in the Ordering Information table Added footnotes 4, 5 and 11 Modified footnote 8 to include ramp time and wait time Removed MAX value for VDR on Data Retention Characteristics table Changed ordering code for Pb-free parts Modified voltage limits in Maximum Ratings section
*D	236628	See ECN	SYT/AJU	Added 45-ns and 70-ns Speed Bins Added Automotive product information
*E	257349	See ECN	PCI	Added test condition for 45 ns part (footnote #13 on page 4)