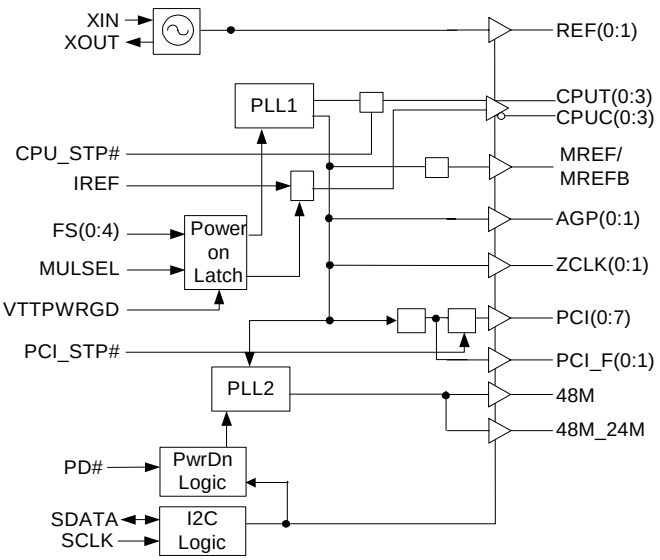
CY28373

Universal Single Chip Clock Solution for SiS658 Pentium® 4

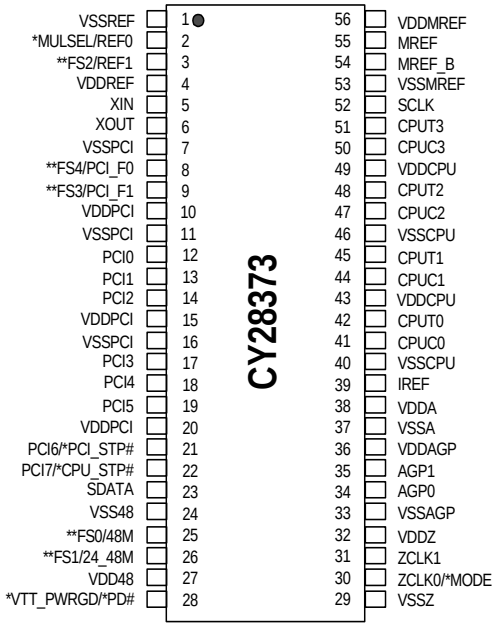
Features

- **Supports SiS658 Pentium® 4 chipsets**
- **Supports Pentium 4 processor**
- **Provides:**
  - **4 Differential programmable CPU clock pairs**
  - **2 MREF clocks for DMCG**
  - **2 ZCLK for MuTIOL**
  - **2 Low-skew/jitter AGP clocks**
  - **8 Low-skew/jitter PCI clocks**
  - **2 Low-skew/jitter fixed PCI clocks**
  - **1 48M output for USB**
  - **1 Programmable 24M or 48M for SIO**
  - **2 REF 14.318 MHz**
- **Dial-a-Frequency® and Dial-a-dB® features**
- **Spread spectrum for best EMI reduction**
- **SMBus compatible for programmability**
- **56-pin SSOP package**

Block Diagram



Pin Configuration[1]



Note:

1. Pins marked with [*] have 200-KΩ internal pull-up resistors. Pins marked with [**] have 200-KΩ internal pull-down resistors

Pin Description

Pin	Name	PWR	I/O	Description
5	XIN	VDD	I	***Oscillator Buffer Input.*** Connect to a crystal or to an external clock.
6	XOUT	VDD	O	***Oscillator Buffer Output.*** Connect to a crystal. Do not connect when an external clock is applied at XIN.
2	MULSEL/REF0	VDD	I/O PU 200K	***Power-on Bidirectional Input/Output.*** At power-up, MULSEL is an input. When the power supply voltage crosses the input threshold voltage, the MULSEL state is latched and this pin becomes REF0, which is a buffered copy of signal applied at XIN. When Byte 12, bit 1 = 1 (default), REF0 is normal strength. When Byte 12 bit 1 = 0, REF0 is high strength. When MULSEL = 0, Ioh is 4 x IREF, When MULSEL = 1, Ioh is 6 x IREF.
3	FS2/REF1	VDD	I/O PD 200K	***Power-on Bidirectional Input/Output.*** At power-up, FS2 is the input. When the power supply voltage crosses the input threshold voltage, the FS2 state is latched and this pin becomes When Byte 12, bit 0 = 1 (default), REF1 is normal strength. When Byte 12 bit 0= 0, REF1 is high strength.
28	VTTPWRGD	VDD	I PU 200K	When Byte 9 bit 7 = 0, this pin becomes a VTT_PWRGD/PD# input. When this input is sampled HIGH when VDD transitions beyond the threshold voltage, the FS(4:0) and MULSEL are latched. After the first high observance any other transitions are ignore.
28	PD#	VDD	I PU 200K	When Byte 9 bit 7 = 1, this pin becomes a PD# input with an internal pull-up. When PD# is asserted LOW, the device enters power-down mode. See power management function.
42, 45, 48, 51	CPUT(0:3)	VDDCPU	O	***True Clocks of the Differential CPU outputs.***
41, 44, 47, 50	CPUC(0:3)	VDDCPU	O	***Complementary Clocks of the Differential CPU outputs.***
12, 13, 14, 17,18, 19	PCI(0:5)	VDDPCI	O	***PCI Clock Outputs.***
30	ZCLK0/MODE	VDDZ	I/O PU 200K	***Power-on Bidirectional Input/Output.*** At power-up, MODE is an input. When the power supply voltage crosses the input threshold voltage, the MODE state is latched and this pin becomes ZCLK0. When MODE = 1, pin21 is PCI6 and pin 22 is PCI7. When MODE = 0, pin 21 is PCI_STP# and pin 22 is CPU_STP#.
31	ZCLK1	VDDZ	O	***MuTIOL Clock Output.***
22	PCI7	VDDPCI	O	When MODE = 1, this pin becomes a PCI clock output.
22	CPU_STP#	VDDPCI	I PU 200K	When MODE = 0, this pin becomes a CPU Clock Disable Input. When asserted LOW, CPUT(0:3) clocks are synchronously disabled in a HIGH state and CPUC(0:3) clocks are synchronously disabled in a LOW state.
21	PCI6	VDDPCI	O	When MODE = 1, this pin becomes a PCI clock output.
21	PCI_STP#	VDDPCI	I PU 200K	When MODE = 0, this pin becomes a PCI Clock Disable Input. When PCI_STP# is asserted LOW, PCI (0:7) clocks are synchronously disabled in a LOW state. This pin does not affect PCI_F (0:1) if they are programmed to be Free-running clocks via the device's SMBus interface.
8	FS4/PCI_F0	VDDPCI	I/O PD 200K	***Power-on Bidirectional Input/Output.*** At power-up, FS4 is an input. When the power supply voltage crosses the input threshold voltage, the FS4 state is latched and this pin becomes PCI_F0 clock output.

Pin Description (continued)

Pin	Name	PWR	I/O	Description
9	FS3/PCI_F1	VDDPCI	I/O PD 200K	***Power-on Bidirectional Input/Output.*** At power-up, FS3 is an input. When the power supply voltage crosses the input threshold voltage, the FS3 state is latched and this pin becomes PCI_F1 clock output.
25	FS0/48M	VDD48M	I/O PD 200K	***Power-on Bidirectional Input/Output.*** At power-up, FS0 is an input. When the power supply voltage crosses the input threshold voltage, the FS0 state is latched and this pin becomes 48M, a USB clock output.
26	FS1/24_48M	VDD48M	I/O PD 200K	***Power-on Bidirectional Input/Output.*** At power-up, FS1 is an input. When the power supply voltage crosses the input threshold voltage, the FS1 state is latched and this pin becomes 24_48M, a SIO programmable clock output.
34,35	AGP(0:1)	VDDAGP	O	***AGP Clock Outputs.***
39	IREF		I	This pin establishes the reference current for the host clocks.
54	MREF_B	VDDMREF	O	***DMCG Clock Output.***
55	MREF	VDDMREF	O	***DMCG Clock Output.***
23	SDATA	VDD	I/O	***Serial Data Input.*** Conforms to the SMBus specification of a Slave Receive/Transmit device. It is an input when receiving data. It is an open drain output when acknowledging or transmitting data.
52	SCLK	VDD	I	***Serial Clock Input.*** Conforms to the SMBus specification.
27	VDD48			***3.3V Power Supply for 48-/24-MHz Clocks***
10, 15, 20	VDDPCI			***3.3V Power Supply for PCI Clocks***
36	VDDAGP			***3.3V Power Supply for AGP Clocks***
43, 49	VDDCPU			***3.3V Power Supply for CPU Clocks***
38	VDDA			***3.3V Power Supply for Analog Circuitry***
56	VDDMREF			***3.3V Power Supply for MREF Clocks***
32	VDDZ			***3.3V Power Supply for ZCLK Clocks***
4	VDDREF			***3.3V Power Supply for REF Clocks***
24	VSS48			***Ground for 48-/24-MHz Clocks***
7, 11, 16	VSSPCI			***Ground for PCI Clocks***
33	VSSAGP			***Ground for AGP Clocks***
40, 46	VSSCPU			***Ground for CPU Clocks***
37	VSSA			***Ground for Analog Circuitry***
53	VSSMREF			***Ground for MREF Clocks***
29	VSSZ			***Ground for ZCLK Clocks***
1	VSSREF			***Ground for REF Clocks***

Table 1. Frequency Selection Table

FS(4:0)	CPU (MHz)	MREF (MHz)	ZCLK (MHz)	AGP (MHz)	PCI (MHz)	VCO (MHz)
00000	100.0	66.7	66.7	66.7	33.3	400.0
00001	100.0	66.7	80.0	66.7	33.3	400.0
00010	105.0	75.0	131.3	65.6	32.8	525.0
00011	100.0	66.7	133.3	66.7	33.3	400.0
00100	133.3	66.7	66.7	66.7	33.3	400.0
00101	133.3	66.7	80.0	66.7	33.3	400.0
00110	133.3	66.7	100.0	67	33.3	400.0
00111	133.3	66.7	133.3	66.7	33.3	400.0
01000	166.7	66.7	66.7	66.7	33.3	666.7
01001	166.7	66.7	83.3	66.7	33.3	666.7
01010	166.7	66.7	111.1	66.7	33.3	666.7
01011	166.7	66.7	133.3	66.7	33.3	666.7
01100	200.0	66.7	66.7	66.7	33.3	400.0
01101	200.0	66.7	80.0	66.7	33.3	400.0
01110	200.0	66.7	100.0	66.7	33.3	400.0
01111	200.0	66.7	133.3	66.7	33.3	400.0
10000	66.7	33.3	66.7	50.0	33.3	400.0
10001	105.0	84.0	140.0	70.0	35.0	420.0
10010	110.0	82.5	132.0	66.0	33.0	660.0
10011	100.0	80.0	133.3	66.7	33.3	400.0
10100	138.0	82.8	138.0	69.0	34.5	414.0
10101	142.0	85.2	142.0	71.0	35.5	426.0
10110	150.0	75.0	150.0	60.0	30.0	600.0
10111	133.3	80.0	133.3	66.7	33.3	400.0
11000	166.7	83.3	66.7	66.7	33.3	666.7
11001	166.7	83.3	83.3	66.7	33.3	666.7
11010	166.7	71.4	125.0	62.5	31.3	500.0
11011	166.7	83.3	133.3	66.7	33.3	666.7
11100	200.0	80.0	66.7	66.7	33.3	400.0
11101	200.0	80.0	80.0	66.7	33.3	400.0
11110	200.0	80.0	100.0	66.7	33.3	400.0
11111	200.0	80.0	133.3	66.7	33.3	400.0

Table 2. Swing Select Functions Through Hardware

MULSEL	Board Target Trace/Term Z	Reference R,IREF = VDD/(3*Rr)	Output Current	VOH@Z
0	50 Ohm	Rr = 221 1%, IREF = 5.00 mA	IOH = 4* Iref	1.0V@50
1	50 Ohm	Rr = 475 1%, IREF = 2.32 mA	IOH = 6* Iref	0.7V@50

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts Byte Write, Byte Read, Block Write, and Block Read operations from the controller. For Block Write/Read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For Byte Write and Byte Read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 3*.

The Block Write and Block Read protocol is outlined in *Table 4* while *Table 5* outlines the corresponding Byte Write and Byte Read protocol. The slave receiver address is 11010010 (D2h).

Table 3. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be ’0000000’

Table 4. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '00000000' stands for block operation	11:18	Command Code – 8 bits '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29:36	Data byte 1 – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 2 – 8 bits	30:37	Byte count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	.....	39:46	Data byte from slave – 8 bits
....	Data Byte (N–1) –8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave – 8 bits
....	Data Byte N – 8 bits	56	Acknowledge
....	Acknowledge from slave	....	Data bytes from slave/Acknowledge
....	Stop	....	Data byte N from slave – 8 bits
		....	Not Acknowledge
		....	Stop

Table 5. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address –7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '1xxxxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code – 8 bits '1xxxxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte from master – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29	Stop	28	Read = 1
		29	Acknowledge from slave
		30:37	Data byte from slave – 8 bits
		38	Not Acknowledge
		39	Stop

Byte 4: Frequency Select Register

Bit	@Pup	Pin#	Name	Description
7	0		FSELECT	0 = Frequency selected by HW latched inputs. 1 = Frequency selected by Byte 4, bits (4:0)
6	1		Spread Enable	0 = No spread, 1 = Spread spectrum enable
5	0			Reserved, set = 0
4	0	8	FS4	Software Frequency Select (4:0)
3	0	9	FS3	
2	0	3	FS2	
1	0	26	FS1	
0	0	25	FS0	

Byte 5: Clock Register

Bit	@Pup	Pin#	Name	Description
7	0			Reserved, set = 0
6	0		Master Output Control	0 = Running, 1 = Three-state all outputs
5	HW	2	MULSEL	MULSEL latched read back
4	HW	8	FS4	FS(4:0) hardware latched read back
3	HW	9	FS3	
2	HW	3	FS2	
1	HW	26	FS1	
0	HW	25	FS0	

Byte 6: CPU Clock Control Register

Bit	@Pup	Pin#	Name	Description
7	0	8	PCI_F0	0 = Free running, 1 = Stop when the PCI_STP# is LOW.
6	0	9	PCI_F1	0 = Free running, 1 = Stop when the PCI_STP# is LOW.
5	1	42, 41	CPU0T/C	0 = Free running, 1 = Stop when the CPU_STP# is LOW.
4	0	45, 44	CPU1T/C	0 = Free running, 1 = Stop when the CPU_STP# is LOW.
3	1	48, 47 51, 50	CPU2T/C CPU3T/C	0 = Free running, 1 = Stop when the CPU_STP# is LOW.
2	1	48, 47 51, 50	CPU2T/C CPU3T/C	1 = Running, 0 = Three-state.
1	1	45, 44	CPU1T/C	1 = Running, 0 = Three-state.
0	1	42, 41	CPU0T/C	1 = Running, 0 = Three-state.

Byte 7: PCI Clock Control Register

Bit	@Pup	Pin#	Name	Description
7	1	9	PCI_F1	1 = Running, 0 = Stopped LOW.
6	1	8	PCI_F0	1 = Running, 0 = Stopped LOW.
5	1	19	PCI5	1 = Running, 0 = Stopped LOW.
4	1	18	PCI4	1 = Running, 0 = Stopped LOW.
3	1	17	PCI3	1 = Running, 0 = Stopped LOW.
2	1	14	PCI2	1 = Running, 0 = Stopped LOW.
1	1	13	PCI1	1 = Running, 0 = Stopped LOW.
0	1	12	PCI0	1 = Running, 0 = Stopped LOW.

Byte 8: Vendor/Device ID Register (all bits are read only)

Bit	@Pup	Name	Description
7	1	Vender_ID3	Cypress Semiconductor's Vendor ID bit [3].
6	0	Vender_ID2	Cypress Semiconductor's Vendor ID bit [2].
5	0	Vender_ID1	Cypress Semiconductor's Vendor ID bit [1].
4	0	Vender_ID0	Cypress Semiconductor's Vendor ID bit [0].
3	0	Revision_ID3	Revision ID bit [3]
2	0	Revision_ID2	Revision ID bit [2]
1	0	Revision_ID1	Revision ID bit [1]
0	0	Revision_ID0	Revision ID bit [0]

Byte 9: Peripheral Clock Control Register

Bit	@Pup	Pin#	Name	Description
7	1	28		1 = VTT_PWRGD; 0 = 28 is PD#
6	0			Reserved, set = 0
5	1	25	48M	1 = Running, 0 = Stopped LOW.
4	1	26	24_48M	1 = Running, 0 = Stopped LOW.
3	0	26	24_48M	Select 24_48M 0 = 24 MHz, 1 = 48 MHz
2	0	55,54	MREF,MREF_B	MREF and MREF_B output multiplexer. 0: MREF = MREFB = from frequency table *Table 1*, 1: MREF = from frequency table *Table 1* and MREFB = 66.6 MHz.
1	1	54	MREF_B	1 = Running, 0 = Stopped LOW.
0	1	55	MREF	1 = Running, 0 = Stopped LOW.

Byte 10: AGP/REF/ZCLK Clock Control Register

Bit	@Pup	Pin#	Name	Description
7	1	21	PCI6	1 = Running, 0 = Stopped LOW.
6	1	22	PCI7	1 = Running, 0 = Stopped LOW.
5	1	3	REF1	1 = Running, 0 = Stopped LOW.
4	1	2	REF0	1 = Running, 0 = Stopped LOW.
3	1	31	ZCLK1	1 = Running, 0 = Stopped LOW.
2	1	30	ZCLK0	1 = Running, 0 = Stopped LOW.
1	1	35	AGP1	1 = Running, 0 = Stopped LOW.
0	1	34	AGP0	1 = Running, 0 = Stopped LOW.

Byte 11: AGP Ratio/Skew Control Register

Bit	@Pup	Pin#	Name	Description
7	0		PCI_DRV	PCI clock output drive strength: 0 = Low drive, 1 = High drive.
6	0		SSMODE	0 = Down Spread. 1 = Center Spread. *See Table 6*
5	1		SST1	Select spread bandwidth. *See Table 6*
4	1		SST0	Select spread bandwidth. *See Table 6*
3	0	34, 35	DASAG1	Programming these bits allow shifting skew of the AGP(0:2) signals relative to their default value. See *Table 7*.
2	0		DASAG0	
1	0		DARAG1	Programming these bits allow modifying the frequency ratio of the AGP clocks relative to the VCO frequency. See *Table 8*.
0	0		DARAG0	

Table 6. Spread Spectrum Table

Mode	SST1	SST0	% Spread
0	0	0	–1.5%
0	0	1	–1.0%
0	1	0	–0.75%
0	1	1	–0.5%
1	0	0	±0.75%
1	0	1	±0.5%
1	1	0	±0.35%
1	1	1	±0.25%

Table 7. Dial-a-Skew™ AGP(0:1)

DASAG(1:0)	AGP(0:1) Skew Shift
00	Default
01	–280 ps
10	+280 ps
11	+480 ps

Table 8. Dial-A-Ratio™ AGP(0:1)

DARAG(1:0)	VCO/AGP Ratio
00	Frequency Selection Default
01	6
10	8
11	10

Byte 12: Peripheral Clocks Register

Bit	@Pup	Pin#	Name	Description
7	1		48M	1= Low drive, 0 = High drive
6	1		24_48M	1= Low drive, 0 = High drive
5	0			Reserved, set = 0
4	0	34, 35	DARZCLK2	Programming these bits allow modifying the frequency ratio of the ZCLK clocks relative to the VCO frequency. See *Table 9*.
3	0		DARZCLK1	
2	0		DARZCLK0	
1	1	2	REF0	1= Low drive, 0 = High drive
0	1	3	REF1	1= Low drive, 0 = High drive

Table 9. Dial-A-Ratio ZCLK(0:1)

DARZCLK(2:0)	VCO/ZCLK Ratio
000	Frequency Selection Default
001	3
010	4
011	5
100	6
101	7
110	8
111	10

Byte 13: Dial-a-Frequency Control Register N

Bit	@Pup	Name	Description
7	0	Reserved	Reserved, set = 0. 1 = Test mode.
6	0	N6, MSB	These bits are for programming the PLL's internal N register. This access allows the user to modify the CPU frequency at very high resolution (accuracy). All other synchronous clocks (clocks that are generated from the same PLL, such as PCI) remain at their existing ratios relative to the CPU clock.
5	0	N5	
4	0	N4	
3	0	N3	
2	0	N2	
1	0	N1	
0	0	N0, LSB	

Byte 14: Dial-A-Frequency Control Register R

Bit	@Pup	Name	Description
7	0	Reserved	Reserved, set = 0
6	0	R5, MSB	These bits are for programming the PLL's internal R register. This access allows the user to modify the CPU frequency at very high resolution (accuracy). All other synchronous clocks (clocks that are generated from the same PLL, such as PCI) remain at their existing ratios relative to the CPU clock.
5	0	R4	
4	0	R3	
3	0	R2	
2	0	R1	
1	0	R0	
0	0	DAF_ENB	R and N register mux selection. 0 = R and N values come from the ROM. 1 = Data is load from DAF (I2C) registers.

Dial-a-Frequency® Feature

Dial-a-Frequency gives the designer direct access to the reference divider (M) and the feedback divider (N) of the internal Phase-Locked Loop (PLL). The algorithm is the same for all P values, which is $F_{cpu} = (P * N) / M$ with the following conditions. M = (20..56), N = (21..127) and N > M > N/2. 'P' is a large value constant that translates the output of the PLL into the CPU frequency. The Value of 'P' is relative to the latest frequency selected in the device prior to enabling the Dial-a-Frequency feature. Furthermore, P is an indication that the frequency ratios between the CPU, SDRAM. AGP (3V66), PCI, and DRCG (CPU/2) clock outputs remains unchanged when the Dial-a-Frequency feature is enabled.

Table 10. P Constants

FS(4:0)	P
00000, 00001, 00010, 00011, 01000, 01001, 01010, 01011, 10001, 10011, 10110, 11000, 11001, 11011	96000000
00100, 00101, 00110, 00111, 10100, 10101, 10111, 11010	128,000,000
01100, 01101, 01110, 01111, 11100, 11101, 11110, 11111	192,000,000
00010	76,800,000
10000	64,000,000

Table 11. Signal Loading

Clock Name	Max Load (in pF)
REF, 48MHz, 24_48MHz, ZCLK, MREF, MREFB	20
AGP, PCI_F, PCI	30
CPUT/C	See *Figure 1*

For Differential CPU Output Signals

Figure 1 shows the test load configuration for the differential Host Clock Outputs.

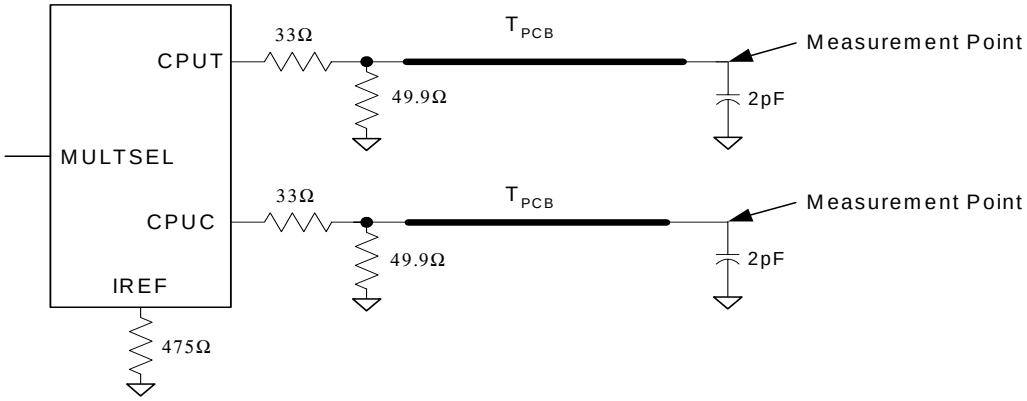


Figure 1. 0.7V Configuration

Table 12. Group Timing Relationships and Tolerances

Parameter	Description	Offset (ns)	Tolerance/Range (ns)	Conditions
t_{AGPPCI}	AGP to PCI	0.5	±0.5	AGP Leads
t_{CPUAGP}	CPU to AGP	2.0	1–4	CPU Leads
$t_{CPUZCLK}$	CPU to ZCLK	2.0	1–4	CPU Leads
t_{CPUPCI}	CPU to PCI	2.0	1–4	CPU Leads

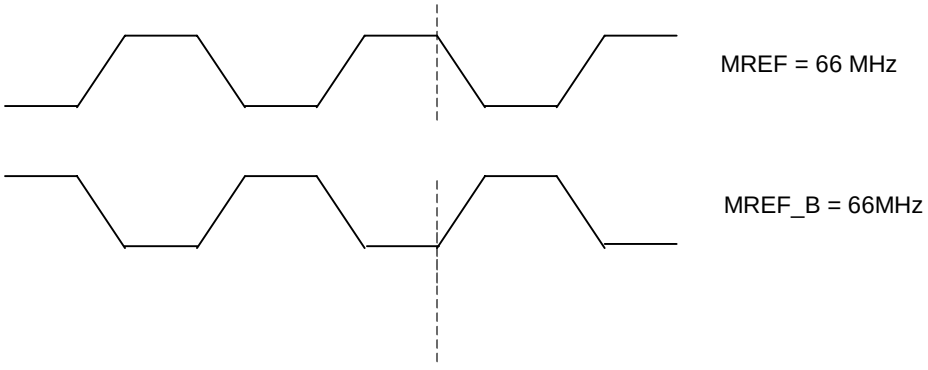


Figure 2. MREF/MREF_B Phase - Same Frequency, Byte 9 bit 2 = 0

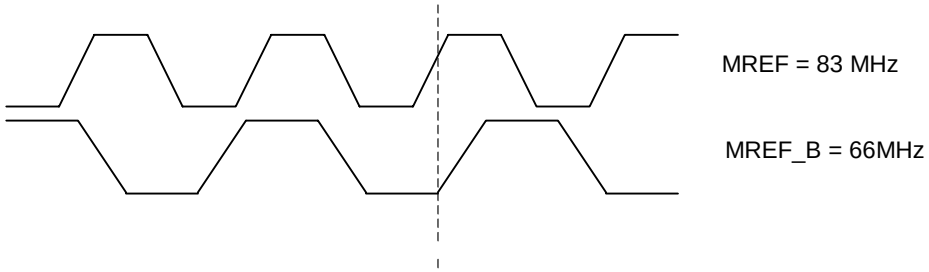


Figure 3. MREF/MREF_B Phase - Different Frequencies, Byte 9 bit 2 = 1

Power Management Functions

All clocks can be individually enabled or stopped via the 2-wire control interface. All clocks maintain a valid high period on transitions from running to stop and on transitions from stopped to running when the chip was not powered OFF.

Power Down Assertion

When PD# is sampled LOW by two consecutive rising edges of CPUC clock then all clocks must be held LOW on their next HIGH-to-LOW transition. CPUT clocks must be held with a value of 2 x Iref.

.

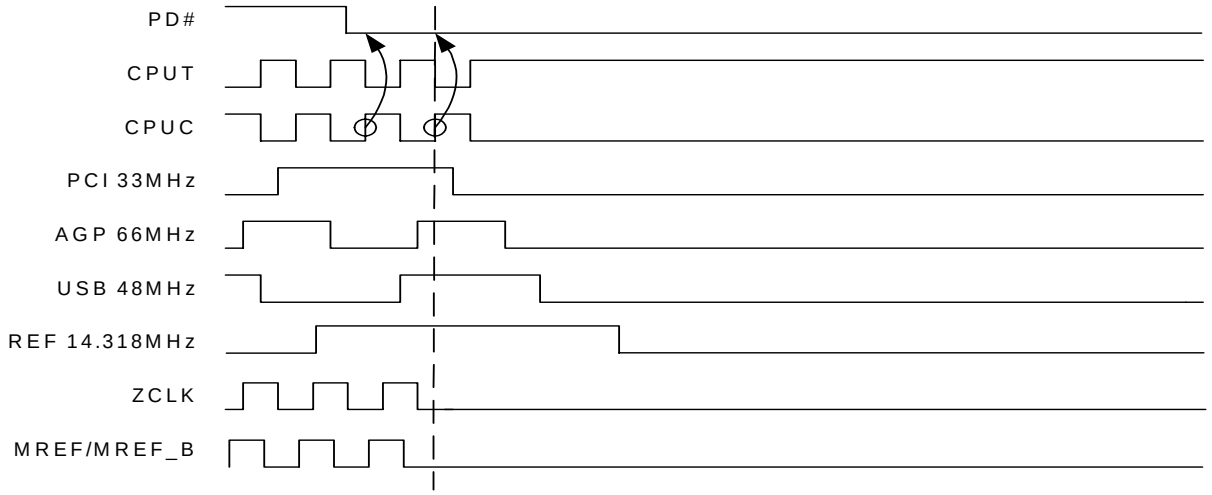


Figure 4. Power Down Assertion Timing Waveform

Power Down Deassertion

The Power-up latency is less than 1.5 ms.

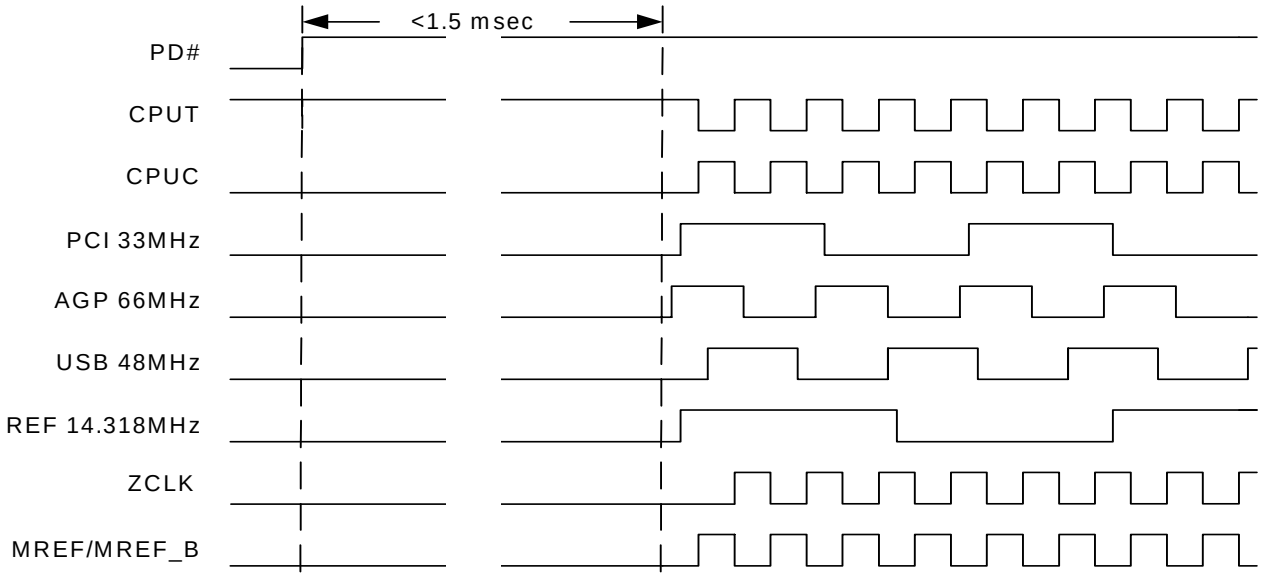


Figure 5. Power Down Deassertion Timing Waveform

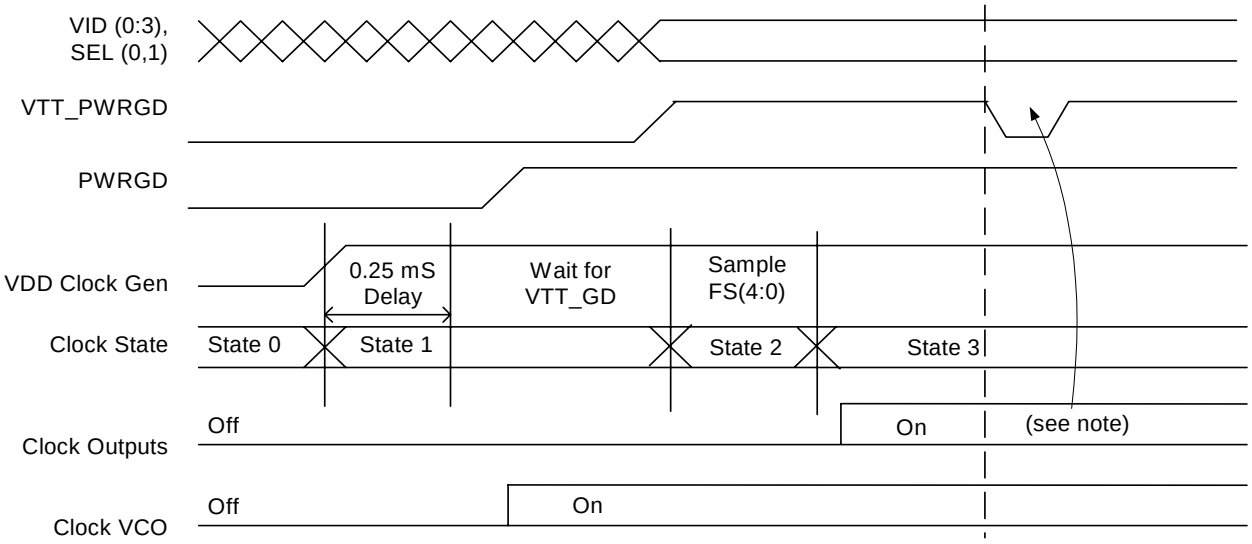


Figure 6. VTT_PWGD Timing Diagram[2]

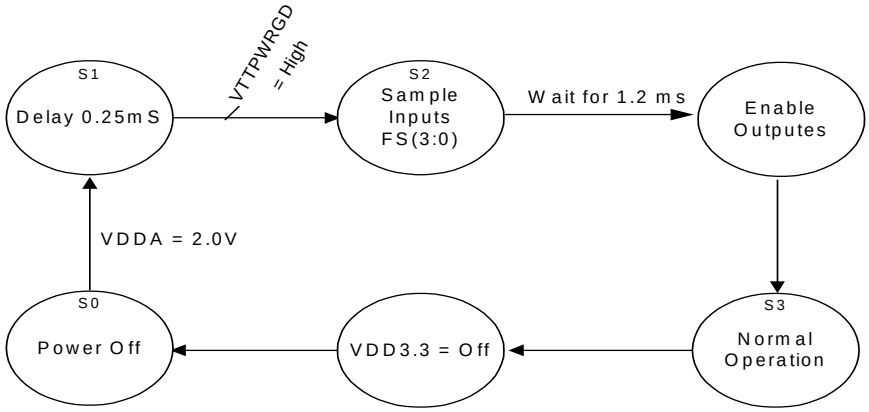


Figure 7. Clock Generator Power-Up/ Run State Diagram

Note:

2. This timing diagram shows that when VTT_PWRGD transitions to a logic HIGH the first time at power up. After the first transition of VTT_PWRGD to HIGH, the device is not affected by additional transitions of VTT_PWRGD.

CPU_STP# Assertion

When CPU_STP# pin is asserted, all CPU outputs will be stopped after being sampled by 2 rising CPUC clock edges. The final state of the stopped CPU signal is CPUT = HIGH and CPUC = LOW. There is no change to the output drive current values during the stopped state. The CPUT is driven HIGH with a current value equal to (Mult 0 'select') x (Iref), and the CPUC signal will not be driven. Due to external pull-down circuitry CPUC will be LOW during this stopped state.

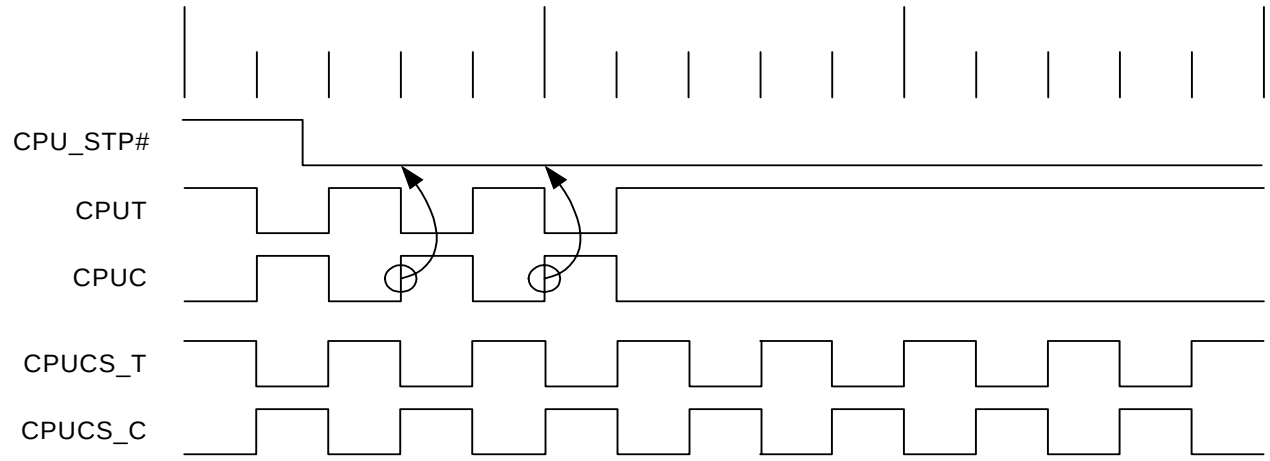


Figure 8. CPU_STP# Assertion Waveform

CPU_STP# Deassertion

The deassertion of the CPU_STP# signal will cause all CPU outputs that were stopped to resume normal operation in a synchronous manner. Synchronous manner meaning that no short or stretched clock pulses will be produce when the clock resumes. The maximum latency from the deassertion to active outputs is no more than two CPU clock cycles.

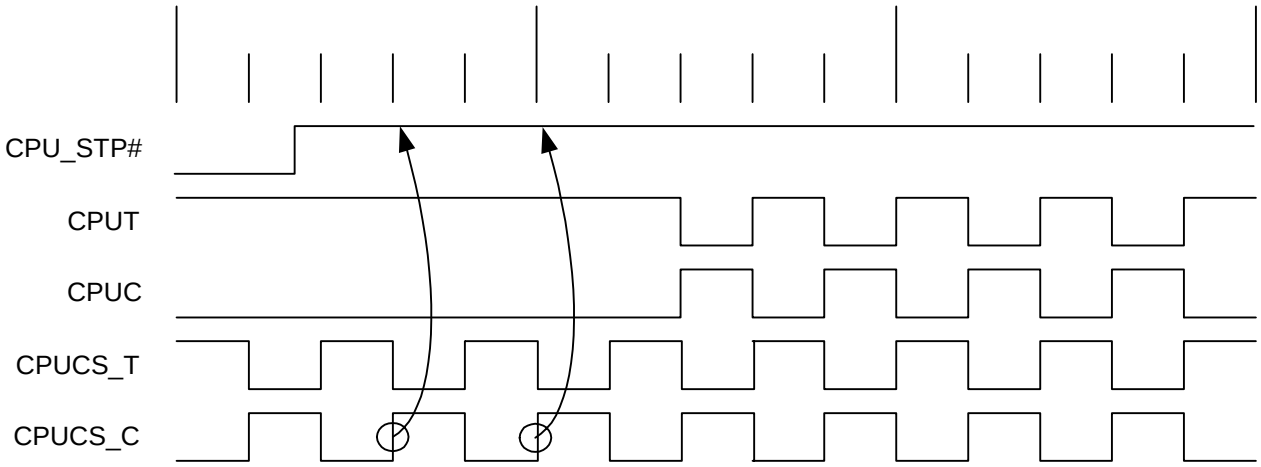


Figure 9. CPU_STP# Deassertion Waveform

PCI_STP# Assertion

The PCI_STP# signal is an active LOW input used for synchronous stopping and starting the PCI outputs while the rest of the clock generator continues to function. The set-up time for capturing PCI_STP# going LOW is 10 ns (t_{setup}). The PCI_F clock will not be affected by this pin.

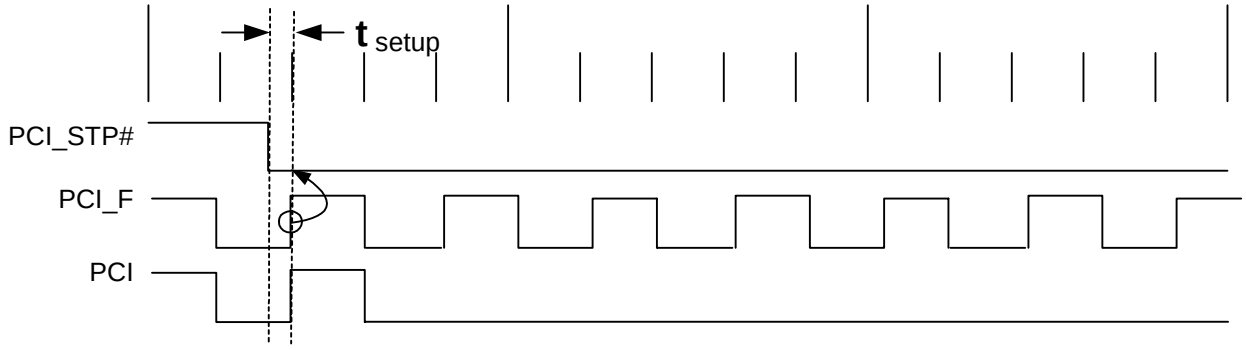


Figure 10. PCI_STP# Assertion Waveform

PCI_STP# Deassertion

The deassertion of the PCI_STP# signal will cause all PCI clocks to resume running in a synchronous manner within 1 PCI clocks period after PCI_STP# transitions to a HIGH level.

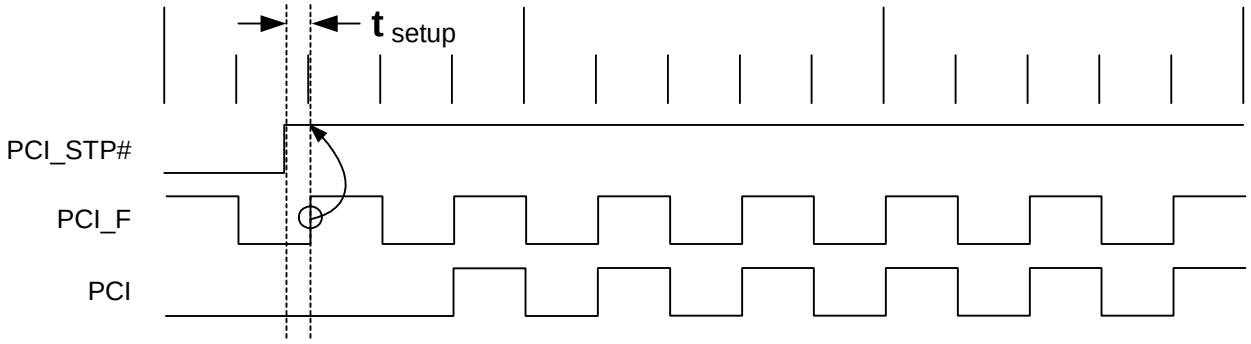


Figure 11. PCI_STP# Deassertion Waveform

Maximum Ratings[3]

Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.3V

Input Voltage Relative to V_{DDQ} or AV_{DD}: ..... V_{DD} + 0.3V

Storage Temperature: ..... –65°C to +150°C

Operating Temperature: ..... 0°C to +70°C

Maximum ESD 2000V

Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field. However, precautions should be take to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range.

$V_{SS} < (V_{IN} \text{ or } V_{OUT}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters ($V_{DD} = V_{DDPCI} = V_{DDAGP} = V_{DD48M} = V_{DDCPU} = V_{DDA} = V_{DDMREF} = V_{DDZ} = V_{DDREF}$ = 3.3V±5%, T_A = 0°C TO +70°C)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL1}	Input Low Voltage	Applicable to all input exclusive of the SMBus control lines			1.0	Vdc
V_{IH1}	Input High Voltage		2.0			Vdc
V_{IL2}	Input Low Voltage	Applicable to SDATA and SCLK			1.0	Vdc
V_{IH2}	Input High Voltage		2.2			Vdc
I_{DD}	Dynamic Supply Current	CPU frequency set at 133.3 MHz[4]		156	180	mA
I_{PD}	Power Down Supply current	PD# = 0		3.8	4.0	mA
I_{PUP}	Internal Pull-up Device Current	Input @ V_{SS}			–25	µA
I_{PWRDN}	Internal Pull-down Device Current	Input @ V_{DD}			10	µA
C_{IN}	Input Pin Capacitance				5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{PIN}	Pin Inductance				7	pF
C_{XTAL}	Crystal Pin Capacitance	Measured from the Xin or Xout to V_{SS}	27	36	45	pF

Note:

3. **Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
4. All outputs loaded as per maximum. *See Table 11*.

AC Parameters

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
Crystal						
T_{DC}	Xin Duty Cycle	45		55	%	5, 6
T_{PERIOD}	Xin Period	69.84		71.0	ns	5, 6
V_{HIGH}	Xin High Voltage	$0.7V_{DD}$		V_{DD}	Volts	
V_{LOW}	Xin Low Voltage	0		$0.3V_{DD}$	Volts	
$T_{RISE/TFALL}$	Xin Rise and Fall Times			10.0	ns	7
T_{CCJ}	Xin Cycle-to-Cycle Jitter			500	ps	5, 8
Txs	Crystal Start-up Time			30	ms	9
P4 CPU at 0.7V						
T_{DC}	CPUT/C Duty Cycle	45		55	%	8, 10
$T_{RISE/TFALL}$	CPUT/C Rise and Fall Times	175		700	ps	10, 11
T_{SKEW}	CPUT/C to CPUCS_T/C Clock Skew			100	ps	8, 10
T_{CCJ}	CPUT/C Cycle-to-Cycle Jitter			150	ps	8, 10
V_{CROSS}	Crossing Point Voltage	280		430	mV	12
MREF/MREFB						
T_{DC}	MREF/MREFB Duty Cycle	45		55	%	8, 10
$T_{RISE/TFALL}$	MREF/MREFB Rise and Fall Times	0.4		1.6	ns	10, 13
T_{SKEW}	MREF/MREFB to CPUCS_T/C Clock Skew			100	ps	8, 10
T_{CCJ}	MREF/MREFB Cycle-to-Cycle Jitter			350	ps	8, 10
ZCLK						
T_{DC}	ZCLK Duty Cycle	45		55	%	8, 10
$T_{RISE/TFALL}$	ZCLK Rise and Fall Times	0.4		1.6	ns	10, 13
T_{SKEW}	ZCLK to CPUCS_T/C Clock Skew			175	ps	8, 10
T_{CCJ}	ZCLK Cycle-to-Cycle Jitter			400	ps	8, 10
AGP						
T_{DC}	AGP Duty Cycle	45		55	%	8, 10
T_{PERIOD}	AGP Period	15		16	ns	8, 10
T_{HIGH}	AGP High Time	5.25			ns	10, 14
T_{LOW}	AGP Low Time	5.05			ns	10, 15
$T_{RISE/TFALL}$	AGP Rise and Fall Times	0.4		1.6	ns	10, 13
T_{SKEW}	Any AGP to Any AGP Clock Skew			175	ps	8, 10
T_{CCJ}	AGP Cycle-to-Cycle Jitter			500	ps	8, 10
PCI						
T_{DC}	PCI Duty Cycle	45		55	%	8, 10
T_{PERIOD}	PC Period	30.0			ns	8, 10
T_{HIGH}	PCI High Time	12.0			ns	10, 14
T_{LOW}	PCI Low Time	12.0			ns	10, 15
$T_{RISE/TFALL}$	PCI Rise and Fall Times	0.5		2.5	ns	10, 13
T_{SKEW}	Any PCI to Any PCI Clock Skew			550	ps	8, 10
T_{CCJ}	PCI, PCI_F Cycle-to-Cycle Jitter			500	ps	8, 10

AC Parameters (continued)

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
48 MHz						
T_{DC}	48-MHz Duty Cycle	45		55	%	8, 10
T_{PERIOD}	48-MHz Period	20.829		20.833	ns	8, 10
$T_{RISE/TFALL}$	48-MHz Rise and Fall Times	1.0		4.0	ns	10, 13
T_{CCJ}	48-MHz Cycle-to-Cycle Jitter			500	ps	8, 10
24 MHz						
T_{DC}	24-MHz Duty Cycle	45		55	%	8, 10
T_{PERIOD}	24-MHz Period	41.660		41.667	ns	8, 10
$T_{RISE/TFALL}$	24-MHz Rise and Fall Times	1.0		4.0	ns	10, 13
T_{CCJ}	24-MHz Cycle-to-Cycle Jitter			500	ps	8, 10
REF						
T_{DC}	REF Duty Cycle	45		55	%	8, 10
T_{PERIOD}	REF Period	69.8		71.0	ns	8, 10
$T_{RISE/TFALL}$	REF Rise and Fall Times	1.0		4.0	ns	10,13
T_{CCJ}	REF Cycle-to-Cycle Jitter			1000	ps	8, 10
MISC						
T_{STABLE}	Output Clock Stabilization			3.0	ms	16

Notes:

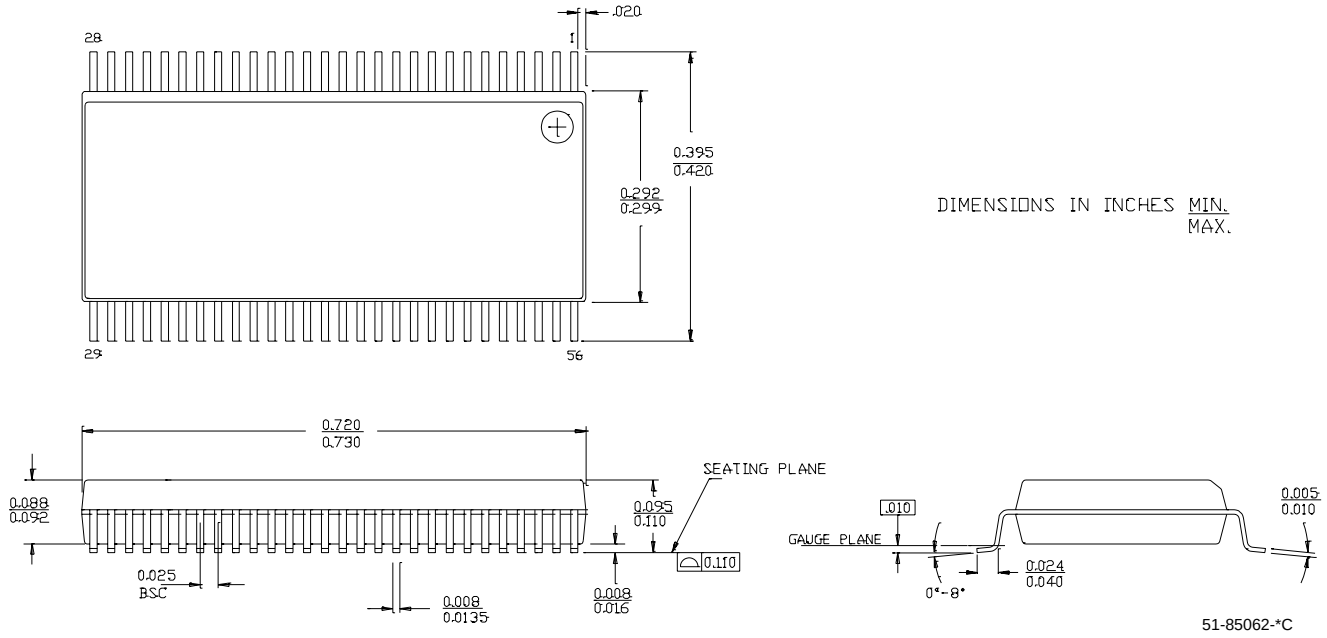
5. When Xin is driven from and external clock source.
6. This is required for the duty cycle on the REF clock out to be as specified. The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within data sheet specifications.
7. Measured between $0.2V_{DD}$ and $0.7V_{DD}$.
8. Probes are placed on the pins and measurements are acquired at 1.5V for 3.3V signals and at zero-crossing for differential signals.
9. When Crystal meets minimum 40-ohm device series resistance specification.
10. All outputs loaded as per loading specified in the loading table. *See Table 11*.
11. Measured from Vol = 0.175V to Voh = 0.525V.
12. Measured at VX, or where subtraction of CLK-CLK# crosses 0 volts.
13. Probes are placed on the pins and measurements are acquired between 0.4V and 2.4V for 3.3V signals and between 20% and 80% for differential signals.
14. Probes are placed on the pins and measurements are acquired at 2.4V.
15. Probes are placed on the pins and measurements are acquired at 0.4V.
16. The time specified is measured from when all V_{DD}s reach their respective supply rail, until the frequency output is stable and operating within the specifications.

Ordering Information

Part Number	Package Type	Product Flow
CY28373OC	56 Pin Shrunk Small Outline package (SSOP)	Commercial, 0° to 70°C
CY28373OCT	56 Pin Shrunk Small Outline package (SSOP) - Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

56-Lead Shrunk Small Outline Package O56



Dial-a-dB and Dial-a-Frequency are registered trademarks of Cypress Semiconductor Corporation. Dial-a-Skew and Dial-a-Ratio are trademarks of Cypress Semiconductor Corporation. Pentium is a registered trademark of Intel Corporation.

Revision History

Document Title: CY28373 Universal Single Chip Clock Solution for SiS658 Pentium® 4 Document #: 38-07460				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	117576	09/10/02	RGL	New Data Sheet
*A	122935	12/18/02	RBI	Add power up requirements to maximum ratings information