CY24207

MediaClock™ PDP Clock Generator

Features

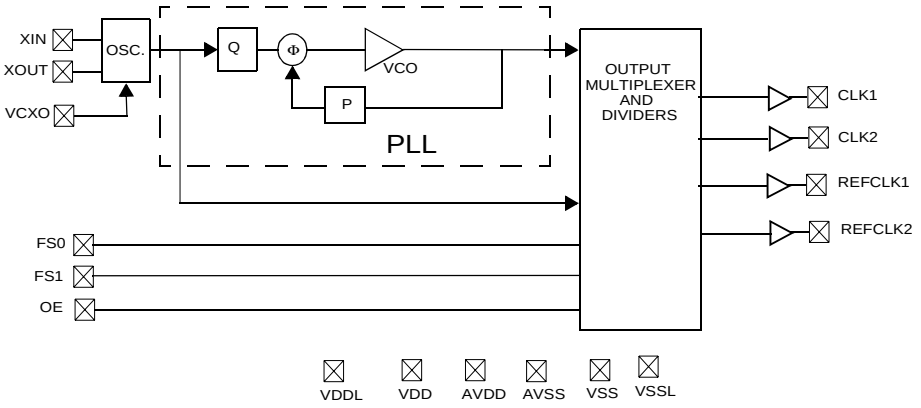
- **Integrated phase-locked loop (PLL)**
- **Low-jitter, high-accuracy outputs**
- **VCXO with Analog Adjust**
- **3.3V operation**

Benefits

- Internal PLL with up to 400-MHz internal operation
- Meets critical timing requirements in complex system designs
- Large ±200-ppm range, better linearity
- Enables application compatibility

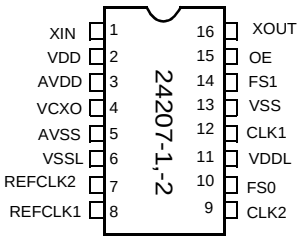
Part Number	Outputs	Input Frequency	Output Frequency Range
CY24207-1	4	27-MHz Crystal Input	Two copies of 27-MHz reference clock output, two copies of 54/53.946053/67.425/67.357642 MHz (frequency selectable)
CY24207-2	4	27-MHz Crystal Input	Two copies of 27-MHz reference clock output, two copies of 54/53.946053/67.425/68.400599 MHz (frequency selectable)

Block Diagram



Pin Configuration

16-pin TSSOP



Frequency Select Options

OE	FS1	FS0	CLK1/CLK2 (-1)[1]	CLK1/CLK2 (-2)[1]	REFCLK 1/2	Unit
0	0	0	off	off	27	MHz
0	0	1	off	off	27	MHz
0	1	0	off	off	27	MHz
0	1	1	off	off	27	MHz
1	0	0	54	54	27	MHz
1	0	1	53.946053 (–1 ppm)	53.946053 (–1 ppm)	27	MHz
1	1	0	67.425	67.425	27	MHz
1	1	1	67.357642 (3.8 ppm)	68.400599(–8.8 ppm)	27	MHz

Note:
1. "off" = output is driven high.

Pin Description

Pin No.	Name	Description
1	XIN	**Reference crystal input**
2	V_{DD}	**Voltage supply**
3	AV_{DD}	**Analog voltage supply**
4	VCXO	**Input analog control for VCXO**
5	AV_{SS}	**Analog ground**
6	V_{SSL}	**CLK ground**
7	REFCLK2	**Reference clock output**
8	REFCLK1	**Reference clock output**
9	CLK1 (–1)	**54/53.946053/67.425/67.357642 MHz clock output (frequency selectable)**
9	CLK1 (–2)	**54/53.946053/67.425/68.400599 MHz clock output (frequency selectable)**
10	FS0	**Frequency Select 0, weak internal pull-up**
11	V_{DDL}	**CLK voltage supply**
12	CLK2 (–1)	**54/53.946053/67.425/67.357642 MHz clock output (frequency selectable)**
12	CLK2 (–2)	**54/53.946053/67.425/68.400599 MHz clock output (frequency selectable)**
13	V_{SS}	**Ground**
14	FS1	**Frequency Select 1, weak internal pull-up**
15	OE	**Output Enable, weak internal pull-up**
16	XOUT	**Reference crystal output**

Absolute Maximum Conditions

Supply Voltage (V_{DD}, AV_{DDL}, V_{DDL}).....–0.5 to +7.0V

DC Input Voltage.....–0.5V to V_{DD}+0.5

Storage Temperature (Non-condensing).....–55°C to +125°C

Junction Temperature ..... –40°C to +125°C

Data Retention @ Tj = 125°C.....> 10 years

Package Power Dissipation..... 350 mW

ESD (Human Body Model) MIL-STD-883..... 2000V

(Above which the useful life may be impaired. For user guidelines, not tested.)

Pullable Crystal Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{NOM}	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut		27.0		MHz
C_{LNOM}	Nominal load capacitance			14		pF
R_1	Equivalent series resistance (ESR)	Fundamental mode			25	Ω
R_3/R_1	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R_1 values are much less than the maximum spec	3			
DL	Crystal drive level	No external series resistor assumed		0.5	2	mW
F_{3SEPHI}	Third overtone separation from 3*F_{NOM}	High side	300			ppm
F_{3SEPLO}	Third overtone separation from 3*F_{NOM}	Low side			–150	ppm
C_0	Crystal shunt capacitance				7	pF
C_0/C_1	Ratio of shunt to motional capacitance		180		250	
C_1	Crystal motional capacitance		14.4	18	21.6	fF

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
$V_{DD}/AV_{DDL}/V_{DDL}$	Operating Voltage	3.135	3.3	3.465	V
T_A	Ambient Temperature	0		70	°C
C_{LOAD}	Max. Load Capacitance			15	pF
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05		500	ms

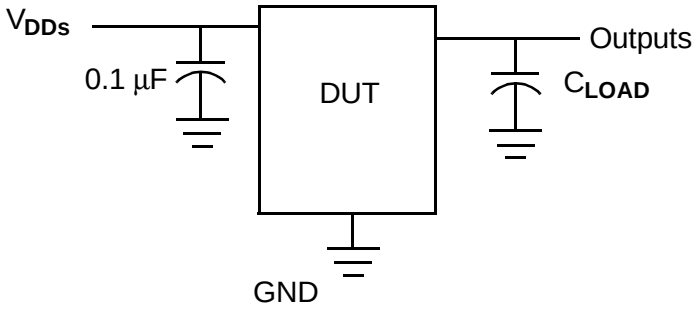
DC Electrical Specifications

Parameter[2]	Name	Description	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5$, V_{DD}/V_{DDL} = 3.3V	12	24		mA
I_{OL}	Output Low Current	V_{OL} = 0.5, V_{DD}/V_{DDL} = 3.3V	12	24		mA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7			V_{DD}
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}			0.3	V_{DD}
I_{VDD}	Supply Current	AV_{DD}/V_{DD} Current			25	mA
I_{VDDL}	Supply Current	V_{DDL} Current (V_{DDL} = 3.47V)			20	mA
C_{IN}	Input Capacitance	excluding XIN and XOUT			7	pF
$f_{\Delta XO}$	V_{CXO} pullability range			±200		ppm
V_{VCXO}	V_{CXO} input range		0		V_{DD}	V
R_{UP}	Pull-up resistor on inputs	V_{DD} = 3.14 to 3.47V, measured at V_{IN} = 0V		100	150	kΩ

AC Electrical Specifications

Parameter[2]	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in *Figure 1*; t1/t2, 50% of V_{DD}	45	50	55	%
ER	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD}, C_{LOAD} = 15 pF. See *Figure 2*.	0.8	1.4		V/ns
EF	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of V_{DD}, C_{LOAD} = 15 pF. See *Figure 2*.	0.8	1.4		V/ns
t_9	Clock Jitter	CLK1, CLK2 Peak-Peak period jitter		120		ps
t_{10}	PLL Lock Time				3	ms

Test and Measurement Set-up



Voltage and Timing Definitions

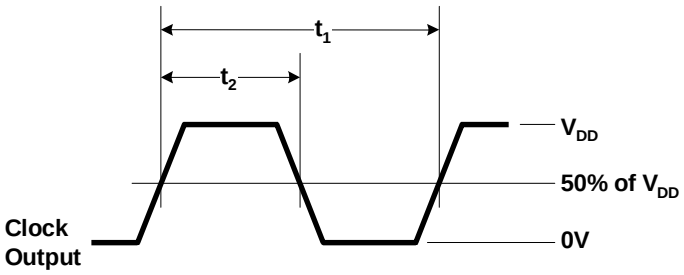


Figure 1. Duty Cycle Definition

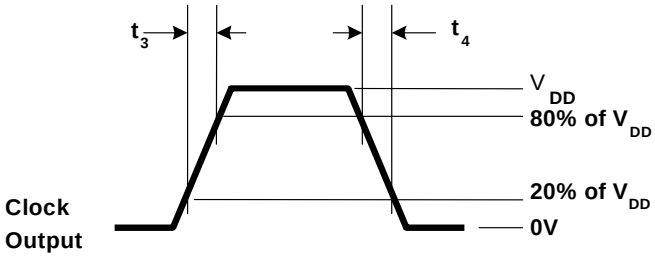


Figure 2. ER = (0.6 x V_{DD}) /t3, EF = (0.6 x V_{DD}) /t4

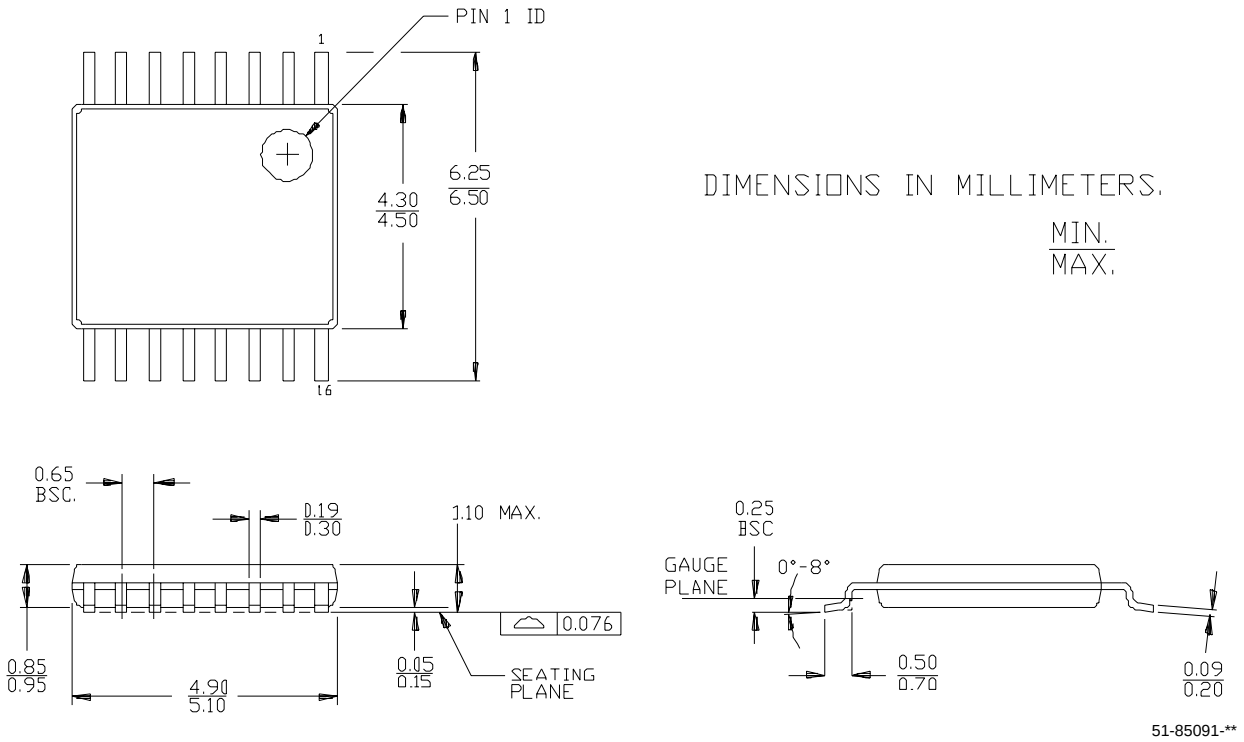
Note:
2. Not 100% tested.

Ordering Information

Ordering Code	Package Type	Operating Range	Operating Voltage
CY24207ZC-1	16-pin TSSOP	Commercial	3.3V
CY24207ZC-1T	16-pin TSSOP	Commercial	3.3V
CY24207ZC-2	16-pin TSSOP	Commercial	3.3V
CY24207ZC-2T	16-pin TSSOP	Commercial	3.3V

Package Drawing and Dimensions

16-lead Thin Shrunk Small Outline Package (4.40 MM Body) Z16



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Document History Page

Document Title: CY24207 MediaClock™ PDP Clock Generator Document Number: 38-07553				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
.	127230	06/26/03	RGL	New Data Sheet
*A	128248	07/31/03	IJATMP	Added -2 part number Added CLK1/CLK2 (-2) column to Frequency Select Options Added new definitions for Pins 9 and 12 in Pin Description table