



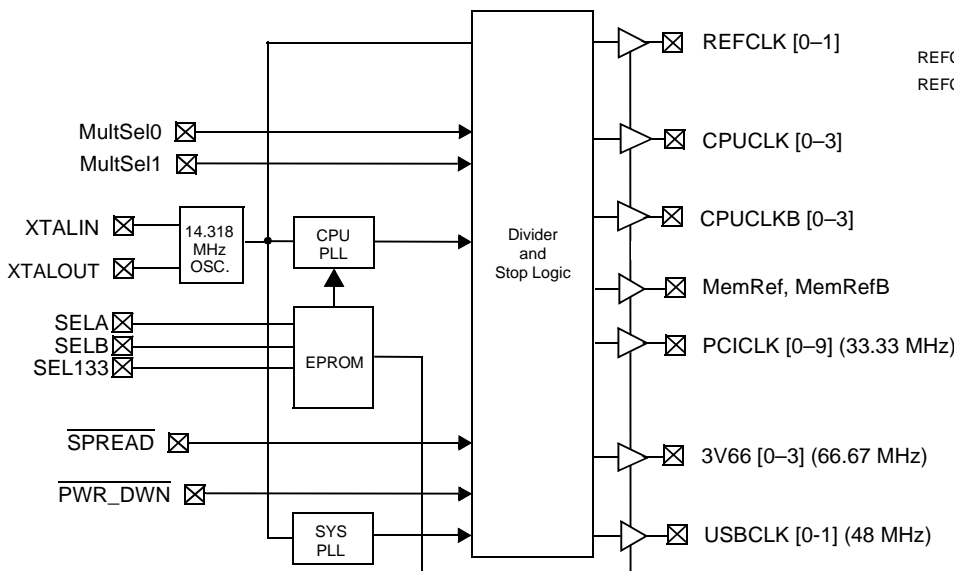
CYPRESS

CY2220

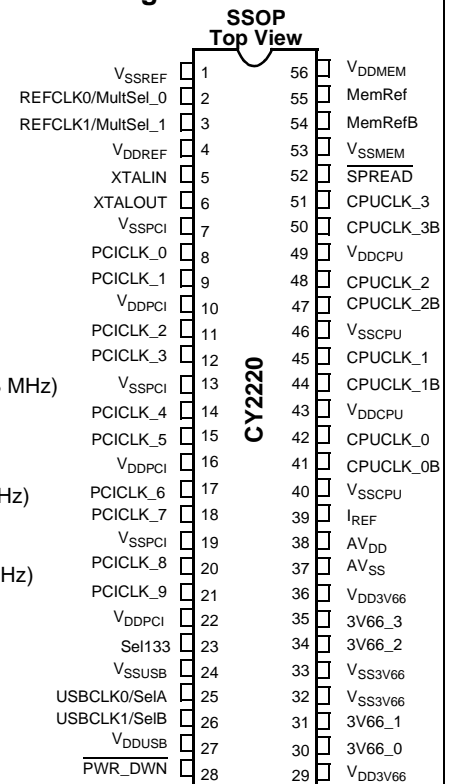
# 133-MHz Spread Spectrum Clock Synthesizer/Driver with Differential CPU Outputs

| Features   | Benefits   |
|--|--|
| <ul style="list-style-type: none"> <li>Compliant to Intel® CK00 Clock Synthesizer/Driver Specifications</li> </ul>   | Supports next generation Pentium® processors using differential clock drivers  |
| <ul style="list-style-type: none"> <li>Multiple output clocks at different frequencies               <ul style="list-style-type: none"> <li>Four pairs of differential CPU outputs, up to 133 MHz</li> <li>Ten synchronous PCI clocks</li> <li>Two Memory Reference clocks, 180 degrees out of phase</li> <li>Four AGP and Hub Link clocks at 66 MHz</li> <li>Two 48-MHz clocks</li> <li>Two reference clocks at 14.318 MHz</li> </ul> </li> </ul> | Motherboard clock generator <ul style="list-style-type: none"> <li>Support Multiple CPUs and a chipset</li> <li>Support for PCI slots and chipset</li> <li>Drives up to two Direct Rambus™ Clock Generators (DRCG)</li> <li>Supports USB host controller and SuperI/O chip</li> <li>Supports ISA slots and I/O chip</li> </ul> |
| <ul style="list-style-type: none"> <li>Spread Spectrum clocking               <ul style="list-style-type: none"> <li>31 kHz modulation frequency</li> <li>Default is -0.6%, which is recommended by Intel</li> </ul> </li> </ul>   | Enables reduction of EMI and overall system cost   |
| <ul style="list-style-type: none"> <li>Power-down features</li> </ul>  | Enables ACPI compliant designs   |
| <ul style="list-style-type: none"> <li>Three Select inputs</li> </ul>  | Supports up to eight CPU clock frequencies   |
| <ul style="list-style-type: none"> <li>Low-skew and low-jitter outputs</li> </ul>  | Meets tight system timing requirements at high frequency   |
| <ul style="list-style-type: none"> <li>OE and Test Mode support</li> </ul>   | Enables ATE and “bed of nails” testing   |
| <ul style="list-style-type: none"> <li>56-pin SSOP package</li> </ul>  | Widely available, standard package enables lower cost  |

## Logic Block Diagram



## Pin Configuration



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**Pin Summary**

| Name                     | Pins                                 | Description  |
|--------------------------|--------------------------------------|--|
| V <sub>SSREF</sub>       | 1                                    | 3.3V Reference ground  |
| V <sub>DDREF</sub>       | 4                                    | 3.3V Reference voltage supply  |
| V <sub>SSPCI</sub>       | 7, 13, 19                            | 3.3V PCI ground  |
| V <sub>DDPCI</sub>       | 10, 16, 22                           | 3.3V PCI voltage supply  |
| V <sub>SS3V66</sub>      | 32, 33                               | 3.3V AGP and Hub Link ground   |
| V <sub>DD3V66</sub>      | 29, 36                               | 3.3V AGP and Hub Link voltage supply   |
| V <sub>SSUSB</sub>       | 24                                   | 3.3V USB ground  |
| V <sub>DDUSB</sub>       | 27                                   | 3.3V USB voltage supply  |
| V <sub>SSCPU</sub>       | 40, 46                               | 3.3V CPU ground  |
| V <sub>DDCPU</sub>       | 43, 49                               | 3.3V CPU voltage supply  |
| V <sub>SSMEM</sub>       | 53                                   | 3.3V Memory ground   |
| V <sub>DDMEM</sub>       | 56                                   | 3.3V Memory voltage supply   |
| AV <sub>SS</sub>         | 37                                   | Analog ground for PLL and Core   |
| AV <sub>DD</sub>         | 38                                   | Analog voltage supply to PLL and Core  |
| I <sub>REF</sub>         | 39                                   | Reference current for external biasing   |
| XTALIN <sup>[1]</sup>    | 5                                    | Reference crystal input  |
| XTALOUT <sup>[1]</sup>   | 6                                    | Reference crystal feedback   |
| CPUCLK [0–3]             | 42, 45, 48, 51                       | CPU clock outputs  |
| CPUCLK [0–3]B            | 41, 44, 47, 50                       | Inverse CPU clock outputs  |
| PCICLK [0–9]             | 8, 9, 11, 12, 14, 15, 17, 18, 20, 21 | PCI clock outputs, synchronously running at 33.33 MHz  |
| MemRef                   | 55                                   | MemRef clock output, drives memory clock generator   |
| MemRefB                  | 54                                   | MemRefB clock output 180 degrees out of phase with MemRef  |
| 3V66_ [0–3]              | 30, 31, 34, 35                       | AGP and Hub Link clock outputs, running at 66 MHz  |
| USBCLK [0–1]/Sel[A–B]    | 25, 26                               | Sel [A–B] inputs are sensed then internally latched on power-up before the pins are used for 48-MHz USB clock outputs      |
| REFCLK[0–1]/MultSel[0–1] | 2, 3                                 | MultSel[0–1] inputs are sensed then internally latched on power-up before the pins are Reference clock outputs, 14.318 MHz |
| PWR_DWN                  | 28                                   | Active LOW input, powers down part when asserted   |
| SPREAD <sup>[2]</sup>    | 52                                   | Active LOW input, enables spread spectrum when asserted  |
| SEL133                   | 23                                   | CPU frequency select input (See Function Table)  |

**Notes:**

- For best accuracy, use a parallel-resonant crystal, C<sub>LOAD</sub> = 18 pF. For crystals with different C<sub>LOAD</sub>, please refer to the application note, "Crystal Oscillator Topics."
- Input is static HIGH or LOW. Frequency of toggling cannot exceed 30 MHz.

**Function Table<sup>[3]</sup>**

| SEL133 | SELA | SELB | CPUCLK (MHz) | MemRef (MHz) | 3V66CLK (MHz) | PCICLK (MHz) | USBCLK (MHz) | REFCLK (MHz) |
|--------|------|------|--------------|--------------|---------------|--------------|--------------|--------------|
| 0      | 0    | 0    | 100          | 50           | 66            | 33           | 48           | 14.318       |
| 0      | 0    | 1    | N/A          | N/A          | N/A           | N/A          | N/A          | N/A          |
| 0      | 1    | 0    | N/A          | N/A          | N/A           | N/A          | N/A          | N/A          |
| 0      | 1    | 1    | Hi-Z         | Hi-Z         | Hi-Z          | Hi-Z         | Hi-Z         | Hi-Z         |
| 1      | 0    | 0    | 133          | 66           | 66            | 33           | 48           | 14.318       |
| 1      | 0    | 1    | N/A          | N/A          | N/A           | N/A          | N/A          | N/A          |
| 1      | 1    | 0    | N/A          | N/A          | N/A           | N/A          | N/A          | N/A          |
| 1      | 1    | 1    | TCLK/2       | TCLK/4       | TCLK/4        | TCLK/8       | TCLK/2       | TCLK         |

**Actual Clock Frequency Values**

| Clock Output | Target Frequency (MHz) | CY2220-1               |       | CY2220-2               |       |
|--------------|------------------------|------------------------|-------|------------------------|-------|
|              |                        | Actual Frequency (MHz) | PPM   | Actual Frequency (MHz) | PPM   |
| CPUCLK       | 100                    | 99.126                 | -8741 | 100.227                | +2270 |
| CPUCLK       | 133                    | 132.769                | -1740 | 133.269                | +2022 |
| USBCLK       | 48                     | 48.008                 | 167   | 48.008                 | 167   |

**Swing Select Functions**

| MultSel0 | MultSel1 | Board Target | Reference R, I <sub>REF</sub> =                       | Output Current                       | V <sub>OH</sub> @ Z, I <sub>ref</sub> = 2.32 mA |
|----------|----------|--------------|---|--------------------------------------|---|
| 0        | 0        | 60Ω          | R <sub>r</sub> = 475 ± 1%, I <sub>ref</sub> = 2.32 mA | I <sub>OH</sub> = 5*I <sub>ref</sub> | 0.71 @ 60                                       |
| 0        | 0        | 50Ω          | R <sub>r</sub> = 475 ± 1%, I <sub>ref</sub> = 2.32 mA | I <sub>OH</sub> = 5*I <sub>ref</sub> | 0.59 @ 50                                       |
| 0        | 1        | 60Ω          | R <sub>r</sub> = 475 ± 1%, I <sub>ref</sub> = 2.32 mA | I <sub>OH</sub> = 6*I <sub>ref</sub> | 0.85 @ 60                                       |
| 0        | 1        | 50Ω          | R <sub>r</sub> = 475 ± 1%, I <sub>ref</sub> = 2.32 mA | I <sub>OH</sub> = 6*I <sub>ref</sub> | 0.71 @ 50                                       |
| 1        | 0        | 60Ω          | R <sub>r</sub> = 475 ± 1%, I <sub>ref</sub> = 2.32 mA | I <sub>OH</sub> = 4*I <sub>ref</sub> | 0.56 @ 60                                       |
| 1        | 0        | 50Ω          | R <sub>r</sub> = 475 ± 1%, I <sub>ref</sub> = 2.32 mA | I <sub>OH</sub> = 4*I <sub>ref</sub> | 0.47 @ 50                                       |
| 1        | 1        | 60Ω          | R <sub>r</sub> = 475 ± 1%, I <sub>ref</sub> = 2.32 mA | I <sub>OH</sub> = 7*I <sub>ref</sub> | 0.99 @ 60                                       |
| 1        | 1        | 50Ω          | R <sub>r</sub> = 475 ± 1%, I <sub>ref</sub> = 2.32 mA | I <sub>OH</sub> = 7*I <sub>ref</sub> | 0.82 @ 50                                       |

**Clock Driver Impedances**

| Buffer Name     | V <sub>DD</sub> Range | Buffer Type | Impedance |           |           |
|-----------------|-----------------------|-------------|-----------|-----------|-----------|
|                 |                       |             | Minimum Ω | Typical Ω | Maximum Ω |
| CPUCLK, CPUCLKB |                       | Type X1     |           |           |           |
| USB, REF        | 3.135–3.465           | Type 3      | 20        | 40        | 60        |
| PCI, 3V66       | 3.135–3.465           | Type 5      | 12        | 30        | 55        |
| MemRef, MemRefB | 3.135–3.465           | Type 5      | 12        | 30        | 55        |

**Note:**

3. TCLK is a test clock driven in on the XTALIN input in test mode.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage.....-0.5 to +7.0V  
 Input Voltage.....-0.5V to  $V_{DD} + 0.5$

Storage Temperature (Non-Condensing).....-65°C to +150°C  
 Junction Temperature.....  
 +150°C  
 Package Power Dissipation.....1W  
 Static Discharge Voltage  
 (per JEDEC EIA/JESD22-A114-A).....2000V

**Operating Conditions** Over which Electrical Parameters are Guaranteed

| Parameter  | Description   | Min.   | Max.     | Unit |
|--|---|--------|----------|------|
| $V_{DDREF}$ , $V_{DDPCI}$ , $AV_{DD}$ ,<br>$V_{DD3V66}$ , $V_{DDUSB}$ , $V_{DDCPU}$ ,<br>$V_{DDMEM}$ | 3.3V Supply Voltages  | 3.135  | 3.465    | V    |
| $T_A$  | Operating Temperature, Ambient  | 0      | 70       | °C   |
| $C_{in}$   | Input Pin Capacitance Nominal Value   | 18 pF  | 18 pF    | pF   |
| $C_{XTAL}$   | XTAL Pin Capacitance  |        | 22.5     | pF   |
| $C_L$  | Max. Capacitive Load on<br>MemRef, USBCLK, REF<br>PCICLK, 3V66                                    |        | 20<br>30 | pF   |
| $f_{(REF)}$  | Reference Frequency, Oscillator Nominal Value   | 14.318 | 14.318   | MHz  |
| $t_{PU}$   | Power-up time for all VDD's to reach minimum<br>specified voltage (power ramps must be monotonic) | 0.05   | 50       | ms   |

**Electrical Characteristics** Over the Operating Range

| Parameter  | Description               | Test Conditions  | Min.                      | Max.  | Unit  |    |
|------------|---------------------------|--|---------------------------|-------|-------|----|
| $V_{IH}$   | High-level Input Voltage  | Except Crystal Pads. Threshold voltage for crystal pads = $V_{DD}/2$ | 2.0                       |       | V     |    |
| $V_{IL}$   | Low-level Input Voltage   | Except Crystal Pads  |                           | 0.8   | V     |    |
| $V_{OH}$   | High-level Output Voltage | MemRef, USB, REF, 3V66   | $I_{OH} = -1$ mA          | 2.4   | V     |    |
|            |                           | PCI  | $I_{OH} = -1$ mA          | 2.4   | V     |    |
| $V_{OL}$   | Low-level Output Voltage  | MemRef, USB, REF, 3V66   | $I_{OL} = 1$ mA           | 0.4   | V     |    |
|            |                           | PCI  | $I_{OL} = 1$ mA           | 0.55  | V     |    |
| $I_{IH}$   | Input High Current        | $0 \leq V_{IN} \leq V_{DD}$  | -5                        | 5     | μA    |    |
| $I_{IL}$   | Input Low Current         | $0 \leq V_{IN} \leq V_{DD}$  | -5                        | 5     | μA    |    |
| $I_{OH}$   | High-level Output Current | CPU<br>For $I_{OH} = 6 \cdot I_{Ref}$ Configuration                  | Type X1, $V_{OH} = 0.65V$ | -12.9 | -14.9 | mA |
|            |                           | USB, REF   | Type 3, $V_{OH} = 2.4V$   | -15   | -51   |    |
|            |                           | 3V66, PCI, MemRef, MemRefB   | Type 5, $V_{OH} = 2.4V$   | -30   | -100  |    |
| $I_{OL}$   | Low-level Output Current  | USB, REF   | Type 3, $V_{OL} = 0.4V$   | 10    | 24    | mA |
|            |                           | 3V66, PCI, MemRef, MemRefB   | Type 5, $V_{OL} = 0.4V$   | 20    | 49    |    |
| $I_{OZ}$   | Output Leakage Current    | Three-state  |                           | 10    | μA    |    |
| $I_{DD3}$  | 3.3V Power Supply Current | $AV_{DD}/V_{DD33} = 3.465V$ , $F_{CPU} = 133$ MHz                    |                           | 250   | mA    |    |
| $I_{DDP3}$ | 3.3V Shutdown Current     | $AV_{DD}/V_{DDQ3} = 3.465V$  |                           | 60    | mA    |    |

**Switching Characteristics<sup>[4]</sup> Over the Operating Range**

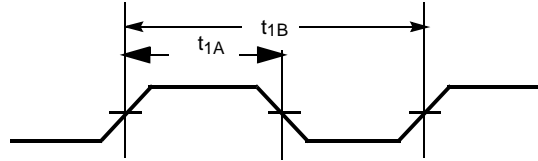
| Parameter              | Output            | Description                      | Test Conditions  | Min.                   | Max.                   | Unit |
|------------------------|-------------------|----------------------------------|--|------------------------|------------------------|------|
| t <sub>1</sub>         | All               | Output Duty Cycle <sup>[5]</sup> | t <sub>1A</sub> /(t <sub>1B</sub> )  | 45                     | 55                     | %    |
| t <sub>2</sub>         | CPU               | Rise Time                        | Measured at 20% to 80% of V <sub>OH</sub>  | 175                    | 700                    | ps   |
| t <sub>2</sub>         | USB, REF          | Rising Edge Rate                 | Between 0.4V and 2.4V  | 0.5                    | 2.0                    | V/ns |
| t <sub>2</sub>         | PCI, 3V66, MemRef | Rising Edge Rate                 | Between 0.4V and 2.4V  | 1.0                    | 4.0                    | V/ns |
| t <sub>3</sub>         | CPU               | Fall Time                        | Measured at 80% to 20% of V <sub>OH</sub>  | 175                    | 700                    | ps   |
| t <sub>3</sub>         | USB, REF          | Falling Edge Rate                | Between 2.4V and 0.4V  | 0.5                    | 2.0                    | V/ns |
| t <sub>3</sub>         | PCI, 3V66, MemRef | Falling Edge Rate                | Between 2.4V and 0.4V  | 1.0                    | 4.0                    | V/ns |
| t <sub>4</sub>         | CPU               | CPU-CPU Skew                     | Measured at Crossover  |                        | 150                    | ps   |
| t <sub>5</sub>         | 3V66              | 3V66-3V66 Skew                   | Measured at 1.5V   |                        | 250                    | ps   |
| t <sub>6</sub>         | PCI               | PCI-PCI Skew                     | Measured at 1.5V   |                        | 500                    | ps   |
| t <sub>7</sub>         | 3V66, PCI         | 3V66-PCI Clock Skew              | 3V66 leads. Measured at 1.5V   | 1.5                    | 3.5                    | ns   |
| t <sub>8</sub>         | CPU               | Cycle-Cycle Clock Jitter         | Measured at Crossover t <sub>8</sub> = t <sub>8A</sub> - t <sub>8B</sub><br>With all outputs running |                        | 200                    | ps   |
| t <sub>9</sub>         | Mref              | Cycle-Cycle Clock Jitter         | Measured at 1.5V t <sub>9</sub> = t <sub>9A</sub> - t <sub>9B</sub>                                  |                        | 250                    | ps   |
| t <sub>9</sub>         | 3V66              | Cycle-Cycle Clock Jitter         | Measured at 1.5V t <sub>9</sub> = t <sub>9A</sub> - t <sub>9B</sub>                                  |                        | 300                    | ps   |
| t <sub>9</sub>         | USB               | Cycle-Cycle Clock Jitter         | Measured at 1.5V t <sub>9</sub> = t <sub>9A</sub> - t <sub>9B</sub>                                  |                        | 350                    | ps   |
| t <sub>9</sub>         | PCI               | Cycle-Cycle Clock Jitter         | Measured at 1.5V t <sub>9</sub> = t <sub>9A</sub> - t <sub>9B</sub>                                  |                        | 500                    | ps   |
| t <sub>9</sub>         | REF               | Cycle-Cycle Clock Jitter         | Measured at 1.5V t <sub>9</sub> = t <sub>9A</sub> - t <sub>9B</sub>                                  |                        | 1000                   | ps   |
|                        | CPU, PCI          | Settle Time                      | CPU and PCI clock stabilization from power-up  |                        | 3                      | ms   |
|                        | CPU               | Rise/Fall Matching               | Measured with test loads <sup>[6, 7]</sup>   |                        | 20%                    |      |
|                        | CPU               | Overshoot                        | Measured with test loads <sup>[7]</sup>  |                        | V <sub>OH</sub> + 0.2  | V    |
|                        | CPU               | Undershoot                       | Measured with test loads <sup>[7]</sup>  | -0.2                   |                        | V    |
| V <sub>oh</sub>        | CPU               | High-level Output Voltage        | Measured with test loads <sup>[7]</sup>  | 0.65                   | 0.74                   | V    |
| V <sub>ol</sub>        | CPU               | Low-level Output Voltage         | Measured with test loads <sup>[7]</sup>  | 0.0                    | 0.05                   | V    |
| V <sub>crossover</sub> | CPU               | Crossover Voltage                | Measured with test loads <sup>[7]</sup>  | 45% of V <sub>OH</sub> | 55% of V <sub>OH</sub> | V    |

**Notes:**

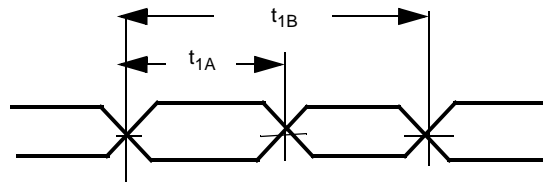
4. All parameters specified with loaded outputs. Parameters not tested in production, but are guaranteed by design characterization.
5. Duty cycle is measured at 1.5V with V<sub>DD</sub> at 3.3V on all output except CPU. Duty Cycle on CPU is measured at V<sub>Crossover</sub>.
6. Determined as a fraction of 2\*(t<sub>RP</sub> - t<sub>RN</sub>)/(t<sub>RP</sub> + t<sub>RN</sub>) Where t<sub>RP</sub> is a rising edge and t<sub>RN</sub> is an intersecting falling edge.
7. The test load is specified in test circuit.

## Switching Waveforms

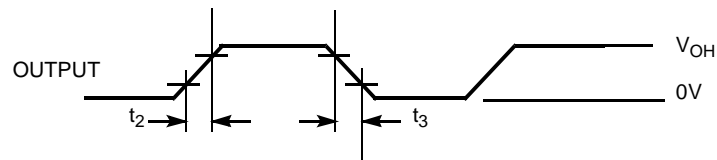
### Duty Cycle Timing (Single Ended Output)



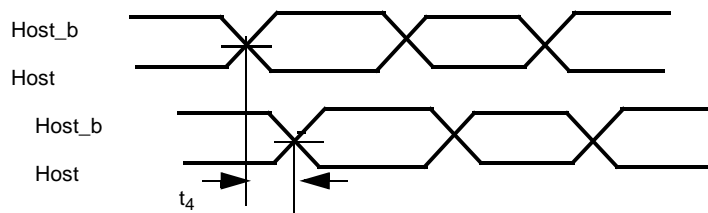
### Duty Cycle Timing (CPU Differential Output)



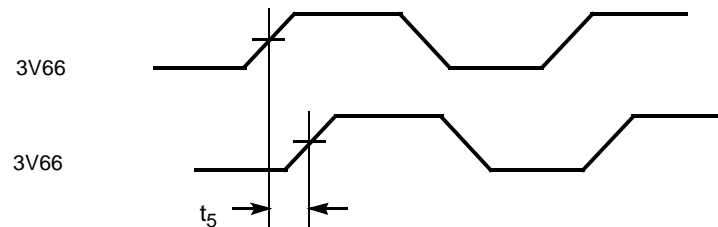
### All Outputs Rise/Fall Time

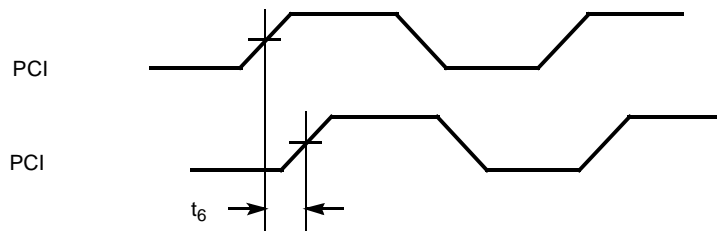
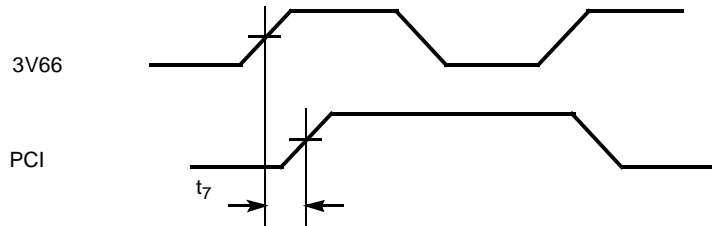
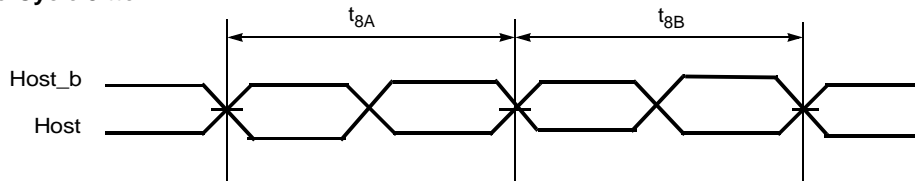
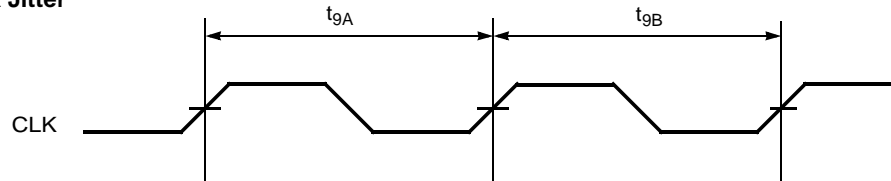
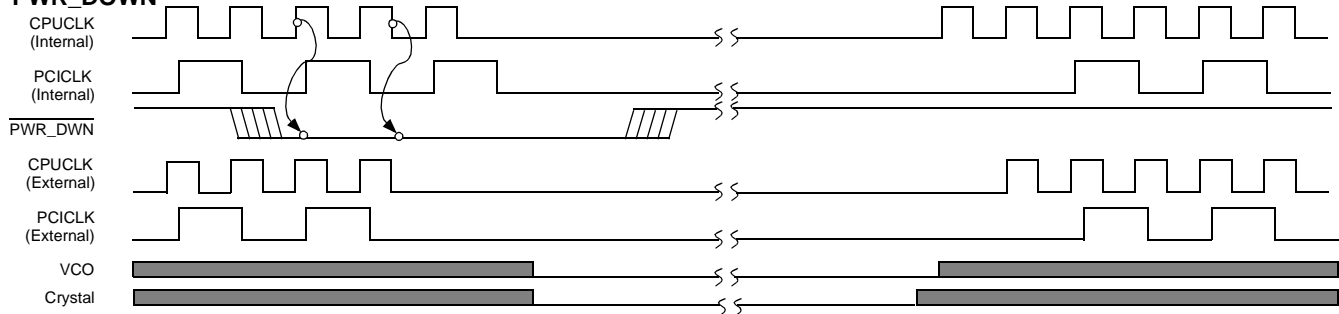


### CPU-CPU Clock Skew

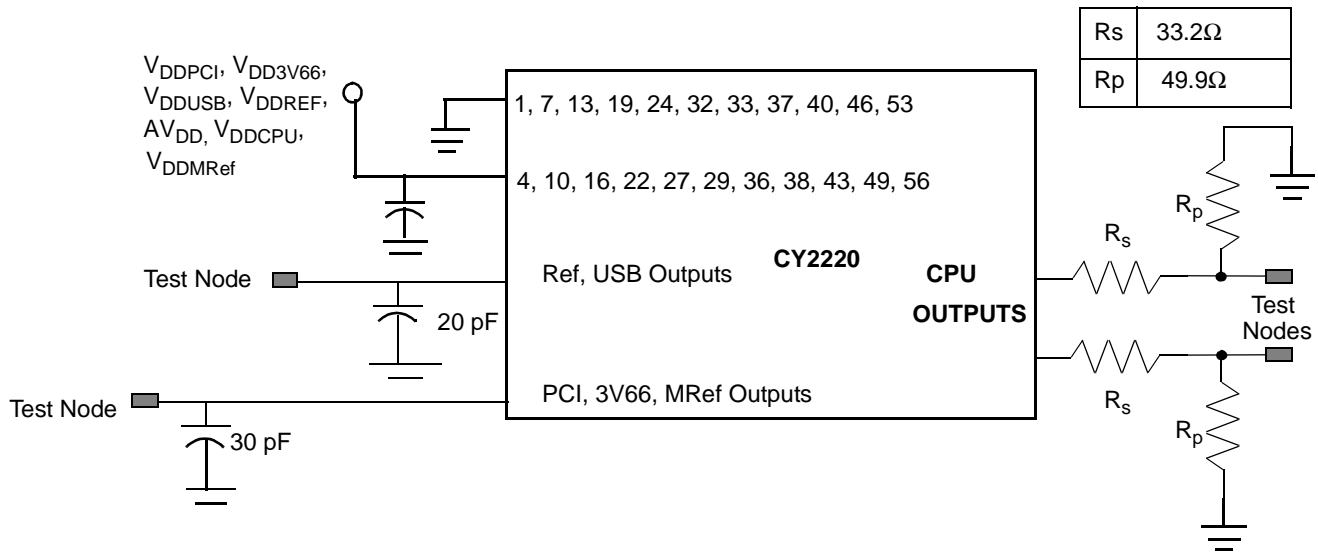


### 3V66-3V66 Clock Skew



**Switching Waveforms (continued)**
**PCI-PCI Clock Skew**

**3V66-PCI Clock Skew**

**CPU Clock Cycle-Cycle Jitter**

**Cycle-Cycle Clock Jitter**

**PWR\_DOWN<sup>[8]</sup>**

**Note:**

8. Shaded section on the VCO and Crystal waveforms indicates that the VCO and crystal oscillator are active, and there is a valid clock.

**Test Circuit**<sup>[9, 10]</sup>

**Ordering Information**

| Ordering Code | Package Name | Package Type | Operating Range |
|---------------|--------------|--------------|-----------------|
| CY2220PVC-1   | O56          | 56-Pin SSOP  | Commercial      |
| CY2220PVC-2   | O56          | 56-Pin SSOP  | Commercial      |

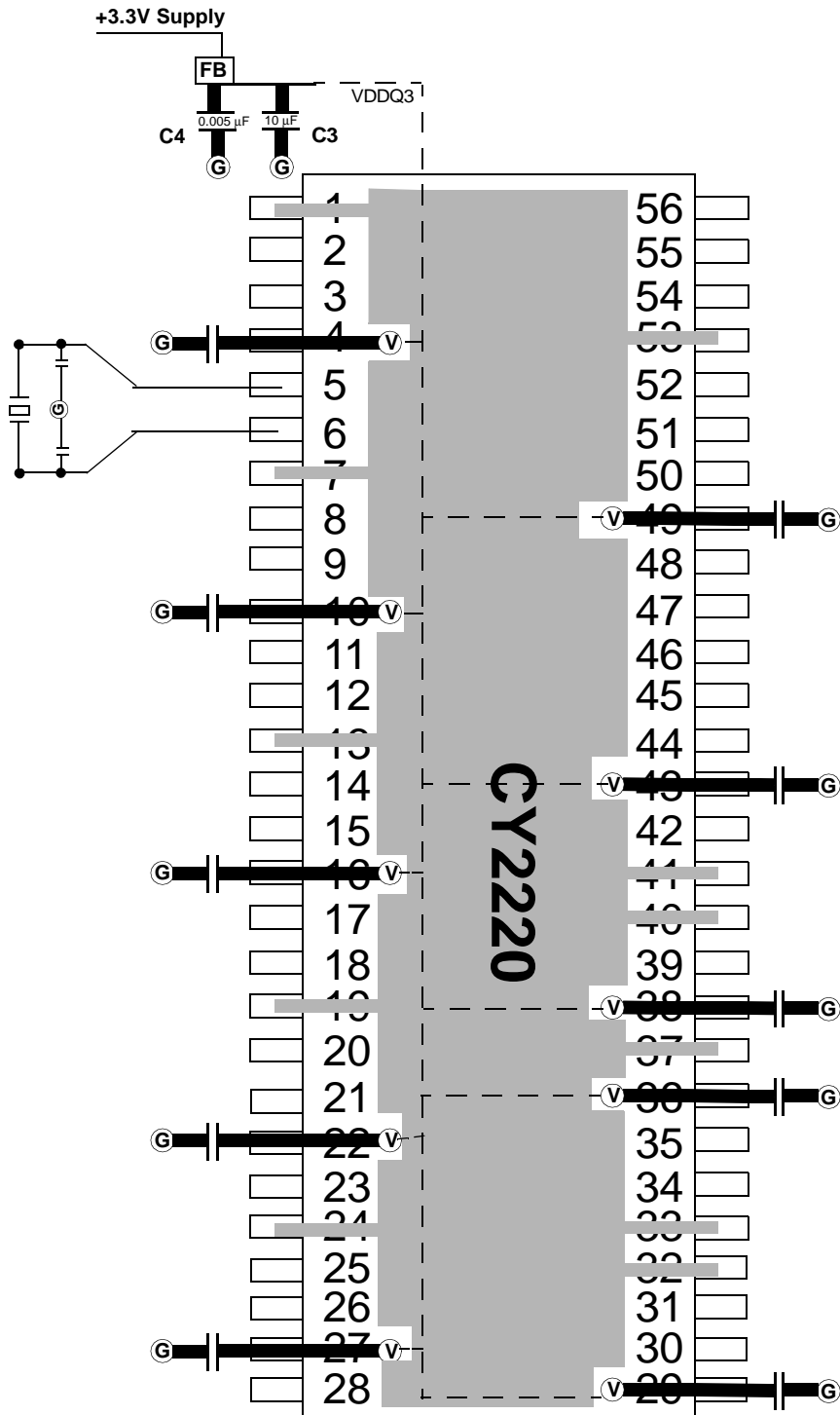
**Notes:**

9. Each supply pin must have an individual decoupling capacitor.

10. All capacitors must be placed as close to the pins as is physically possible.



Layout Example



FB = Dale ILB1206 - 300 (30Ω @ 100 MHz)

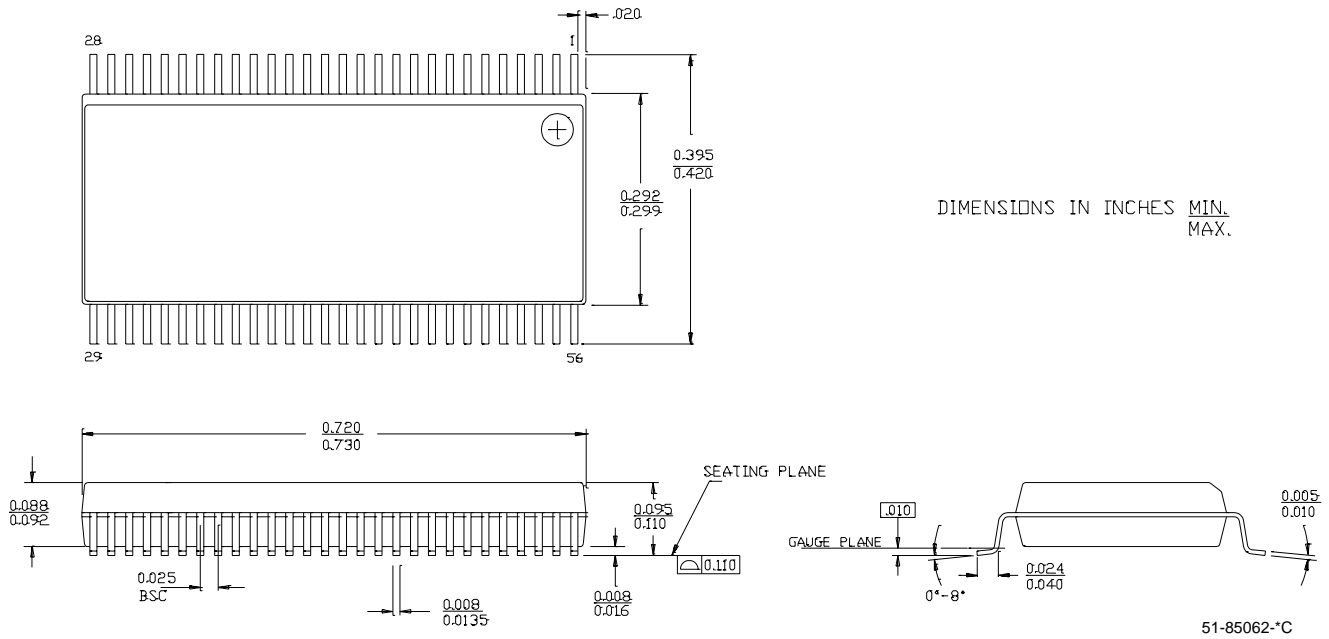
Ceramic Caps C3 = 10–22 μF C4 = 0.005 μF

⊗ = VIA to GND plane layer ⊙ = VIA to respective supply plane layer

Note: Each supply plane or strip should have a ferrite bead and capacitors  
All bypass caps = 0.01 μF ceramic

Package Diagram

56-Lead Shrunken Small Outline Package O56



| <b>Document Title: CY2220 133-MHz Spread Spectrum Clock Synthesizer/Driver with Differential CPU Outputs</b> |                |                   |                        |   |
|--|----------------|-------------------|------------------------|---|
| <b>Document Number: 38-07206</b>   |                |                   |                        |   |
| <b>REV.</b>  | <b>ECN NO.</b> | <b>Issue Date</b> | <b>Orig. of Change</b> | <b>Description of Change</b>                                    |
| **   | 111730         | 01/17/02          | DSG                    | Change from Spec number: 38-00813 to 38-07206                   |
| *A   | 121841         | 12/30/02          | RBI                    | Power up requirements added to Operating Conditions Information |