CS4922

MPEG/G.729A Audio Decoder System

Features

- DSP Optimized for Audio Decode, 24-bit Fixed Point w/48-bit Accumulator
- On-Chip Functional Blocks Include:
  - DSP with RAM and ROM Memories
  - CD Quality Stereo DAC with Output Filtering
  - Mono Output & Digital Volume Control
  - S/PDIF Transmitter, Bidirectional PCM Audio Port
  - Internal Phase Locked Loop for Clocking
  - Dedicated Compressed Serial Input Interface
- MPEG-1 & MPEG-2 Layers 1 & 2 With All Sample/Bit Rates and Ancillary Data Support.
- MPEG-1 & MPEG-2 Packetized Audio Stream and Elementary Stream Input
- G.729A Audio Decode
- PCM Synthesis for Auxiliary Audio
- Pin Compatibility with CS4920A and Primary Feature/Firmware Compatible
- +5 Volt Only CMOS, 44 pin PLCC

Description

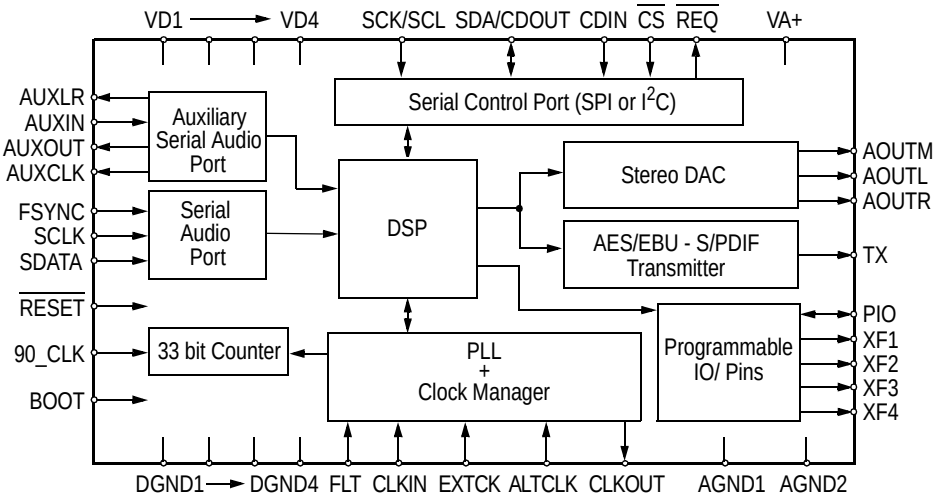
The CS4922 is a complete audio decompression subsystem implemented in a single high integration mixed signal CMOS chip. The CS4922 has been widely used in direct broadcast system set-top boxes and proprietary embedded systems which pull compressed audio from local system memory.

The CS4922 is tailored to include the necessary hardware and firmware to ensure proper audio/video synchronization for MPEG-2 audio decompression. In addition to audio decoding this programmable DSP solution provides robust error concealment and feature implementations like ancillary data support and PCM synthesis.

The CS4922 can also support the decode of other compression standards such as G.729A with a separate download image. The flexible architecture of the CS4922 provides the ability to mix compressed audio with data from the auxiliary PCM port.

ORDERING INFORMATION

CS4922-CL	44-pin PLCC
CDB4922	Evaluation Board



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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Contacting Cirrus Logic Support

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1 CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5V; CLKIN = 27 MHz; Full-Scale Output Sinewave, 1.125 kHz; Word Clock = 48 kHz (PLL in use); Logic 0 = GND, Logic 1 = VD+; Measurement Bandwidth is 20 Hz to 20 kHz; Local components as shown in "Typical Connection Diagram"; SPI mode, I^2S audio data; unless otherwise specified.)

Parameter*			Symbol	Min	Typ	Max	Units
Dynamic Performance							
DAC Resolution				16	-	-	Bits
DAC Differential Nonlinearity			DNL	-	-	±0.9	LSB
Total Harmonic Distortion	AOUTL, AOUTR AOUTM	(Note 1)	THD	- -	0.01 0.02	0.015 0.03	%
Instantaneous Dynamic Range (DAC not muted, A weighted)	AOUTL, AOUTR AOUTM	(Note 1)	IDR	85 80	90 85	-	dB
Interchannel Isolation		(Note 1)		-	85	-	dB
Interchannel Gain Mismatch				-	-	0.2	dB
Frequency Response				-3.0	-	+0.2	dB
Full Scale output Voltage	AOUTL, AOUTR AOUTM	(Note 1)		2.66 2.7	2.88 3.0	3.2 3.3	Vpp
Gain Drift				-	100	-	ppm/°C
Deviation from Linear Phase				-	-	5	Deg
Out of Band Energy	(Fs/2 to 2Fs)			-	-60	-	dB
Analog Output Load	Resistance: Capacitance:			8 -	- -	- 100	kΩ pF
Power Supply							
Power Supply Rejection	(1 kHz)			-	40	-	dB
Power Supply Consumption	VA+ VD+			- -	20 100	40 140	mA mA

Notes: 1. 10 kΩ, 100pF load for each analog signal (Left, Right).
30 kΩ, 100pF load for analog Mono signal.

D/A INTERPOLATION FILTER CHARACTERISTICS (See Figures 20 through 23)

Parameter		Symbol	Min	Typ	Max	Units
Passband (to -3 dB corner)	(Fs is conversion freq.).		0	-	0.476Fs	Hz
Passband Ripple.			-	-	±0.1	dB
Transition Band.			0.442Fs	-	0.567Fs	Hz
Stop Band.			≥0.567Fs	-	-	Hz
Stop Band Rejection.			50	-	-	dB
Stop Band Rejection with Ext. 2Fs RC filter.			57	-	-	dB
Group Delay.			-	12/Fs	-	s

* Refer to *Parameter Definitions* on page 31 of this data sheet.

Specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	-0.3	6.0	V
	Positive Analog	VA+	-0.3	6.0	V
	| | VA+ | - | VD+ | |		-	0.4	V
Input Current, Any Pin Except Supplies		I_{in}	-	±10	mA
Digital Input Voltage		V_{IND}	-0.3	(VD+) + 0.4	V
Ambient Operating Temperature (power applied)		T_{Amax}	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V; all voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.50	5.0	5.50	V
	Positive Analog	VA+	4.50	5.0	5.50	V
	| | VA+ | - | VD+ | |		-	-	0.4	V
Ambient Operating Temperature		T_A	0	-	70	°C

DIGITAL CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5V±10%; measurements performed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	TBD	2.25	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage at I_o = -2.0 mA	V_{OH}	VD x 0.9	-	-	V
Low-Level Output Voltage at I_o = 2.0 mA	V_{OL}	-	-	VD x 0.1	V
Input Leakage Current (Note 2)	I_{in}	-	-	1.0	µA

Notes: 2. Not Valid for pin numbers 9, 12, 13, and 30 which are configured with on-chip pull-down resistors. Not valid for pin number 29 which is a static input signal and should be tied to either VD+ or DGND.

SWITCHING CHARACTERISTICS - CLOCKS (T_A = 25 °C; VA+, VD+ = 5V; Inputs: Logic 0 = DGND, Logic 1 = VD+, C_L = 20pF)

Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency	CLKIN		27		MHz
Master Clock Duty Cycle	CYCK	40	50	60	%
Clock Output	CLKOUT	-	-	256 Fs	MHz

SWITCHING CHARACTERISTICS - EXTERNAL FLAGS (T_A = 25 °C; VA+, VD+ = 5V; Inputs: Logic 0 = DGND, Logic 1 = VD+, C_L = 20pF)

Parameter	Symbol	Min	Typ	Max	Units
Rise time of XF1-XF4 (Note 3)	t_{rxf}			200	ns
Fall time of XF1-XF4	t_{fxf}			100	ns

Notes: 3. Assumes 2kΩ pull-up to 5V supply on XF1-XF4 pins.

SWITCHING CHARACTERISTICS - PROGRAMMABLE INPUT/OUTPUT (T_A = 25 °C; VA+, VD+ = 5V; Inputs: Logic 0 = DGND, Logic 1 = VD+, C_L = 20pF)

Parameter	Symbol	Min	Typ	Max	Units
I_O = 0					
Input Frequency	f_{pio}			350	kHz
Risetime of PIO	t_{rpio}			200	ns
Fall time of PIO	t_{fpio}			200	ns
I_O = 1					
Rise time of PIO	t_{rpo}			200	ns
Fall time of PIO	t_{fpo}			200	ns

SWITCHING CHARACTERISTICS - BOOT INITIALIZATION (T_A = 25 °C; VA+, VD+ = 5V; Inputs: Logic 0 = DGND, Logic 1 = VD+, C_L = 20pF)

Parameter		Symbol	Min	Max	Units
BOOT Setup Time to $\overline{\text{RESET}}$ Rising		t_{bsu}	350	-	ns
$\overline{\text{RESET}}$ Rising to Boot Hold Time		t_{bh}	450	-	ns
$\overline{\text{CS}}$ Setup Time to $\overline{\text{RESET}}$ Rising	(Note 4)	t_{cssu}	200	-	ns
$\overline{\text{RESET}}$ Rising to $\overline{\text{CS}}$ Hold Time		t_{csh}	400	-	ns
$\overline{\text{RESET}}$ Low Time		t_{rlow}	50	-	µs
SCK/SCL Delay Time from $\overline{\text{RESET}}$ Rising	(Note 5)	t_{rsc}	2	-	ms
SCK/SCL falling to $\overline{\text{CS}}$ rising on last byte of download		t_{sfcr}	3	-	µs

Notes: 4. The mode of the Serial Control Port is selected by $\overline{\text{CS}}$. $\overline{\text{CS}}$ = 1 is I^2C® . $\overline{\text{CS}}$ = 0 is SPI mode.

5. This delay is necessary after any rising edge of $\overline{\text{RESET}}$ to allow time for the part to initialize and for the on-board PLL to stabilize.

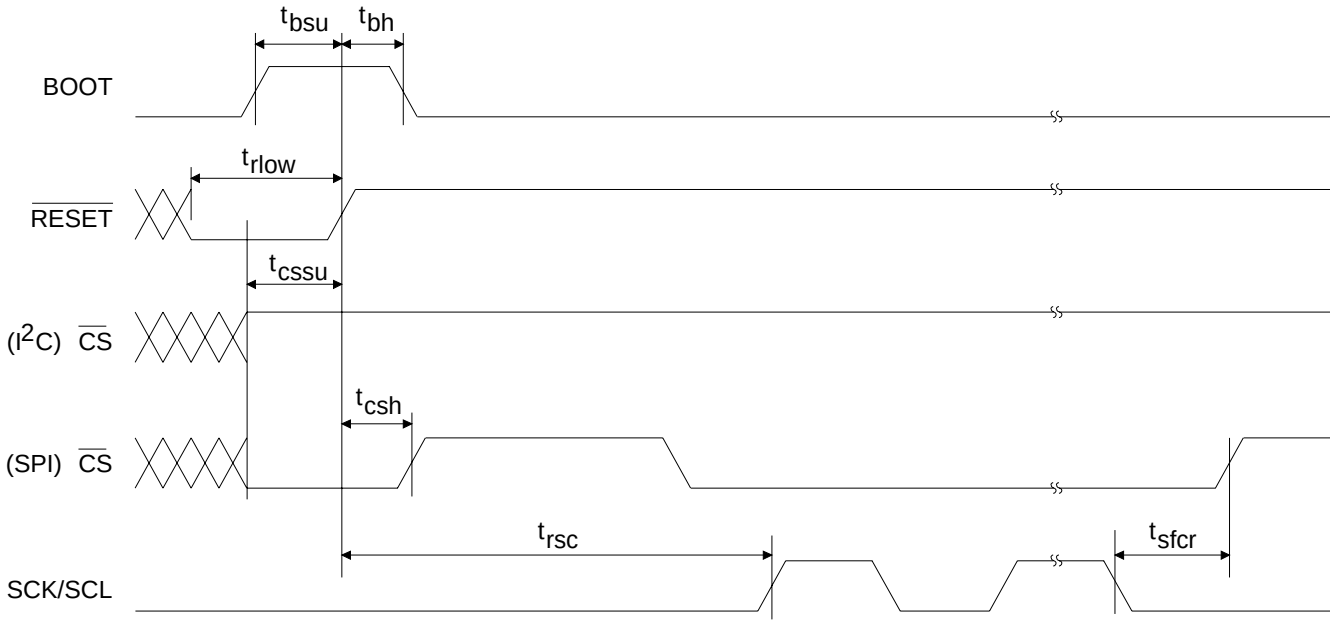


Figure 1. Boot Timing

SWITCHING CHARACTERISTICS - CONTROL PORT (SPI MODE) (T_A = 25 °C; VA+, VD+ = 5V; Inputs: Logic 0 = DGND, Logic 1 = VD+, C_L = 20pF)

Parameter			Symbol	Min	Max	Units
SPI Mode (CS = 0)						
SCK/SCL Clock Frequency	(slow mode) (fast mode)		f_{sck} f_{sck}	- -	350 2000	kHz
$\overline{CS}$ Falling to SCK/SCL Rising	(slow mode)		t_{css}	20	-	ns
Rise Time of Both CDIN and SCK/SCL Lines	(slow mode)		t_r	-	50	ns
Fall Time of Both CDIN and SCK/SCL Lines	(slow mode) (fast mode)		t_f t_f	- -	300 50	ns ns
SCK/SCL Low Time	(slow mode) (fast mode)		t_{scl} t_{scl}	1100 150	- -	ns ns
SCK/SCL High Time	(slow mode) (fast mode)		t_{sch} t_{sch}	1100 150	- -	ns ns
Setup Time CDIN to SCK/SCL Rising	(slow mode) (fast mode)		t_{cdisu}	250 50	- -	ns ns
Hold Time SCK/SCL Rising to CDIN		(Note 6)	t_{cdih}	50	-	ns
Transition Time from SCK/SCL to CDOUT Valid		(Note 7)	t_{scdov}	-	40	ns
Time from SCK/SCL Rising to $\overline{REQ}$ Rising		(Note 7)	t_{scrh}	-	200	ns
Rise Time for $\overline{REQ}$		(Note 8)	t_{rr}	-	50	ns
Fall Time for $\overline{REQ}$		(Note 9)	t_{rf}	-	20	ns
Hold Time for $\overline{REQ}$ from SCK/SCL Rising		(Note 9)	t_{scrl}	0	-	ns
Time from SCK/SCL Falling to $\overline{CS}$ Rising			t_{sccsh}	20	-	ns
High Time Between Active $\overline{CS}$			t_{csht}	200	-	ns

Notes:
6. Data must be held for sufficient time to bridge 300(50) ns transition time of SCK/SCL.
7. CDOUT should NOT be sampled during this time period.
8. $\overline{REQ}$ will only go HIGH if there is no data in SCPOUT at the rising edge of SCL/SCK during a READ operation as shown. DSP frequency is 20 MHz. Pull-up resistor is 2 kΩ. C_L = 20 pF.
9. If $\overline{REQ}$ went HIGH as indicated in note 7, then $\overline{REQ}$ will hold high at least until the next rising edge of SCK/SCL. If data is in SCPOUT at this time $\overline{REQ}$ will go active LOW again. This condition should be treated as a new READ process. Address and R/$\overline{W}$ bit should be sent again.

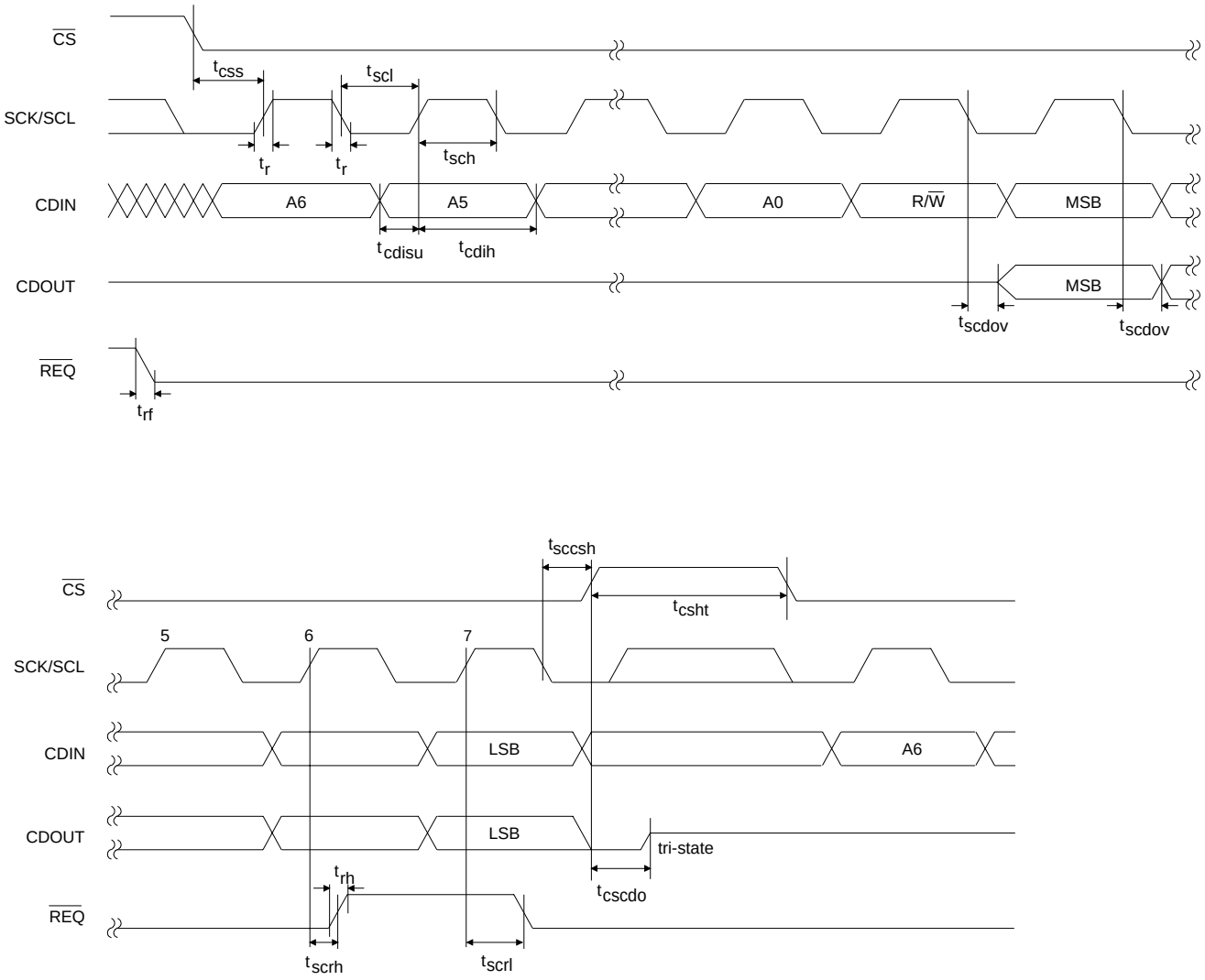


Figure 2. SPI Control Port Timing

SWITCHING CHARACTERISTICS - CONTROL PORT (I^2C MODE) (T_A = 25 °C; VA+, VD+ = 5V; Inputs: Logic 0 = DGND, Logic 1 = VD+, C_L = 20pF)

Parameter		Symbol	Min	Max	Units
I^2C® Mode ($\overline{CS}$=1)	***(Note 10)***				
SCK/SCL Clock Frequency	(slow mode) (fast mode)	f_{scl}		100 400	kHz
Bus Free Time Between Transmissions		t_{buf}	4.7		µs
Start Condition Hold Time (prior to first clock pulse)		t_{hdst}	4.0		µs
Clock Low Time	slow fast	t_{low}	4.7 1.2		µs
Clock High Time	slow fast	t_{high}	4.0 1.0		µs
SDA Setup Time to SCK/SCL Rising		t_{sud}	250		ns
SDA Hold Time from SCK/SCL Falling	(Note 11)	t_{hdd}	0		µs
Rise Time of Both SDA and SCK/SCL	(Note 12)	t_r		50	ns
Fall Time of Both SDA and SCK/SCL		t_f		300	ns
Time from SCK/SCL Falling to CS4920 ACK		t_{sca}		40	ns
Time from SCK/SCL Falling to SDA Valid During READ Operation		t_{scsdv}		40	ns
Time from SCK/SCL Rising to $\overline{REQ}$ Rising	(Note 13)	t_{scrh}		200	ns
Hold Time for $\overline{REQ}$ from SCK/SCL Rising	(Note 14)	t_{scrl}	0		ns
Rise Time for $\overline{REQ}$	(Note 13)	t_{rr}		50	ns
Fall Time for $\overline{REQ}$	(Note 14)	t_{rf}		20	ns
Setup Time for Stop Condition		t_{susp}	4.7		µs

Notes: 10. Use of I^2C® bus compatible interface requires a license from Philips.

11. Data must be held for sufficient time to bridge the 300ns transition time of SCK/SCL.

12. This rise time is shorter than the I^2C specifications recommend, please refer to the section on SCP communications for more information.

13. $\overline{REQ}$ will only go HIGH if there is no data in the SCPOUT register at the rising edge of SCL/SCK during a READ operation as shown. DSP frequency is 20 MHz. Pull-up resistor is 2 kΩ C_L = 20pF.

14. if $\overline{REQ}$ went HIGH as indicated in Note 13 then $\overline{REQ}$ will hold HIGH at least until the next rising edge of SCK/SCL. If data is in the SCPOUT register at this time $\overline{REQ}$ will go active LOW again. This condition should be treated as a new READ process. The address and R/$\overline{W}$ should be sent again following a new START condition.

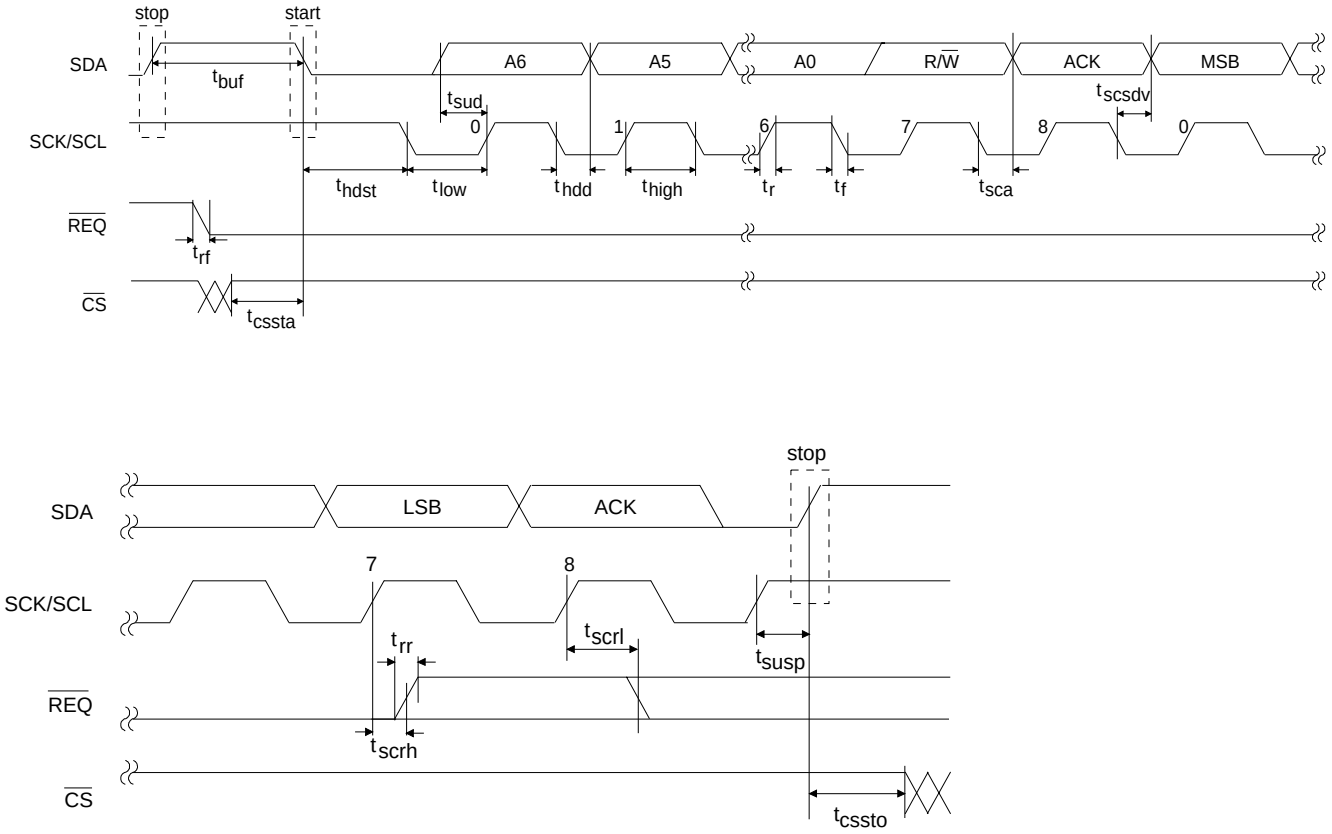


Figure 3. I²C® Control Port Timing

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT (T_A = 25 °C; VA+, VD+ = 5V; Inputs: Logic 0 = GND, Logic 1 = VD+; C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Units
SCLK Frequency			-	-	12.5	MHz
SCLK Pulse Width Low		t_{sckl}	25	-	-	ns
SCLK Pulse Width High		t_{sckh}	25	-	-	ns
SCLK rising to FSYNC edge delay	(Note 15)	t_{sfds}	20	-	-	ns
SCLK rising to FSYNC edge setup	(Note 15)	t_{sfs}	20	-	-	ns
SDATA valid to SCLK rising setup	(Note 15)	t_{sss}	20	-	-	ns
SCLK rising to SDATA hold time	(Note 15)	t_{ssh}	20	-	-	ns
Rise time of SCLK		t_{sclr}	-	-	20	ns

Notes: 15. The table above assumes data is output on the falling edge and latched on the rising edge. The SCLK edge is selectable in setting the EDG bit in the ASICN register. The diagram is for EDG = 1.

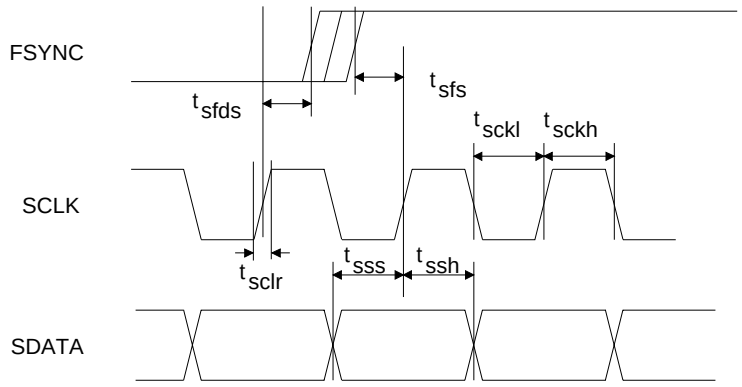


Figure 4. Serial Audio Port Timing

SWITCHING CHARACTERISTICS - AUXILIARY DIGITAL AUDIO PORT

Parameter		Symbol	Min	Typ	Max	Units
Input Sample Rate	(Note 16)	Fs	16	-	48	kHz
AUXCLK Period	(Note 17)	tsclk	-	1/(32Fs) 1/(64Fs) 1/(128Fs)	-	ns
AUXCLK to AUXLR valid		tlrun	0	-	25	ns
AUXCLK to AUXOUT data valid		tdoun	0	-	25	
AUXIN data setup time to AUXCLK		tdisu	50	-	-	ns
AUXIN data hold time from AUXCLK		tdiho	3	-	-	ns

Notes: 16. Fs determined by clock input rate and configuration of on-chip PLL.

17. AUXCLK frequency selectable @ 32, 64, or 128 Fs via AUXCN register bits 1:0.

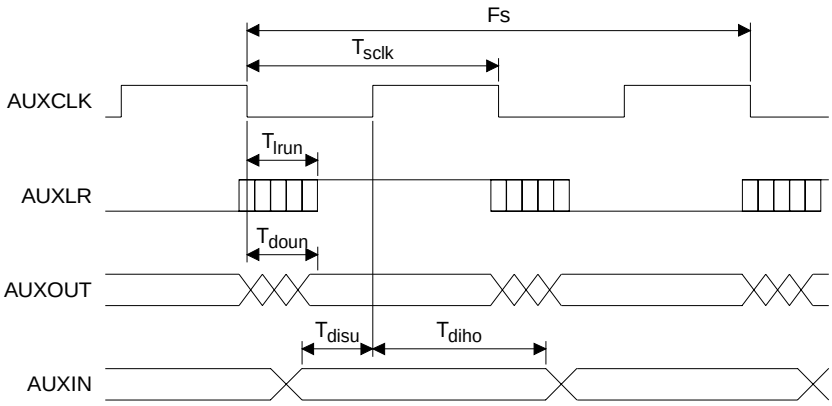


Figure 5. Auxiliary Audio Port Timing

2 TYPICAL CONNECTION DIAGRAM

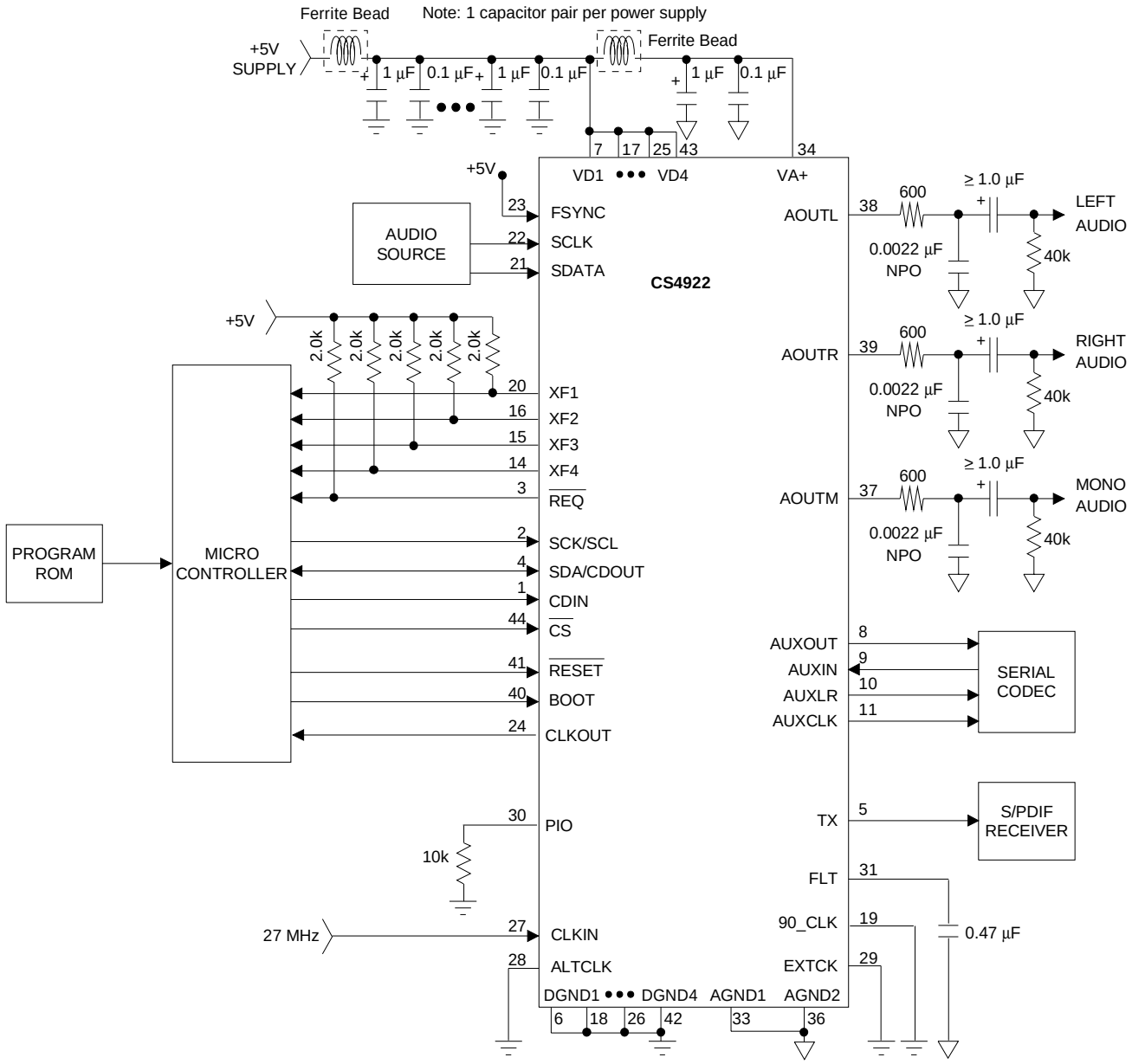


Figure 6. Typical Connection Diagram

3 THEORY OF OPERATION

3.1 Introduction

The CS4922 is a complete audio subsystem on a chip. It consists of a general-purpose Digital Signal Processor (DSP), and a number of supplementary analog and digital blocks. These supplementary blocks include a PLL clock multiplier, a serial audio input port, an auxiliary serial audio port, a CD quality stereo Digital-to-Analog Converter (DAC), an AES/EBU - S/PDIF compatible digital audio transmitter, and a serial control port. Figure 6 shows a typical connection diagram for the CS4922 in which a micro controller is used for loading the program code.

The CS4922 is RAM based audio decoder that can be used to process compressed digital audio signals. Serial audio data broadcast on networks such as cable TV, direct broadcast satellite TV, or the telephone system can be decompressed and converted to standard analog and digital signals. A wide variety of standard and proprietary decompression algorithms can be supported.

CS4922 application code is available which performs industry standard MPEG 1 and 2, layers I and II. Application code is also available for G.729A decode.

The DSP has a 24-bit fixed point data path, 5K words of program RAM, and 3K words of data RAM. The execution unit includes a 48-bit accumulator. The DSP can provide up to 12 MIPS.

Either compressed digital audio data or PCM data can be delivered.

For analog reproduction of the digital input, a stereo DAC using delta-sigma architecture is built-in. Switched-capacitor filters perform most of the reconstruction process. Only a simple external passive filter is needed to complete reconstruction.

In addition to the analog output, an AES/EBU - S/PDIF compatible output is provided. This allows the designer the flexibility of transmitting the audio data in a standard digital format to an external system.

To facilitate the downloading of DSP code to the CS4922, a serial control port, communicating in either I^2C® or SPI format, is used. This port may also be used during run time to issue control commands to the DSP.

4 PERIPHERALS

Six on-chip peripherals make the audio decoder ideal for decoding broadcast digital audio signals. It has a PLL clock manager, a CD quality DAC, a digital audio transmitter, a three pin serial port for audio data input, a serial bi-directional auxiliary port for digital audio data, and an SPI/I^2C port for serial control information. Each peripheral has I/O mapped data, control, and status registers. Many peripherals can also generate interrupts.

4.1 Clock Manager

The clock manager is primarily a clock multiplier circuit that takes a reference frequency of 27 MHz on CLKIN which is used for deriving internal clocking. At the heart of the clock manager circuit is a PLL (Phase-Locked Loop) circuit. The PLL is configured by software to produce the appropriate DSP Clock for the desired sample rate. All other internal clocks required for the DAC and other peripherals are derived from this root clock.

The PLL's internal VCO requires a capacitor to be connected to the FLT pin (pin 31). The typical value of the FLT capacitor is 0.47 µf, which is sufficient for all allowable CLKIN input frequencies. It must be stressed that the best analog performance can only be achieved by placing the capacitor as close as possible to the FLT pin and that the proper layout precautions be taken to avoid noise coupling onto the FLT pin.

The CLKOUT pin is a divided version of the DSP clock. A diagram of the CLKOUT generation circuit is shown in Figure 7.

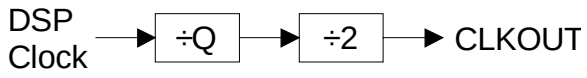


Figure 7. CLKOUT Generation Circuit

The DSP clock is divided by a programmable divider and an additional divide by 2 before being output. The divider output is determined by the value of the Q value which can be accessed through the application software. The divide by 2 guarantees a 50% duty cycle output. The Q value provides effective divides ranging from 1 to 1024, which means the frequency of CLKOUT can vary from the DSP clock frequency divided by 2 to the DSP clock frequency divided by 2048. CLKOUT can be used to synchronize external devices or generate most compressed bit rate clocks.

4.2 33-bit Counter

The 33-bit-counter can be used to support MPEG synchronization of audio and video. This loadable counter is targeted to operate at 90 kHz. The 90 kHz clock may be derived from a 27 MHz master clock provided at CLKIN (if available) or from a 90 kHz clock provided at Pin 19 90_CLK. The selection of the counter clock is made via the register bit DIV which is accessible through the application code. When set, the DIV bit divides the clock at CLKIN by 300 and provides the divided clock to 33-bit-counter.

4.3 Digital to Analog Converter

The digital to analog converter (DAC) is a dual channel CD quality DAC. It is designed with delta sigma architecture. The baseband audio is interpolated to 128Fs (192Fs) before going into the modulator. The modulator is third order and is followed by a 1 bit DAC/switch capacitor filter stage. An external passive filter completes the reconstruction process. The output is single ended with a drive capability down to 8 kΩ. Figure 8 is a block diagram of the DAC.

The interpolation filter produces images which are attenuated by at least 56 dB from .584Fs to 128Fs (192Fs). At a 48 kHz sample rate, a full scale signal at 20 kHz will produce an image at 28 kHz which is attenuated by more than 60 dB.

The out-of-band quantization noise from the delta sigma modulator extends from .417Fs to 128Fs (192Fs). This noise is attenuated by the switch capacitor filter and the continuous time filters. The total quantization noise and thermal noise from the analog filters integrated over the .417Fs to 128Fs (192Fs) is more than 50 dB below full scale power.

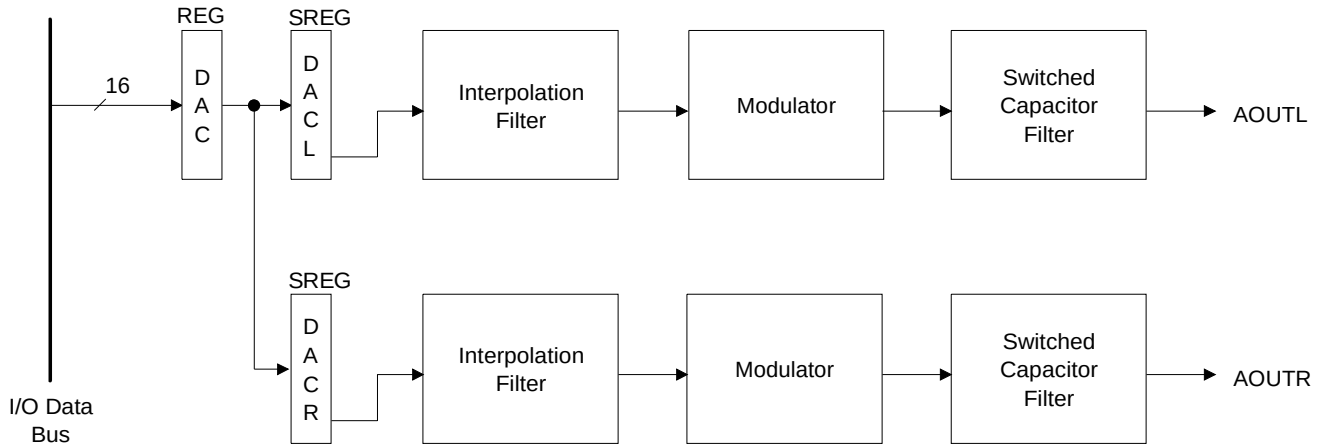


Figure 8. DAC

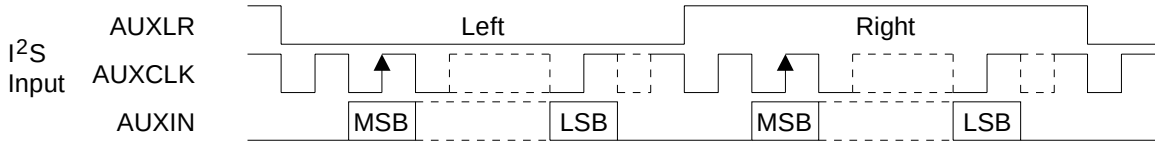


Figure 9. Auxiliary Data Input Formats

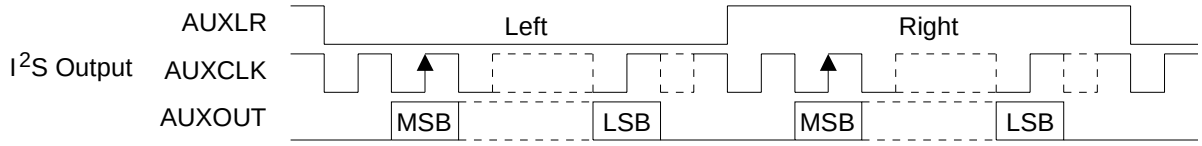


Figure 10. Auxiliary Data Output Formats

4.4 Digital Audio Transmitter

The transmitter encodes digital audio data according to the Sony®/Philips® Digital Interface Format (S/PDIF) or the AES/EBU interface format. The encoded data is output on the TX pin. More information on the S/PDIF and AES/EBU standards are available from Crystal's application note library.

4.5 Audio Serial Input Port

The audio serial input port has a three pin interface consisting of FSYNC, SCLK, and SDATA. FSYNC is only used to frame data when the audio data is in a PCM format. Systems, such as MPEG decoders, which use the audio serial input port for compressed audio data should tie FSYNC to +5V.

SCLK used to clock SDATA (serial data input) into an internal FIFO. The active edge of SCLK is determined by the application code running on the CS4922. Consult the documentation for each application download to determine your system requirements.

4.6 Auxiliary Digital Audio Port

The CS4922 auxiliary port provides a path for the internal DSP core to directly read and write framed PCM digital audio data. The auxiliary port is designed to operate in a full duplex mode that can support simultaneous PCM input and output. It is important to note that the CS4922 always masters the audio clocks on the Auxiliary Digital Audio Port.

The port has the capability to support two digital audio formats. The formats are illustrated in Figures 9, 10, and 11. The input and output formats are always configured to operate in the same mode. The input and output sampling rates are the same as the sample rate for the on-chip DAC. The AUX port can support 18 bit samples at 64Fs (I^2S Format) or 20 bit samples at 128Fs (Left Justified Format).

The CS4922 Auxiliary digital audio port physically is implemented with four device pins: AUXCLK pin 11, AUXLR pin 10, AUXIN pin 9, and AUXOUT pin 8. AUXCLK is utilized as the primary synchronous clock. AUXOUT is the serial audio data output pin and AUXIN is the serial audio data input pin. AUXLR is an output pin used for framing the auxiliary digital audio port. AUXLR cycles at the same Fs as the on-chip stereo DAC. Fs is programmed by the DSP. AUXLR and AUXOUT transition with the falling edge of AUXCLK. The rising edge of AUXCLK samples AUXIN.

4.7 Serial Control Port

The serial control port (SCP) can operate in I^2C or SPI compatible modes. In either mode, the control port performs eight bit transfers and is always configured as a slave. As a slave, it cannot drive the clock signal nor initiate data transfers. The port can request to be serviced by activating the $\overline{REQ}$ pin. The port is an asynchronous interface which provides interrupts and handshaking signals to allow

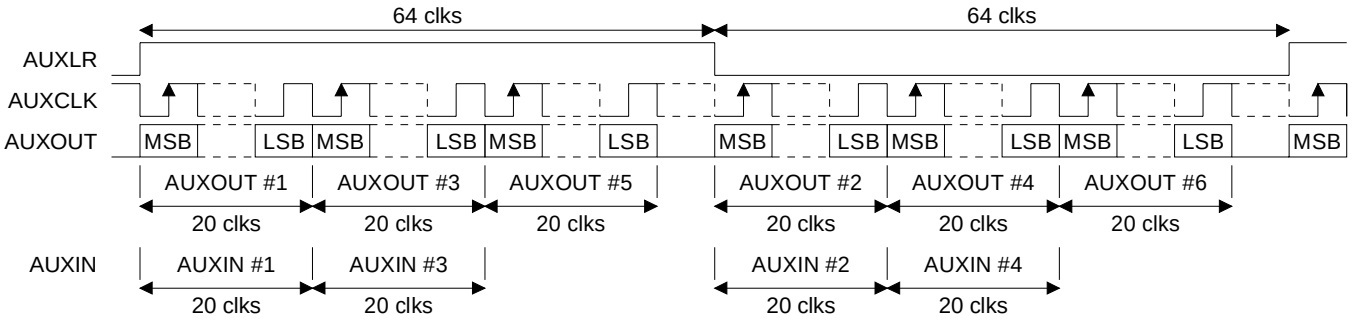


Figure 11. Multi-channel Auxiliary Data Formats

communication between the on-chip DSP and an off-chip device such as a micro controller. Figure 13 shows a block diagram of the port.

4.7.1 I²C Mode

The status of $\overline{CS}$ sets the mode of the SCP during a hardware and software reset. If $\overline{CS}$ is high during a reset the mode is I²C. Note that in most systems where I²C is the preferred control mode, $\overline{CS}$ is connected to the digital supply.

For normal I²C operation SCL/SCK, SDA, and $\overline{REQ}$ are used. $\overline{CS}$ and CDIN are typically connected to the digital supply. SCL/SCK is the serial clock input which is always driven by an external device. SDA is the serial data Input/Output signal. $\overline{REQ}$ is the active low request signal, which is driven low when there is valid data in the serial control port output SCPOUT register.

As an I²C compatible port, data is communicated on the SDA pin and is clocked by the rising edge of SCL/SCK. The Philips I²C bus specification provides details of this interface. Note the CS4922 does not meet the rise time specification of the SCL/SCK signal. For more details please refer to the section on Rise Time of SCL/SCK.

Figure 12 shows the relative timing necessary for an I²C write operation for a single byte. A 'write' is defined as the transfer of data from an I²C bus master to the CS4922 serial control port. A transfer is initiated with a start condition followed by a 7 bit address and a read/write bit (set low for a write). This address is the address assigned to the device being written to during the transfer. In the case of the CS4922, this address is stored in the SCPCN register. Immediately following power up, the CS4922's Address checking Enable (AEN) bit is set to zero. The AEN bit must be set high for the CS4922 to compare the address of the intended I²C device on the bus to its internal address. This means the CS4922 will respond to any address on the I²C bus until its address is initialized and address checking is enabled. To avoid bus conflicts the CS4922 should be held in reset ($\overline{RESET}$ active low) until the master is ready to communicate with the CS4922 and sets the address in the SCPCN. The address can only be set using the I²C bus interface, so the master should use the intended I²C address when downloading microcode to the CS4922 to avoid conflict with other devices on the bus. Once the microcode is loaded into the CS4922 the microcode should either initialize the I²C address or provide a means for the master to program the I²C address. If the CS4922 is the only device on the I²C bus, address checking is optional. However, I²C bus protocol is still required. In other words, the address bits and read/write bit are still required.

If a write to the CS4922 is specified, 8 bits of data on SDA will be shifted into the input shift register as shown in Figure 13. When the shift register is full, the 8 bit data is transferred to the Serial Control Port Input (SCPIN) register on the falling edge of the 8th data bit and an acknowledge (ACK) is sent back to the master..

If the CS4922 fails to ACK it is possible that the byte was rejected and it should be transmitted again. If the second attempt fails the CS4922 should be issued a hardware reset to reinitialize the communication path.

If the DSP core of the CS4922 wants to send a byte to the master, it first writes the byte to the Serial Control Port Output (SCPOUT) register. A write to the SCPOUT sets the request pin ($\overline{REQ}$) active low. The master must recognize the request and issue a read operation to the DSP. Figure 14 shows the relative timing of a single byte read. The master must send the 7 bit address (if address checking is enabled it must match the address in the SCPCN register) and the read bit. For I^2C protocol, it is always the device receiving the transfer that must ACK. Therefore, the CS4922 will ACK the address and the read bit. After the ACK by the CS4922 (the falling edge of SCL/SCK), the serial shift register is loaded with the byte to be sent and the most significant bit is placed on the SDA line.

The 8 bit value in the serial shift register is shifted out by the master. The data is valid on the rising edge of SCL/SCK and transitions immediately fol-

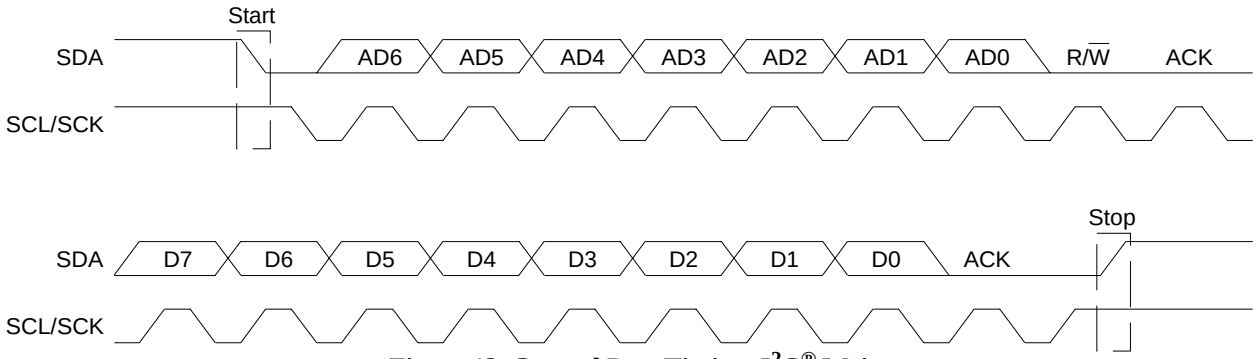


Figure 12. Control Port Timing, I^2C® Write

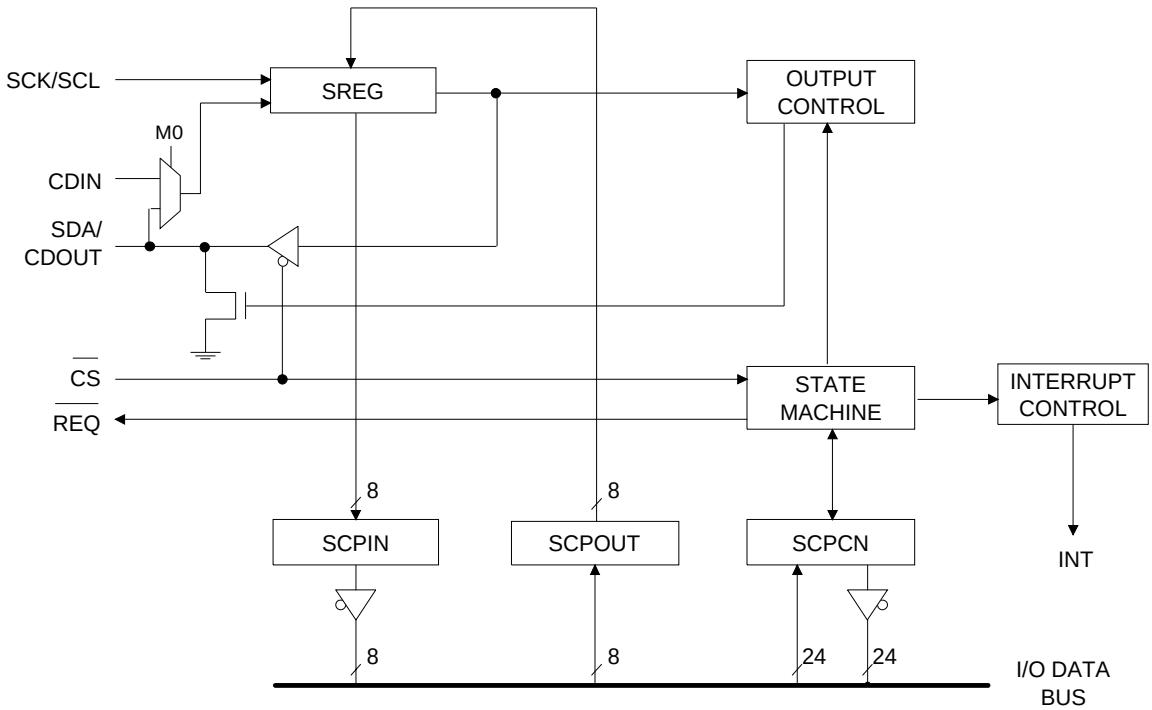


Figure 13. Serial Control Port

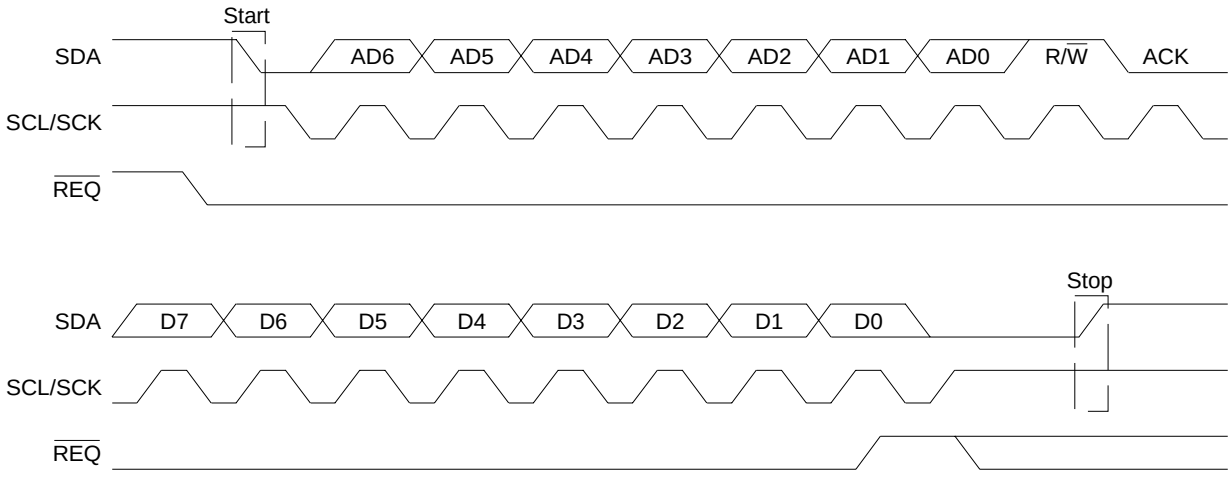


Figure 14. Control Port Timing, I²C® Read

lowing the falling edge. For I²C the REQ line will be de-asserted immediately following the rising edge of the last data bit of the current byte being transferred, if there is no data in the SCPOUT register. The REQ line is guaranteed to stay de-asserted (high) until the rising edge of the SCL/SCK for the ACK. This signals the host that the transfer is complete.

If there is data placed in SCPOUT prior to the rising edge of SCL/SCK for the last data bit, then REQ will remain asserted (low). Immediately following the falling edge of SCL/SCK for the ACK, the new data byte will be loaded into the serial shift register. The host should continue to read this new byte. It is important to note that once the data is in the shift register, clocks on the SCL/SCK line will shift the data bits out of the shift register. A STOP condition on the bus will not prevent this from occurring. The host must read the byte prior to any other bus activity or the data will be lost.

If data is placed in SCPOUT after the rising edge of SCL/SCK for the last data bit, but before the rising edge of SCL/SCK for the ACK, REQ will not be asserted until after the rising edge of SCL/SCK for the ACK. This should be treated as a completed transfer. The data written to SCPOUT will not be loaded into the shift register on the falling edge of SCL/SCK for the ACK. Therefore, a new read operation is required to read this byte.

4.7.2 Rise Time on SCL/SCK

The Philips I²C bus specification allows for rise times of the SCL/SCK line up to 1 µs. The CS4922 does not meet this specification. If the I²C bus master(s) has a rise time in excess of 50 ns the CS4922 will be unable to reliably communicate across the bus. In some systems a stronger pull-up resistor on the SCL/SCK line will provide the rise time needed for proper operation, but this is only helpful when the current rise time is near 50 ns. In cases where the CS4922 will be used in a system where a longer rise time on SCL/SCK is expected, a CMOS compatible buffer should be used. Figure 15 shows the necessary connections. Note the buffer is only used for the SCL/SCK connecting directly to the CS4922. Other devices on the I²C bus may need to hold SCL/SCK low while accepting data.

4.7.3 SPI mode

The status of CS sets the mode of the SCP during a hardware and software reset. If CS is low during a reset the mode is SPI. It is important to note that CS should be low when either a hardware of software reset is issued to ensure the mode remains SPI.

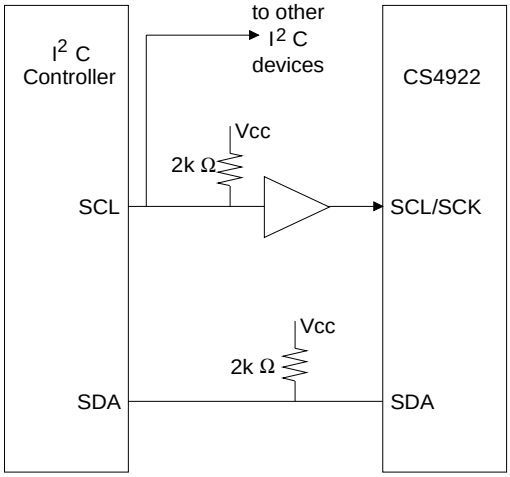


Figure 15. I²C® Connection Diagram

For normal SPI operation SCL/SCK, $\overline{CS}$, CDIN, CDOUT and $\overline{REQ}$ are used. SCL/SCK is the serial clock input which is always driven by an external device. $\overline{CS}$ is the active low enable signal. CDIN is the control data input. CDOUT is the control data output. $\overline{REQ}$ is the active low request signal, which is driven low when there is valid data in the serial control port output SCPOUT register.

As an SPI compatible port, data is communicated on the CDIN and CDOUT pins and is clocked by the rising edge of SCL/SCK. $\overline{CS}$ is used to select the device on which the CDIN and CDOUT signals will be valid.

Figure 16 shows the relative timing necessary for an SPI write operation of a single byte. A 'write' is defined as the transfer of data from an SPI bus master to the CS4922 serial control port via CDIN. A transfer is initiated with $\overline{CS}$ being driven active low. This is followed by a 7 bit address and a read/write bit (set low for a write). For SPI mode, this address is typically not used, however it is still necessary to clock an address across the bus followed by the read/write bit.

If a write to the CS4922 is specified, 8 bits of data on CDIN will be shifted into the input shift register as shown in Figure 13. When the shift register is full, the 8 bit data is transferred to the Serial Control Port Input (SCPIN) register on the falling edge of the 8th data bit.

If the DSP core of the CS4922 wants to send a byte to the master, it first writes the byte to the Serial Control Port Output (SCPOUT) register. A write to the SCPOUT sets the request pin ($\overline{REQ}$) active low. The master must recognize the request and issue a read operation to the DSP. Figure 17 shows the relative timing of a single byte read. The master must send the 7 bit address (if address checking is enabled it must match the address in the SCPCN register) and the read bit. After the falling edge of SCL/SCK for the read/write bit, the serial shift register is loaded with the byte to be sent and the most significant bit is placed on the CDOUT line.

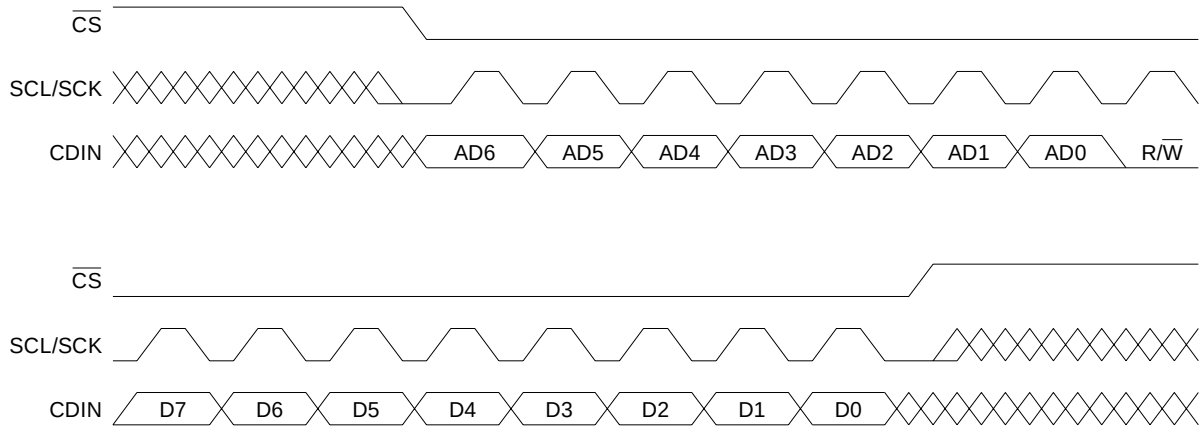


Figure 16. Control Port Timing, SPI Write

The 8 bit value in the serial shift register is shifted out by the master. The data is valid on the rising edge of SCL/SCK and transitions immediately following the falling edge. For SPI, the $\overline{REQ}$ line will be de-asserted immediately following the rising edge of the second to last data bit, of the current byte being transferred, if there is no data in the SCPOUT register. The $\overline{REQ}$ line is guaranteed to stay de-asserted (high) until the rising edge of the SCL/SCK for the last data bit. This signals the host that the transfer is complete.

If there is data placed in SCPOUT prior to the rising edge of SCL/SCK for the second to last data bit, then $\overline{REQ}$ will remain asserted (low). Immediately following the falling edge of SCL/SCK for the last data bit, the new data byte will be loaded into the serial shift register. The host should continue to read this new byte. It is important to note that once the data is in the shift register, clocks on the SCL/SCK line will shift the data bits out of the shift register. The host should read the byte prior to any other bus activity or the data will be lost. If $\overline{CS}$ is de-asserted SCK/SCL will not shift the data out. However the data is still in the shift register. Once $\overline{CS}$ becomes active (low) each SCL/SCK will shift the data out of the register.

If data is placed in SCPOUT after the rising edge of SCL/SCK for the second to last data bit, but before the rising edge of SCL/SCK for the last data bit, $\overline{REQ}$ will not be asserted until after the rising edge of SCL/SCK for the last data bit. This should be treated as a completed transfer. The data written to SCPOUT will not be loaded into the shift register on the falling edge of SCL/SCK for the last data bit. Therefore, a new read operation is required to read this byte.

4.8 External Flag Pins

The CS4922 has four external flag pins: XF1-XF4. An external pull-up (2.2 kΩ typical) is required for proper operation on each pin. The usage of the XF pins is completely defined by the application code running on the CS4922.

The MPEG application, for example, uses XF1 as a compressed data throttle indicator. When the XF1 pin is low, the host may continue to send compressed data to the CS4922. When XF1 is high, the

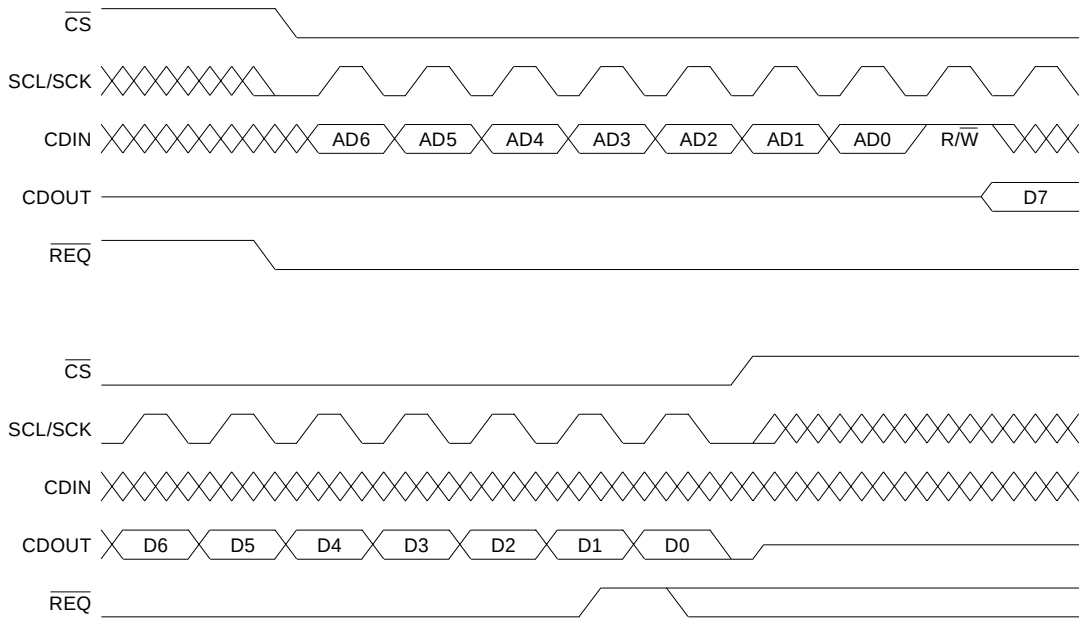


Figure 17. Control Port Timing, SPI Read

host should hold off data delivery until XF1 falls low once again.

Please see the documentation for the application code being used in your system for a complete description.

5 BOOT PROCEDURE

The CS4922 is a RAM based audio decoder. Consequently, program and data RAM must be loaded from external memory after power up or any other time a new program needs to be downloaded. During the loading procedure (boot), data is transferred through the serial control port to program and data memory. This procedure is controlled by a program stored internally in ROM.

The boot procedure is initiated by a low to high transition of the reset ($\overline{\text{RESET}}$) pin with the BOOT pin high. This initializes the program counter to location 1000_H, the first location in ROM which prepares the CS4922 for download. After the ROM program transfers data from the control port to memory, it internally issues a software reset. The software reset clears all registers and transfers control to the application now resident in RAM.

A hardware reset ($\overline{\text{RESET}}$ pin toggled low) with the BOOT pin low has the same effect as a software reset.

The CS4922 will boot from a micro controller using the serial control port. When booting, it can communicate in an I^2C or SPI format. If the $\overline{\text{CS}}$ (chip select) pin is high when boot is initiated, the port will communicate in I^2C format. If the $\overline{\text{CS}}$ pin is low when boot is initiated, the port will communicate in SPI. Please refer to the timing requirements found at the beginning of this document.

Nodes in an I^2C network have unique network addresses. A message in an I^2C network consists of the address of the node receiving the message followed by the message data. When the control port is configured for I^2C format, it normally compares the address to an address stored in an internal register. During the boot procedure, the control port is programmed to ignore the address. The SCP section on I^2C operation explains the mechanics of writing to the CS4922.

The boot program in internal ROM expects data transferred through the control port to adhere to a proprietary download image format. The download image always concludes with two bytes containing FF and three bytes containing a check sum. The check sum is generated by summing all the previous data, address, and length bytes and truncating to 24 bits.

During download, the CS4922 generates a checksum on the download image as it is received. This check sum is compared to the value found at the tail of the download image. If they do not match, the $\overline{\text{REQ}}$ (request) pin is pulled low and the processor does not issue the software reset. It stays in a loop until boot is initiated again.

If the download image format is corrupted to the point that the CS4922 does not know which bytes represent the check sum, then $\overline{\text{REQ}}$ will not drop to indicate download failure. This should never happen in a stable system.

During initial system testing we recommend downloading an image that has only the check sum corrupted (the final 3 bytes). If $\overline{\text{REQ}}$ drops after the complete application code image has been transferred, then the download procedure is functioning properly. If $\overline{\text{REQ}}$ does not drop, then there is a problem with the download procedure.

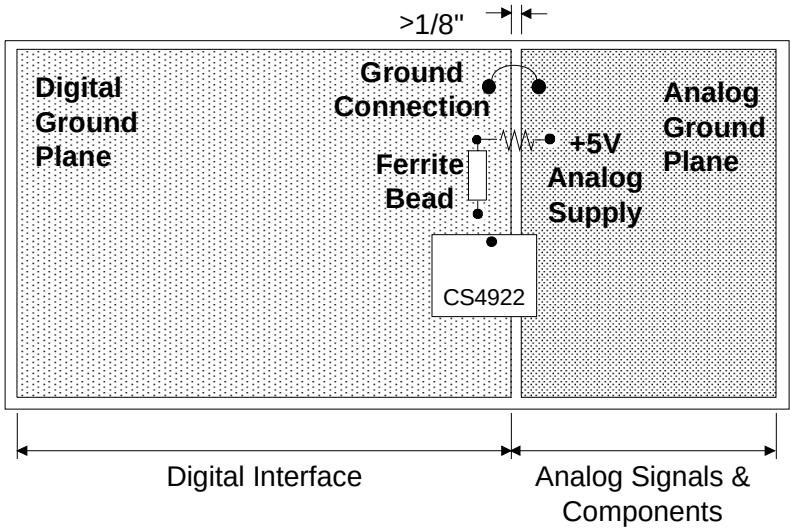
6 POWER SUPPLY AND GROUNDING

When using separate supplies, the digital power should be connected to the CS4922 via a ferrite bead, positioned closer than 1" to the device (see Figure 18). The CS4922 VA+ pin should be derived from the cleanest power source available. If only one supply is available, use the suggested arrangement in Figure 1.

The CS4922 should be positioned such that the analog pins (pins 29 - 39) are over the analog ground plane, while the rest of the pins lay over the digital ground plane as illustrated in Figures 18 and 19. The analog and digital grounds on the CS4922 are not connected internally; this should be accomplished externally through a point-to-point connection across the ground split as shown in Figure 18. A separate power plane for the chip is preferable.

Figure 19 illustrates the optimum ground and decoupling layout for the CS4922 assuming a surface-mount socket and surface mount capacitors. Surface-mount sockets are useful since the pad locations are exactly the same as the actual chip; therefore, given that space for the socket is left on the board, the socket can be optional for production. Figure 19 depicts mostly the top layer containing signal traces and assumes the bottom or interlayer contains a solid ground plane (analog or digital), except where the digital supply needs to run to the power pins. The important points with regards to this diagram are that the ground plane is SOLID under the CS4922 and connects all ground pins with thick traces providing the absolute lowest impedance between ground pins. The decoupling capacitors are placed as close as possible to the device which, in this case, is the socket boundary. The lowest value capacitor is placed closest to the chip. Vias are placed near the AGND and DGND pins, under the IC, and should be attached to the solid ground plane (analog or digital) on another layer. The negative side of the decoupling capacitors should also attach to the same solid ground plane. Traces bringing the power to the CS4922 should be wide thereby keeping the impedance low.

If using through-hole sockets, effort should be made to find a socket with the minimum height which will minimize the socket impedance. When using a through-hole socket, the vias under the chip in Figure 19 are not needed since the pins serve the same function.



Note that the CS4922 is oriented with its digital pins towards the digital end of the board.

Figure 18. CS4922 Suggested Layout

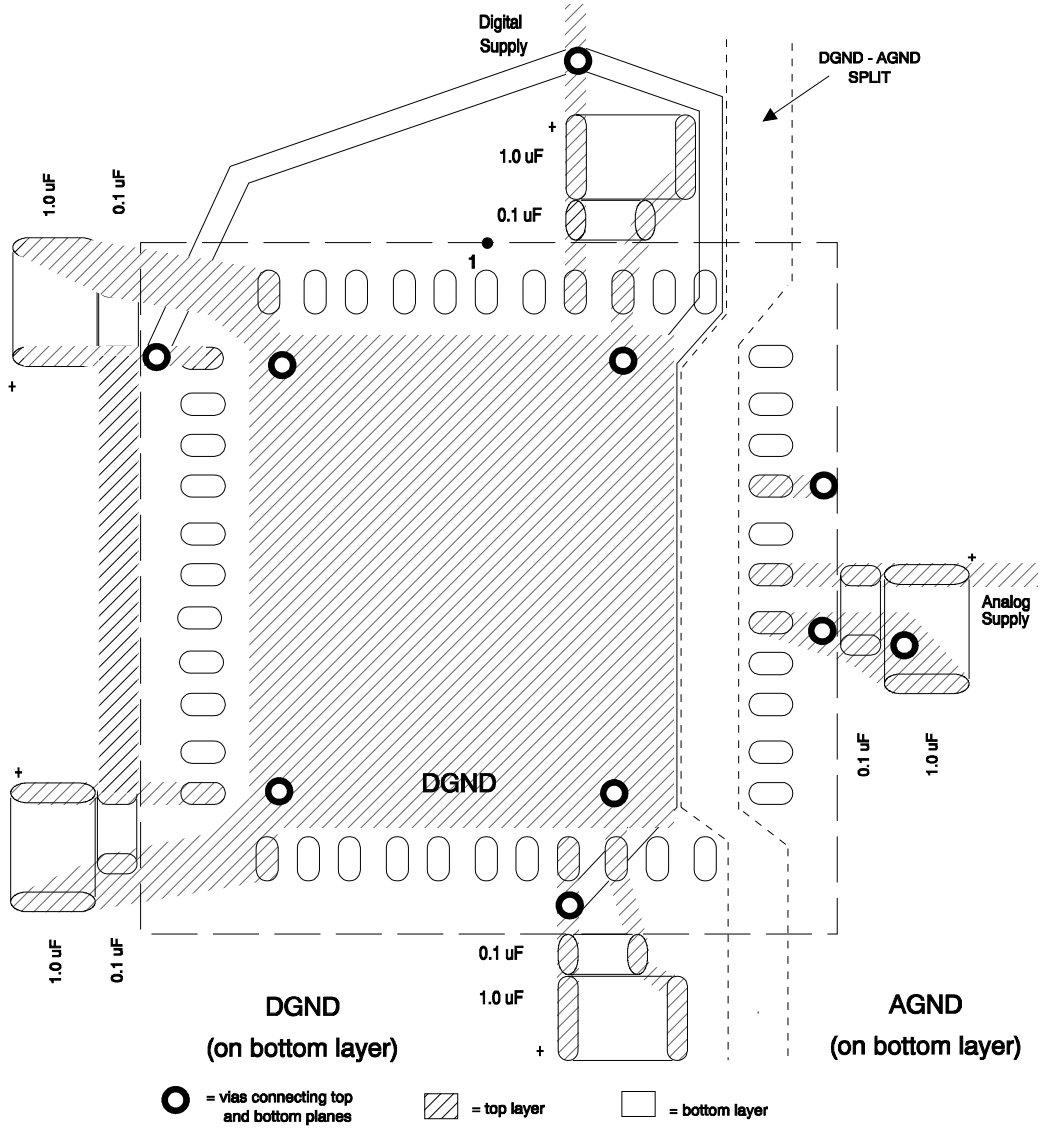


Figure 19. CS4922 Surface Mount Decoupling Layout

7 DAC FILTER RESPONSE PLOTS

Figures 20 through 23 show the overall frequency response, passband ripple and transition band for the CS4922 DACs. Figure 23 shows the DACs' deviation from linear phase. Fs is the selected sample frequency. Since the sample frequency is programmable, the filters will adjust to the selected sample frequency. Fs is also the FSYNC frequency.

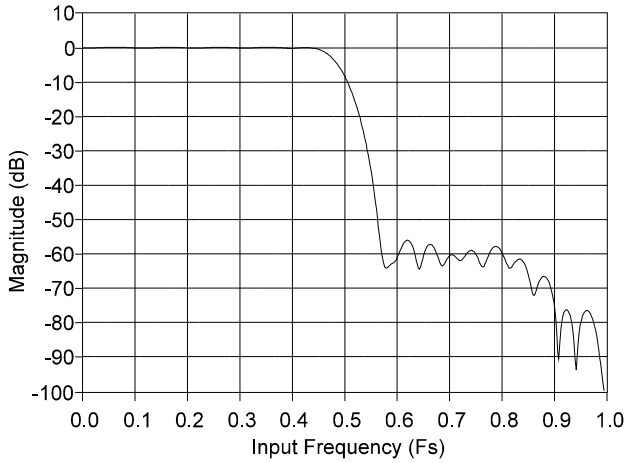


Figure 20. DAC Frequency Response

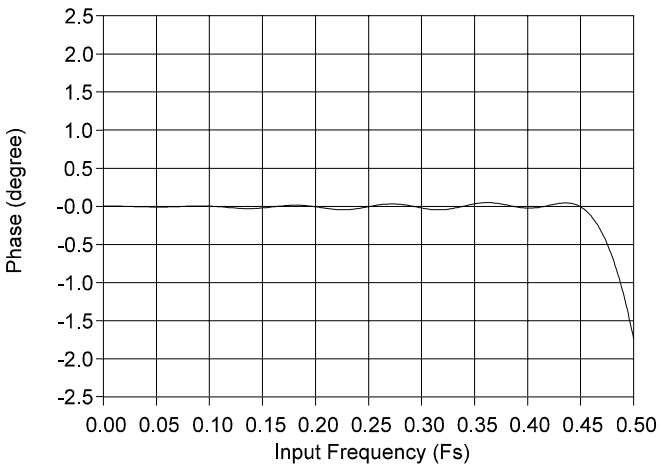


Figure 21. DAC Phase Response

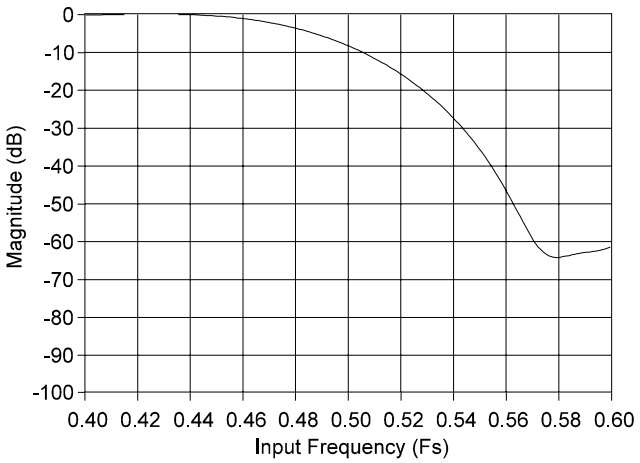


Figure 22. DAC Transition Band

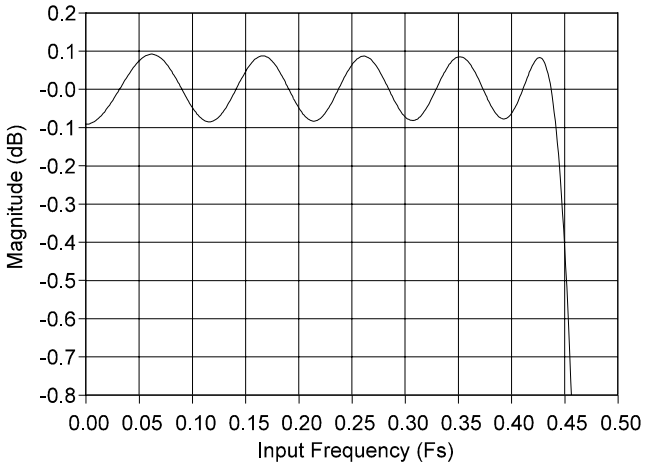
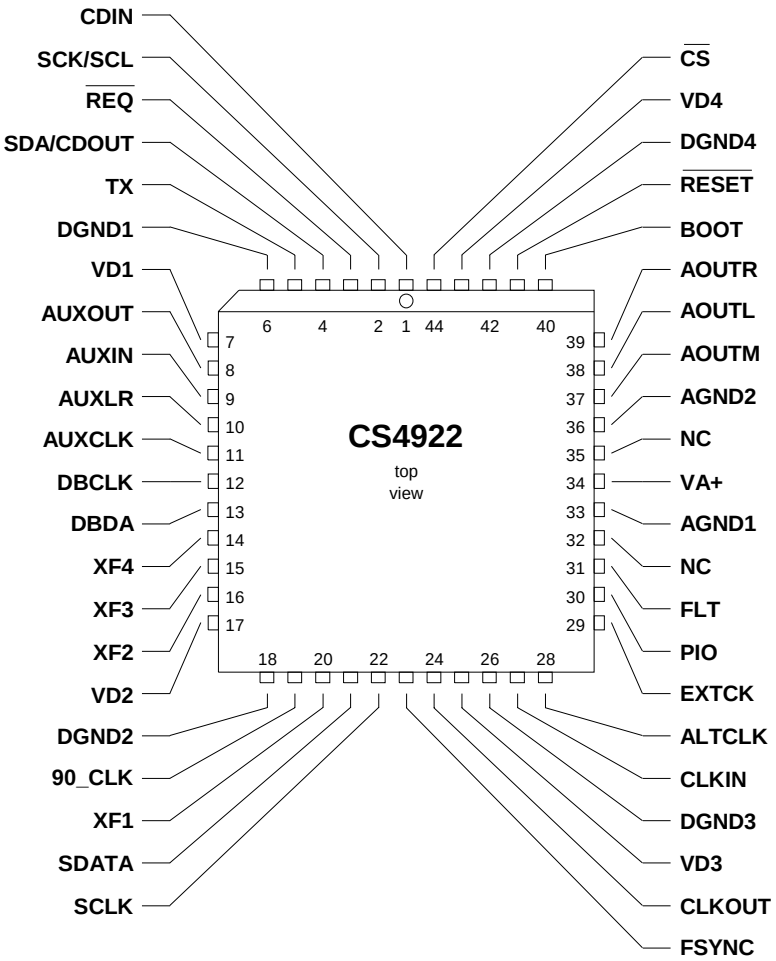


Figure 23. DAC Passband Ripple

8 PIN DESCRIPTIONS



Power Supplies

VD1, VD2, VD3, VD4 - Positive Digital Power Supply, PINS 7, 17, 25, 43.

The +5V supply is connected to these pins to power the various digital subcircuits on the chip. See decoupling section in this data sheet for decoupling recommendations.

DGND1, DGND2, DGND3, DGND4 - Digital Ground, PINS 6, 18, 26, 42.

Digital power supply ground.

VA+ - Positive Analog Power Supply, PIN 34.

The analog +5V supply for the analog-to-digital converter and the PLL. Analog performance is highly dependent on the quality of this supply. See decoupling section in this data sheet for decoupling recommendations.

AGND1, AGND2 - Analog Ground, PIN 33, 36.

Analog power supply ground.

Digital-to-Analog Converter

AOUTL, AOUTR - Analog Outputs, Left and Right Channels, PINS 38, 39.

These DAC outputs are centered at approximately 2.2V. An external filter is required to diminish out-of-band noise. See Typical Connection Diagram, Figure 1.

AOUTM - Mono Analog Output, PIN 37.

Mono is the summation of AOUTL and AOUTR. Mono output is 180° out-of-phase with the sum of AOUTL and AOUTR. Mono is centered at approximately 2.2V. An external filter is required to diminish out-of-band noise. See Typical Connection Diagram, Figure 1.

Serial Audio Port

FSYNC - Frame Synchronization Clock Input, PIN 23.

When SCLK and SDATA are used for delivering compressed data to the CS4922 (e.g. the MPEG application code), the FSYNC pin should be tied to the +5V supply. When SCLK and SDATA are used for delivering PCM data (e.g. the G.729A application code), FSYNC transitions delineate left and right audio data, or the start of a data frame.

SCLK - Serial Clock Input, PIN 22.

SCLK is used to clock the serial audio data on SDATA into the device. The active edge of SCLK is determined by the application code running on the CS4922.

SDATA - Serial Audio Data Input, PIN 21.

SDATA is an audio data input pin for the CS4922. The data is clocked in on the active edge of SCLK.

Digital Audio Transmitter

TX - Transmitter Output, PIN 5.

Biphase mark encoded data is output at logic levels from the TX pin. This output typically connects to the input of an RS-422 or optical transmitter. With additional external circuitry, the port can support either AES/EBU or S/PDIF formats.

Clock Manager

CLKOUT - Clock Output, PIN 24.

CLKOUT can be used to synchronize peripheral devices such as a micro controller or an audio source. The clock frequency is determined by a divide by Q in the clock manager. The maximum CLKOUT frequency is the maximum DSP frequency divided by 2.

ALTCLK - Clock Input, PIN 28.

When EXTCK is high, ALTCLK is an input for an externally generated clock. This clock directly becomes the DSP clock and the clock frequency should be 512Fs or 768Fs.

EXTCK - External Clock Select, PIN 29.

Setting EXTCK high allows ALTCLK to be used as an input for an external VCO. Setting EXTCK low disables ALTCLK. Note that EXTCK should be tied directly to either digital power or ground for proper operation.

FLT - PLL Filter, PIN 31.

A capacitor (typically 0.47 µF) connected to this pin filters the control voltage for the on-chip VCO. Trace length should be minimized to the pin.

CLKIN - Clock Input, PIN 27.

The 27 MHz clock input to the CLKIN is used to synchronize the PLL's. It is typical for SCLK for the audio data and CLKIN to be derived from the same clock source to avoid asynchronous noise between the audio source and the DSP.

90_CLK - Optional SCR/PCR 33-Bit Counter Clock, PIN 19

The 90_CLK pin is an input clock signal (typically 90 kHz) which is used to clock the internal 33-bit counter. The 33-bit counter's clock source is set to 90_CLK when DIV = 0 in the CM0 register. Otherwise when DIV = 1, the 33-bit counter will be clocked by CLKIN ÷ 300.

Control

DBCLK, DBDA - Debug Port, PINS 12, 13.

It is required that a pull-up be used (typically 2.2 kΩ) on pin 13.

$\overline{\text{RESET}}$ - PIN 41.

The CS4922 enters a reset state while $\overline{\text{RESET}}$ is low. When in reset condition, all internal registers are set to 0, the digital audio transmitter, serial control port, and ALTCLK pin are disabled, and the stereo DAC is muted. Normal operation is resumed one internal clock cycle after the rising edge of $\overline{\text{RESET}}$.

BOOT - PIN 40.

Boot enable pin. Pin must be set high to initiate the download of a program. While BOOT is high, $\overline{\text{RESET}}$ must be toggled high. This starts the internal boot program.

XF1, XF2, XF3, XF4 - External Flags, PINS 20, 16, 15, 14.

The XF pins are software controllable outputs via the LINT register. These pins are open drain so an external pullup is required (typically 2.2 kΩ) for proper operation of the pins.

PIO - PIN 30.

This pin should be grounded through a 10 kΩ resistor in normal operation.

Serial Control Port

$\overline{\text{REQ}}$ - Request Output, PIN 3.

This pin is driven low when the DSP needs servicing from an external device. A write to the SCPOUT will cause the $\overline{\text{REQ}}$ to go low. A pull-up resistor is required for proper operation (2.2kΩ is typical).

$\overline{\text{CS}}$ - Chip Select Input, PIN 44.

In SPI format, all communication between the host and the CS4922 is initiated when the host drives the $\overline{\text{CS}}$ pin low. This pin also serves as the communication format select during a reset or power up. When $\overline{\text{CS}}$ is high during a reset or power up the SCP will be configured in $I^2C^®$ mode. When low, it is configured in SPI mode. The mode is selectable in software by setting the M0 bit in the SCPCN.

SCK/SCL - Serial Clock Input, PIN 2.

SCK/SCL clocks data into or out of the serial control port. This is always driven by an external device because the CS4922 always operates in slave mode.

SDA/CDOUT - Serial Data I/O / Control Data Output, PIN 4.

In SPI mode, CDOUT is a data output for the serial control data. In I^2C interface mode, SDA is a bi-directional data I/O. It is required that a pull-up be used (2.2 kΩ is typical in I^2C mode).

CDIN - Control Data Input, PIN 1.

In SPI mode, CDIN is the data input for the serial control port. It has no function in I^2C mode. The pin should be connected to either digital power or ground when the CS4922 is used in I^2C systems.

Auxiliary Digital Audio Port

AUXLR - Auxiliary Sample Clock, PIN 10.

This output signal determines which channel is currently being input on the AUXIN pin or output on the AUXOUT pin. It is also the sample clock, Fs.

AUXIN - Auxiliary Data Input, PIN 9.

Two's complement MSB first serial data is input on this pin. The data is clocked by AUXCLK and the channnel is determined by AUXLR.

AUXOUT - Auxiliary Data Output, PIN 8.

Two's complement MSB first serial data is output on this pin. The data is clocked by AUXCLK and the channel is determined by AUXLR.

AUXCLK - Auxiliary Serial Clock Output, PIN 11.

This is the auxiliary audio port serial clock output. This output is used to clock data in on the AUXIN pin and shift data out on the AUXOUT pin. Its frequency is selectable in software.

9 PARAMETER DEFINITIONS

Resolution

The number of bits in the input words to the DACs.

Differential Nonlinearity

The worst case deviation from the ideal codewidth; expressed in LSBs.

Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the rms sum of all the in-band harmonics of the test signal.

Instantaneous Dynamic Range

The Signal-to-(Noise + Distortion) ratio (S/(N+D)) with a 1 kHz, -60 dB from full scale DAC input signal, with 60 dB added to compensate for the small signal. Use of a small signal reduces the harmonic distortion components of the noise to insignificant levels. Units are in dB.

Interchannel Isolation

The amount of 1kHz signal present on the output of the grounded input channel with 1 kHz, 0dB signal present on the other channel. Units are in dB.

Interchannel Gain Mismatch

The difference in output voltages for each channel with a full scale digital input. Units are in dB.

Frequency Response

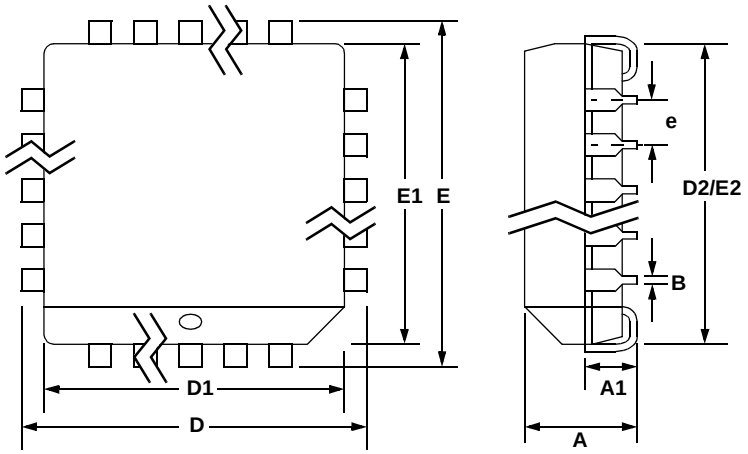
Worst case variation in output signal level versus frequency over 10 Hz to 20 kHz. Units in dB.

Out of Band Energy

The ratio of the rms sum of the energy from 0.46×Fs to 2.1×Fs compared to the rms full-scale signal value. Tested with 48 kHz Fs giving a out-of-band energy range of 22 kHz to 100 kHz.

10 PACKAGE DIMENSIONS

44L PLCC PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.165	0.180	4.043	4.572
A1	0.090	0.120	2.205	3.048
B	0.013	0.021	0.319	0.533
D	0.685	0.695	16.783	17.653
D1	0.650	0.656	15.925	16.662
D2	0.590	0.630	14.455	16.002
E	0.685	0.695	16.783	17.653
E1	0.650	0.656	15.925	16.662
E2	0.590	0.630	14.455	16.002
e	0.040	0.060	0.980	1.524

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• Notes •


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