CS4227

# Six Channel, 20-Bit Codec

## Features

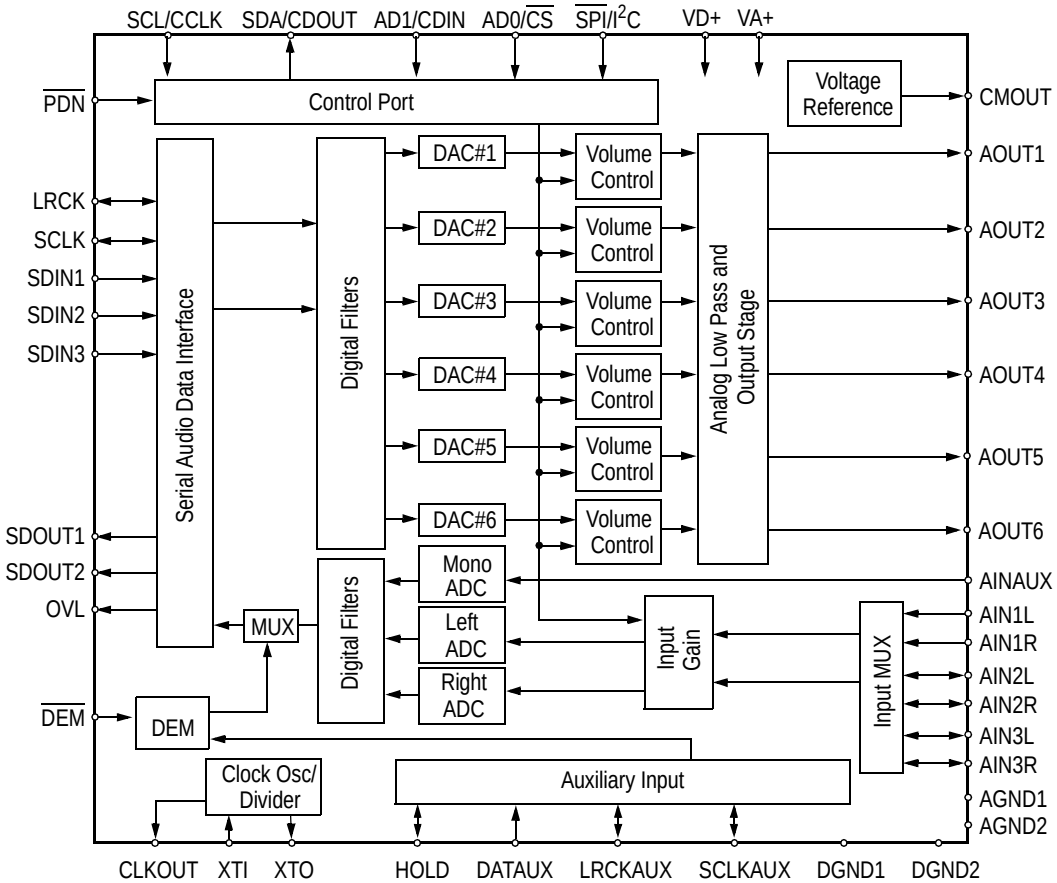
- Stereo 20-bit A/D Converters
- Six 20-bit D/A Converters
- 108 dB DAC Signal-to-Noise Ratio (EIAJ)
- Mono 20-bit A/D Converter
- Programmable Input Gain & Output Attenuation
- On-chip Anti-aliasing and Output Smoothing Filters
- De-emphasis for 32 kHz, 44.1 kHz, 48 kHz

## Description

The CS4227 is a single-chip codec providing stereo analog-to-digital and six digital-to-analog converters using delta-sigma conversion techniques. This +5 V device also contains volume controls that are independently selectable for each of the six D/A channels. Applications include Dolby® Pro-logic™, THX®, and Dolby Digital AC-3™ home theater systems, DSP based car audio systems, and other multi-channel applications.

**ORDERING INFORMATION**

| | | |
|---|---|---|
| CS4227-KQ | -10° to +70° C | 44-pin TQFP |
| CS4227-BQ | -40° to +85° C | 44-pin TQFP |
| CDB4227 | | Evaluation Board |




*Preliminary Product Information* | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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# 1. CHARACTERISTICS AND SPECIFICATIONS

## ANALOG CHARACTERISTICS ($T_A$ = 25 °C; VA+, VD+ = +5 V; Full Scale Input Sine wave, 997 kHz; Fs = 44.1 kHz; Measurement Bandwidth is 20 Hz to 20 kHz; Local components as shown in Figure 5; SPI mode, Format 3, unless otherwise specified.)

| Parameter | Symbol | CS4227-KQ | | | CS4227-BQ | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| ***Analog Input Characteristics*** - Minimum gain setting (0 dB) Differential Input; unless otherwise specified. | | | | | | | | |
| ADC Resolution Stereo Audio channels | | 16 | - | 20 | 16 | - | 20 | Bits |
| Mono channel | | 16 | - | 20 | 16 | - | 20 | Bits |
| Total Harmonic Distortion | THD | | 0.003 | - | | 0.003 | - | % |
| Dynamic Range (A weighted, Stereo) | | 92 | 95 | - | 90 | 93 | - | dB |
| (unweighted, Stereo) | | - | 92 | - | - | 90 | - | dB |
| (A weighted, Mono) | | 89 | - | - | 87 | - | - | dB |
| Total Harmonic -1 dB, Stereo (Note 1) | THD+N | - | -88 | -82 | - | -86 | -80 | dB |
| Distortion + Noise -1 dB, Mono (Note 1) | | - | - | -72 | - | - | -70 | dB |
| Interchannel Isolation | | - | 90 | - | - | 90 | - | dB |
| Interchannel Gain Mismatch | | - | 0.1 | - | - | 0.1 | - | dB |
| Programmable Input Gain Span | | 8 | 9 | 10 | 8 | 9 | 10 | dB |
| Gain Step Size | | 2.7 | 3 | 3.3 | 2.7 | 3 | 3.3 | dB |
| Offset Error (with high pass filter) | | - | - | 0 | - | - | 0 | LSB |
| Full Scale Input Voltage (Single Ended): | | 0.90 | 1.0 | 1.10 | 0.90 | 1.0 | 1.10 | Vrms |
| Gain Drift | | - | 100 | - | - | 100 | - | ppm/°C |
| Input Resistance (Note 2) | | 10 | - | - | 10 | - | - | kΩ |
| Input Capacitance | | - | - | 15 | - | - | 15 | pF |
| CMOUT Output Voltage | | - | 2.3 | - | - | 2.3 | - | V |
| ***A/D Decimation Filter Characteristics*** | | | | | | | | |
| Passband (Note 3) | | 0.02 | - | 20.0 | 0.02 | - | 20.0 | kHz |
| Passband Ripple | | - | - | 0.01 | - | - | 0.01 | dB |
| Stopband (Note 3) | | 27.56 | - | 5617.2 | 27.56 | - | 5617.2 | kHz |
| Stopband Attenuation (Note 4) | | 80 | - | - | 80 | - | - | dB |
| Group Delay (Fs = Output Sample Rate) (Note 5) | $t_{gd}$ | - | 15/Fs | - | - | 15/Fs | - | s |
| Group Delay Variation vs. Frequency | $\Delta t_{gd}$ | - | - | 0 | - | - | 0 | µs |

Notes:
1. Referenced to typical full-scale differential input voltage (2Vrms).
2. Input resistance is for the input selected. Non-selected inputs have a very high (>1MΩ) input resistance. The input resistance will vary with gain value selected, but will always be greater than the min. value specified.
3. Filter characteristics scale with output sample rate.
4. The analog modulator samples the input at 5.6448 MHz for an output sample rate of 44.1 kHz. There is no rejection of input signals which are multiples of the sampling frequency (n x 5.6448 MHz ±20.0 kHz where n = 0,1,2,3...).
5. Group delay for Fs = 44.1 kHz, $t_{gd}$ = 15/44.1 kHz = 340 µs

## ANALOG CHARACTERISTICS (Continued)

| Parameter | Symbol | CS4227-KQ | | | CS4227-BQ | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| ***High Pass Filter Characteristics*** | | | | | | | | |
| Frequency Response: -3 dB (Note 3) | | - | 3.4 | - | - | 3.4 | - | Hz |
| -0.13 dB | | - | 20 | - | - | 20 | - | Hz |
| Phase Deviation @ 20 Hz (Note 3) | | - | 10 | - | - | 10 | - | Deg. |
| Passband Ripple | | - | - | 0 | - | - | 0 | dB |
| ***Analog Output Characteristics*** - Minimum Attenuation, 10 k, 100 pF load; unless otherwise specified. | | | | | | | | |
| DAC Resolution | | 16 | - | 20 | 16 | - | 20 | Bits |
| Signal-to-Noise/Idle (DAC muted, A weighted) Channel Noise | | 101 | 108 | - | 99 | 106 | - | dB |
| Dynamic Range (DAC not muted, A weighted) | | 93 | 98 | - | 91 | 96 | - | dB |
| (DAC not muted, unweighted) | | - | 95 | - | - | 93 | - | dB |
| Total Harmonic Distortion | THD | - | 0.003 | - | - | 0.003 | - | % |
| Total Harmonic Distortion + Noise (Stereo) | THD+N | - | -88 | -83 | - | -86 | -81 | dB |
| Interchannel Isolation | | - | 90 | - | - | 90 | - | dB |
| Interchannel Gain Mismatch | | - | 0.1 | - | - | 0.1 | - | dB |
| Attenuation Step Size (All Outputs) | | 0.7 | 1 | 1.3 | 0.7 | 1 | 1.3 | dB |
| Programmable Output Attenuation Span | | -84 | -86 | - | -84 | -86 | - | dB |
| Offset Voltage (relative to CMOUT) | | - | ±15 | - | - | ±15 | - | mV |
| Full Scale Output Voltage | | 0.92 | 1.0 | 1.08 | 0.92 | 1.0 | 1.08 | Vrms |
| Gain Drift | | - | 100 | - | - | 100 | - | ppm/°C |
| Out-of-Band Energy (Fs/2 to 2Fs) | | - | -60 | - | - | -60 | - | dBFs |
| Analog Output Load Resistance: | | 10 | - | - | 10 | - | - | kΩ |
| Capacitance: | | - | - | 100 | - | - | 100 | pF |
| ***Combined Digital and Analog Filter Characteristics*** | | | | | | | | |
| Frequency Response 10 Hz to 20 kHz | | - | ±0.1 | - | - | ±0.1 | - | dB |
| Deviation from Linear Phase | | - | ±0.5 | - | - | ±0.5 | - | Deg. |
| Passband: to 0.01 dB corner (Notes 6, 7) | | 0 | - | 20.0 | 0 | - | 20.0 | kHz |
| Passband Ripple (Note 7) | | - | - | ±0.01 | - | - | ±0.01 | dB |
| Stopband (Notes 6 ,7) | | 24.1 | - | - | 24.1 | - | - | kHz |
| Stopband Attenuation (Note 8) | | 70 | - | - | 70 | - | - | dB |
| Group Delay (Fs = Input Word Rate) (Note 5) | tgd | - | 16/Fs | - | - | 16/Fs | - | s |
| ***Analog Loopback Performance*** | | | | | | | | |
| Signal-to-noise Ratio (CCIR-2K weighted, -20 dB input) | CCIR-2K | - | 71 | - | - | 71 | - | dB |
| ***Power Supply*** | | | | | | | | |
| Power Supply Current Operating | | - | 90 | 113 | - | 90 | 115 | mA |
| Power Down | | - | 1 | 3 | - | 1 | 3 | mA |
| Power Supply Rejection (1 kHz, 10 $mV_{rms}$) | | - | 45 | - | - | 45 | - | dB |

Notes: 6. The passband and stopband edges scale with frequency. For input word rates, Fs, other than 44.1 kHz, the 0.05 dB passband edge is 0.4535xFs and the stopband edge is 0.5465xFs.

7. Digital filter characteristics.

8. Measurement bandwidth is 10 Hz to 3Fs.

Specifications are subject to change without notice

## SWITCHING CHARACTERISTICS ($T_A$ = 25 °C; VA+, VD+ = +5 V ±5%; outputs loaded with 30 pF.)

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Audio ADC's and DAC's Sample Rate | | Fs | 4 | - | 50 | kHz |
| XTI Frequency | XTI = 256, 384, or 512 Fs | | 1.024 | - | 26 | MHz |
| XTI Pulse Width High | XTI = 512 Fs | | 10 | - | - | ns |
| | XTI = 384 Fs | | 21 | - | - | |
| | XTI = 256 Fs | | 31 | - | - | |
| XTI Pulse Width Low | XTI = 512 Fs | | 10 | - | - | ns |
| | XTI = 384 Fs | | 21 | - | - | |
| | XTI = 256 Fs | | 31 | - | - | |
| XTI Jitter Tolerance | | | - | 500 | - | ps |
| CLKOUT Jitter | (Note 9) | | - | 200 | - | psRMS |
| CLKOUT Duty Cycle (high timer/cycle time) | (Note 10) | | 40 | 50 | 60 | % |
| $\overline{\text{PDN}}$ Low Time | (Note 11) | | 500 | - | - | ns |
| SCLK Falling Edge to SDOUT Output Valid | DSCK = 0 | $t_{dpd}$ | - | - | Note 12 | ns |
| LRCK edge to MSB valid | | $t_{lrpd}$ | - | - | 40 | ns |
| SDIN Setup Time Before SCLK Rising Edge | DSCK = 0 | $t_{ds}$ | - | - | 25 | ns |
| SDIN Hold Time After SCLK Rising Edge | DSCK = 0 | $t_{dh}$ | - | - | 25 | ns |
| ***Master Mode*** | | | | | | |
| SCLK Falling to LRCK Edge | DSCK = 0 | $t_{mslr}$ | - | ±10 | - | ns |
| SCLK Period | (Note 14) | - | - | - | - | - |
| SCLK Duty Cycle | | | - | 50 | - | % |
| ***Slave Mode*** | | | | | | |
| SCLK Period | | $t_{sckw}$ | Note 13 | - | - | ns |
| SCLK High Time | | $t_{sckh}$ | 40 | - | - | ns |
| SCLK Low Time | | $t_{sckl}$ | 40 | - | - | ns |
| SCLK Rising to LRCK Edge | DSCK = 0 | $t_{lrckd}$ | 20 | - | - | ns |
| LRCK Edge to SCLK Rising | DSCK = 0 | $t_{lrcks}$ | 40 | - | - | ns |

Notes: 9. CLKOUT Jitter is for 256x Fs selected as output frequency measured from falling edge to falling edge. Jitter is greater for 384x Fs and 512x Fs as selected output frequency.

10. For CLKOUT frequency equal to 1x Fs, 384x Fs, and 512x Fs. See Master Clock Output section.

11. After powering up the CS4227, $\overline{\text{PDN}}$ should be held low for 1 ms to allow the power supply to settle.

12. $\frac{1}{(384)\text{Fs}} + 20$

13. $\frac{1}{(128)\text{Fs}}$

14. $\frac{1}{(256)\text{Fs}}$

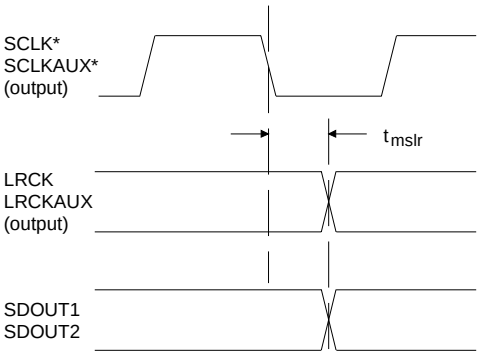
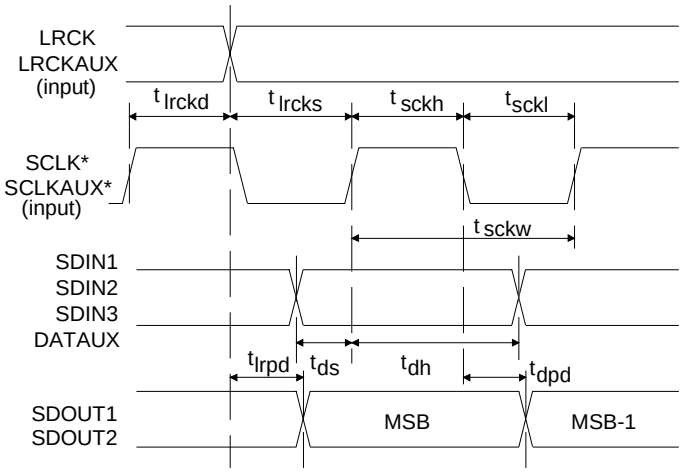



**Figure 1. Audio Ports Master Mode Timing**




*SCLK, SCLKAUX shown for DSCK = 0 and ASCK = 0.
SCLK & SCLKAUX inverted for DSCK = 1 and ASCK = 1, respectively.

**Figure 2. Audio Ports Slave Mode and Data I/O Timing**

## SWITCHING CHARACTERISTICS - CONTROL PORT ($T_A$ = 25 °C; VA+, VD+ = +5 V ±5%; Inputs: logic 0 = DGND, logic 1 = VD+; $C_L$ = 30 pF)

| Parameter | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| ***SPI Mode ($\overline{SPI}$/I2C = 0)*** | | | | | |
| CCLK Clock Frequency | | $f_{sck}$ | - | 6 | MHz |
| $\overline{CS}$ High Time Between Transmissions | | $t_{csh}$ | 1.0 | - | µs |
| $\overline{CS}$ Falling to CCLK Edge | | $t_{css}$ | 20 | - | ns |
| CCLK Low Time | | $t_{scl}$ | 66 | - | ns |
| CCLK High Time | | $t_{sch}$ | 66 | - | ns |
| CDIN to CCL Rising Setup Time | | $t_{dsu}$ | 40 | - | ns |
| CCLK Rising to DATA Hold Time | (Note 15) | $t_{dh}$ | 15 | - | ns |
| CCLK Falling to CDOUT stable | | $t_{pd}$ | - | 45 | ns |
| Rise Time of CDOUT | | $t_{r1}$ | - | 25 | ns |
| Fall Time of CDOUT | | $t_{f1}$ | - | 25 | ns |
| Rise Time of CCLK and CDIN | (Note 16) | $t_{r2}$ | - | 100 | ns |
| Fall Time of CCLK and CDIN | (Note 16) | $t_{f2}$ | - | 100 | ns |

Notes: 15. Data must be held for sufficient time to bridge the transition time of CCLK.

16. For $F_{SCK}$ < 1 MHz.

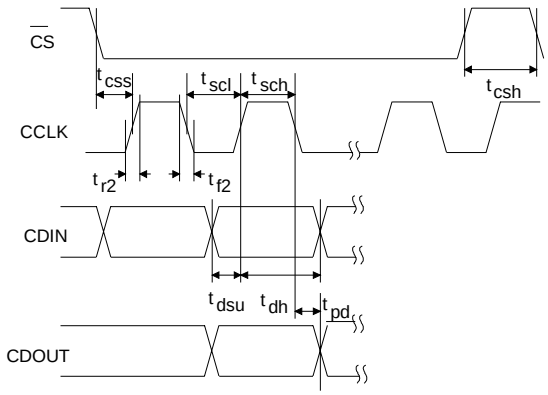



**Figure 3. Control Port SPI Mode**

## SWITCHING CHARACTERISTICS - CONTROL PORT ($T_A$ = 25 °C; VA+, VD+ = +5 V ±5%; Inputs: logic 0 = DGND, logic 1 = VD+; $C_L$ = 30 pF)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| ***$I^2C$® Mode ($\overline{SPI}$/I2C = 1)*** ***(Note 17)*** | | | | |
| SCL Clock Frequency | $f_{scl}$ | - | 100 | kHz |
| Bus Free Time Between Transmissions | $t_{buf}$ | 4.7 | - | µs |
| Start Condition Hold Time (prior to first clock pulse) | $t_{hdst}$ | 4.0 | - | µs |
| Clock Low Time | $t_{low}$ | 4.7 | - | µs |
| Clock High Time | $t_{high}$ | 4.0 | - | µs |
| Setup Time for Repeated Start Condition | $t_{sust}$ | 4.7 | - | µs |
| SDA Hold Time for SCL Falling (Note 18) | $t_{hdd}$ | 0 | - | µs |
| SDA Setup Time to SCL Rising | $t_{sud}$ | 250 | - | ns |
| Rise Time of Both SDA and SCL Lines | $t_r$ | - | 1 | µs |
| Fall Time of Both SDA and SCL Lines | $t_f$ | - | 300 | ns |
| Setup Time for Stop Condition | $t_{susp}$ | 4.7 | - | µs |

Notes: 17. $I^2C$® is a registered trademark of Philips Semiconductors.

18. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

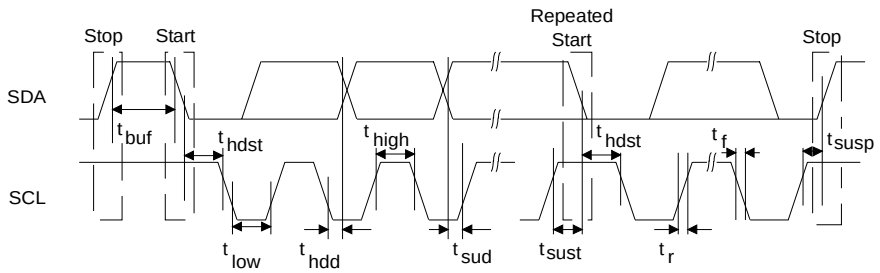



**Figure 4. Control Port $I^2C$ Mode**

## ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0 V, all voltage with respect to 0 V.)

| Parameter | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Power Supplies | Digital<br>Analog | VD+<br>VA+ | -0.3<br>-0.3 | 6.0<br>6.0 | V |
| Input Current | (Note 19) | | - | ±10 | mA |
| Analog Input Voltage | (Note 20) | | -0.7 | (VA+) + 0.7 | V |
| Digital Input Voltage | (Note 20) | | -0.7 | (VD+) + 0.7 | V |
| Ambient Temperature | (Power Applied) | | -55 | +125 | °C |
| Storage Temperature | | | -65 | +150 | °C |

Notes: 19. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

20. The maximum over or under voltage is limited by the input current.

WARNING: WARNING:Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

## RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0 V, all voltage with respect to 0 V.)

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power Supplies<br>\|VA+ - VD+\| < 0.4 V | Digital<br>Analog | VD+<br>VA+ | 4.75<br>4.75 | 5.0<br>5.0 | 5.25<br>5.25 | V |
| Operating Ambient Temperature | | $T_A$ | -10 | 25 | 70 | °C |

## DIGITAL CHARACTERISTICS ($T_A$ = 25 °C; VA+, VD+ = +5 V ±5%)

| Parameter | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| High-level Input Voltage | (Except XTI) | $V_{IH}$ | 2.8 | (VD+) + 0.3 | V |
| Low-level Input Voltage | (Except XTI) | $V_{IL}$ | -0.3 | 0.8 | V |
| High-level Output Voltage | (Except XTO) | $V_{OH}$ | (VD+) - 1.0 | - | V |
| Low-level Output Voltage | (Except XTO) | $V_{OL}$ | - | 0.4 | V |
| Input Leakage Current | (Digital Inputs) | | - | 10 | µA |
| Output Leakage Current | (High-Impedance Digital Outputs) | | - | 10 | µA |

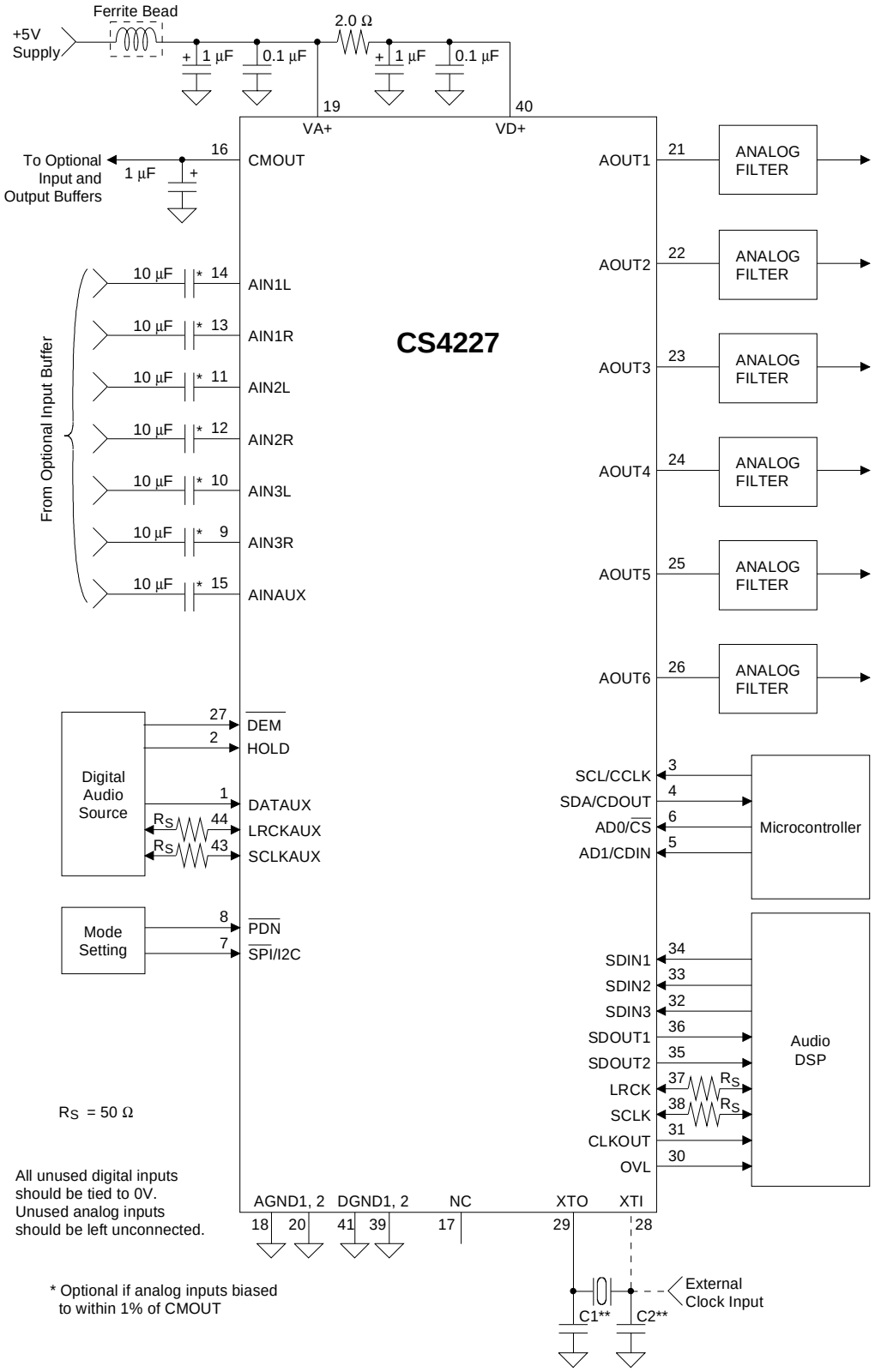



**Figure 5. Recommended Connection Diagram**
**(Also see recommended layout diagrams, Figure 14)**

# 2. FUNCTIONAL DESCRIPTION

## 2.1 Overview

The CS4227 has 2 channels of 20-bit analog-to-digital conversion and 6 channels of 20-bit digital-to-analog conversion. A mono 20-bit ADC is also provided. All ADCs and DACs are delta-sigma converters. The stereo ADC inputs have adjustable input gain, while the DAC outputs have adjustable output attenuation.

Digital audio data received by the DACs and transmitted from the ADCs is communicated over separate serial ports, allowing concurrent writing to and reading from the device. The CS4227 functions are controlled via a serial microcontroller interface. Figure 1 shows the recommended connection diagram for the CS4227.

## 2.2 Analog Inputs

### *2.2.1 Line Level Inputs*

AIN1R, AIN1L, AIN2R, AIN2L, AIN3R, AIN3L and AINAUX are the line level input pins (See Figure 5). These pins are internally biased to the CMOUT voltage (nominally 2.3 V). A 10 µF DC blocking capacitor allows signals centered around 0 V to be input. Figure 6 shows an optional dual op amp buffer which combines level shifting with a gain of 0.5 to attenuate the standard line level of 2 $V_{rms}$ to 1 $V_{rms}$. The CMOUT reference level is used to bias the op-amps to approximately one half the supply voltage. With this input circuit, the 10 µF DC blocking caps in Figure 5 may be omitted. Any remaining DC offset will be removed by the internal high-pass filters.

Selection of the stereo input pair for the 20-bit ADC's is accomplished by setting the AIS1/0 bits, which are accessible in the ADC Control Byte. On-chip anti-aliasing filters follow the input mux, providing anti-aliasing for all input channels.

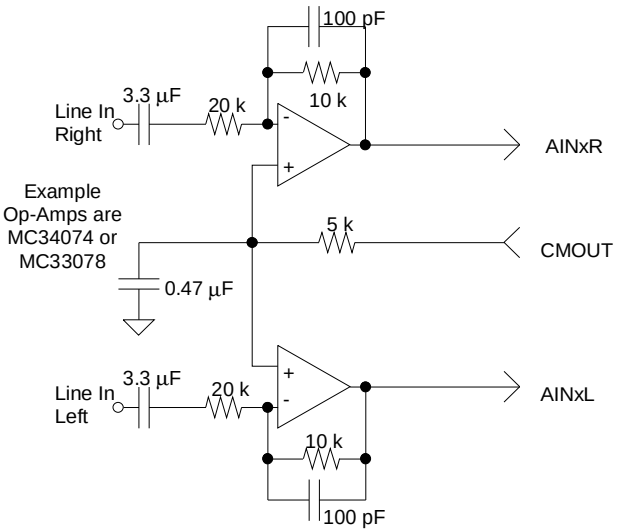



**Figure 6. Optional Line Intput Buffer**

The analog inputs may also be configured as differential inputs. This is enabled by setting bits AIS1/0 = 3. In the differential configuration, the left channel inputs reside on pins 10 and 11, and the right channel inputs reside on pins 12 and 13 as described in the table below. In differential mode, the full scale input level is 2 $V_{rms}$.

| Single-ended | Pin # | Differential Inputs |
|---|---|---|
| AIN3L | Pin 10 | AINL+ |
| AIN3R | Pin 9 | unused |
| AIN2L | Pin 11 | AINL- |
| AIN2R | Pin 12 | AINR- |
| AIN1L | Pin 14 | unused |
| AIN1R | Pin 13 | AINR+ |

**Table 1. Single-ended vs Differential Input Pin Assignments**

The analog signal is input to the mono ADC via the AINAUX pin.

Independent Muting of both the stereo ADC's and the mono ADC is possible through the ADC Control Byte (#11) with the MUTR, MUTL and MUTM bits.

### *2.2.2 Adjustable Input Gain*

The signals from the line inputs are routed to a programmable gain circuit which provides up to 9 dB of gain in 3 dB steps, adjustable through the Input Control Byte. Right and left channel gain settings are controlled independently with the GNR1/0 and GNL1/0 bits. To minimize audible artifacts, level changes should be done with the channel muted, as the changes occur immediately on register updates.

The ADC Status Report Byte provides feedback of input level for each ADC channel. This register continously monitors the ADC output and records the peak output level since the last register read. Reading this register causes it to reset to 0, whereupon peak monitoring begins again.

### *2.2.3 High Pass Filter*

The operational amplifiers in the input circuitry driving the CS4227 may generate a small DC offset into the A/D converter. The CS4227 includes a high pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multichannel system.

The characteristics of this first-order high pass filter are outlined below for an output sample rate of 44.1 kHz. This filter response scales linearly with sample rate.

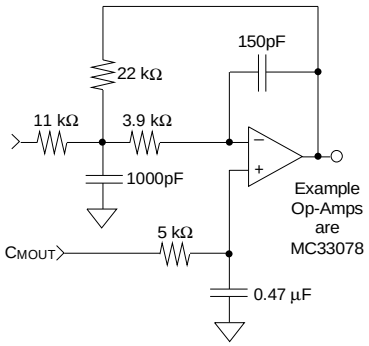
| | |
|---|---|
| Frequency Response | -3dB @ 3.4 Hz<br>-0.13 dB @ 20 Hz |
| Phase Deviation | 10 degrees @ 20 Hz |
| Passband Ripple | None |

**Table 2. High Pass Filter Characteristics**

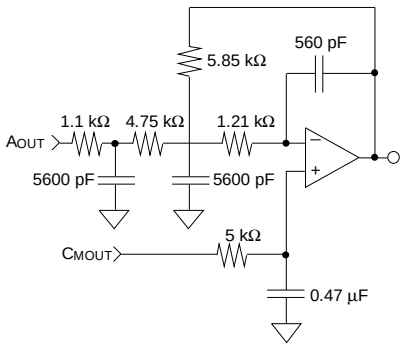
## 2.3 Analog Outputs

### *2.3.1 Line Level Outputs*

The CS4227 contains an on-chip buffer amplifier producing single-ended outputs capable of driving 10 kΩ loads. Each output (AOUT 1-6) will produce a nominal 2.83 $V_{pp}$ (1 $V_{rms}$) output with a 2.3 volt quiescent voltage for a full scale digital input. The recommended off-chip analog filter is a 2nd order Butterworth with a -3 dB corner at Fs (see Figure 7). This filter provides out-of-band noise attenuation along with a gain of 2, providing a 2 $V_{rms}$ output signal. A 3rd order Butterworth filter with a -3 dB corner at 0.75 Fs can be used if greater out of band noise filtering is desired. The CS4227 DAC interpolation filter is a linear phase design which has been pre-compensated for an external 2nd order Butterworth filter to provide a flat frequency response and linear phase response over the passband. If this filter is not used, small frequency response magnitude and phase errors will occur.




**2-Pole Butterworth Filter**




**3-Pole Butterworth Filter**

**Figure 7. Butterworth Filters**

### *2.3.2 Output Level Attenuator*

The DAC outputs are each routed through an attenuator which is adjustable in 1 dB steps. Output attenuation is available through the Output Attenuator Data Bytes. Level changes are implemented such that the noise is attenuated by the same amount as the signal (equivalent to using an analog attenuator after the signal source) until the residual output noise is equal to the noise floor in the mute state. Level changes only take effect on zero crossings to minimize audible artifacts. If there is no zero crossing, then the requested level change will occur after a time-out period between 512 and 1024 frames (11.6 ms to 23.2 ms at 44.1 kHz frame rate). There is a separate zero crossing detector for each channel. Each ACC bit in the DAC Status Report Byte provides information on when a volume control change has taken effect. This bit goes high when a new setting is loaded and returns low when it has taken effect. Volume control changes can be instantaneous by setting the Zero Crossing Disable (ZCD) bit in the DAC Control Byte (#3) to 1.

Each output can be independently muted via mute control bits, MUT6-1, in the DAC Control Byte (#3). The mute also takes effect on a zero-crossing or after a timeout. In addition, the CS4227 has an optional mute on consecutive zeros feature, where all DAC outputs will mute if they receive between 512 and 1024 consecutive zeros (or -1 code) on all six channels. A single non-zero value will unmute the DAC outputs. This feature can be disabled with the MUTC bit in the DAC Control Byte (#3).

## 2.4 Clock Generation

The master clock to operate the CS4227 may be generated by using the on-chip inverter and an external crystal or by using an external clock source. If the active clock source stops for 10 µs, the CS4227 will enter a power down state. In all modes it is required to have SCLK and LRCK synchronous to the selected master clock.

### *2.4.1 Clock Source*

The CS4227 requires a high frequency master clock to run the internal logic. The clock enable bit (CE) must be set to 0 after power-up of the device (see Power-up/Reset/Power Down Mode section). A high frequency crystal can be connected to XTI and XTO, or a high frequency clock can be applied to XTI. This high frequency clock can be 256 Fs, 384 Fs or 512 Fs; this is set by the CI0/1 bits in the Clock Mode Byte (#1). When using the on-chip crystal oscillator, external loading capacitors are required (see Figure 5). High frequency crystals (>8 MHz) should be parallel resonant, fundamental mode and designed for 20 pF loading (equivalent to 40 pF to ground on each leg).

### *2.4.2 Master Clock Output*

CLKOUT is a master clock output provided to allow synchronization of external components. Available CLKOUT frequencies of 1 Fs, 256 Fs, 384 Fs, and 512 Fs, are selectable by the CO0/1 bits of the Clock Mode Byte.

Generation of CLKOUT for 384 Fs and 512 Fs is accomplished with an on chip clock multiplier and may contain clock jitter. The source of the 256 Fs CLKOUT is a divided down clock from the XTI/XTO input. If 384 Fs is chosen as the input clock at XTI and 256 Fs is chosen as the output, CLKOUT will have approximately a 33% duty cycle. In all other cases CLKOUT will typically have a 50% duty cycle.

### *2.4.3 Synchronization*

The DSP port and Auxiliary port must operate synchronously to the CS4227 clock source. The serial port will force a reset of the data paths in an attempt to resynchronize if non-synchronous data is input to the CS4227. It is advisable to mute the DACs when changing from one clock source to another to avoid the output of undesirable audio signals as the CS4227 resynchronizes.

## 2.5 Digital Interfaces

There are 2 digital audio interface ports: the audio DSP port and the auxiliary digital audio port. The serial data is represented in 2's complement format with the MSB-first in all formats.

### *2.5.1 Audio DSP Serial Interface Signals*

The serial interface clock, SCLK, is used for transmitting and receiving audio data. The active edge of SCLK is chosen by setting the DSCK bit in the DSP Port Mode Byte (#14). SCLK can be generated by the CS4227 (master mode) or it can be input from an external SCLK source (slave mode). Mode selection is set with the DMS1/0 bits in the DSP Port Mode Byte (#14). The number of SCLK cycles in one system sample period is programmable to be 32, 48, 64, or 128 by setting the DCK1/0 bits in the DSP Port Mode Byte (#14). When SCLK is an input, 64 SCLK's per system sample period is not recommended, due to potential interference effects; if possible 128 SCLK's per sample period should be used instead. For master mode, bursting of a 128 Fs clock is preferrable over evenly distributed clocks.

The Left/Right clock (LRCK) is used to indicate left and right data and the start of a new sample period. It may be output from the CS4227, or it may be generated from an external controller. The frequency of LRCK must be equal to the system sample rate, Fs.

SDIN1, SDIN2, and SDIN3 are the data input pins, each of which drives a pair of DACs. SDOUT1 and SDOUT2 can carry the output data from the two 20-bit ADC's, the mono ADC and the auxiliary digital audio port. Selection depends on the IS1/0 bits in the ADC control byte (#11). The audio DSP port may also be configured so that all 6 DAC's data is input on SDIN1, and all 3 ADC's data is output on SDOUT1. Table 3 outlines the serial interface ports.

| DAC Inputs | | |
|---|---|---|
| SDIN1 | left channel | DAC #1 |
| | right channel | DAC #2 |
| | single line | All 6 DAC channels |
| SDIN2 | left channel | DAC #3 |
| | right channel | DAC #4 |
| SDIN3 | left channel | DAC #5 |
| | right channel | DAC #6 |

**Table 3. DSP Serial Input Ports**

### *2.5.2 Audio DSP Serial Interface Formats*

The audio DSP port supports 7 alternate formats, shown in Figures 8, 9, and 10. These formats are chosen through the DSP Port Mode Byte (#14) with the DDF2/1/0 bits.

Formats 5 and 6 are single line data modes where all DAC channels are combined onto a single input and all ADC channels are combined onto a single output. Format 6 is available in master mode only. See Figure 10.

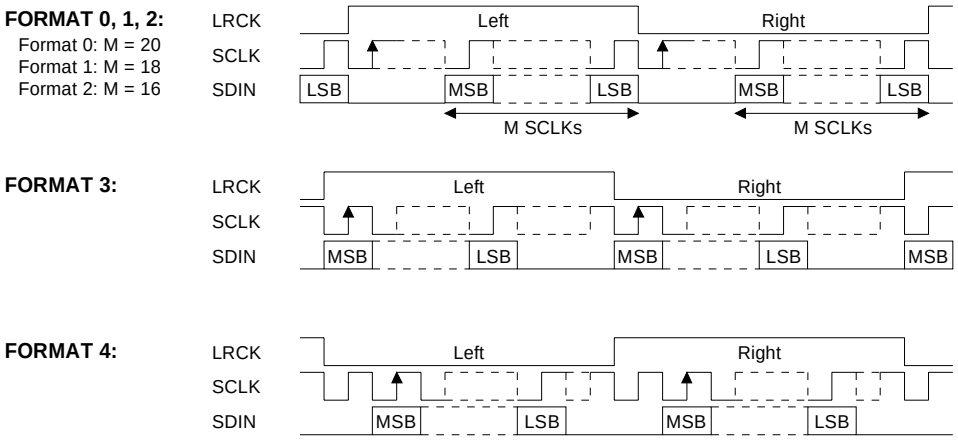
### *2.5.3 Auxiliary Audio Port Signals*

The auxiliary port provides an alternate way to input digital audio signals into the CS4227. This port consists of clock, data and left/right clock pins named, SCLKAUX, DATAUX and LRCKAUX. The Auxiliary Audio Port input is output on SDOUT1 when IS is set to 1 or 2 in the ADC Control Byte. Additionally, setting IS to 2 routes the stereo ADC outputs to SDOUT2. There is approximately a two frame delay from DATAUX to SDOUT1. When the auxiliary port is used, the frequency of LRCKAUX must be equal to the system sample rate, Fs, but no particular phase relationship is required.

De-emphasis can be performed on input data to the auxiliary audio port; this is controlled by the Auxiliary Port Control Byte (#16).

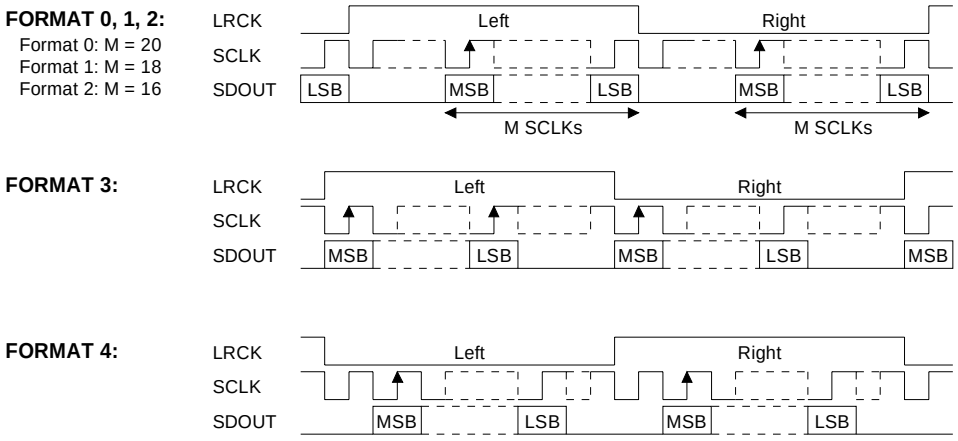
### *2.5.4 Auxiliary Audio Port Formats*

Input data on DATAUX is clocked into the part by SCLKAUX using the format selected in the Auxiliary Port Mode Byte. The auxiliary audio port sup-




Note: SCLK shown for DSCK = 0. SCLK inverted for DSCK = 1.

**Figure 8. Audio DSP and Auxiliary Port Data Input Formats**




Note: SCLK shown for DSCK = 0. SCLK inverted for DSCK = 1.

**Figure 9. Audio DSP Port Data Output Formats**

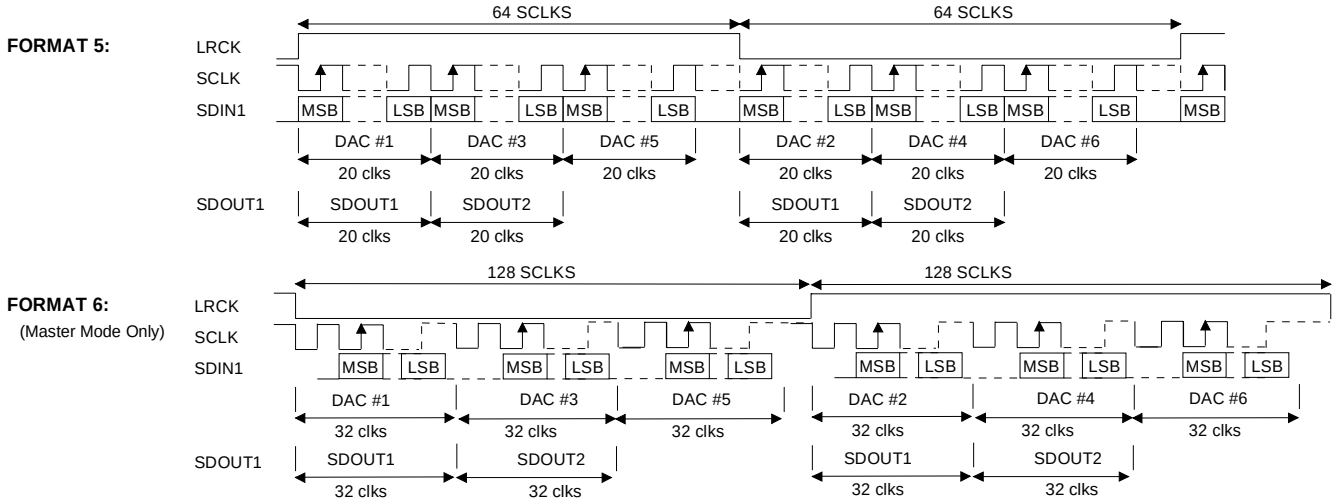



**Figure 10. One Data Line Modes**

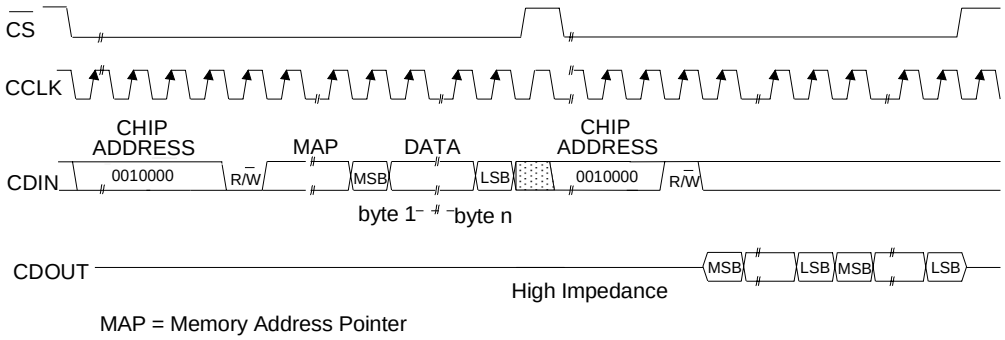



**Figure 11. Control Port Timing, SPI Mode**

ports the same 5 formats as the audio DSP port in multi-data line mode. LRCKAUX is used to indicate left and right data samples, and the start of a new sample period. SCLKAUX and LRCKAUX may be output from the CS4227, or they may be generated from an external source, as set by the AMS1/0 control bits in the Auxiliary Port Mode Byte (#15).

## 2.6 Control Port Signals

The control port is used to load all the internal settings. The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has 2 modes: SPI and $I^2C^®$, with the CS4227 as a slave device. The SPI mode is selected by setting the $\overline{SPI}$/I2C pin low, and $I^2C^®$ is selected by setting the $\overline{SPI}$/I2C pin high. The state of this pin is continuously monitored.

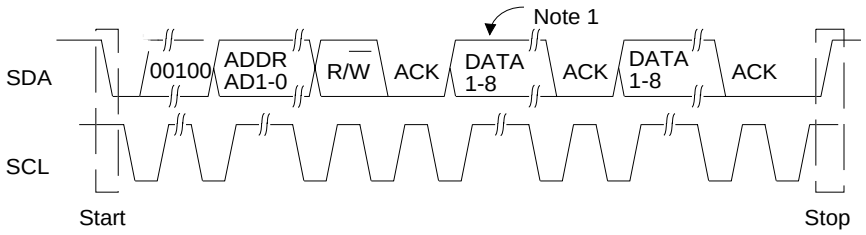
### *2.6.1 SPI Mode*

In SPI mode, $\overline{CS}$ is the CS4227 chip select signal, CCLK is the control port bit clock, (input into the CS4227 from the microcontroller), CDIN is the input data line from the microcontroller, CDOUT is the output data line to the microcontroller, and the chip address is 0010000. Data is clocked in on the rising edge of CCLK and out on the falling edge.

Figure 11 shows the operation of the control port in SPI mode. To write to a register, bring $\overline{CS}$ low. The first 7 bits on CDIN form the chip address, and they must be 0010000. The eighth bit is a read/write indicator (R/$\overline{W}$), which should be low to write. The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into register designated by the MAP. During writes, the CDOUT output stays in the high impedance state. It may be externally pulled high or low with a 47 kΩ resistor.

The CS4227 has a MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, then the MAP will stay constant for successive reads or writes. If INCR is set to a 1, then MAP will auto increment after each byte is read or written, allowing block reads or writes of successive registers.

To read a register, the MAP has to be set to the correct address by executing a partial write cycle which finishes ($\overline{CS}$ high) immediately after the MAP byte. The auto MAP increment bit (INCR) may be set or not, as desired. To begin a read, bring $\overline{CS}$ low, send out the chip address and set the read/write bit (R/$\overline{W}$) high. The next falling edge of CCLK will clock out the MSB of the addressed register (CDOUT will leave the high impedance state). If the MAP auto increment bit is set to 1, the data for successive registers will appear consecutively.




Note 1: If operation is a write, this byte contains the Memory Address Pointer, MAP.

**Figure 12. Control Port Timing, I²C® Mode**

### *2.6.2 I²C® Mode*

In I²C® mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in Figure 12. There is no $\overline{CS}$ pin. Pins AD0, AD1 form the partial chip address. The upper 5 bits of the 7 bit address field must be 00100. To communicate with a CS4227, the LSBs of the chip address field, which is the first byte sent to the CS4227, should match the settings of the AD1, AD0 pins. The eighth bit of the address bit is the R/$\overline{W}$ bit (high for a read, low for a write). If the operation is a write, the next byte is the Memory Address Pointer which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the Memory Address Pointer will be output. Setting the auto increment bit in MAP, allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. Use of the I²C bus® compatible interface requires a license from Philips. I²C bus® is a registered trademark of Philips Semiconductors.

### *2.6.3 Control Port Bit Definitions*

All registers can be written and read back, except the DAC Status Report Byte (#10) and ADC Status Report Byte (#13), which are read only. See the following bit definition tables for bit assignment information.

## 2.7 Power-up/Reset/Power Down Mode

Upon power up, the user should hold $\overline{PDN}$ = 0 for approximately 1ms. In this state, the control port is reset to its default settings. At the end of the $\overline{PDN}$, the device remains in a low power mode in which CMOUT will not supply current, but the control port is active. The desired settings should be loaded while keeping the RS bit set to 1. Normal operation is achieved by setting the CE bit to zero in the Clock Mode Byte (#1) and the RS bit to zero in the Converter Control Byte (#2). Once done, the part powers up and an offset calibration occurs. This process lasts approximately 50 ms.

Reset/power down is achieved by lowering the $\overline{PDN}$ pin causing the part to enter power down. Once $\overline{PDN}$ goes high, the control port is functional and the desired settings should be loaded in while keeping the RS bit set to 1. The remainder of the chip remains in a low power reset state until the RS bit in the Convertor Control Byte is set to 0. After clearing the RS bit, the CE bit (Clock Enable) in the Clock Mode Byte (#1) should also be set to zero.

The CS4227 will also enter a stand by mode if the master clock source stops for approximately 10 µs or if the LRCK is not synchronous to the master clock. The control port will retain its current settings.

## 2.8 DAC Calibration

Output offset voltage is minimized by an internal calibration cycle. A calibration will automatically occur anytime the part comes out of reset, including the power-up reset, or when the master clock source to the part changes by changing the CE or CI bits in the Clock Mode Byte.

The CS4227 can be re-calibrated whenever desired. A control bit, CAL, in the Converter Control Byte, is provided to initiate a calibration. The sequence is:

1) Set CAL to 1, the CS4227 sets CALP to 1 and begins to calibrate.
2) CALP will go to 0 when the calibration is completed.

Additional calibrations can be implemented by setting CAL to 0 and then to 1.

## 2.9 De-Emphasis

The CS4227 is capable of digital de-emphasis for 32, 44.1, or 48 kHz sample rates. Implementation of digital de-emphasis requires reconfiguration of the digital filter to maintain the filter response shown in Figure 13 at multiple sample rates. The Auxiliary Port Control Byte selects the de-emphasis control method. De-emphasis may be enabled under hardware control, using the DEM pin (DEM2/1/0=4,5,6), or by software control using the DEM bit (DEM2/1/0=0,1,2,3)

## 2.10 Hold Function

If the digital audio source presents invalid data to the CS4227, the CS4227 may be configured to cause the last valid digital input level to be held constant (this sounds much better than a potentially random output level). Holding the previous output sample occurs when the user asserts the HOLD pin (HOLD = 1) at any time during the stereo sample period. During a HOLD condition, AUXPort input data is ignored. DAC outputs can be automatically muted after an extended HOLD period (>15 samples) by setting the MOH bit = 0 in the Auxiliary Port Control Byte. DACs will not be automatically muted when MOH = 1. When the HOLD pin is deasserted (HOLD = 0), the DAC outputs will return to one of two different states controlled by the UMV (Unmute on Valid Data) bit in the Auxiliary Port Control Byte. When UMV = 0, the DAC outputs will unmute when the HOLD is removed. When UMV = 1, the DACs must be unmuted in the DAC Control Byte after the HOLD is removed. This allows the user to unmute the DAC after the invalid data has passed through the DSP.

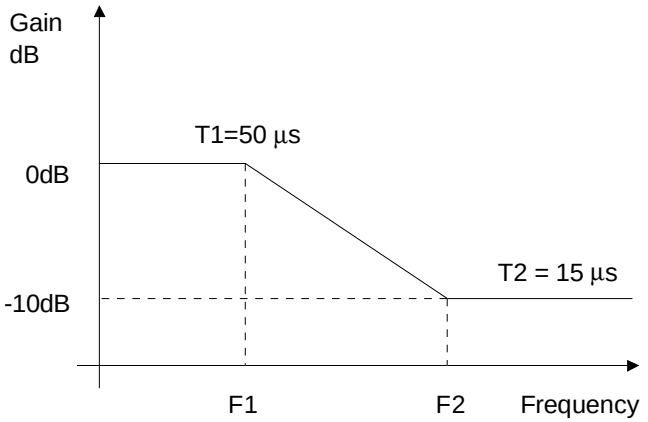



**Figure 13. De-emphasis Curve.**

## 2.11 Power Supply, Layout, and Grounding

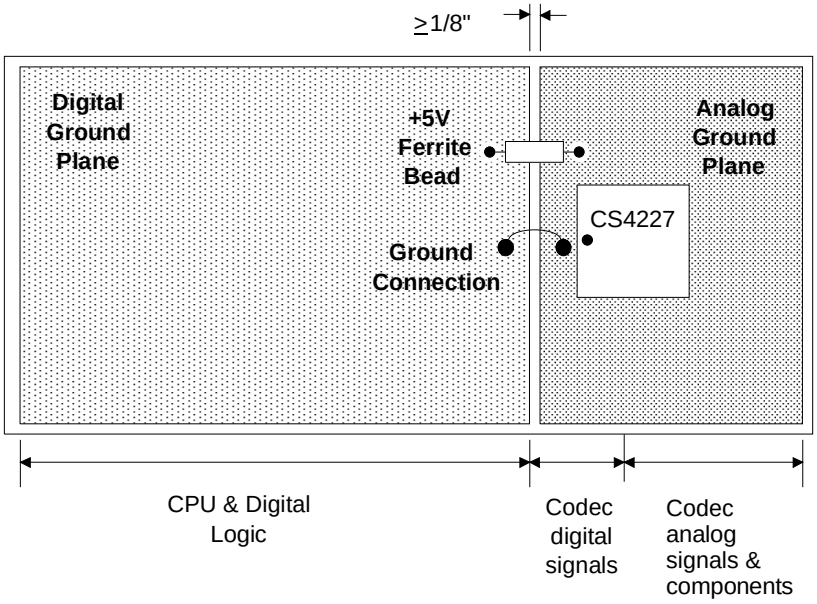
The CS4227, along with associated analog circuitry, should be positioned near the split between ground planes, and have its own, separate, ground plane (see Figure 14). Preferably, it should also have its own power plane. The +5 V supply must be connected to the CS4227 via a ferrite bead, positioned closer than 1" to the device. A single connection between the CS4227 ground and the board ground should be positioned as shown in Figure 14. The location of the 1 µF CMOUT filtering capicator should be as close to the CS4227 as possible. See Crystal's layout Applications Note, and the CDB4227 evaluation board data sheet for recommended layout of the decoupling components.

The CS4227 will mute the analog outputs and enter the Power Down Mode if the supply drops below approximately 4 volts.

## 2.12 ADC and DAC Filter Response Plots

Figures 15 through 20 show the overall frequency response, passband ripple and transition band for the CS4227 ADC's and DAC's.






Note that the CS4227 is oriented with its digital pins towards the digital end of the board.

**Figure 14. Suggested Layout Guideline**

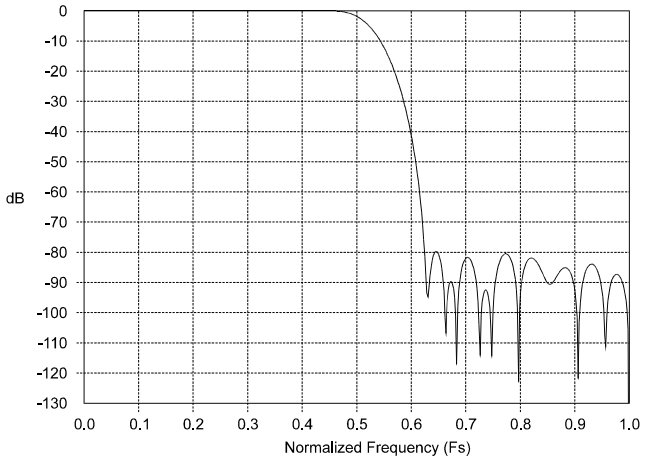



**Figure 15. 20-bit ADC Filter Response**

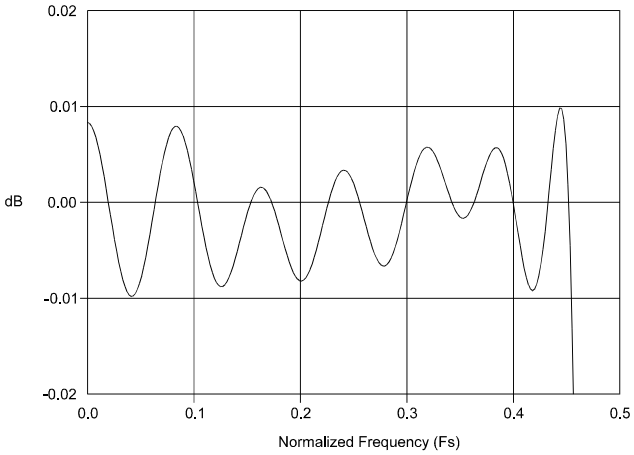



**Figure 16. 20-bit ADC Passband Ripple**

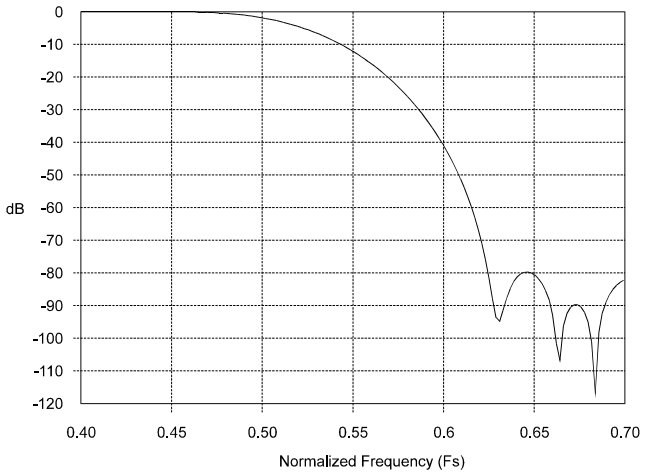



**Figure 17. 20-bit ADC Transition Band**

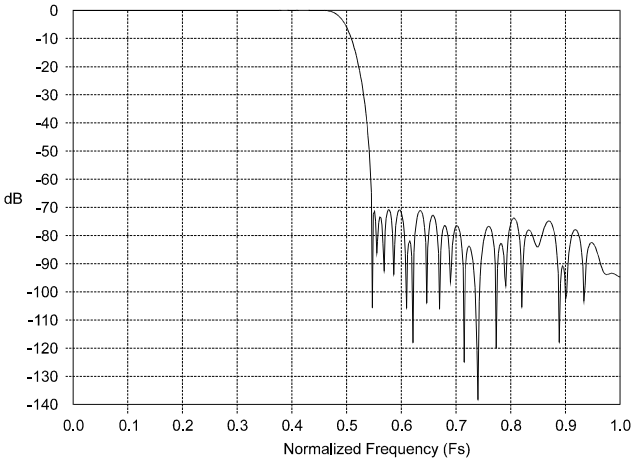



**Figure 18. DAC Frequency Response**

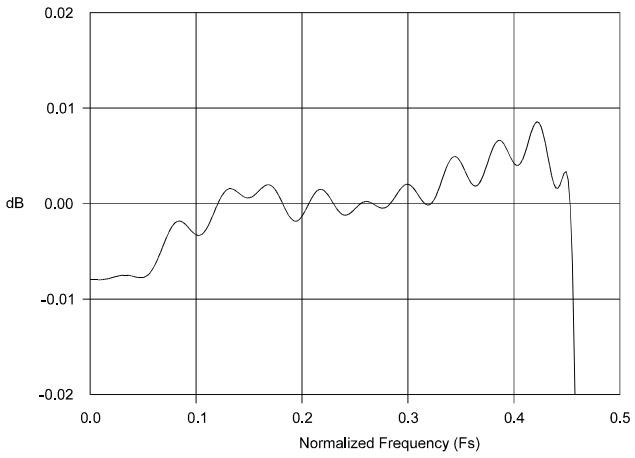



**Figure 19. DAC Passband Ripple**

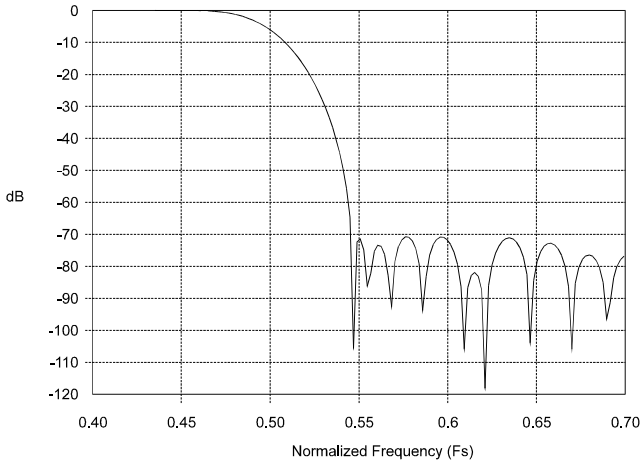



**Figure 20. DAC Transition Band**

## 2.13 Memory Address Pointer (MAP)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| INCR | 0 | 0 | MAP4 | MAP3 | MAP2 | MAP1 | MAP0 |

MAP4-MAP0 Register Pointer

INCR Auto Increment Control Bit
0 - No auto increment
1 - Auto increment on

This register defaults to 01h.

## 2.14 Reserved Byte (0)

This byte is reserved for internal use and must be set to 00h for normal operation.

This register defaults to 00h.

## 2.15 Clock Mode Byte (1)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | CO1 | CO0 | CI1 | CI0 | 0 | 0 | CE |

CE Master clock enable
0 - Clock Enabled
1 - Clock Disabled

CI1-CI0 Determines frequency of XTI
0 - 256 Fs
1 - 384 Fs
2 - 512 Fs
3 - not used

CO1-CO0 Sets CLKOUT frequency
0 - 256 Fs
1 - 384 Fs
2 - 512 Fs
3 - 1 Fs

This register defaults to 01h.

### *2.16 Converter Control Byte (2)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CALP | CLKE | DU | 0 | 0 | 0 | CAL | RS |

RS — Chip reset
0 - No Reset
1 - Reset

CAL — Calibration control bit
0 - Normal operation
1 - Rising edge initiates calibration

The following bits are read only:

DU — Shows selected De-Emphasis setting used by DAC's
0 - Normal Flat DAC frequency response
1 - De-Emphasis selected

CLKE — Clocking system status
0 - No errors
1 - Crystal is not oscillating, or requesting clock change in progress

CALP — Calibration status
0 - Calibration done
1 - Calibration in progres

This register defaults to 01h.

### *2.17 DAC Control Byte (3)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ZCD | MUTC | MUT6 | MUT5 | MUT4 | MUT3 | MUT2 | MUT1 |

MUT6-MUT1 — Mute control bits
0 - Normal output level
1 - Selected DAC output muted

MUTC — Controls mute on consecutive zeros function
0 - 512 consecutive zeros will mute DAC
1 - DAC output will not mute on zeros

ZCD — Zero crossing disable
0 - DAC mutes and volume control changes occur on zero-crossings
1 - DAC mutes and volume control changes occur immediately.

This register defaults to 3Fh.

### *2.18 Output Attenuator Data Byte (4, 5, 6, 7, 8, 9)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |

ATT6-ATT0 Sets attenuator level
0 - No attenuation
127 - 127 dB attenuation
ATT0 represents 1.0 dB of attenuation

This register defaults to 7Fh.

### *2.19 DAC Status Report Byte (Read Only) (10)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | - | ACC6 | ACC5 | ACC4 | ACC3 | ACC2 | ACC1 |

ACC6-ACC1 Acceptance Bit
0 - ATT6-ATT0 has been accepted.
1 - New setting is waiting for zero-crossing to be accepted.

This register is read-only.

### *2.20 ADC Control Byte (11)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| IS1 | IS0 | 0 | AIS1 | AIS0 | MUTM | MUTR | MUTL |

MUTL, MUTR, MUTM - Left, right and mono channel mute control
0 - Normal output level
1 - Selected ADC output muted

AIS1-AIS0 ADC analog input mux control
0 - Selects stereo pair 1
1 - Selects stereo pair 2
2 - Selects stereo pair 3
3 - Differential Input

IS1-IS0 Input mux selection
0 - Stereo ADC output to SDOUT1, Mono ADC output to SDOUT2
1 - Auxiliary Digital Input Port to SDOUT1, Mono ADC output to SDOUT2
2 - Auxiliary Digital Input Port to SDOUT1, Stereo ADC output to SDOUT2
3 - Not used.

This register defaults to 00h.

### *2.21 Input Control Byte (12)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OVRM | 0 | 0 | 0 | GNR1 | GNR0 | GNL1 | GNL0 |

GNL1-GNL0 Sets left input gain
- 0 - 0 dB
- 1 - 3 dB
- 2 - 6 dB
- 3 - 9 dB

GNR1-GNR0 Sets right input gain
- 0 - 0 dB
- 1 - 3 dB
- 2 - 6 dB
- 3 - 9 dB

OVRM ADC Overflow Mask

This register defaults to 00h.

### *2.22 ADC Status Report Byte (Read Only) (13)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LVM1 | LVM0 | LVR2 | LVR1 | LVR0 | LVL2 | LVL1 | LVL0 |

LVL2-LVL0, LVR2-0 Left and Right ADC output level
- 0 - Normal output levels
- 1 - -6 dB level
- 2 - -5 dB level
- 3 - -4 dB level
- 4 - -3 dB level
- 5 - -2 dB level
- 6 - -1 dB level
- 7 - Clipping

LVLM1-LVLM0 Mono ADC output level
- 0 - Normal output level
- 1 - -6 dB level
- 2 - -3 dB level
- 3 - Clipping

These bits are 'sticky'. They constantly monitor the ADC output for the peak levels and hold the maximum output. They are reset to 0 when read.

This register is read only.

### *2.23 DSP Port Mode Byte (14)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DCK1 | DCK0 | DMS1 | DMS0 | DSCK | DDF2 | DDF1 | DDF0 |

DDF2-DDF0 Data format
- 0 - Right justified, 20-bit
- 1 - Right justified, 18-bit
- 2 - Right justified, 16-bit
- 3 - Left justified, 20-bit in / 24-bit out
- 4 - $I^2S$ compatible, 20-bit in / 24-bit out
- 5 - One Data Line Mode (Figure 10)
- 6 - One Data Line (Master Mode only, Figure 10)
- 7 - Not used

DSCK Set the polarity of clocking data
- 0 - Data clocked in on rising edge, out on falling edge
- 1 - Data clocked in on falling edge, out on rising edge

DMS1-DMS0 Sets the mode of the port
- 0 - Slave
- 1 - Master Burst - SCLKs are gated 128 Fs clocks
- 2 - Master Non-Burst - SCLKs are evenly distributed (No 48 Fs SCLK)
- 3 - not used - default to Slave

DCK1-DCK0* Set number of bit clocks per Fs period
- 0 - 128
- 1 - 48 - Master Burst or Slave mode only
- 2 - 32 - All formats will default to 16 bits
- 3 - 64

This register defaults to 00h.

* Ignored in data formats 5 and 6.

## *2.24 Auxiliary Port Mode Byte (15)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ACK1 | ACK0 | AMS1 | AMS0 | ASCK | ADF2 | ADF1 | ADF0 |

ADF2-ADF0 Data format
0 - Right justified, 20-bit data
1 - Right justified, 18-bit data
2 - Right justified, 16-bit data
3 - Left justified, 20-bit
4 - $I^2S$ compatible, 20-bit
5 - Not used
6 - Not used
7 - Not used

ASCK Sets the polarity of clocking data
0 - Data clocked in on rising edge
1 - Data clocked in on falling edge

AMS1-AMS0 Sets the mode of the port.
0 - Slave
1 - Master Burst - SCLKAUXs are gated 128 Fs clocks
2 - Master Non-Burst - SCLKAUXs are evenly distributed in LRCKAUX frame
3 - Not used - default to slave

ACK1-ACK0 Set number of bit clocks per Fs period.
0 - 128
1 - 48 - Master Burst or Slave mode only
2 - 32 - All input formats will default to 16 bits.
3 - 64

This register defaults to 00h.

### *2.25 Auxilliary Port Control Byte (16)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | UMV | MOH | 0 | DEM2 | DEM1 | DEM0 |

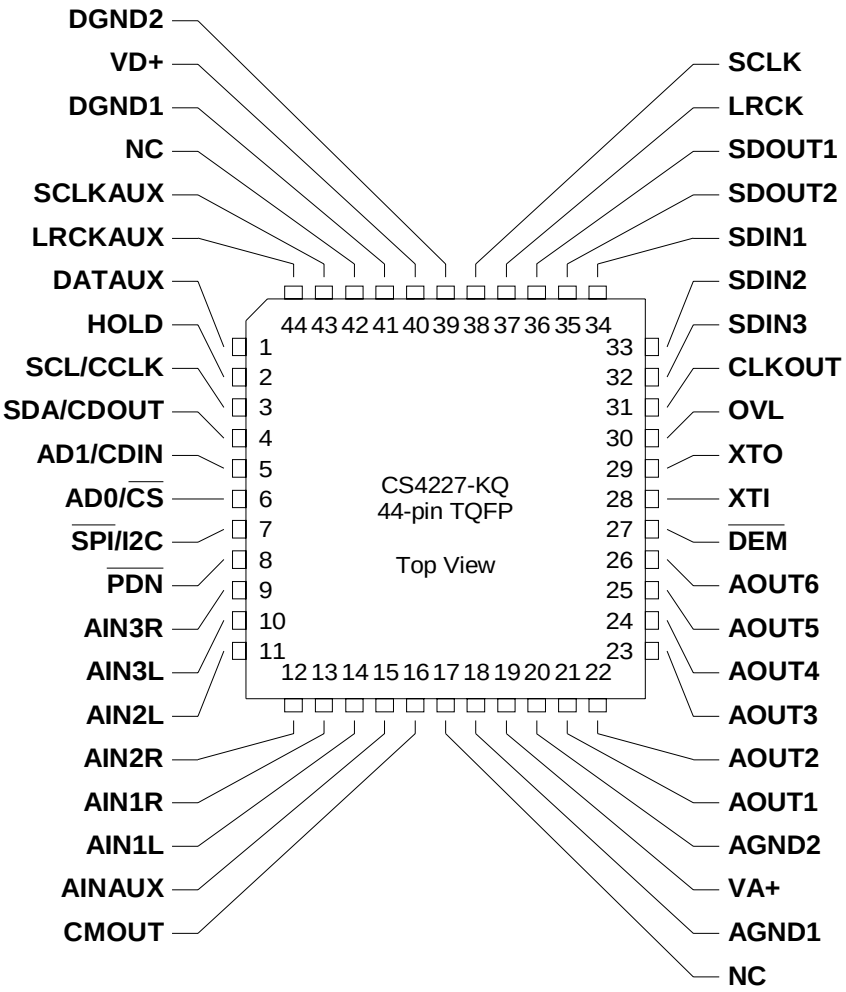
DEM 2-0 Selects de-emphasis response/source
- 0 - De-emphasis off
- 1 - De-emphasis on 32 kHz
- 2 - De-emphasis on 44.1 kHz
- 3 - De-emphasis on 48 kHz
- 4 - De-emphasis pin 32 kHz
- 5 - De-emphasis pin 44.1 kHz
- 6 - De-emphasis pin 48 kHz
- 7 - Reserved

MOH Mute On Hold
- 0 - Extended Hold (16 frames) mutes DAC outputs
- 1 - DACs not muted

UMV Unmute on Valid Data
- 0 - DACs unmute when HOLD is removed
- 1 - DACs must be unmuted in DAC control byte after HOLD is removed.

This register defaults to 00h.

## 3. PIN DESCRIPTIONS




*Power Supply*

**VA+ - Analog Power Input**

+5 V analog supply.

**AGND1, AGND2 - Analog Ground**

Analog grounds.

**VD+ - Digital Power Input**

+ 5 V digital supply.

**DGND1, DGND2 - Digital Ground**

Digital grounds.

*Analog Inputs*

**AIN1L, AIN1R - Left and Right Channel Mux Input 1**

Analog signal input connections for the right and left channels for multiplexer input 1.

**AIN2L, AIN2R - Left & Right Channel Mux Input 2**

Analog signal input connections for the right and left channels for multiplexer input 2.

**AIN3L, AIN3R - Left & Right Channel Mux Input 3**

Analog signal input connections for the right and left channels for multiplexer input 3.

**AINAUX - Auxiliary Line Level Input**

Analog signal input for the mono A/D converter.

*Analog Outputs*

**AOUT1, AOUT2, AOUT3, AOUT4, AOUT5, AOUT6 - Audio Outputs**

The analog outputs from the 6 D/A converters. Each output can be independently controlled for output amplitude.

**CMOUT - Common Mode Output**

This common mode voltage output may be used for level shifting when DC coupling is desired. The load on CMOUT must be DC only, with an impedance of not less than 50 kΩ. CMOUT should be bypassed with a 1.0 µF to AGND.

*Digital Audio Interface Signals*

**SDIN1 - Serial Data Input 1**

Digital audio data for the DACs 1 and 2 is presented to the CS4227 on this pin. This pin is also used for one-line data input modes.

**SDIN2 - Serial Data Input 2**

Digital audio data for the DACs 3 and 4 is presented to the CS4227 on this pin.

**SDIN3 - Serial Data Input 3**

Digital audio data for the DACs 5 and 6 is presented to the CS4227 on this pin.

**SDOUT1- Serial Data Output 1**

Digital audio data from the 20-bit stereo audio ADCs is output from this pin. When IS = 1 or 2, DATAAUX is output on SDOUT1. This pin is also used for one line data output modes.

**SDOUT2 - Serial Data Output 2**

Digital audio data from the mono audio ADC is output from this pin. When IS = 2, the stereo audio ADC's are output from this pin

**SCLK - DSP Serial Port Clock I/O**

SCLK clocks digital audio data into the DACs via SDIN1/2/3, and clocks data out of the ADCs on SDOUT1/2. Active clock edge depends on the DSCK bit.

### LRCK - Left/Right Select Signal I/O

The Left/Right select signal. This signal has a frequency equal to the sample rate. The relationship of LRCK to the left and right channel data depends on the selected format.

### $\overline{\text{DEM}}$ - De-emphasis Control

When low, $\overline{\text{DEM}}$ controls the activation of the standard 50/15 us de-emphasis filter for either 32, 44.1 or 48 kHz sample rates. This pin is enabled by the DEM2-0 bits in the Auxiliary Port Control Byte.

### OVL - Overload Indicator

This pin goes high if either of the stereo audio ADCs or the mono ADC is clipping.

*Auxillary Digital Audio Signals*

### DATAUX - Auxiliary Data Input

DATAUX is the auxiliary audio data input line, usually connected to an external digital audio source.

### LRCKAUX - Auxiliary Word Clock Input or Output

In auxiliary slave mode, LRCKAUX is a word clock (at Fs) from an external digital audio source. In auxiliary master mode, LRCKAUX is a word clock output (at Fs) to clock an external digital audio source.

### SCLKAUX - Auxiliary Bit Clock Input or Output

In auxiliary slave mode, SCLKAUX is the serial data bit clock from an external digital audio source, used to clock in data on DATAAUX. In auxiliary master mode, SCLKAUX is a serial data bit clock output.

### HOLD - HOLD Control

This pin is sampled on the active edge of SCLKAUX. If it is high any time during the frame, DATAUX data is ignored and the previous "good" sample is output to the serial output port.

*Control Port Signals*

### $\overline{\text{SPI}}$/I2C - Control Port Format

Setting this pin low configures the control port for the SPI interface; a high state configures the control port for the $I^2C$ interface. The state of this pin sets the function of the control port input/output pins .

### SCL/CCLK - Serial Control Interface Clock

SCL/CCLK is the serial control interface clock, and is used to clock control bits into and out of the CS4227.

### AD0/$\overline{\text{CS}}$ - Address Bit / Control Port Chip Select

In $I^2C$® mode, AD0 is a chip address bit. In SPI software control mode, $\overline{\text{CS}}$ is used to enable the control port interface on the CS4227.

### AD1/CDIN - Address Bit / Serial Control Data In

In $I^2C$® mode, AD1 is a chip address bit. In SPI software control mode, CDIN is the input data line for the control port interface.

### SDA/CDOUT - Serial Control Data Out

In $I^2C$® mode, SDA is the control data I/O line. In SPI software control mode, CDOUT is the output data from the control port interface on the CS4227.

*Clock and Crystal Pins*

### XTI, XTO - Crystal connections

Input and output connections for the crystal which may be used to operate the CS4227. Alternatively, a clock may be input into XTI.

### CLKOUT - Master Clock Output

CLKOUT allows external circuits to be synchronized to the CS4227. Alternate output frequencies are selectable by the control port.

*Miscellaneous Pins*

### $\overline{\text{PDN}}$ - Powerdown Pin

When low, the CS4227 enters a low power mode and all internal states are reset, including the control port. When high, the control port becomes operational and the RS bit must be cleared before normal operation will occur.

### NC - No Connect

# 4. PARAMETER DEFINITIONS

## Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dbFs signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

## Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 20 Hz to 20 kHz), including distortion components. Expressed in decibels. ADCs are measured at -1 dBFs as suggested in AES 17-1991 Annex A.

## Idle Channel Noise / Signal-to-Noise-Ratio

The ratio of the rms analog output level with 1kHz full scale digital input to the rms analog output level with all zeros into the digital input. Measured A-weighted over a 10 Hz to 20 kHz bandwidth. Units in decibels. This specification has been standardized by the Audio Engineering Society, AES17-1991, and referred to as Idle Channel Noise. This specification has also been standardized by the Electronic Industries Association of Japan, EIAJ CP-307, and referred to as Signal-to-Noise-Ratio.

## Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the rms sum of all the in-band harmonics of the test signal. Units in decibels.

## Interchannel Isolation

A measure of crosstalk between channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

## Frequency Response

A measure of the amplitude response variation from 20 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

## Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units are in decibels.

## Gain Error

The deviation from the nominal full scale output for a full scale input.

## Gain Drift

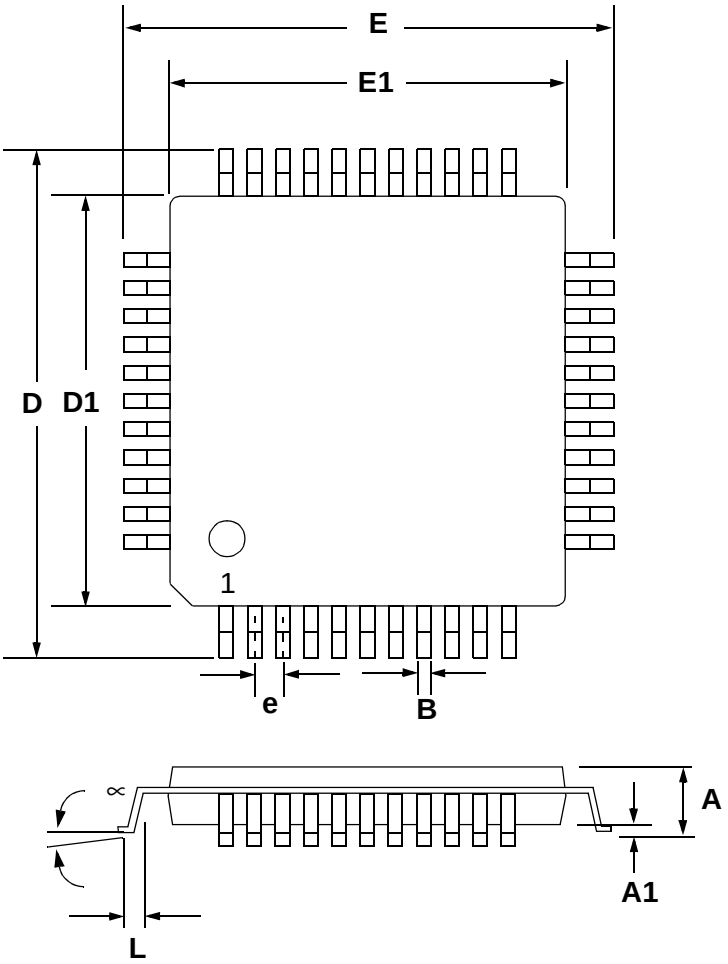
The change in gain value with temperature. Units in ppm/°C.

## Offset Error

For the ADCs, the deviation in LSB's of the output from mid-scale with the selected input grounded. For the DAC's, the deviation of the output from zero (relative to CMOUT) with mid-scale input code. Units are in volts.

## 5. PACKAGE DIMENSIONS

### 44L TQFP PACKAGE DRAWING




| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.000 | 0.065 | 0.00 | 1.60 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 |
| B | 0.012 | 0.018 | 0.30 | 0.45 |
| D | 0.478 | 0.502 | 11.70 | 12.30 |
| D1 | 0.404 | 0.412 | 9.90 | 10.10 |
| E | 0.478 | 0.502 | 11.70 | 12.30 |
| E1 | 0.404 | 0.412 | 9.90 | 10.10 |
| e | 0.029 | 0.037 | 0.70 | 0.90 |
| L | 0.018 | 0.030 | 0.45 | 0.75 |
| ∝ | 0.000 | 7.000 | 0.00 | 7.00 |

| | TYP | MAX | TYP | MAX |
|---|---|---|---|---|
| Coplanarity | .001 | .004 | .025 | .10 |

***JEDEC # : MS-026***

# • Notes •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