Chrontel CH7301 DVI Transmitter Device

1. FEATURES

- DVI Transmitter up to 165M pixels/second
- DVI low jitter PLL
- DVI hot plug detection
- Supporting graphics resolutions up to1600 x 1200 pixels
- Providing RGB output
- DAC connection detection
- Programmable power management
- Fully programmable through serial port
- Complete Windows and DOS driver support
- Low voltage interface support to graphics device
- Offered in a 64-pin LQFP package

2. GENERAL DESCRIPTION

The CH7301 is a display controller device which accepts a digital graphics input signal, and encodes and transmits data through a DVI or DFP (Digital flat panel). The device accepts data over one 12-bit wide variable voltage data port which supports four different RGB data formats.

The DVI processor includes a low jitter PLL for generation of the high frequency serialized clock, and all circuitry required to encode, serialize and transmit data. The CH7301 comes in versions able to drive a DFP display at a pixel rate of up to 165MHz, supporting UXGA resolution displays. No scaling of input data is performed on the data output to the DVI device. See Figure 1 for the functional block diagram of the CH7301.

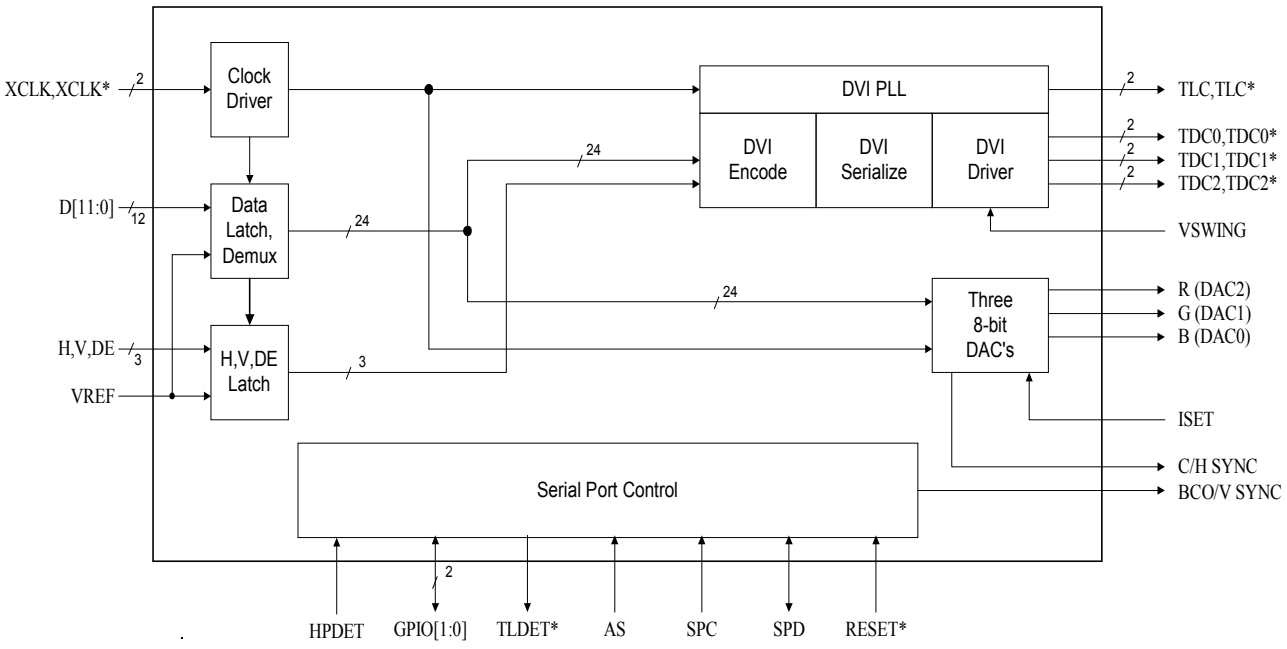

Figure 1. Functional Block Diagram

3. PIN DESCRIPTIONS

3.1 Package Diagram

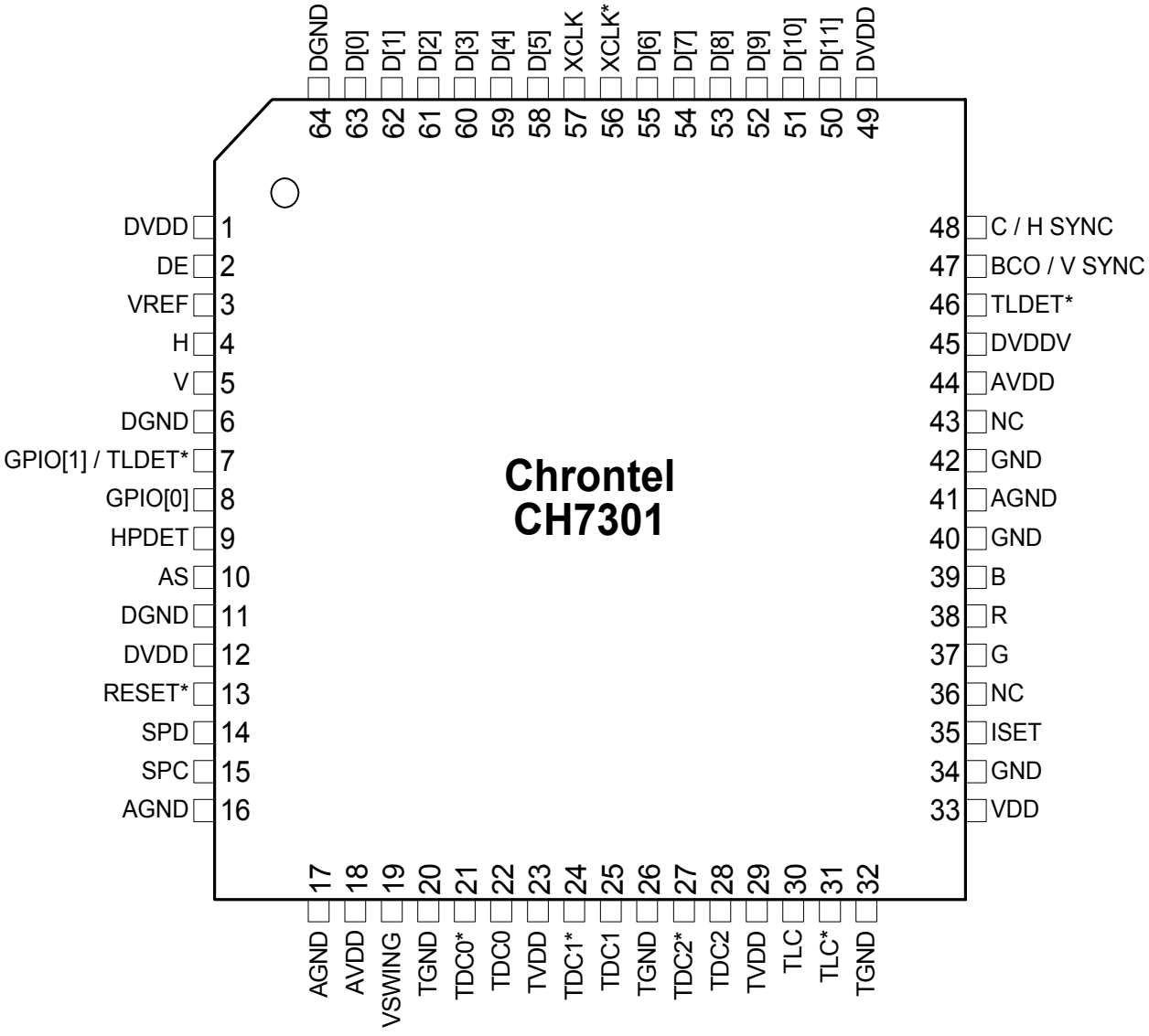

Figure 2. 64-Pin LQFP

3.2 Pin Description

Table 1. Pin Description

64-Pin LQFP	# Pins	Type	Symbol	Description
2	1	In	DE	**Data Enable** This pin accepts a data enable signal which is high when active video data is input to the device, and low all other times. The levels are 0 to DVDDV, and the VREF signal is used as the threshold level. This input is used by the DVI.
3	1	In	VREF	**Reference Voltage Input** The VREF pin inputs a reference voltage of DVDDV / 2. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, sync, data enable and clock inputs.
4	1	In/Out	H	**Horizontal Sync Input / Output** This pin receives / sends out horizontal sync input from / output to the graphics controller.
5	1	In/Out	V	**Vertical Sync Input / Output** This pin receives / sends vertical sync input from / output to the graphics controller.
7	2	In/Out	GPIO[1] / TLDET*	**General Purpose Input - Output[1] /** **DVI Detect Output** (Open drain or internal weak pull-up) This pin provides a general purpose I/O controlled via the serial port bus. The internal pull-up will be to the DVDD supply. When the GPIO[1] pin is configured as an input, this pin can be used to output the DVI detect signal (pulls low when a termination change has been detected on the HPDET input). This is an open drain output. The output is released through serial port control.
8	2	In/Out	GPIO[0]	**General Purpose Input - Output[0]** (Open drain or internal weak pull-up) This pin provides a general purpose I/O controlled via the serial port. This allows an external switch to be used to select NTSC or PAL at power-up.
9	1	In	HPDET	**Hot Plug Detect** (internal pull-down) This input pin determines whether the DVI is connected to a DVI monitor. When terminated, the monitor is required to apply a voltage greater than 2.4 volts. Changes on the status of this pin will be relayed to the graphics controller via the TLDET* or GPIO[1]/TLDET* pin pulling low.
10	1	In	AS	**Address Select** (Internal pull-up) This pin determines the serial port address of the device (1,1,1,0,1,AS*,AS).
13	1	In	RESET*	**Reset * Input** (Internal pull-up) When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port register.
14	1	In/Out	SPD	**Serial Port Data Input / Output** This pin functions as the serial data pin of the serial port interface, and uses the DVDD supply.

Table 1. Pin Description

64-Pin LQFP	# Pins	Type	Symbol	Description
15	1	In	SPC	**Serial Port Clock Input** This pin functions as the clock pin of the serial port interface, and uses the DVDD supply.
19	1	In	VSWING	**DVI Swing Control** This pin sets the swing level of the DVI outputs. A 2.4K ohm resistor should be connected between this pin and TGND using short and wide traces.
22, 21	2	Out	TDC0, TDC0*	**DVI Data Channel 0 Outputs** These pins provide the DVI differential outputs for data channel 0 (blue).
25, 24	2	Out	TDC1, TDC1*	**DVI Data Channel 1 Outputs** These pins provide the DVI differential outputs for data channel 1 (green).
28, 27	2	Out	TDC2, TDC2*	**DVI Data Channel 2 Outputs** These pins provide the DVI differential outputs for data channel 2 (red).
30, 31	2	Out	TLC, TLC*	**DVI Clock Outputs** These pins provide the differential clock output for the DVI interface corresponding to data on the TDC[0:2] outputs.
35	1	In	ISET	**Current Set Resistor Input** This pin sets the DAC current. A 140 ohm resistor should be connected between this pin and GND (DAC ground) using short and wide traces.
37	1	Out	G	**Green Output**
38	1	Out	R	**Red Output**
39	1	Out	B	**Blue Output**
43	1		NC	**No Connect**
46	1	Out	TLDET*	**DVI Detect Output** This pin provides an open drain output which pulls low when a termination change has been detected on the HPDET input. The output is released through serial port control.
47	1	Out	BCO / V SYNC	**Buffered Clock Output** This output pin provides a buffered clock output, driven by the DVDD supply. The output clock can be selected using the BCO register. A buffered version of VGA vertical sync can be acquired from this pin. (Refer to Register 22h, BCO register)
48	1	Out	C / H SYNC	**Composite / Horizontal Sync Output** A buffered version of VGA horizontal sync can be acquired from this pin. (Refer to Register 21h, DC register)
50 – 55, 58 – 63	12	In	D[11] - D[0]	**Data[11] through Data[0] Inputs** These pins accept the 12 data inputs from a digital video port of a graphics controller. The levels are 0 to DVDDV, and the VREF signal is used as the threshold level.

Table 1. Pin Description

64-Pin LQFP	# Pins	Type	Symbol	Description
57, 56	2	In	XCLK, XCLK*	**External Clock Inputs** These inputs form a differential clock signal input to the CH7301 for use with the H, V, DE and D[11:0] data. If differential clocks are not available, the XCLK* input should be connected to VREF. The output clocks from this pad cell are able to have their polarities reversed under the control of the MCP bit (in register 1Ch).
1, 12, 49	3	Power	DVDD	**Digital Supply Voltage (3.3V)**
6, 11, 64	3	Power	DGND	**Digital Ground**
45	1	Power	DVDDV	**I/O Supply Voltage (3.3V to 1.1V)**
23, 29	2	Power	TVDD	**DVI Transmitter Supply Voltage (3.3V)**
20, 26, 32	3	Power	TGND	**DVI Transmitter Ground**
18, 44	2	Power	AVDD	**PLL Supply Voltage (3.3V)**
16, 17, 41,42	4	Power	AGND	**PLL Ground**
33	1	Power	VDD	**DAC Supply Voltage (3.3V)**
34, 36, 40	3	Power	GND	**DAC Ground**

4. MODES OF OPERATION

The CH7301 is capable of being operated as a single DVI output link. Descriptions of the single DVI output link operating mode, with a block diagram of the data flow within the device is shown on **Figure 1**.

4.1 DVI Output

In DVI Output mode, multiplexed input data, sync and clock signals are input to the CH7301 from the graphics controller's digital output port. Data will be 2X multiplexed, and the clock inputs can be 1X or 2X times the pixel rate. Some examples of modes supported are shown in the table below, and a block diagram of the CH7301 is shown on the following page. For the table below, clock frequencies for given modes were taken from VESA DISPLAY MONITOR TIMING SPECIFICATIONS if they were detailed there, not VESA TIMING DEFINITION FOR FLAT PANEL MONITORS. The device is not dependent upon this set of timing specifications. Any values of pixels/line, lines/frame and clock rate are acceptable, as long as the pixel rate remains below 165MHz. For correct DVI operation, the input data format must be selected to be one of the RGB input formats.

Table 2. DVI Outputs

Graphics Resolution	Active Aspect Ratio	Pixel Aspect Ratio	Refresh Rate (Hz)	XCLK Frequency (MHz)	DVI Frequency (Mbits)
720x400	4:3	1.35:1.00	<85	<35.5	<355
640x400	8:5	1:1	<85	<31.5	<315
640x480	4:3	1:1	<85	<36	<360
720x480[1]	4:3	9:8	59.94	27	270
720x576[2]	4:3	15:12	50	27	270
800x600	4:3	1:1	<85	<57	<570
1024x768	4:3	1:1	<85	<95	<950
1280x720	16:9	1:1	<60	<67	<670
1280x768	15:9	1:1	<60	<75	<750
1280x1024	4:3	1:1	<85	<158	<1580
1366x768	16:9	1:1	<60	<80	<800
1600x1200	4:3	1:1	<60	<165	<1650
1920x1080	16:9	1:1	<30[2]	<140	<1400

[1] These DVD compatible modes are input in a non-interlaced RGB data format.

[2] 30Hz in progressive scan modes, 60Hz in interlaced modes.

5. INPUT INTERFACE

Two distinct methods of transferring data to the CH7301 are described. They are:

- Multiplexed data, clock input at 1X pixel rate
- Multiplexed data, clock input at 2X pixel rate

For the multiplexed data, clock at 1X pixel rate, the data applied to the CH7301 is latched with both edges of the clock (also referred to as dual-edge transfer mode). For the multiplexed data, clock at 2X pixel rate, the data applied to the CH7301 is latched with one edge of the clock. The polarity of the pixel clock can be reversed under serial port control.

5.1 Input Clock and Data Timing Diagram

The figure below shows the timing diagram for input data and clocks. The first XCLK/XCLK* waveform represents the input clock for the multiplexed data, clock at 2X pixel rate method. The second XCLK/XCLK* waveform represents the input clock for the multiplexed data, clock at 1X pixel rate method.

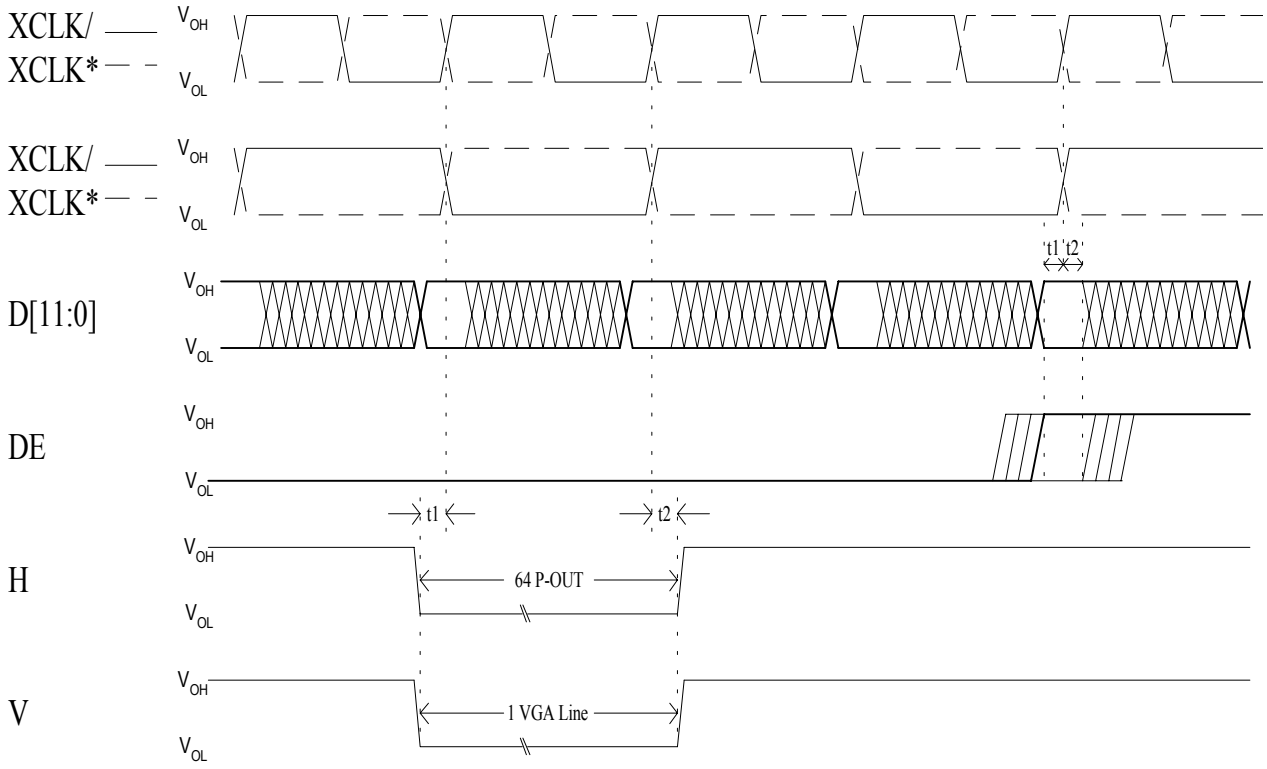

Figure 3. Interface Timing

Table 3. Interface Timing

Symbol	Parameter	Min	Typical	Max	Unit
V_{OH}	Output high level of interface signals	DVDDV - 0.2		DVDDV + 0.2	V
V_{OL}	Output Low level of interface signals	-0.2		0.2	V
t1[1]	D[11:0] & DE to XCLK = XCLK* Delay (setup time)	0.5			ns
t2[1]	XCLK = XCLK* to D[11:0] & DE Delay (hold time)	0.5			ns
DVDDV	Digital I/O Supply Voltage	1.1 – 5%		3.3 + 5%	V

[1] D[11:0], H, V DE times measured when input equals Vref+100mV on rising edges, Vref-100mV on falling edges.

5.2 Input Clock and Data Formats

The 12 data inputs support 5 different multiplexed data formats, each of which can be used with a 1X clock latching data on both clock edges, or a 2X clock latching data with a single edge. The data received by the CH7301 can be used to drive the DVI output, the VGA to TV encoder, or directly drive the DAC's. The multiplexed input data formats are (IDF[2:0]):

IDF	Description
0	12-bit multiplexed RGB input (24-bit color), (multiplex scheme 1)
1	12-bit multiplexed RGB2 input (24-bit color), (multiplex scheme 2)
2	8-bit multiplexed RGB input (16-bit color, 565)
3	8-bit multiplexed RGB input (15-bit color, 555)
4	8-bit multiplexed YCrCb input (24-bit color), (Y, Cr and Cb are multiplexed)

For multiplexed input data formats, either both transitions of the XCLK/XCLK* clock pair, or each rising or falling edge of the clock pair (depending upon MCP bit, rising refers to a rising edge on the XCLK signal, a falling edge on the XCLK* signal) will latch data from the graphics chip. The multiplexed input data formats are shown in the figures below. The Pixel Data bus represents a 12-bit or 8-bit multiplexed data stream, which contains either RGB or YCrCb formatted data. The input data rate is 2X the pixel rate, and each pair of Pn values (eg; P0a and P0b) will contain a complete pixel encoded as shown in the tables below. It is assumed that the first clock cycle following the leading edge of the incoming horizontal sync signal contains the first word (Pxa) of a pixel, if an active pixel was present immediately following the horizontal sync. This does not mean that active data should immediately follow the horizontal sync, however. When the input is a YCrCb data stream the color-difference data will be transmitted at half the data rate of the luminance data, with the sequence being set as Cb, Y, Cr, Y, where Cb0,Y0,Cr0 refers to co-sited luminance and color-difference samples and the following Y1 byte refers to the next luminance sample, per CCIR-656 standards (the clock frequency is dependent upon the current mode, and is not 27MHz as specified in CCIR-656). All non-active pixels should be 0 in RGB formats, and 16 for Y and 128 for CrCb in YCrCb formats.

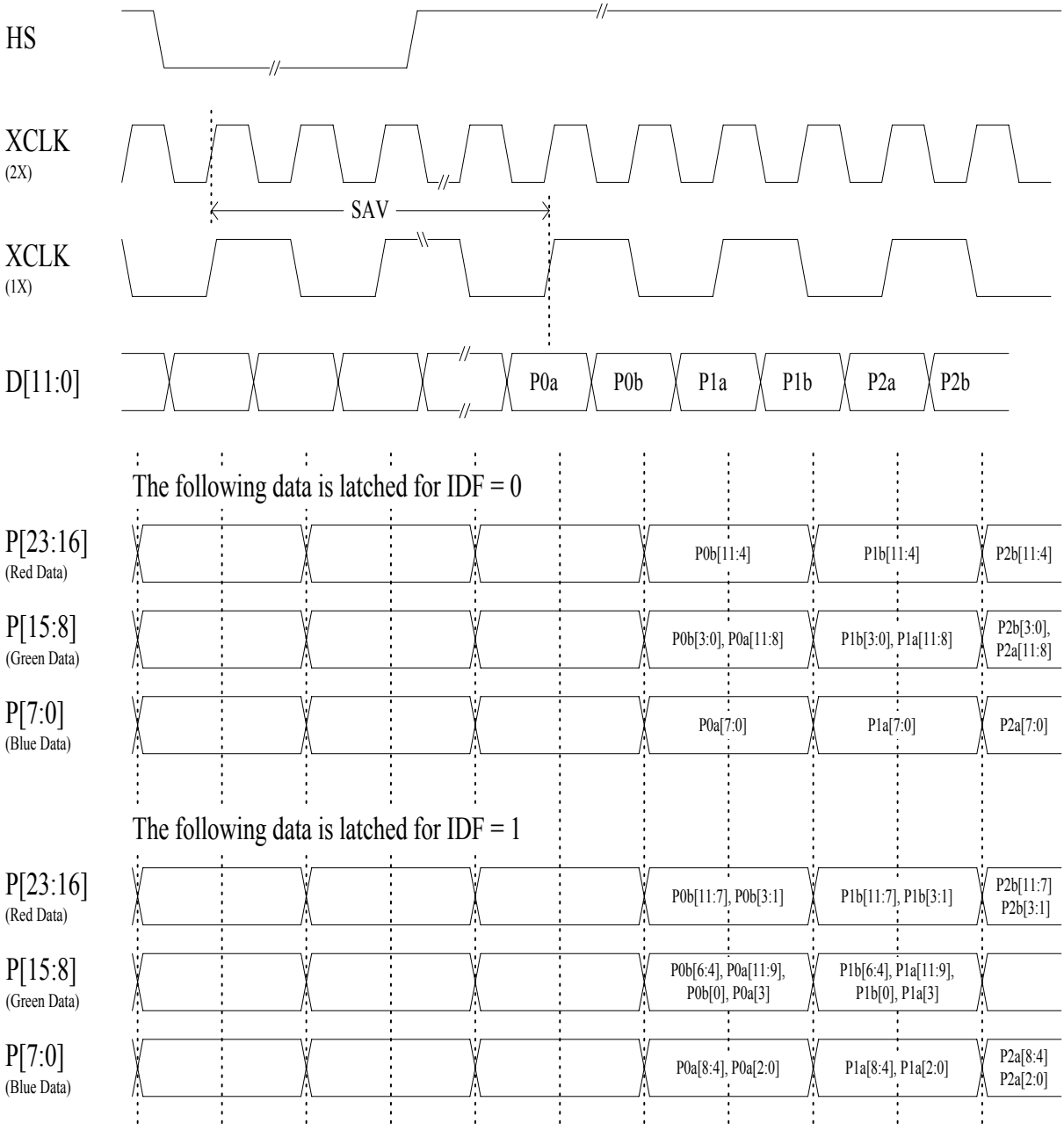

Figure 4. Multiplexed Input Data Formats (IDF = 0, 1)

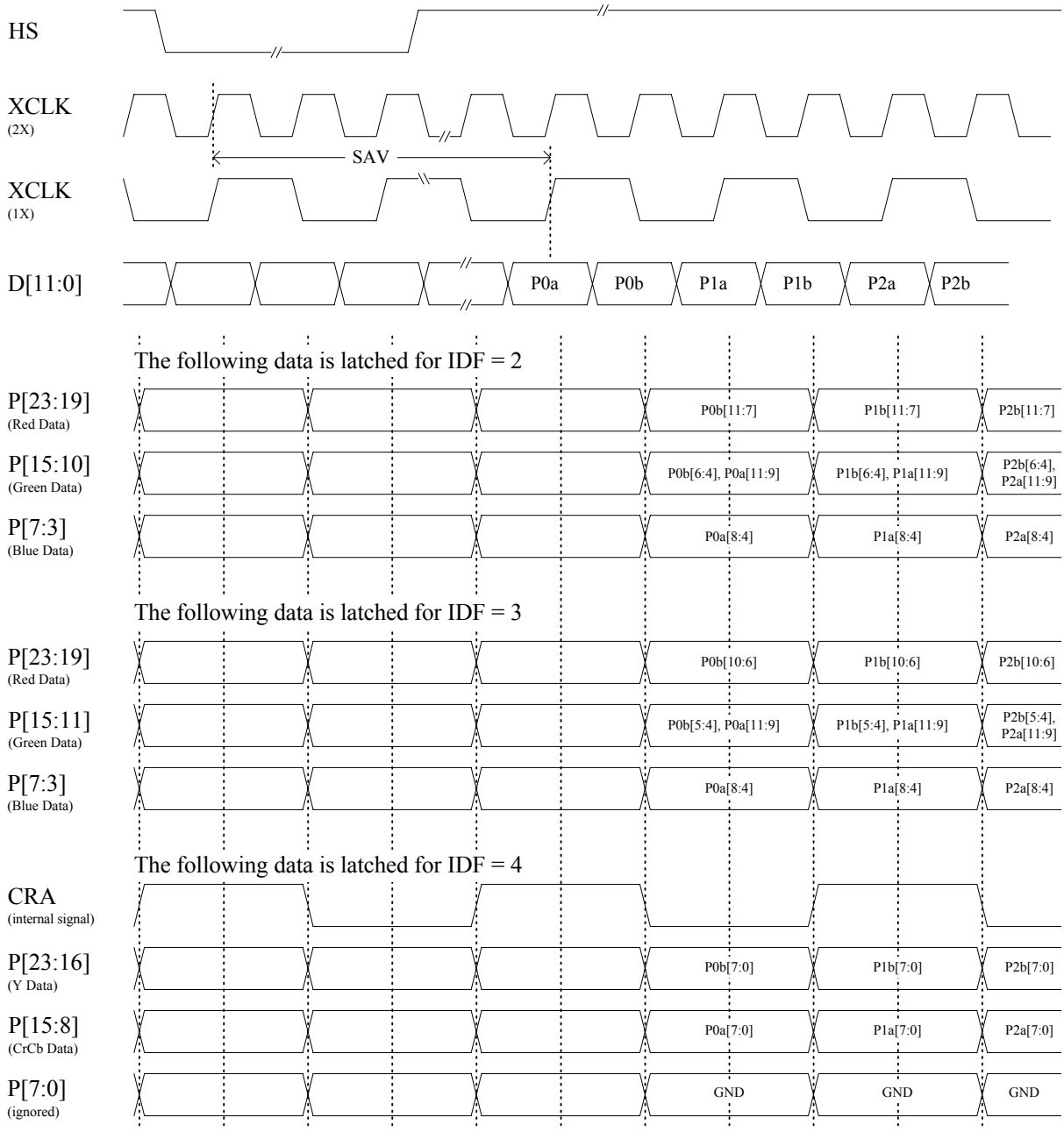

Figure 5. Multiplexed Input Data Formats (IDF = 2, 3, 4)

Table 4. Multiplexed Input Data Formats (IDF = 0, 1)

IDF = Format =		0 12-bit RGB (12-12)				1 12-bit RGB (12-12)			
Pixel #		P0a	P0b	P1a	P1b	P0a	P0b	P1a	P1b
Bus Data	D[11]	G0[3]	R0[7]	G1[3]	R1[7]	G0[4]	R0[7]	G1[4]	R1[7]
	D[10]	G0[2]	R0[6]	G1[2]	R1[6]	G0[3]	R0[6]	G1[3]	R1[6]
	D[9]	G0[1]	R0[5]	G1[1]	R1[5]	G0[2]	R0[5]	G1[2]	R1[5]
	D[8]	G0[0]	R0[4]	G1[0]	R1[4]	B0[7]	R0[4]	B1[7]	R1[4]
	D[7]	B0[7]	R0[3]	B1[7]	R1[3]	B0[6]	R0[3]	B1[6]	R1[3]
	D[6]	B0[6]	R0[2]	B1[6]	R1[2]	B0[5]	G0[7]	B1[5]	G1[7]
	D[5]	B0[5]	R0[1]	B1[5]	R1[1]	B0[4]	G0[6]	B1[4]	G1[6]
	D[4]	B0[4]	R0[0]	B1[4]	R1[0]	B0[3]	G0[5]	B1[3]	G1[5]
	D[3]	B0[3]	G0[7]	B1[3]	G1[7]	G0[0]	R0[2]	G1[0]	R1[2]
	D[2]	B0[2]	G0[6]	B1[2]	G1[6]	B0[2]	R0[1]	B1[2]	R1[1]
	D[1]	B0[1]	G0[5]	B1[1]	G1[5]	B0[1]	R0[0]	B1[1]	R1[0]
	D[0]	B0[0]	G0[4]	B1[0]	G1[4]	B0[0]	G0[1]	B1[0]	G1[1]

Table 5. Multiplexed Input Data Formats (IDF = 2, 3)

IDF = Format =		2 RGB 5-6-5				3 RGB 5-5-5			
Pixel #		P0a	P0b	P1a	P1b	P0a	P0b	P1a	P1b
Bus Data	D[11]	G0[4]	R0[7]	G1[4]	R1[7]	G0[5]	X	G1[5]	X
	D[10]	G0[3]	R0[6]	G1[3]	R1[6]	G0[4]	R0[7]	G1[4]	R1[7]
	D[9]	G0[2]	R0[5]	G1[2]	R1[5]	G0[3]	R0[6]	G1[3]	R1[6]
	D[8]	B0[7]	R0[4]	B1[7]	R1[4]	B0[7]	R0[5]	B1[7]	R1[5]
	D[7]	B0[6]	R0[3]	B1[6]	R1[3]	B0[6]	R0[4]	B1[6]	R1[4]
	D[6]	B0[5]	G0[7]	B1[5]	G1[7]	B0[5]	R0[3]	B1[5]	R1[3]
	D[5]	B0[4]	G0[6]	B1[4]	G1[6]	B0[4]	G0[7]	B1[4]	G1[7]
	D[4]	B0[3]	G0[5]	B1[3]	G1[5]	B0[3]	G0[6]	B1[3]	G1[6]

Table 6. Multiplexed Input Data Formats (IDF = 4)

IDF = Format =		4 YCrCb 8-bit							
Pixel #		P0a	P0b	P1a	P1b	P2a	P2b	P3a	P3b
Bus Data	D[7]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
	D[6]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
	D[5]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
	D[4]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
	D[3]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
	D[2]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
	D[1]	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
	D[0]	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]

When IDF = 4 (YCrCb mode), the data inputs can also be used to transmit sync information to the device. In this mode, the embedded sync will follow the VIP2 convention, and the first byte of the 'video timing reference code' will be assumed to occur when a Cb sample would occur, if the video stream was continuous. This is shown below:

Table 7. Embedded Sync

IDF = Format =		4 YCrCb 8-bit							
Pixel #		P0a	P0b	P1a	P1b	P2a	P2b	P3a	P3b
Bus Data	Dx[7]	FF	00	00	S[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
	Dx[6]	FF	00	00	S[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
	Dx[5]	FF	00	00	S[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
	Dx[4]	FF	00	00	S[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
	Dx[3]	FF	00	00	S[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
	Dx[2]	FF	00	00	S[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
	Dx[1]	FF	00	00	S[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
	Dx[0]	FF	00	00	S[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]

In this mode, the S[7..0] byte contains the following data:

S[6] = F = 1 during field 2, 0 during field 1

S[5] = V = 1 during field blanking, 0 elsewhere

S[4] = H = 1 during EAV (synchronization reference at the end of active video)

0 during SAV (synchronization reference at the start of active video)

Bits S[7] and S[3..0] are ignored.

5.3 Hot Plug Detection

The CH7301 has the capability of signaling to the graphics controller when the termination of the DVI outputs has changed. The operation of this circuit is as follows. The HPDET input pin of the CH7301 should be connected to pin 16 of the DVI connector. When a DVI monitor is connected to the DVI connector, this pin will be pulled high (above 2.4 volts). When a DVI monitor is not connected to the DVI connector, the internal pull-down on the HPDET pin will pull low. The CH7301 will detect any transition at the HPDET pin. When the HPIE (Hot Plug Interrupt Enable) bit in serial port register 1Eh is high, the CH7301 will pull low on the TLDET* pin. When the HPIE2 (Hot Plug Interrupt Enable 2) bit in serial port register 20h is high, the CH7301 will pull low on the GPIO[1] / TLDET* pin. This should signal the driver to read the DVIT bit in register 20h to determine the state of the HPDET pin. The TLDET* pin will continue to pull low until the driver sets the HPIR (Hot Plug Interrupt Reset) bit in register 1Eh high. The driver should then set the HPIR bit low.

6. REGISTER CONTROL

The CH7301 is controlled via a serial port. The serial port bus uses only the SPC clock to latch data into registers, and does not use any internally generated clocks so that the device can be written to in all power down modes. The device retains all register states.

The CH7301 contains a total of 37 registers for user control.

6.1 Control Registers Map

The controls are listed below, divided into three sections: general controls, input / output controls, DVI controls. A register map and register description follows.

• General Controls

ResetIB	Software serial reset
ResetDB	Software datapath reset
PD[7:0]	Power down controls (DVIP, DVIL, TVD, DACPD[2:0], FDP)
VID[7:0]	Version ID register
DID[7:0]	Device ID register
TSTP[1:0]	Enable/select test pattern generation (color bar, ramp)

• Input/Output Controls

XCM	XCLK 1X, 2X select
XCMD[3:0]	Delay adjust between XCLK and D[11:0]
MCP	XCLK polarity control
HPIE, HPIE2	Hot plug detect interrupt enable
HPIR	Hot plug detect interrupt reset
IDF[2:0]	Input data format
IBS	Input buffer select
DES	Decode embedded sync (TV-Out data only)
TERM[5:0]	Termination detect/check (DVIT, DACT2, DACT1, DACT0, SENSE)
BCOEN	Enable BCO Output
BCO[2:0]	Select output signal for BCO pin
BCOP	BCO polarity
GPIOL[1:0]	Read or write level for GPIO pins
GOENB[1:0]	Direction control for GPIO pins
SYNCO[1:0]	Enables/selects sync output for RGB and bypass modes
DACG[1:0]	DAC gain control
DACBP	DAC bypass
XOSC[2:0]	Crystal oscillator adjustments

• DVI Controls

TPPD[2:0]	DVI PLL phase detector trim
TPCP[1:0]	DVI PLL charge pump trim
TPVT[5:0]	DVI PLL VDD trim
TPVCO[10:0]	DVI PLL VCO trim
TPLPF[3:0]	DVI PLL low pass filter
DVID[3:0]	DVI transmitter drive strength
DVII	DVI output invert
CTL[3:0]	DVI control inputs

6.2 Registers Read/Write

Regarding the CH7301 registers read/write operation, please see applications note AN-41 for details.

Table 8. Serial Port Register Map

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1Ch						MCP		XCM
1Dh					XCMD3	XCMD2	XCMD1	XCMD0
1Eh	GOENB1	GOENB0	GPIOL1	GPIOL0	HPIR	HPIE		
1Fh	IBS	DES				IDF2	IDF1	IDF0
20h	HPIE2	XOSC2	DVIT		DACT2	DACT1	DACT0	SENSE
21h	XOSC1	XOSC0		SYNCO1	SYNCO0	DACG1	DACG0	DACBP
22h				BCOEN	BCOP	BCO2	BCO1	BCO0
31h	TPPD3	TPPD2	TPPD1	TPPD0	CTL3	CTL2	CTL1	CTL0
32h	TPVCO7	TPVCO6	TPVCO5	TPVCO4	TPVCO3	TPVCO2	TPVCO1	TPVCO0
33h	DVID2	DVID1	DVID0	DVII			TPCP1	TPCP0
35h			TPVT5	TPVT4	TPVT3	TPVT2	TPVT1	TPVT0
36h	TPLPF3	TPLPF2	TPLPF1	TPLPF0				
37h	TPVCO10	TPVCO9	TPVCO8					
48h				ResetIB	ResetDB		TSTP1	TSTP0
49h	DVIP	DVIL	TV		DACPD2	DACPD1	DACPD0	FPD
4Ah	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
4Bh	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0

All register bits not defined in the register map are reserved bits, and should be left at the default value.

Table 8 shows the CH7301 control register map. The details are described as follows:

Clock Mode Register

Symbol: **CM**
Address: **1Ch**
Bits: **2**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:					Reserved	MCP	Reserved	XCM
TYPE:					R/W	R/W	R/W	R/W
DEFAULT:					0	0	0	0

Bit 0 of register CM signifies the XCLK frequency. A value of '0' is used when the XCLK is at the pixel frequency (duel edge clocking mode) and a value of '1' is used when the XCLK is twice the pixel frequency (single edge clocking mode).

Bit 2 of register CM controls the phase of the XCLK clock input to the CH7301. A value of '1' inverts the XCLK signal at the input of the device. This control is used to select which edge of the XCLK signal to use for latching input data.

Input Clock Register

Symbol: **IC**
Address: **1Dh**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	XCMD3	XCMD2	XCMD1	XCMD0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	1	0	0	0

Bits 3-0 of register IC controls the delay applied to the XCLK signal before latching input data.

GPIO Control Register

Symbol: **GPIO**
Address: **1Eh**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	GOENB1	GOENB0	GPIOL1	GPIOL0	HPIR	HPIE	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	0	0	0	0	0	0

Bit 2 of register GPIO enables the hot plug interrupt detection signal to be output from the P-OUT pin. A value of '1' allows the hot plug detect circuit to pull the TLDET* pin low when a change of state has taken place on the hot plug detect pin. A value of '0' disables the interrupt signal.

Bit 3 of register GPIO resets the hot plug detection circuitry. A value of '1' causes the CH7301 to release the TLDET* pin. When a hot plug interrupt is asserted by the CH7301, the CH7301 driver should read register 20h to determine the state of the DVI termination. After having read this register, the HPIR bit should be set high to reset the circuitry, and then set low again.

Bits 5-4 of register GPIO control the GPIO pins. When the corresponding GOENB bits are low, these register values are driven out of the corresponding GPIO pins. When the corresponding GOENB bits are high, these register values can be read to determine the level forced into the corresponding GPIO pins.

Bits 7-6 of register GPIO control the direction of the GPIO pins. A value of '1' sets the corresponding GPIO pin to an input, and a value of '0' sets the corresponding pin to an output.

Input Data Format Register

Symbol: **IDF**
Address: **1Fh**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	IBS					IDF2	IDF1	IDF0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

Bits 2-0 of register IDF select the input data format. See Input Interface on section 5.2 on page 8 for a listing of available formats.

Bit 7 of register IDF selects the input buffer used for the data and clock input pins.

Connection Detect Register

Symbol: **CD**
Address: **20h**
Bits: **6**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HPIE2	Reserved	DVIT	Reserved	DACT2	DACT1	DACT0	SENSE
TYPE:	R/W	R/W	R	R	R	R	R	R/W
DEFAULT:	0	0	0	0	0	0	0	0

The Connection Detect Register provides a means to determine the status of the DAC outputs and the DVI hot plug detect pin. The status bits, DACT[2:0] correspond to the termination of the three DAC outputs. However, the values contained in these STATUS BITS ARE NOT VALID until a sensing procedure is performed. Use of this register requires a sequence of events to enable the sensing of outputs, then reading out the applicable status bits. The detection sequence works as follows:

1) Set the power management register to enable all DAC's.

2) Set the SENSE bit to a 1. This forces a constant output from the DAC's.

3) Reset the SENSE bit to 0. This triggers a comparison between the voltage present on these analog outputs and the reference value. During this step, each of the three status bits corresponding to individual DAC outputs will be set if they are CONNECTED.

4) Read the status bits. The status bits, DACT[2:0] now contain valid information which can be read to determine which outputs are connected to a display monitor. Again, a "1" indicates a valid connection, a "0" indicates an unconnected output.

Bit 5 of register CD can be read at any time to determine the level of the hot plug detect pin. When the hot plug detect pin changes state, and the DVI output is selected, the TLDET* output pin will be pulled low signifying a change in the DVI termination. At this point, the HPIR bit in register 1Eh should be set high, then low to reset the hot plug detect circuit.

Bit 7 of register CD enables the hot plug interrupt detection signal output from the GPIO[1] pin. A value of '1' allows the hot plug detect circuit to pull the GPIO[1] / TLDET* pin low when a change of state has taken place on the hot plug detect pin. A value of '0' disables the interrupt signal. The GOENB1 control bit in register 1Eh should be set to '1' when HPIE2 is set to '1'.

DAC Control Register

Symbol: **DC**
Address: **21h**
Bits: **6**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved		SYNCO1	SYNCO0	DACG1	DACG0	DACBP
TYPE:	R/W	R/W		R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0		0	0	0	0	0

Bit 0 of register DC selects the DAC bypass mode. A value of '1' outputs the incoming data directly at the DAC[2:0] outputs.

Bits 2-1 of register DC control the DAC gain. DACG1 should be low when the input data format is RGB (IDF = 0-3), and high when the input data format is YCrCb (IDF = 4).

Bits 4-3 of register DC select the signal to be output from the C/H Sync pin according to **Table 9** below.

Table 9. Composite / Horizontal Sync Output

SYNCO[1:0]	C/H Sync Output
00	No Output
01	VGA Horizontal Sync
10	Not Valid
11	Not Valid

Buffered Clock Output Register

Symbol: **BCO**
Address: **22h**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	BCOEN	BCOP	BCO2	BCO1	BCO0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

Bits 2-0 of register BCO select the signal output at the BCO pin, according to **Table 10** below:

Table 10. BCO Output Signal

BCO[2:0]	Buffered Clock Output	BCO[2:0]	Buffered Clock Output
000	Not Valid	100	Not Valid
001	Not Valid	101	Not Valid
010	Not Valid	110	VGA Vertical Sync
011	Not Valid	111	Not Valid

Bit 3 of register BCO selects the polarity of the BCO output. A value of '1' does not invert the signal at the output pad.

Bit 4 of register BCO enables the BCO output. When BCOEN is high, the BCO pin will output the selected signal. When BCOEN is low, the BCO pin will be held in tri-state mode.

Termination Register

Symbol: **TERM**
Address: **23h**
Bits: **1**

BIT	7	6	5	4	3	2	1	0
SYMBOL	Reserved	Reserved	Reserved	Reserved	Reserved	HPDD	Reserved	Reserved
TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

HPDD (bit 2) of register TERM disables the hardware hot plug detection function. This function (default on) tri-states the DVI outputs when the hot plug detect pin (HPDET) is pulled low in accordance with the DVI specification, revision 1.0. This function is independent of the hot plug interrupt function (HPIE, register 1Eh, bit 2 and HPIE2, register 20h, bit 7) controlled via the SPP interface.

HPDD = 0 => hardware hot plug interrupt is enabled
= 1 => hardware hot plug interrupt is disabled

DVI Control Input Register

Symbol: **TCTL**
Address: **31h**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	TPPD3	TPPD 2	TPPD 1	TPPD 0	CTL3	CTL2	CTL1	CTL0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

Bits 3-0 of register TCTL set the DVI control inputs applied to the green and red channels during sync intervals. It is recommended to leave these controls at the default value.

Bits 7-4 of register TCTL control the DVI PLL phase detector. The default value is recommended.

DVI PLL VCO Control Register

Symbol: **TVCO**
Address: **32h**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	TPVCO7	TPVCO6	TPVCO5	TPVCO4	TPVCO3	TPVCO2	TPVCO1	TPVCO0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	1	0	0	0	1	1

Register TVCO controls the state of the DVI PLL VCO, and should be set according to **Table 11**.

DVI PLL Charge Pump Control Register

Symbol: **TPCP**
Address: **33h**
Bits: **5**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	DVID2	DVID1	DVID0	DVII	Reserved	Reserved	TPCP1	TPCP0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	0	0	0

Bits 1-0 of register TPCP control the DVI PLL charge pump. The default value shown on **Table 11** is recommended.

Bits 3-2 of register TPCP are reserved bits, and should be left at the default value (see **Table 11**).

Bit 4 of register TPCP inverts the DVI outputs. A value of 1 inverts the outputs. The default value shown on **Table 11** is recommended.

Bits 7-5 of register TPCP control the DVI transmitter output drive level. The default value shown on **Table 11** is recommended.

DVI PLL Divider Register

Symbol: **TPD**
Address: **34h**
Bits: **6**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:		TPLLB	TPFFD1	TPFFD0	TPFBD3	TPFBD2	TPFBD1	TPFBD0
TYPE:		R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	0	1	1	0

Bits 3-0 of register TPD control the DVI PLL feedback divider. The default value is recommended.

Bits 5-4 of register TPD control the DVI PLL feed forward divider. The default value is recommended.

Bit 6 of register TPDC places the DVI PLL in a bypass mode. A value of '1' in this register places the PLL in bypass, and a value of '0' places the PLL in normal operating mode.

Please see **Table 11** for the default values in terms of the frequency ranges.

DVI PLL Supply Control Register

Symbol: **TPVT**
Address: **35h**
Bits: **5**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	TPVT5	TPVT4	TPVT3	TPVT2	TPVT1	TPVT0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	1	1	0	0	0	0

Bits 5-0 of register TPVT control the DVI PLL supply voltage. The default value is recommended.

Bits 7-6 of register TPVT are reserved bits, and should be left at the default value.

Please see **Table 11** for the default values in terms of the frequency ranges.

DVI PLL Filter Register

Symbol: **TPF**
Address: **36h**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	TPLPF3	TPLPF2	TPLPF1	TPLPF0	Reserved	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	1	0	0	0	0	0

Bits 3-0 of register TPT are reserved bits, and should be left at the default value.

Bits 7-4 of register TPT control the DVI PLL low pass filter. The default value is recommended.

Please see **Table 11** for the default values in terms of the frequency ranges.

Table 11. The Registers Default Settings In Terms Of The Frequency Ranges

Register		<= 65MHz	> 65MHz
31h	TCTL	00h	00h
32h	TVCO	23h	2Dh
33h	TPCP	08h	06h
34h	TPD	16h	26h
35h	TPVT	30h	30h
36h	TPF	60h	A0h
37h	TVCOO	00h	00h

DVI PLL VCO Control Overflow Register

Symbol: **TVCOO**
Address: **37h**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	TPVCO10	TPVCO9	TPVCO8	Reserved	Reserved	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

Bits 4-0 of register TCT are reserved bits, and should be left at the default value.

Bits 7-5 of register TCT contain the MSB values for the DVI PLL VCO control. This control is described in detail in the TVCO register description. The default value is recommended.

Test Pattern Register

Symbol: **TSTP**
Address: **48h**
Bits: **5**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:				ResetIB	ResetDB	RSA	TSTP1	TSTP0
TYPE:				R/W	R/W	R/W	R/W	R/W
DEFAULT:				1	1	0	0	0

Bits 1-0 of register TSTP control the test pattern generation block. This test pattern can be used for both the DVI output and the display monitor output. The pattern generated is determined by **Table 12** below.

Table 12. Test Pattern Control

TSTP[1:0]	Buffered Clock Output
00	No test pattern – Input data is used
01	Color Bars
1X	Horizontal Luminance Ramp

Bit 2 of register TSTP is a test control, and should be left at the default value.
Bit 3 of register TSTP controls the datapath reset signal. A value of '0' holds the datapath in a reset condition, while a value of '1', places the datapath in normal mode. The datapath is also reset at power on by an internally generated power on reset signal.
Bit 4 of register TSTP controls the serial port reset signal. A value of '0' holds the serial port registers in a reset condition, while a value of '1', places the serial port registers in normal mode. The serial port registers are also reset at power on by an internally generated power on reset signal.

Power Management Register

Symbol: **PM**
Address: **49h**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	DVIP	DVIL	Reserved	Reserved	DACPD2	DACPD1	DACPD0	FPD
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	1	0

Register PM controls which circuitry within the CH7301 is operating, according to **Table 13** below.

Table 13. Power Management

DVIP	**DVIL**	**TV**	**DACPD[2:0]**	**FPD**	**Operating State**	**Functional Description**
X	X	1	000	0	VGA to RGB Bypass On	All DACs on
X	X	0	XXX	0	VGA to RGB Bypass Off	All DACs off
1	1	X	XXX	0	DVI Encode, Serialize, Transmitter, and PLL on	DVI is in normal function
X	X	X	XXX	1	Full Power Down	All circuitry is powered down except serial port

Version ID Register

Symbol: **VID**
Address: **4Ah**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	1	0	0	1	0	1	0	1

Register VID is a read only register containing the version ID number of the CH7301.

Device ID Register

Symbol: **DID**
Address: **4Bh**
Bits: **8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	0	0	0	1	0	1	1	1

Register DID is a read only register containing the device ID number of the CH7301.

7. ELECTRICAL SPECIFICATIONS

Table 14. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	DVDD, AVDD, TVDD, VDD relative to GND	- 0.5		5.0	V
	Input voltage of all digital pins[1]	GND - 0.5		VDD + 0.5	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{AMB}	Ambient operating temperature	0		85	°C
TSTOR	Storage temperature	- 65		150	°C
T_J	Junction temperature			150	°C
TVPS	Vapor phase soldering (one minute)			220	°C

Notes:

1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can induce destructive latch.

Table 15. Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
VDD	DAC power supply voltage	3.1	3.3	3.6	V
AVDD	Analog supply voltage	3.1	3.3	3.6	V
DVDD, TVDD	Digital supply voltage	3.1	3.3	3.6	V
DVDDV	Digital supply voltage (P-OUT pin)	1.1	1.8	3.6	V
RL	Output load to DAC outputs		37.5		Ω

Table 16. Electrical Characteristics (Operating Conditions: T_A = 0°C - 70°C, VDD, AVDD, DVDD, TVDD = 3.3V ± 5%)

Symbol	Description	Min	Typ	Max	Units
	Video D/A resolution	10	10	10	Bits
	Full scale output current		33.89		mA
	Video level error			10	%
I_{VDD}	3 DAC's Enabled		100	110	mA
I_{AVDD}	DVI PLL Disabled		5	7	mA
I_{AVDD}	DVI PLL Enabled (85 MHz Pixel Clock)		17	22	mA
I_{DVDD}	TV-Out Enabled, DVI Disabled		85	150	mA
I_{DVDD}	TV-Out Disabled, DVI Enabled (85 MHz Pixel Clock)		50	70	mA
I_{TVDD}	Pixel Clock = 85 MHz		70	90	mA
	DVDDV (1.8V) current (15pF load)		4		mA

Table 17. Digital Inputs / Outputs

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{SPDOL}	SPD Output Low Voltage	IOL = 2.0 mA			0.4	V
V_{SPDIH}	SPD Input High Voltage		2.7		DVDD + 0.5	V
V_{SPDIL}	SPD Input Low Voltage		GND-0.5		1.4	V
V_{DATAIH}	D[0-11] Input High Voltage		Vref-0.25		DVDD+0.5	V
V_{DATAIL}	D[0-11] Input Low Voltage		GND-0.5		Vref+0.25	V
$V_{P-OUTOH}$	P-OUT Output High Voltage	IOL = - 400 µA	DVDDV-0.2			V
$V_{P-OUTOL}$	P-OUT Output Low Voltage	IOL = 3.2 mA			0.2	V

Note:

V_{SP} - refers to serial port pins SPD and SPC.
V_{DATA} - refers to all digital pixel and clock inputs.
V_{SPD} - refers to serial port data pin SPD as an output.
V_{P-OUT} - refers to pixel data output Time - Graphics.

8. REVISION HISTORY

Rev. #	Date	Section	Description
1.0	03/07/03	All	First official release of CH7301C datasheet, rev. 1.0

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ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH7301C-T	LQFP	64	3.3V

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