



## 24-BIT, 192-kHz SAMPLING, ADVANCED SEGMENT, AUDIO STEREO DIGITAL-TO-ANALOG CONVERTER

### FEATURES

- 24-Bit Resolution
- Analog Performance:
  - Dynamic Range: 123 dB
  - THD+N: 0.0005%
- Differential Current Output: 4 mA p-p
- 8× Oversampling Digital Filter:
  - Stop-Band Attenuation: –98 dB
  - Pass-Band Ripple: ±0.0002 dB
- Sampling Frequency: 10 kHz to 200 kHz
- System Clock: 128, 192, 256, 384, 512, or 768 f<sub>s</sub> With Autodetect
- Accepts 16-, 20-, and 24-Bit Audio Data
- PCM Data Formats: Standard, I<sup>2</sup>S, and Left-Justified
- DSD Format Interface Available
- Interface Available for Optional External Digital Filter or DSP
- TDMCA or Serial Port (SPI/I<sup>2</sup>C)
- User-Programmable Mode Controls:
  - Digital Attenuation: 0 dB to –120 dB, 0.5 dB/Step
  - Digital De-Emphasis
  - Digital Filter Rolloff: Sharp or Slow
  - Soft Mute
  - Zero Flag for Each Output
- Compatible With PCM1792 (Pins and Mode Controls)
- Dual Supply Operation:
  - 5-V Analog, 3.3-V Digital

- 5-V Tolerant Digital Inputs
- Small 28-Lead SSOP Package, Lead-Free Product

### APPLICATIONS

- A/V Receivers
- SACD Players
- DVD Players
- HDTV Receivers
- Car Audio Systems
- Digital Multitrack Recorders
- Other Applications Requiring 24-Bit Audio

### DESCRIPTION

The PCM1796 is a monolithic CMOS integrated circuit that includes stereo digital-to-analog converters and support circuitry in a small 28-lead SSOP package. The data converters use TI's advanced segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1796 provides balanced current outputs, allowing the user to optimize analog performance externally. The PCM1796 accepts PCM and DSD audio data formats, providing easy interfacing to audio DSP and decoder chips. The PCM1796 also interfaces with external digital filter devices (DF1704, DF1706, PMD200). Sampling rates up to 200 kHz are supported. A full set of user-programmable functions is accessible through an SPI or I<sup>2</sup>C serial control port, which supports register write and readback functions. The PCM1796 also supports the time division multiplexed command and audio (TDMCA) data format.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## ORDERING INFORMATION

| PRODUCT   | PACKAGE      | PACKAGE CODE | OPERATION TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA |
|-----------|--------------|--------------|-----------------------------|-----------------|-----------------|-----------------|
| PCM1796DB | 28-lead SSOP | 28DB         | -25°C to 85°C               | PCM1796         | PCM1796DB       | Tube            |
|           |              |              |                             |                 | PCM1796DBR      | Tape and reel   |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted<sup>(1)</sup>

|  |  | PCM1796                                     |
|--|--|---|
| Supply voltage   | V <sub>CC1</sub> , V <sub>CC2L</sub> , V <sub>CC2R</sub>   | -0.3 V to 6.5 V                             |
|  | V <sub>DD</sub>  | -0.3 V to 4 V                               |
| Supply voltage differences: V <sub>CC1</sub> , V <sub>CC2L</sub> , V <sub>CC2R</sub> |  | ±0.1 V                                      |
| Ground voltage differences: AGND1, AGND2, AGND3L, AGND3R, DGND                       |  | ±0.1 V                                      |
| Digital input voltage  | LRCK, DATA, BCK, SCK, MSEL, <u>RST</u> , MS <sup>(2)</sup> , MDI, MC, MDO <sup>(2)</sup> , ZEROL <sup>(2)</sup> , ZEROR <sup>(2)</sup> | -0.3 V to 6.5 V                             |
|  | ZEROL <sup>(3)</sup> , ZEROR <sup>(3)</sup> , MDO <sup>(3)</sup> , MS <sup>(3)</sup>   | -0.3 V to (V <sub>DD</sub> + 0.3 V) < 4 V   |
| Analog input voltage   |  | -0.3 V to (V <sub>CC</sub> + 0.3 V) < 6.5 V |
| Input current (any pins except supplies)   |  | ±10 mA                                      |
| Ambient temperature under bias   |  | -40°C to 125°C                              |
| Storage temperature  |  | -55°C to 150°C                              |
| Junction temperature   |  | 150°C                                       |
| Lead temperature (soldering)   |  | 260°C, 5 s                                  |
| Package temperature (IR reflow, peak)  |  | 260°C                                       |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input mode or I<sup>2</sup>C mode

(3) Output mode except for I<sup>2</sup>C mode

## ELECTRICAL CHARACTERISTICS

all specifications at T<sub>A</sub> = 25°C, V<sub>CC1</sub> = V<sub>CC2L</sub> = V<sub>CC2R</sub> = 5 V, V<sub>DD</sub> = 3.3 V, f<sub>S</sub> = 44.1 kHz, system clock = 256 f<sub>S</sub>, and 24-bit data unless otherwise noted

| PARAMETER                         | TEST CONDITIONS | PCM1796DB                                   |        |         | UNIT |
|-----------------------------------|-----------------|---|--------|---------|------|
|                                   |                 | MIN   | TYP    | MAX     |      |
| <b>RESOLUTION</b>                 |                 |   | 24     |         | Bits |
| <b>DATA FORMAT (PCM Mode)</b>     |                 |   |        |         |      |
| Audio data interface format       |                 | Standard, I <sup>2</sup> S, left-justified  |        |         |      |
| Audio data bit length             |                 | 16-, 20-, 24-bit selectable                 |        |         |      |
| Audio data format                 |                 | MSB first, twos complement                  |        |         |      |
| f <sub>S</sub> Sampling frequency |                 | 10  |        | 200     | kHz  |
| System clock frequency            |                 | 128, 192, 256, 384, 512, 768 f <sub>S</sub> |        |         |      |
| <b>DATA FORMAT (DSD Mode)</b>     |                 |   |        |         |      |
| Audio data interface format       |                 | DSD (direct stream digital)                 |        |         |      |
| Audio data bit length             |                 | 1 Bit                                       |        |         |      |
| f <sub>S</sub> Sampling frequency |                 |   | 2.8224 |         | MHz  |
| System clock frequency            |                 | 2.8224                                      |        | 11.2896 | MHz  |

**ELECTRICAL CHARACTERISTICS (Continued)**

all specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{CC1} = V_{CC2L} = V_{CC2R} = 5\text{ V}$ ,  $V_{DD} = 3.3\text{ V}$ ,  $f_S = 44.1\text{ kHz}$ , system clock =  $256 f_S$ , and 24-bit data unless otherwise noted

| PARAMETER  | TEST CONDITIONS                           | PCM1796DB               |     |         | UNIT          |
|--|---|-------------------------|-----|---------|---------------|
|  |   | MIN                     | TYP | MAX     |               |
| <b>DIGITAL INPUT/OUTPUT</b>                      |   |                         |     |         |               |
| Logic family                                     |   | TTL compatible          |     |         |               |
| $V_{IH}$<br>$V_{IL}$                             | Input logic level                         | 2                       |     |         | VDC           |
|  |   | 0.8                     |     |         |               |
| $I_{IH}$<br>$I_{IL}$                             | Input logic current                       | $V_{IN} = V_{DD}$       | 10  |         | $\mu\text{A}$ |
|  |   | $V_{IN} = 0\text{ V}$   | -10 |         |               |
| $V_{OH}$<br>$V_{OL}$                             | Output logic level                        | $I_{OH} = -2\text{ mA}$ | 2.4 |         | VDC           |
|  |   | $I_{OL} = 2\text{ mA}$  | 0.4 |         |               |
| <b>DYNAMIC PERFORMANCE (PCM MODE) (1)(2)</b>     |   |                         |     |         |               |
| THD+N at $V_{OUT} = 0\text{ dB}$                 | $f_S = 44.1\text{ kHz}$                   | 0.0005%                 |     | 0.001%  |               |
|  | $f_S = 96\text{ kHz}$                     | 0.001%                  |     |         |               |
|  | $f_S = 192\text{ kHz}$                    | 0.0015%                 |     |         |               |
| Dynamic range                                    | EIAJ, A-weighted, $f_S = 44.1\text{ kHz}$ | 120                     | 123 |         | dB            |
|  | EIAJ, A-weighted, $f_S = 96\text{ kHz}$   | 123                     |     |         |               |
|  | EIAJ, A-weighted, $f_S = 192\text{ kHz}$  | 123                     |     |         |               |
| Signal-to-noise ratio                            | EIAJ, A-weighted, $f_S = 44.1\text{ kHz}$ | 120                     | 123 |         | dB            |
|  | EIAJ, A-weighted, $f_S = 96\text{ kHz}$   | 123                     |     |         |               |
|  | EIAJ, A-weighted, $f_S = 192\text{ kHz}$  | 123                     |     |         |               |
| Channel separation                               | $f_S = 44.1\text{ kHz}$                   | 116                     | 119 |         | dB            |
|  | $f_S = 96\text{ kHz}$                     | 118                     |     |         |               |
|  | $f_S = 192\text{ kHz}$                    | 117                     |     |         |               |
| Level Linearity Error                            | $V_{OUT} = -120\text{ dB}$                |                         |     | $\pm 1$ | dB            |
| <b>DYNAMIC PERFORMANCE (MONO MODE) (1)(2)(3)</b> |   |                         |     |         |               |
| THD+N at $V_{OUT} = 0\text{ dB}$                 | $f_S = 44.1\text{ kHz}$                   | 0.0005%                 |     |         |               |
|  | $f_S = 96\text{ kHz}$                     | 0.001%                  |     |         |               |
|  | $f_S = 192\text{ kHz}$                    | 0.0015%                 |     |         |               |
| Dynamic range                                    | EIAJ, A-weighted, $f_S = 44.1\text{ kHz}$ | 126                     |     |         | dB            |
|  | EIAJ, A-weighted, $f_S = 96\text{ kHz}$   | 126                     |     |         |               |
|  | EIAJ, A-weighted, $f_S = 192\text{ kHz}$  | 126                     |     |         |               |
| Signal-to-noise ratio                            | EIAJ, A-weighted, $f_S = 44.1\text{ kHz}$ | 126                     |     |         | dB            |
|  | EIAJ, A-weighted, $f_S = 96\text{ kHz}$   | 126                     |     |         |               |
|  | EIAJ, A-weighted, $f_S = 192\text{ kHz}$  | 126                     |     |         |               |

(1) Filter condition:

THD+N: 20-Hz HPF, 20-kHz AES17 LPF

Dynamic range: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted

Signal-to-noise ratio: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted

Channel separation: 20-Hz HPF, 20-kHz AES17 LPF

Analog performance specifications are measured using the System Two™ Cascade audio measurement system by Audio Precision™ in the averaging mode.

(2) Dynamic performance and dc accuracy are specified at the output of the postamplifier as shown in Figure 36.

(3) Dynamic performance and dc accuracy are specified at the output of the measurement circuit as shown in Figure 38.

**ELECTRICAL CHARACTERISTICS (Continued)**

all specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{CC1} = V_{CC2L} = V_{CC2R} = 5\text{ V}$ ,  $V_{DD} = 3.3\text{ V}$ ,  $f_S = 44.1\text{ kHz}$ , system clock =  $256 f_S$ , and 24-bit data unless otherwise noted

| PARAMETER  | TEST CONDITIONS                  | PCM1796DB            |      |     | UNIT     |
|--|----------------------------------|----------------------|------|-----|----------|
|  |                                  | MIN                  | TYP  | MAX |          |
| <b>DSD MODE DYNAMIC PERFORMANCE (1) (2) (44.1 KHZ, 64 f<sub>S</sub>)</b> |                                  |                      |      |     |          |
| THD+N at FS  | 2 V rms                          | 0.0007%              |      |     |          |
| Dynamic range  | -60 dB, EIAJ, A-weighted         | 122                  |      |     | dB       |
| Signal-to-noise ratio  | EIAJ, A-weighted                 | 122                  |      |     | dB       |
| <b>ANALOG OUTPUT</b>   |                                  |                      |      |     |          |
| Gain error   |                                  | -7                   | ±2   | 7   | % of FSR |
| Gain mismatch, channel-to-channel  |                                  | -3                   | ±0.5 | 3   | % of FSR |
| Bipolar zero error   | At BPZ                           | -2                   | ±0.5 | 2   | % of FSR |
| Output current   | Full scale (0 dB)                | 4                    |      |     | mA p-p   |
| Center current   | At BPZ                           | -3.5                 |      |     | mA       |
| <b>DIGITAL FILTER PERFORMANCE</b>  |                                  |                      |      |     |          |
| De-emphasis error  |                                  | ±0.1                 |      |     | dB       |
| <b>FILTER CHARACTERISTICS-1: SHARP ROLLOFF</b>                           |                                  |                      |      |     |          |
| Pass band  | ±0.0002 dB                       | 0.454 f <sub>S</sub> |      |     |          |
|  | -3 dB                            | 0.49 f <sub>S</sub>  |      |     |          |
| Stop band  |                                  | 0.546 f <sub>S</sub> |      |     |          |
| Pass-band ripple   |                                  | ±0.0002              |      |     | dB       |
| Stop-band attenuation  | Stop band = 0.546 f <sub>S</sub> | -98                  |      |     | dB       |
| Delay time   |                                  | 38/f <sub>S</sub>    |      |     | s        |
| <b>FILTER CHARACTERISTICS-2: SLOW ROLLOFF</b>                            |                                  |                      |      |     |          |
| Pass band  | ±0.001 dB                        | 0.21 f <sub>S</sub>  |      |     |          |
|  | -3 dB                            | 0.448 f <sub>S</sub> |      |     |          |
| Stop band  |                                  | 0.79 f <sub>S</sub>  |      |     |          |
| Pass-band ripple   |                                  | ±0.001               |      |     | dB       |
| Stop-band attenuation  | Stop band = 0.732 f <sub>S</sub> | -80                  |      |     | dB       |
| Delay time   |                                  | 38/f <sub>S</sub>    |      |     | s        |

(1) Filter condition:

THD+N: 20-Hz HPF, 20-kHz AES17 LPF

Dynamic range: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted

Signal-to-noise ratio: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted

Channel separation: 20-Hz HPF, 20-kHz AES17 LPF

Analog performance specifications are measured using the System Two Cascade audio measurement system by Audio Precision in the averaging mode.

(2) Dynamic performance and dc accuracy are specified at the output of the postamplifier as shown in Figure 37.

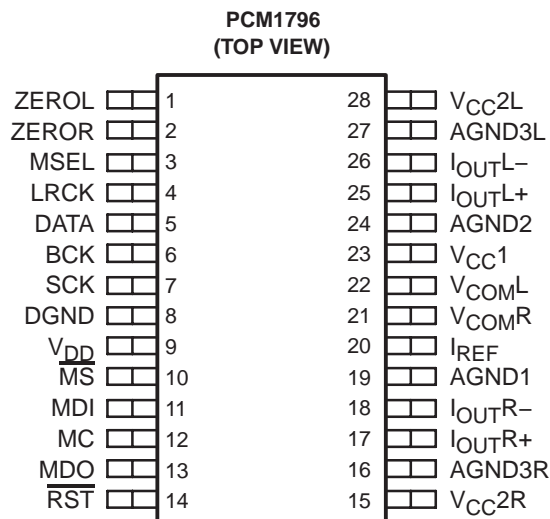
## ELECTRICAL CHARACTERISTICS (Continued)

all specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{CC1} = V_{CC2L} = V_{CC2R} = 5\text{ V}$ ,  $V_{DD} = 3.3\text{ V}$ ,  $f_S = 44.1\text{ kHz}$ , system clock =  $256 f_S$ , and 24-bit data unless otherwise noted

| PARAMETER                        | TEST CONDITIONS    | PCM1796DB               |     |      | UNIT               |
|----------------------------------|--------------------|-------------------------|-----|------|--------------------|
|                                  |                    | MIN                     | TYP | MAX  |                    |
| <b>POWER SUPPLY REQUIREMENTS</b> |                    |                         |     |      |                    |
| $V_{DD}$                         |                    | 3                       | 3.3 | 3.6  | VDC                |
| $V_{CC1}$                        | Voltage range      | 4.75                    | 5   | 5.25 | VDC                |
| $V_{CC2L}$                       |                    |                         |     |      |                    |
| $V_{CC2R}$                       |                    |                         |     |      |                    |
| $I_{DD}$                         | Supply current (1) | $f_S = 44.1\text{ kHz}$ | 7   | 9    | mA                 |
|                                  |                    | $f_S = 96\text{ kHz}$   | 13  |      |                    |
|                                  |                    | $f_S = 192\text{ kHz}$  | 25  |      |                    |
| $I_{CC}$                         | Supply current (1) | $f_S = 44.1\text{ kHz}$ | 18  | 23   | mA                 |
|                                  |                    | $f_S = 96\text{ kHz}$   | 19  |      |                    |
|                                  |                    | $f_S = 192\text{ kHz}$  | 20  |      |                    |
| Power dissipation (1)            |                    | $f_S = 44.1\text{ kHz}$ | 115 | 150  | mW                 |
|                                  |                    | $f_S = 96\text{ kHz}$   | 140 |      |                    |
|                                  |                    | $f_S = 192\text{ kHz}$  | 180 |      |                    |
| <b>TEMPERATURE RANGE</b>         |                    |                         |     |      |                    |
| Operation temperature            |                    | -25                     |     | 85   | $^\circ\text{C}$   |
| $\theta_{JA}$ Thermal resistance | 28-pin SSOP        |                         | 100 |      | $^\circ\text{C/W}$ |

(1) Input is BPZ data.

## PIN ASSIGNMENTS



## Terminal Functions

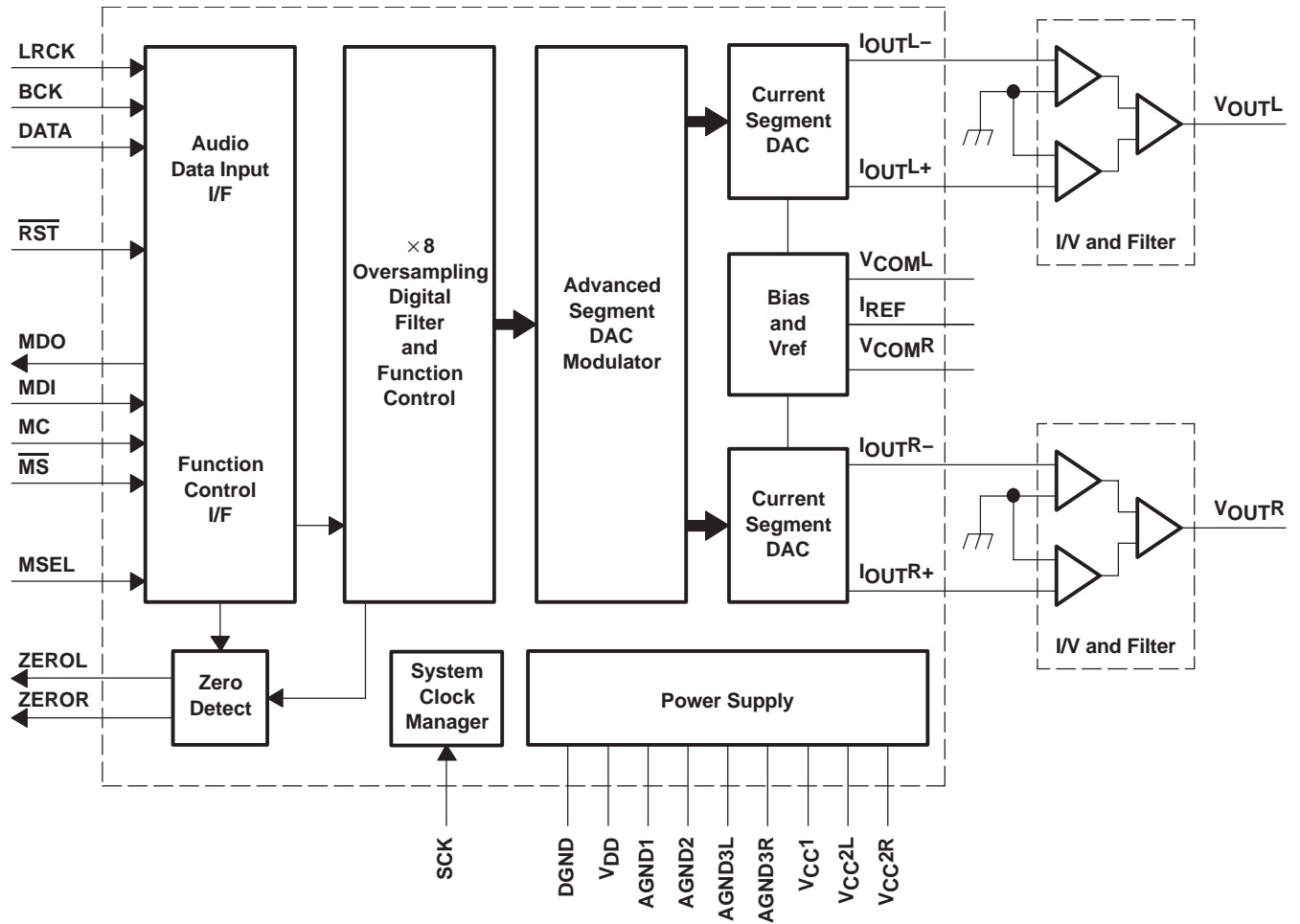
| TERMINAL<br>NAME   | PIN | I/O | DESCRIPTIONS  |
|--------------------|-----|-----|---|
| AGND1              | 19  | –   | Analog ground (internal bias)                               |
| AGND2              | 24  | –   | Analog ground (internal bias)                               |
| AGND3L             | 27  | –   | Analog ground (L-channel DACFF)                             |
| AGND3R             | 16  | –   | Analog ground (R-channel DACFF)                             |
| BCK                | 6   | I   | Bit clock input <sup>(1)</sup>                              |
| DATA               | 5   | I   | Serial audio data input <sup>(1)</sup>                      |
| DGND               | 8   | –   | Digital ground  |
| I <sub>OUTL+</sub> | 25  | O   | L-channel analog current output+                            |
| I <sub>OUTL-</sub> | 26  | O   | L-channel analog current output–                            |
| I <sub>OUTR+</sub> | 17  | O   | R-channel analog current output+                            |
| I <sub>OUTR-</sub> | 18  | O   | R-channel analog current output–                            |
| I <sub>REF</sub>   | 20  | –   | Output current reference bias pin                           |
| LRCK               | 4   | I   | Left and right clock (f <sub>S</sub> ) input <sup>(1)</sup> |
| MC                 | 12  | I   | Mode control clock input <sup>(1)</sup>                     |
| MDI                | 11  | I   | Mode control data input <sup>(1)</sup>                      |
| MDO                | 13  | I/O | Mode control readback data output <sup>(3)</sup>            |
| $\overline{MS}$    | 10  | I/O | Mode control chip-select input <sup>(2)</sup>               |
| MSEL               | 3   | I   | I <sup>2</sup> C/SPI select <sup>(1)</sup>                  |
| $\overline{RST}$   | 14  | I   | Reset <sup>(1)</sup>  |
| SCK                | 7   | I   | System clock input <sup>(1)</sup>                           |
| V <sub>CC1</sub>   | 23  | –   | Analog power supply, 5 V                                    |
| V <sub>CC2L</sub>  | 28  | –   | Analog power supply (L-channel DACFF), 5 V                  |
| V <sub>CC2R</sub>  | 15  | –   | Analog power supply (R-channel DACFF), 5 V                  |
| V <sub>COML</sub>  | 22  | –   | L-channel internal bias decoupling pin                      |
| V <sub>COMR</sub>  | 21  | –   | R-channel internal bias decoupling pin                      |
| V <sub>DD</sub>    | 9   | –   | Digital power supply, 3.3 V                                 |
| ZEROL              | 1   | I/O | Zero flag for L-channel <sup>(2)</sup>                      |
| ZEROR              | 2   | I/O | Zero flag for R-channel <sup>(2)</sup>                      |

<sup>(1)</sup> Schmitt-trigger input, 5-V tolerant

<sup>(2)</sup> Schmitt-trigger input and output. 5-V tolerant input and CMOS output

<sup>(3)</sup> Schmitt-trigger input and output. 5-V tolerant input. In I<sup>2</sup>C mode, this pin becomes an open-drain 3-state output; otherwise, this pin is a CMOS output.

**FUNCTIONAL BLOCK DIAGRAM**



TYPICAL PERFORMANCE CURVES

DIGITAL FILTER

Digital Filter Response

AMPLITUDE  
vs  
FREQUENCY

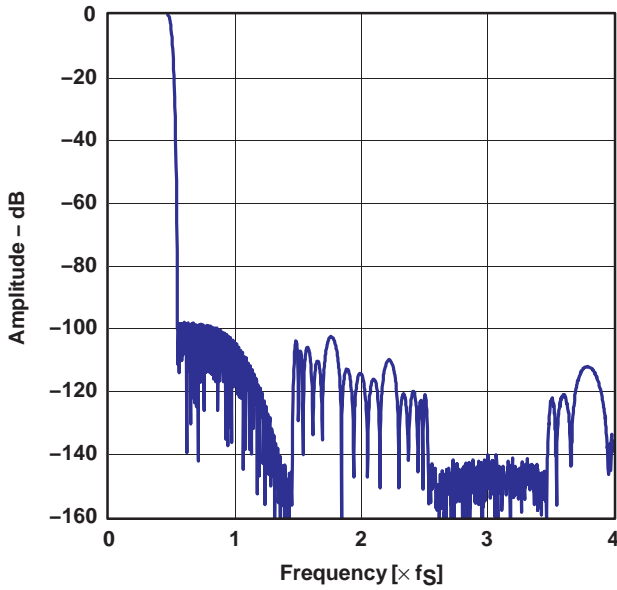


Figure 1. Frequency Response, Sharp Rolloff

AMPLITUDE  
vs  
FREQUENCY

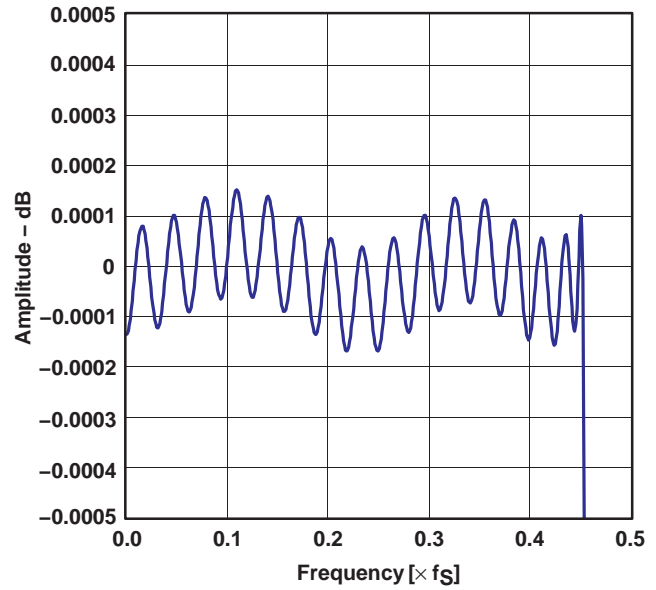


Figure 2. Pass-Band Ripple, Sharp Rolloff

AMPLITUDE  
vs  
FREQUENCY

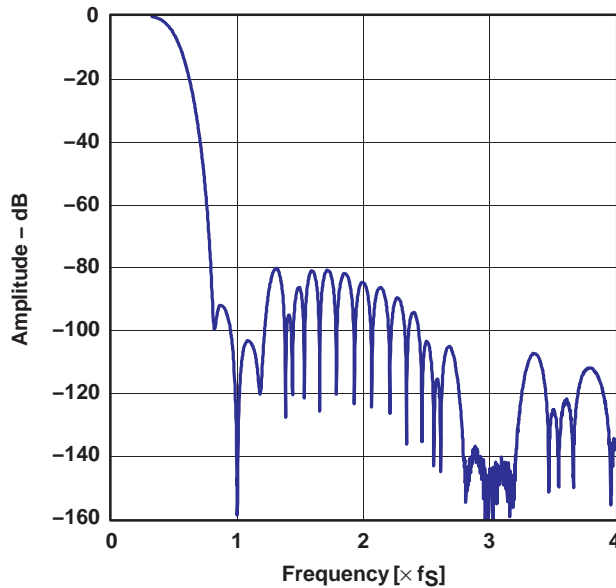


Figure 3. Frequency Response, Slow Rolloff

AMPLITUDE  
vs  
FREQUENCY

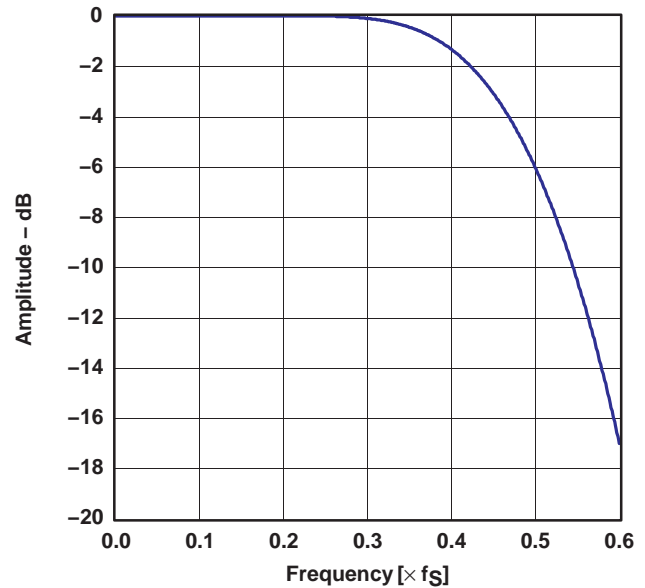


Figure 4. Transition Characteristics, Slow Rolloff



De-Emphasis Filter

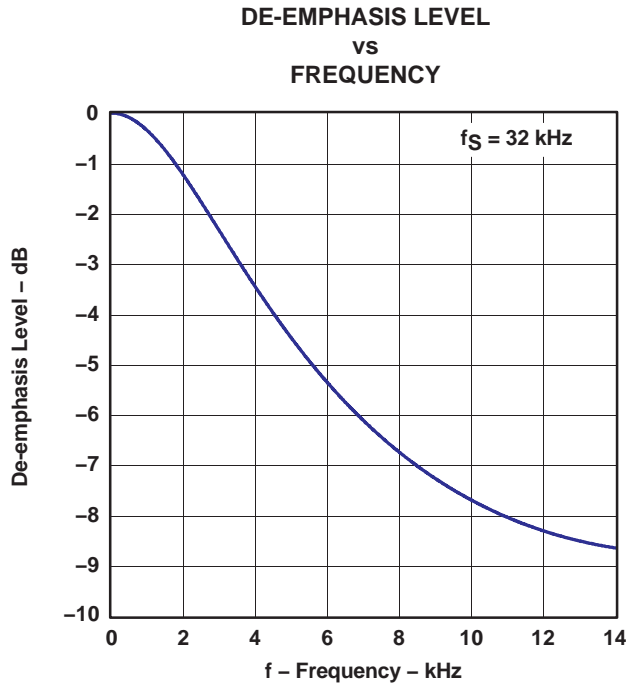


Figure 5

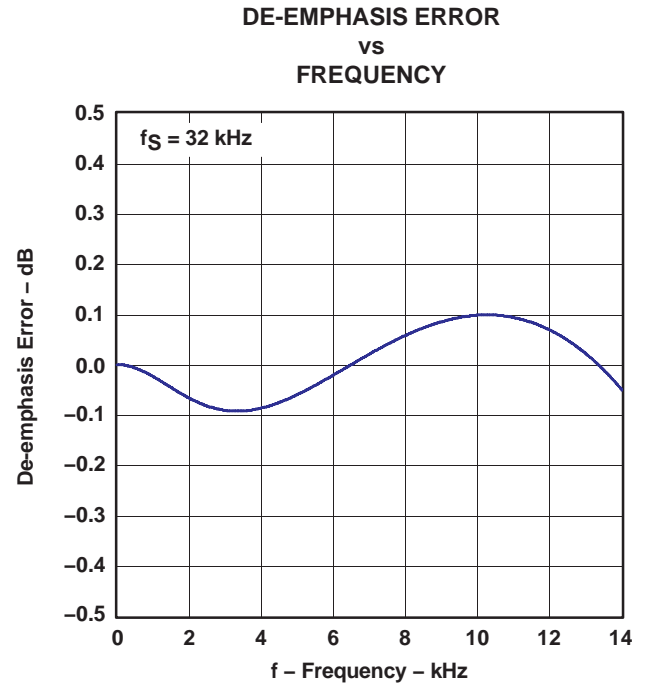


Figure 6

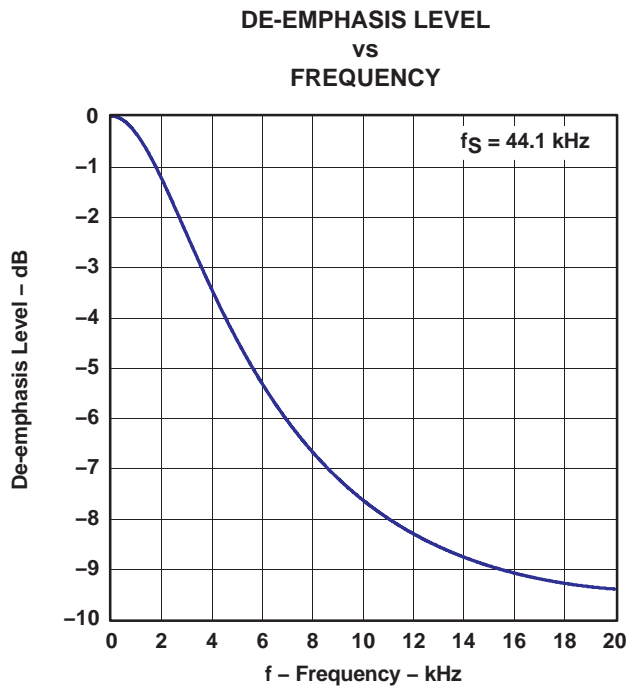


Figure 7

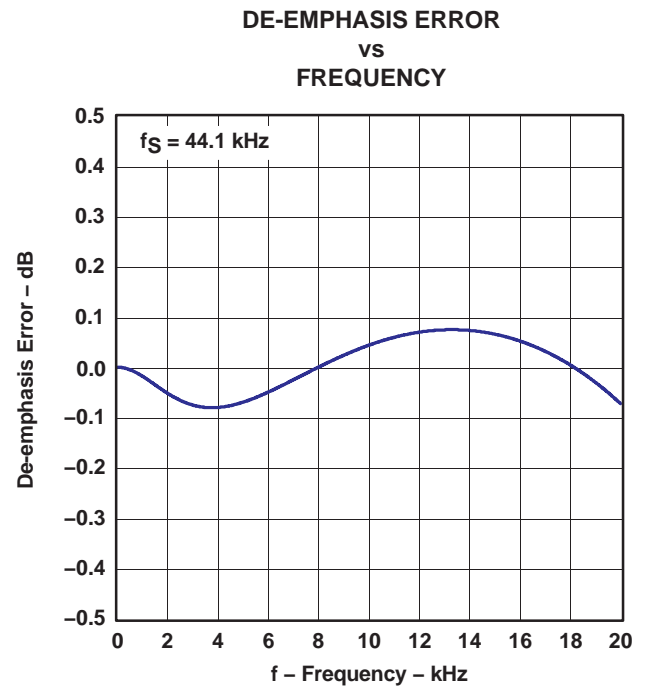


Figure 8

De-Emphasis Filter (Continued)

DE-EMPHASIS LEVEL  
VS  
FREQUENCY

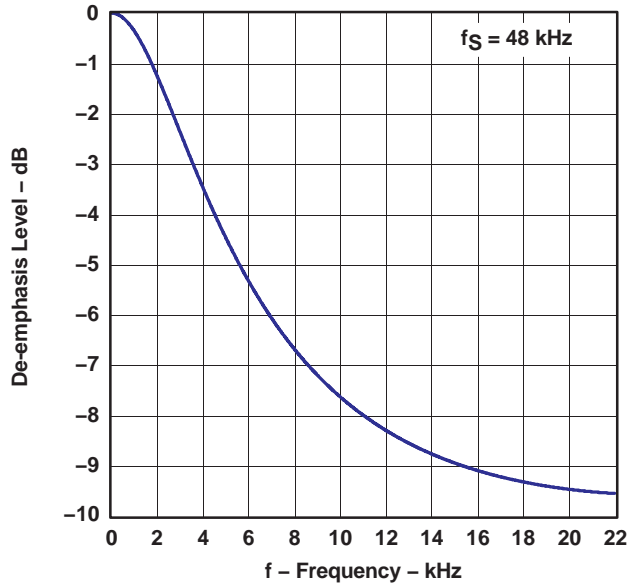


Figure 9

DE-EMPHASIS ERROR  
VS  
FREQUENCY

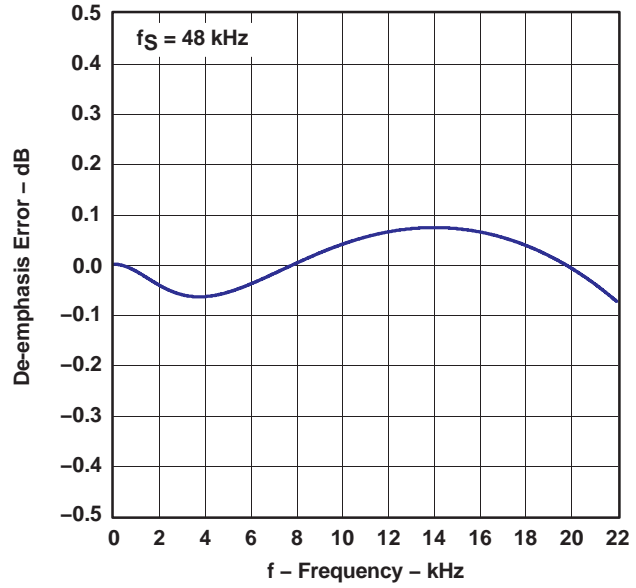


Figure 10

## ANALOG DYNAMIC PERFORMANCE

### Supply Voltage Characteristics

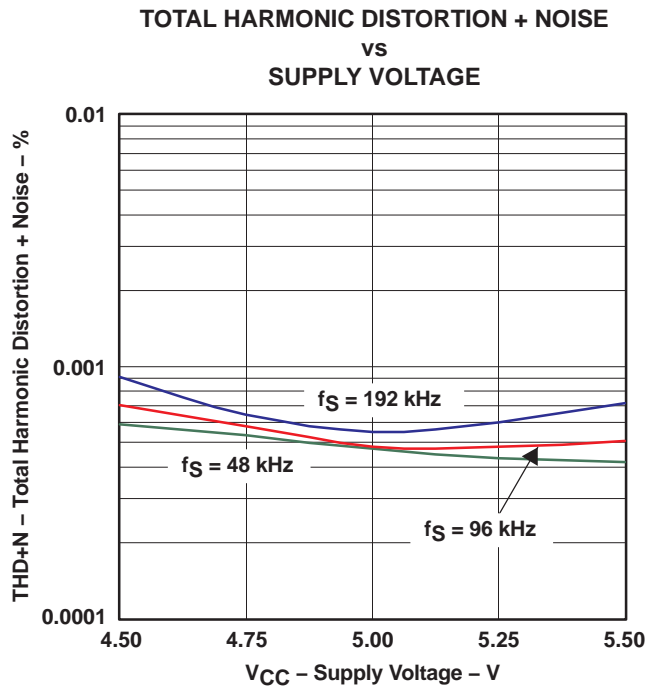


Figure 11

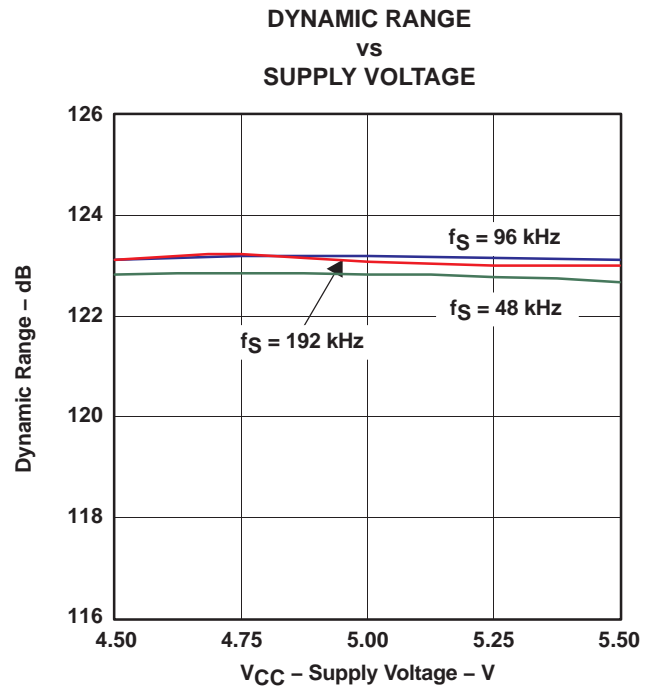


Figure 12

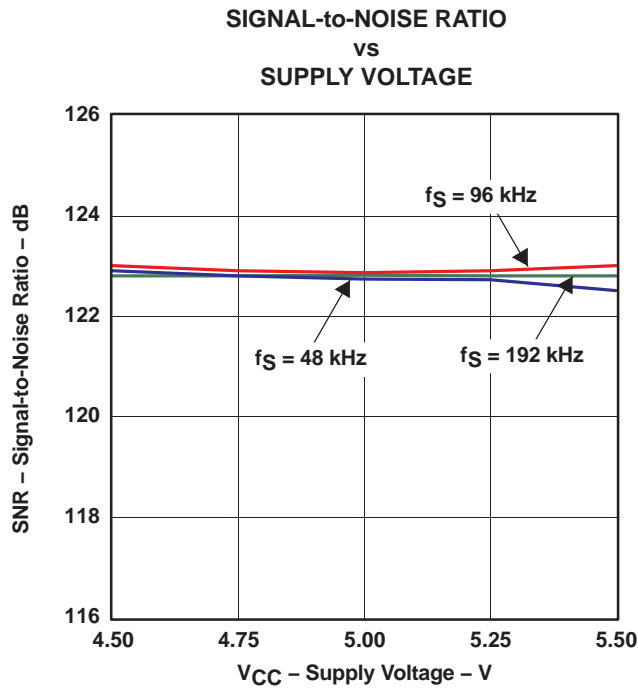


Figure 13

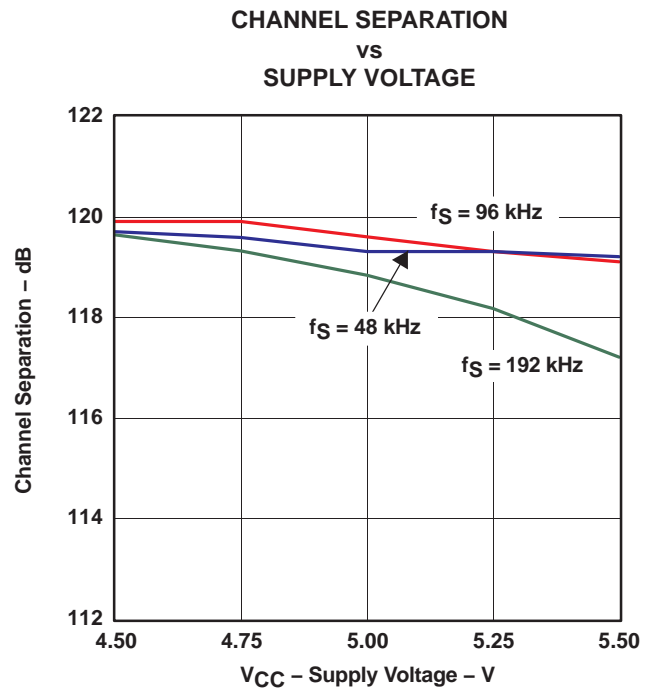


Figure 14

NOTE: PCM mode, T<sub>A</sub> = 25°C, V<sub>DD</sub> = 3.3 V, measurement circuit is Figure 36.

Temperature Characteristics

TOTAL HARMONIC DISTORTION + NOISE  
vs  
FREE-AIR TEMPERATURE

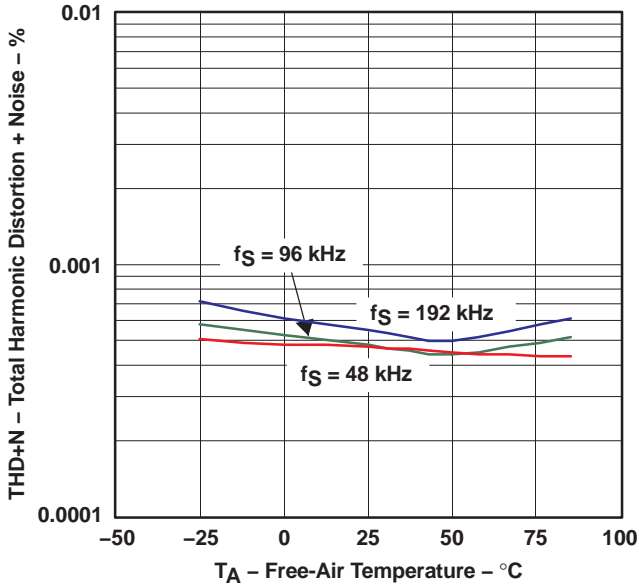


Figure 15

DYNAMIC RANGE  
vs  
FREE-AIR TEMPERATURE

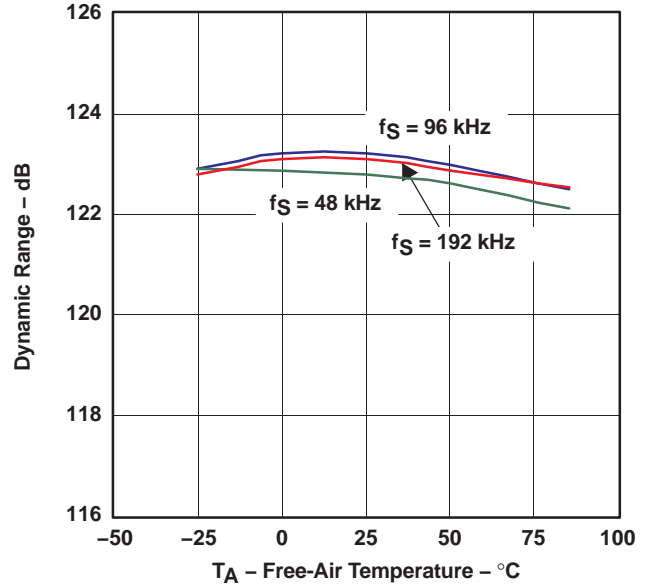


Figure 16

SIGNAL-to-NOISE RATIO  
vs  
FREE-AIR TEMPERATURE

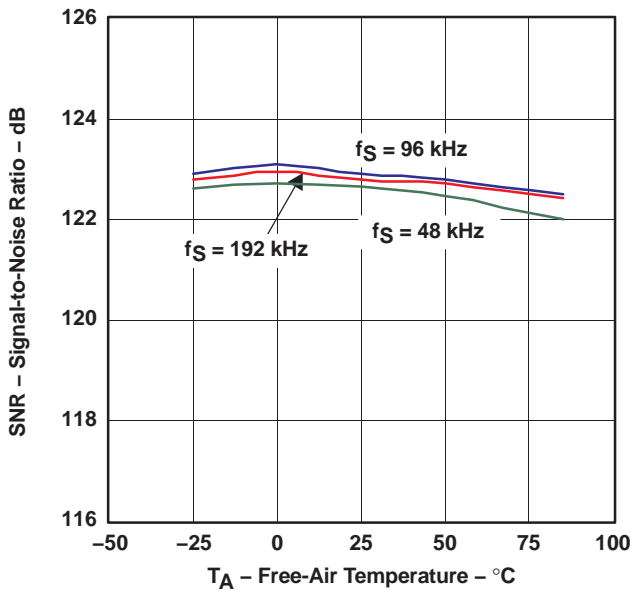


Figure 17

CHANNEL SEPARATION  
vs  
FREE-AIR TEMPERATURE

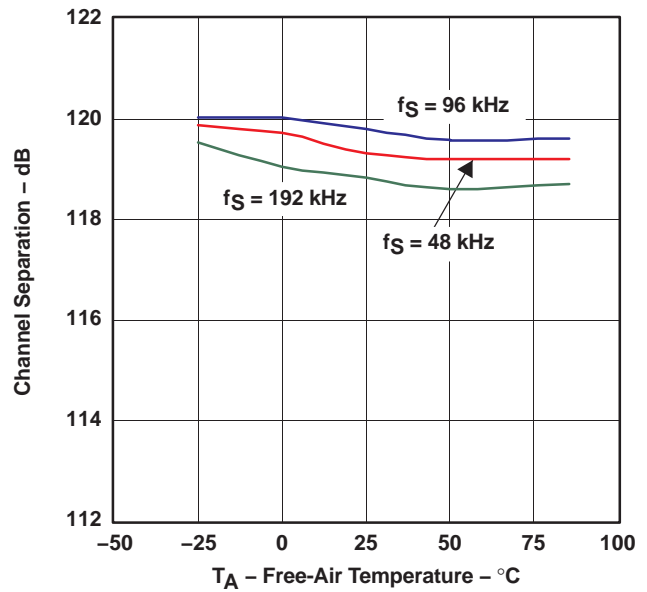
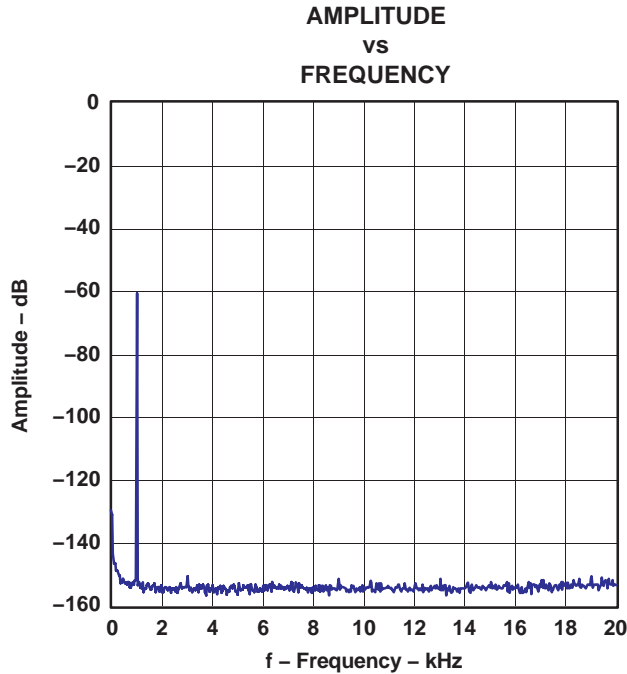


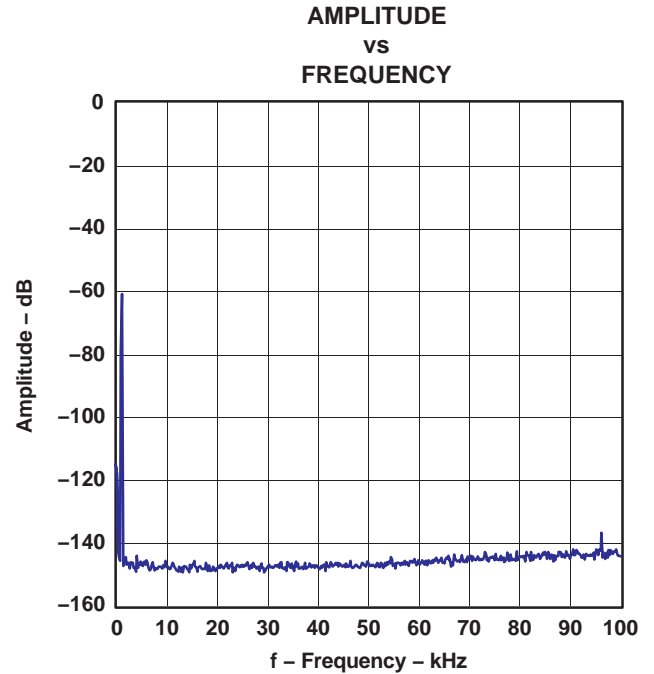
Figure 18

NOTE: PCM mode,  $V_{DD} = 3.3\text{ V}$ ,  $V_{CC} = 5\text{ V}$ , measurement circuit is Figure 36.



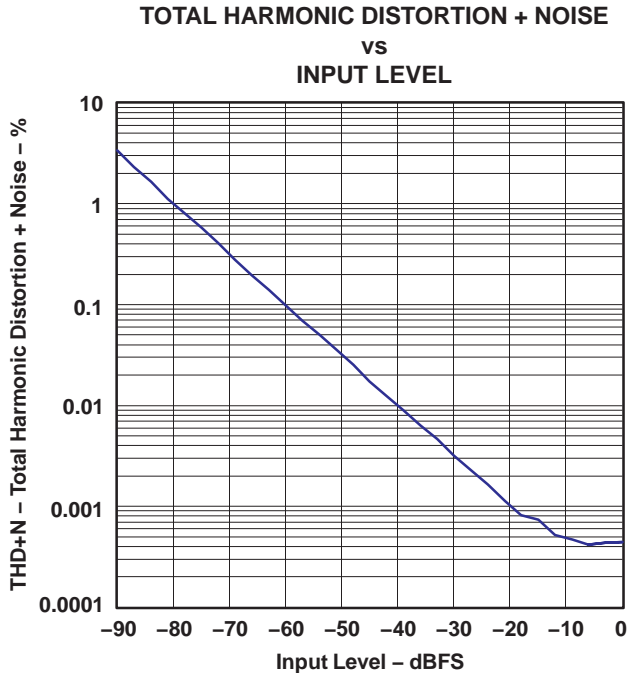
NOTE: PCM mode,  $f_S = 48$  kHz, 32768 point 8 average,  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3$  V  $V_{CC} = 5$  V, measurement circuit is Figure 36.

Figure 19. -60-dB Output Spectrum, BW = 20 kHz



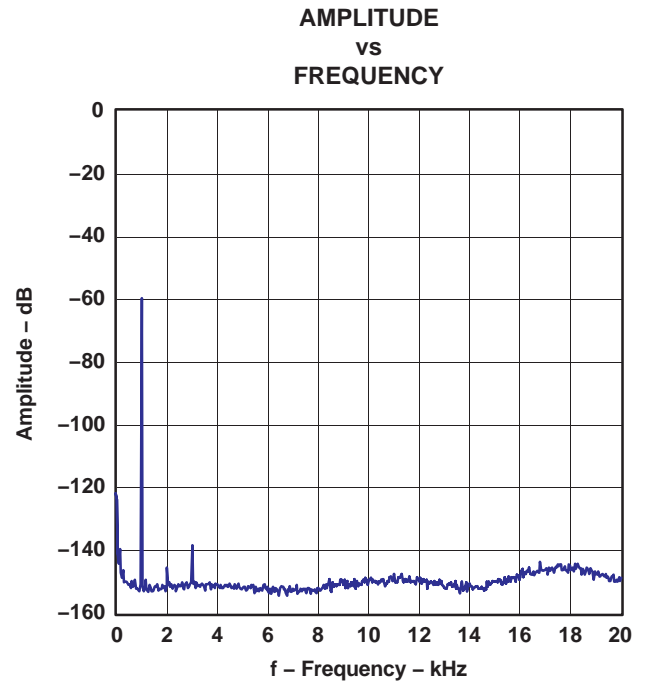
NOTE: PCM mode,  $f_S = 96$  kHz, 32768 point 8 average,  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3$  V  $V_{CC} = 5$  V, measurement circuit is Figure 36.

Figure 20. -60-dB Output Spectrum, BW = 100 kHz



NOTE: PCM mode,  $f_S = 48$  kHz,  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3$  V,  $V_{CC} = 5$  V, measurement circuit is Figure 36.

Figure 21. THD+N vs Input Level, PCM Mode



NOTE: DSD mode (FIR-2), 32768 point 8 average,  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3$  V,  $V_{CC} = 5$  V, measurement circuit is Figure 37.

Figure 22. -60-dB Output Spectrum, DSD Mode

## SYSTEM CLOCK AND RESET FUNCTIONS

### System Clock Input

The PCM1796 requires a system clock for operating the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the SCK input (pin 7). The PCM1796 has a system clock detection circuit that automatically senses the frequency at which the system clock is operating. Table 1 shows examples of system clock frequencies for common audio sampling rates. If the oversampling rate of the delta-sigma modulator is selected as  $128 f_S$ , the system clock frequency is required to be over  $256 f_S$ .

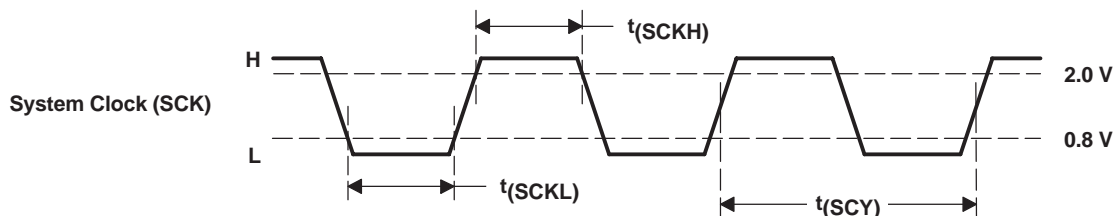
Figure 23 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. One of the Texas Instruments PLL1700 family of multiclock generators is an excellent choice for providing the PCM1796 system clock.

**Table 1. System Clock Rates for Common Audio Sampling Frequencies**

| SAMPLING FREQUENCY | SYSTEM CLOCK FREQUENCY ( $f_{SCK}$ ) (MHz) |                      |                       |                       |                       |                       |
|--------------------|--|----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
|                    | 128 $f_S$                                  | 192 $f_S$            | 256 $f_S$             | 384 $f_S$             | 512 $f_S$             | 768 $f_S$             |
| 32 kHz             | 4.096 <sup>(1)</sup>                       | 6.144 <sup>(1)</sup> | 8.192                 | 12.288                | 16.384                | 24.576                |
| 44.1 kHz           | 5.6488 <sup>(1)</sup>                      | 8.4672               | 11.2896               | 16.9344               | 22.5792               | 33.8688               |
| 48 kHz             | 6.144 <sup>(1)</sup>                       | 9.216                | 12.288                | 18.432                | 24.576                | 36.864                |
| 96 kHz             | 12.288                                     | 18.432               | 24.576                | 36.864                | 49.152 <sup>(1)</sup> | 73.728 <sup>(1)</sup> |
| 192 kHz            | 24.576                                     | 36.864               | 49.152 <sup>(1)</sup> | 73.728 <sup>(1)</sup> | — <sup>(2)</sup>      | — <sup>(2)</sup>      |

<sup>(1)</sup> This system clock rate is not supported in I<sup>2</sup>C fast mode.

<sup>(2)</sup> This system clock rate is not supported for the given sampling frequency.



| PARAMETERS |                                   | MIN          | MAX | UNITS |
|------------|-----------------------------------|--------------|-----|-------|
| $t_{SCY}$  | System clock pulse cycle time     | 13           |     | ns    |
| $t_{SCKH}$ | System clock pulse duration, HIGH | $0.4t_{SCY}$ |     | ns    |
| $t_{SCKL}$ | System clock pulse duration, LOW  | $0.4t_{SCY}$ |     | ns    |

**Figure 23. System Clock Input Timing**

## Power-On and External Reset Functions

The PCM1796 includes a power-on reset function. Figure 24 shows the operation of this function. With  $V_{DD} > 2\text{ V}$ , the power-on reset function is enabled. The initialization sequence requires 1024 system clocks from the time  $V_{DD} > 2\text{ V}$ . After the initialization period, the PCM1796 is set to its default reset state, as described in the *MODE CONTROL REGISTERS* section of this data sheet.

The PCM1796 also includes an external reset capability using the  $\overline{\text{RST}}$  input (pin 14). This allows an external controller or master reset circuit to force the PCM1796 to initialize to its default reset state.

Figure 25 shows the external reset operation and timing. The  $\overline{\text{RST}}$  pin is set to logic 0 for a minimum of 20 ns. The  $\overline{\text{RST}}$  pin is then set to a logic 1 state, thus starting the initialization sequence, which requires 1024 system clock periods. The external reset is especially useful in applications where there is a delay between the PCM1796 power up and system clock activation.

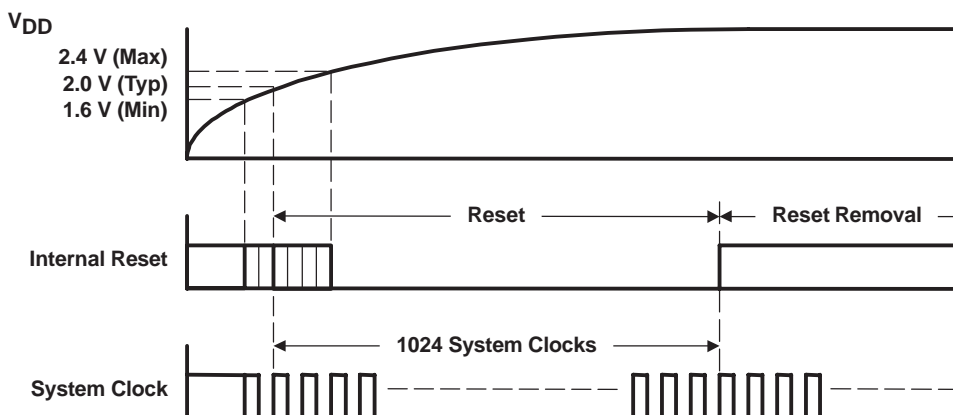


Figure 24. Power-On Reset Timing

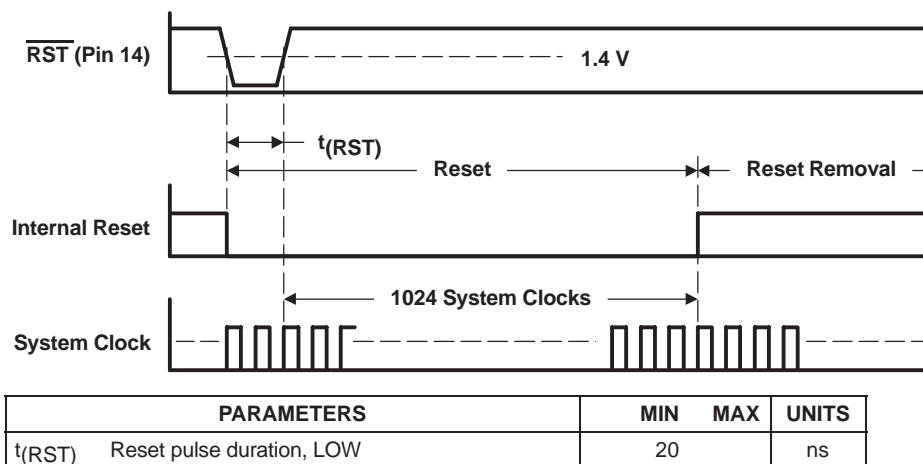


Figure 25. External Reset Timing

## AUDIO DATA INTERFACE

### Audio Serial Interface

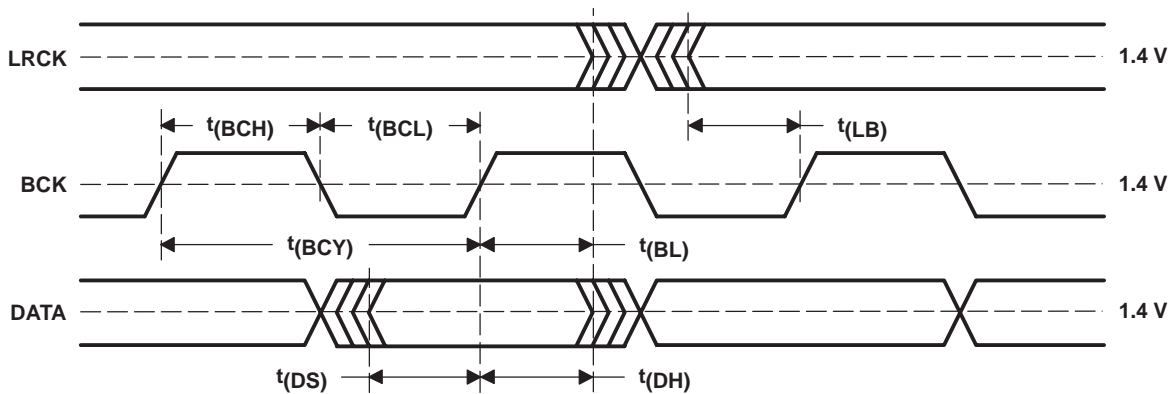
The audio interface port is a 3-wire serial port. It includes LRCK (pin 4), BCK (pin 6), and DATA (pin 5). BCK is the serial audio bit clock, and it is used to clock the serial data present on DATA into the serial shift register of the audio interface. Serial data is clocked into the PCM1796 on the rising edge of BCK. LRCK is the serial audio left/right word clock.

The PCM1796 requires the synchronization of LRCK and system clock, but does not need a specific phase relation between LRCK and system clock.

If the relationship between LRCK and system clock changes more than  $\pm 6$  BCK, internal operation is initialized within  $1/f_S$  and analog outputs are forced to the bipolar zero level until resynchronization between LRCK and system clock is completed.

### PCM Audio Data Formats and Timing

The PCM1796 supports industry-standard audio data formats, including standard right-justified, I<sup>2</sup>S, and left-justified. The data formats are shown in Figure 27. Data formats are selected using the format bits, FMT[2:0], in control register 18. The default data format is 24-bit I<sup>2</sup>S. All formats require binary 2s complement, MSB-first audio data. Figure 26 shows a detailed timing diagram for the serial audio interface.

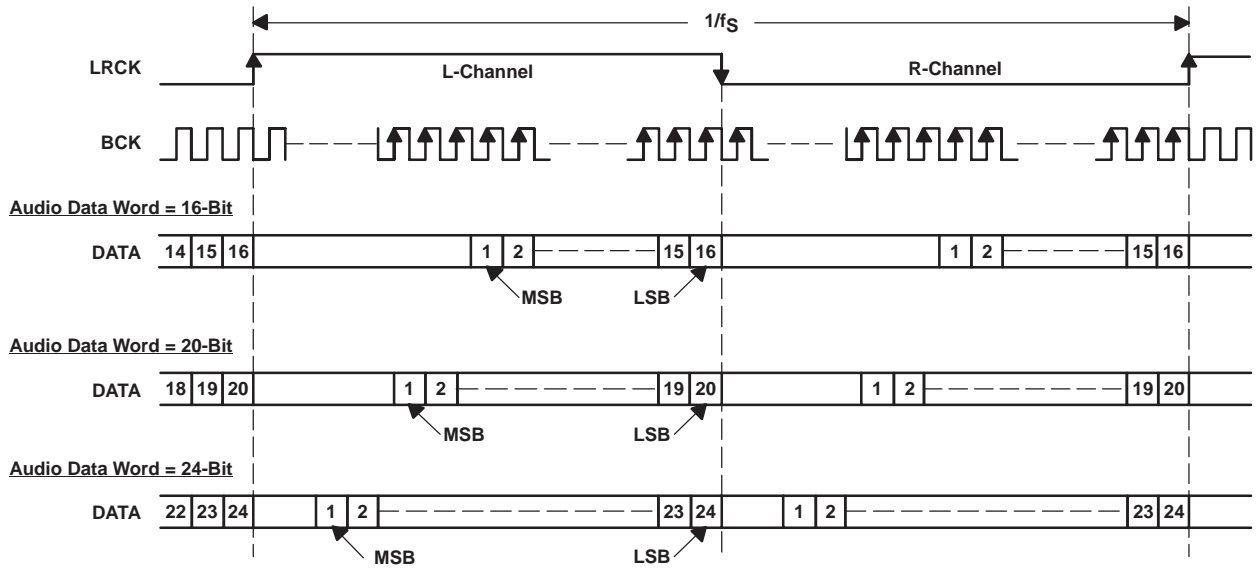


| PARAMETERS |                              | MIN                    | MAX | UNITS |
|------------|------------------------------|------------------------|-----|-------|
| $t(BCY)$   | BCK pulse cycle time         | 70                     |     | ns    |
| $t(BCL)$   | BCK pulse duration, LOW      | 30                     |     | ns    |
| $t(BCH)$   | BCK pulse duration, HIGH     | 30                     |     | ns    |
| $t(BL)$    | BCK rising edge to LRCK edge | 10                     |     | ns    |
| $t(LB)$    | LRCK edge to BCK rising edge | 10                     |     | ns    |
| $t(DS)$    | DATA setup time              | 10                     |     | ns    |
| $t(DH)$    | DATA hold time               | 10                     |     | ns    |
| —          | LRCK clock data              | 50% $\pm$ 2 bit clocks |     |       |

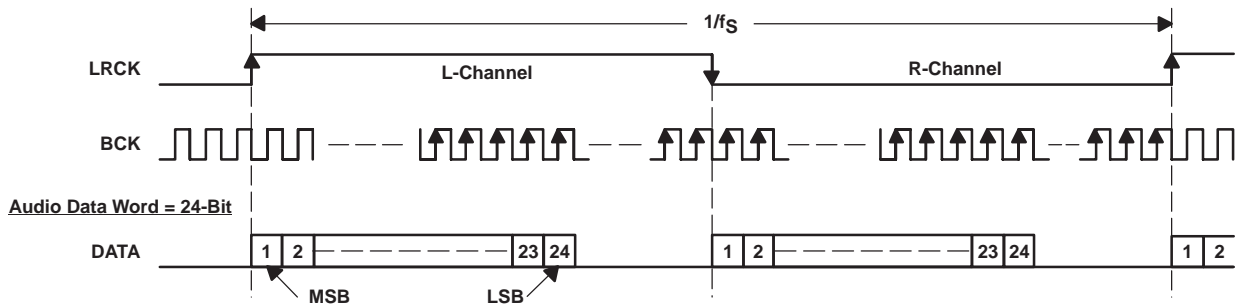
Figure 26. Timing of Audio Interface



**(1) Standard Data Format (Right-Justified); L-Channel = HIGH, R-Channel = LOW**



**(2) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW**



**(3) I<sup>2</sup>S Data Format; L-Channel = LOW, R-Channel = HIGH**

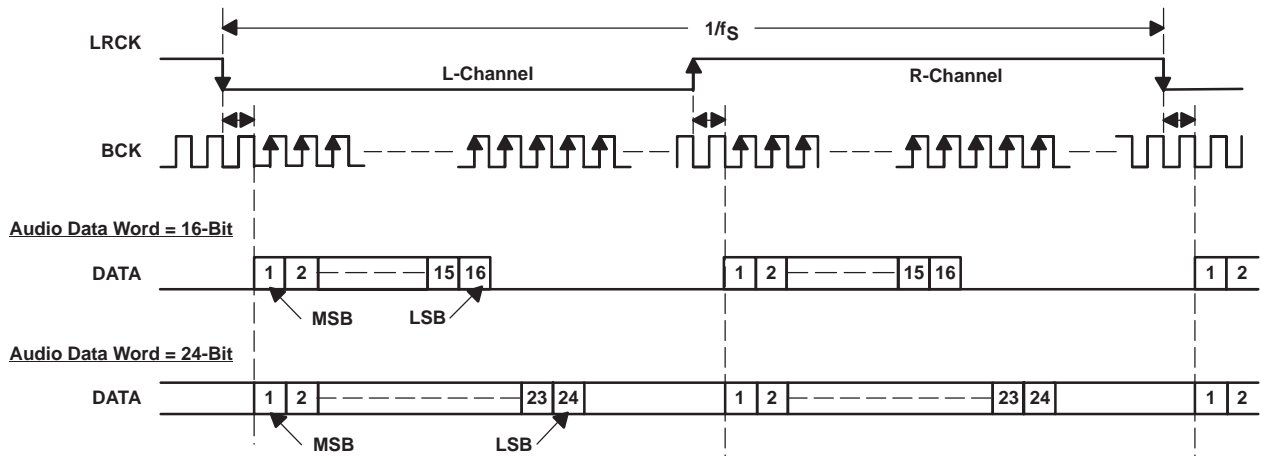


Figure 27. Audio Data Input Formats

## External Digital Filter Interface and Timing

The PCM1796 supports an external digital filter interface comprising a 3- or 4-wire synchronous serial port, which allows the use of an external digital filter. External filters include the Texas Instruments' DF1704 and DF1706, the Pacific Microsonics PMD200, or a programmable digital signal processor.

In the external DF mode, LRCK (pin 4), BCK (pin 6) and DATA (pin 5) are defined as WDCK, the word clock; BCK, the bit clock; and DATA, the monaural data. The external digital filter interface is selected by using the DFTH bit of control register 20, which functions to bypass the internal digital filter of the PCM1796.

When the DFMS bit of control register 19 is set, the PCM1796 can process stereo data. In this case, ZEROL (pin 1) and ZEROR (pin 2) are defined as L-channel data and R-channel data input, respectively.

Detailed information for the external digital filter interface mode is provided in the *APPLICATION FOR EXTERNAL DIGITAL FILTER INTERFACE* section of this data sheet.

## Direct Stream Digital (DSD) Format Interface and Timing

The PCM1796 supports the DSD format interface operation, which includes out-of-band noise filtering using an internal analog FIR filter. For DSD operation, SCK (pin 7) is redefined as BCK, DATA (pin 5) as DATAL (left channel audio data), and LRCK (pin 4) as DATAR (right channel audio data). BCK (pin 6) must be forced low in the DSD mode. The DSD format interface is activated by setting the DSD bit of control register 20.

Detailed information for the DSD mode is provided in the *APPLICATION FOR DSD FORMAT (DSD MODE) INTERFACE* section of this data sheet.

## TDMCA Interface

The PCM1796 supports the time-division-multiplexed command and audio (TDMCA) data format to enable control of and communication with a number of external devices over a single serial interface.

Detailed information for the TDMCA format is provided in the *TDMCA INTERFACE FORMAT* section of this data sheet.

## FUNCTION DESCRIPTIONS

### Zero Detect

The PCM1796 has a zero-detect function. When the PCM1796 detects the zero conditions as shown in Table 2, the PCM1796 sets ZEROL (pin 1) and ZEROR (pin 2) to HIGH.

**Table 2. Zero Conditions**

| MODE             |     | DETECTING CONDITION AND TIME  |
|------------------|-----|---|
| PCM              |     | DATA is continuously LOW for 1024 LRCKs.  |
| External DF Mode |     | DATA is continuously LOW for $8 \times 1024$ WDCKs.                                 |
| DSD              | DZ0 | There are an equal number of 1s and 0s in every 8 bits of DSD input data for 23 ms. |
|                  | DZ1 | The input data is 1001 0110 continuously for 23 ms.                                 |

## SERIAL CONTROL INTERFACE

The PCM1796 supports SPI and I<sup>2</sup>C that sets mode control registers as shown in Table 4. This serial control interface is selected by MSEL (pin 3), SPI is activated when MSEL is set to LOW, and I<sup>2</sup>C is activated when MSEL is set to HIGH.

### SPI Interface

The SPI interface is a 4-wire synchronous serial port that operates asynchronously to the serial audio interface and the system clock (SCK). The serial control interface is used to program and read the on-chip mode registers. The control interface includes MDO (pin 13), MDI (pin 11), MC (pin 12), and  $\overline{MS}$  (pin 10). MDO is the serial data output, used to read back the values of the mode registers; MDI is the serial data input, used to program the mode registers; MC is the serial bit clock, used to shift data in and out of the control port, and  $\overline{MS}$  is the mode control enable, used to enable the internal mode register access.

### Register Read/Write Operation

All read/write operations for the serial control port use 16-bit data words. Figure 28 shows the control data word format. The most significant bit is the read/write ( $R/\overline{W}$ ) bit. For write operations, the  $R/\overline{W}$  bit must be set to 0. For read operations, the  $R/\overline{W}$  bit must be set to 1. There are seven bits, labeled  $IDX[6:0]$ , that hold the register index (or address) for the read and write operations. The least significant eight bits,  $D[7:0]$ , contain the data to be written to, or the data that was read from, the register specified by  $IDX[6:0]$ .

Figure 29 shows the functional timing diagram for writing or reading the serial control port.  $\overline{MS}$  is held at a logic 1 state until a register needs to be written or read. To start the register write or read cycle,  $\overline{MS}$  is set to logic 0. Sixteen clocks are then provided on MC, corresponding to the 16 bits of the control data word on MDI and readback data on MDO. After the eighth clock cycle has completed, the data from the indexed-mode control register appears on MDO during the read operation. After the sixteenth clock cycle has completed, the data is latched into the indexed-mode control register during the write operation. To write or read subsequent data,  $\overline{MS}$  must be set to 1 once.

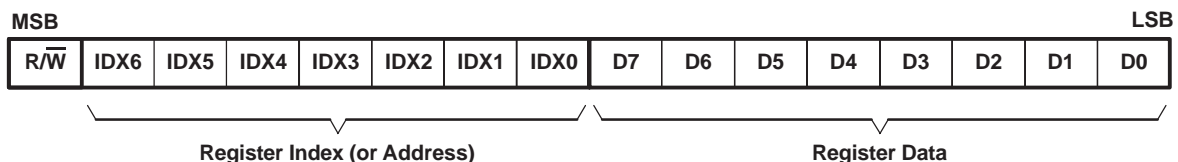
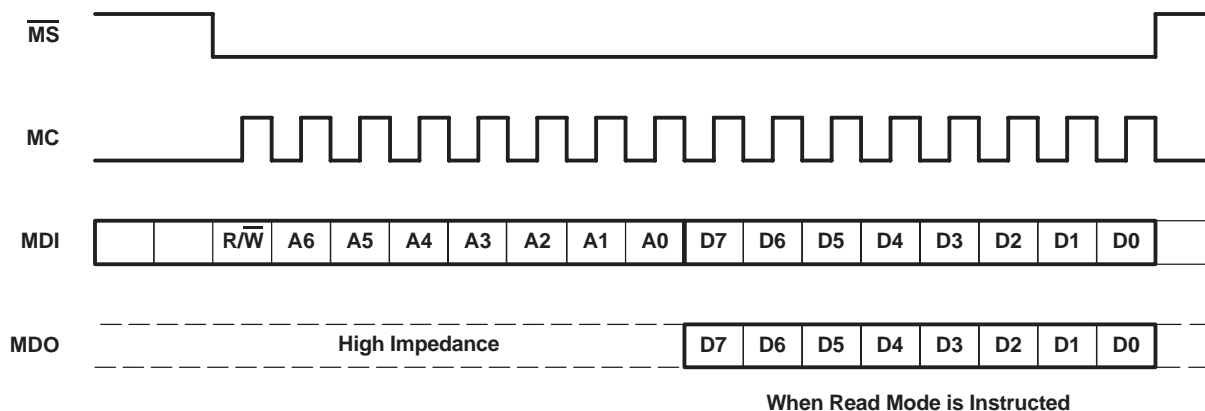
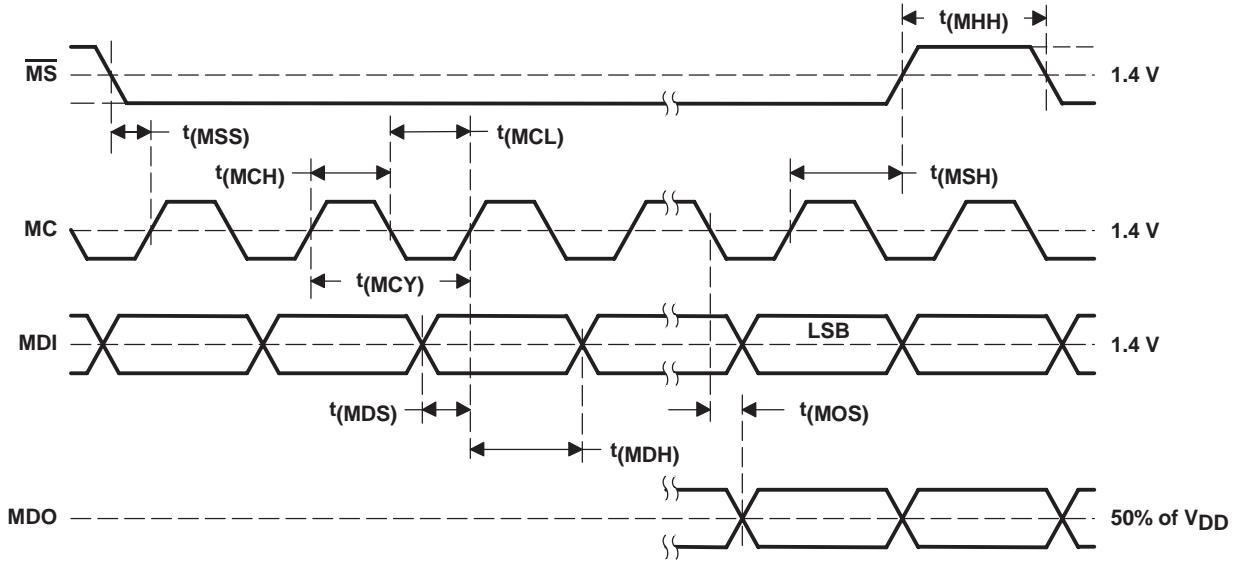


Figure 28. Control Data Word Format for MDI



NOTE: Bit 15 is used for selection of write or read. Setting  $R/\overline{W} = 0$  indicates a write, while  $R/\overline{W} = 1$  indicates a read. Bits 14–8 are used for the register address. Bits 7–0 are used for register data.

Figure 29. Serial Control Format



| PARAMETER   | MIN | MAX | UNITS |
|---|-----|-----|-------|
| $t(MCY)$ MC pulse cycle time                            | 100 |     | ns    |
| $t(MCL)$ MC low-level time                              | 40  |     | ns    |
| $t(MCH)$ MC high-level time                             | 40  |     | ns    |
| $t(MHH)$ $\overline{MS}$ high-level time                | 80  |     | ns    |
| $t(MSS)$ $\overline{MS}$ falling edge to MC rising edge | 15  |     | ns    |
| $t(MSH)$ $\overline{MS}$ hold time <sup>(1)</sup>       | 15  |     | ns    |
| $t(MDH)$ MDI hold time                                  | 15  |     | ns    |
| $t(MDS)$ MDI setup time                                 | 15  |     | ns    |
| $t(MOS)$ MC falling edge to MDO stable                  |     | 30  | ns    |

<sup>(1)</sup> MC rising edge for LSB to MS rising edge

Figure 30. Control Interface Timing

## I<sup>2</sup>C INTERFACE

The PCM1796 supports the I<sup>2</sup>C serial bus and the data transmission protocol for standard and fast mode as a slave device. This protocol is explained in I<sup>2</sup>C specification 2.0.

In I<sup>2</sup>C mode, the control terminals are changed as follows.

| TERMINAL NAME   | TDMCA NAME | PROPERTY     | DESCRIPTION                |
|-----------------|------------|--------------|----------------------------|
| $\overline{MS}$ | ADR0       | Input        | I <sup>2</sup> C address 0 |
| MDI             | ADR1       | Input        | I <sup>2</sup> C address 1 |
| MC              | SCL        | Input        | I <sup>2</sup> C clock     |
| MDO             | SDA        | Input/output | I <sup>2</sup> C data      |

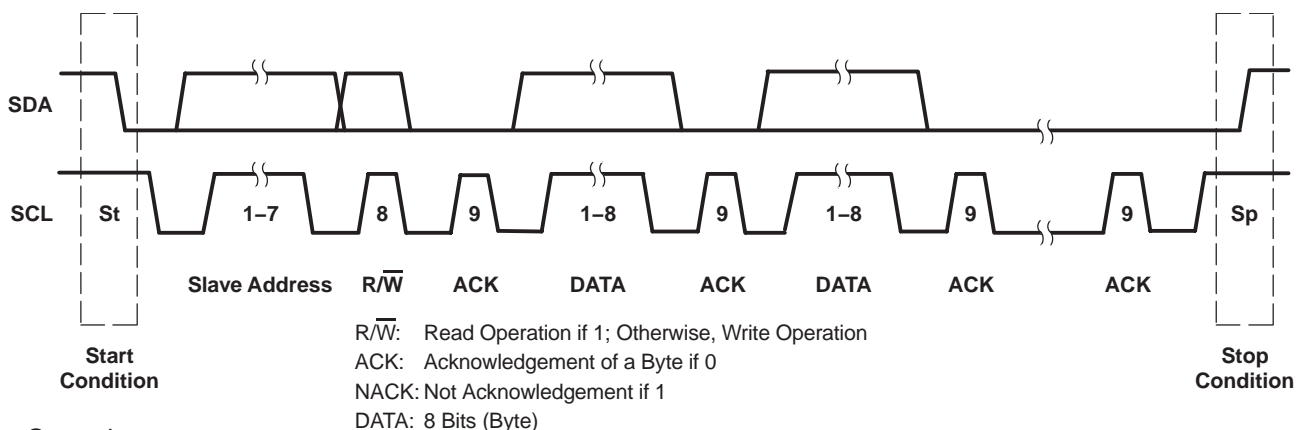
### Slave Address

| MSB |   |   |   |   | LSB  |      |                   |
|-----|---|---|---|---|------|------|-------------------|
| 1   | 0 | 0 | 1 | 1 | ADR1 | ADR0 | R/ $\overline{W}$ |

The PCM1796 has 7 bits for its own slave address. The first five bits (MSBs) of the slave address are factory preset to 10011. The next two bits of the address byte are the device select bits which can be user-defined by the ADR1 and ADR0 terminals. A maximum of four PCM1796s can be connected on the same bus at one time. Each PCM1796 responds when it receives its own slave address.

### Packet Protocol

A master device must control packet protocol, which consists of start condition, slave address, read/write bit, data if write or acknowledge if read, and stop condition. The PCM1796 supports only slave receivers and slave transmitters.



#### Write Operation

|             |    |               |                |     |      |     |      |     |  |     |    |
|-------------|----|---------------|----------------|-----|------|-----|------|-----|--|-----|----|
| Transmitter | M  | M             | M              | S   | M    | S   | M    | S   |  | S   | M  |
| Data Type   | St | Slave Address | $\overline{W}$ | ACK | DATA | ACK | DATA | ACK |  | ACK | Sp |

#### Read Operation

|             |    |               |   |     |      |     |      |     |  |      |    |
|-------------|----|---------------|---|-----|------|-----|------|-----|--|------|----|
| Transmitter | M  | M             | M | S   | S    | M   | S    | M   |  | M    | M  |
| Data Type   | St | Slave Address | R | ACK | DATA | ACK | DATA | ACK |  | NACK | Sp |

M: Master Device

S: Slave Device

St: Start Condition

Sp: Stop Condition

$\overline{W}$ : Write

R: Read

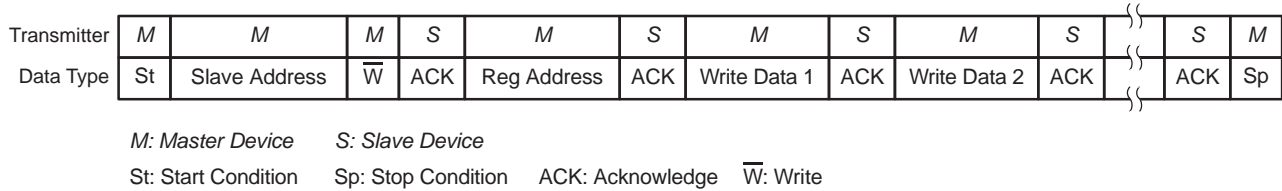
ACK: Acknowledge

NACK: Not Acknowledge

Figure 31. Basic I<sup>2</sup>C Framework

### Write Register

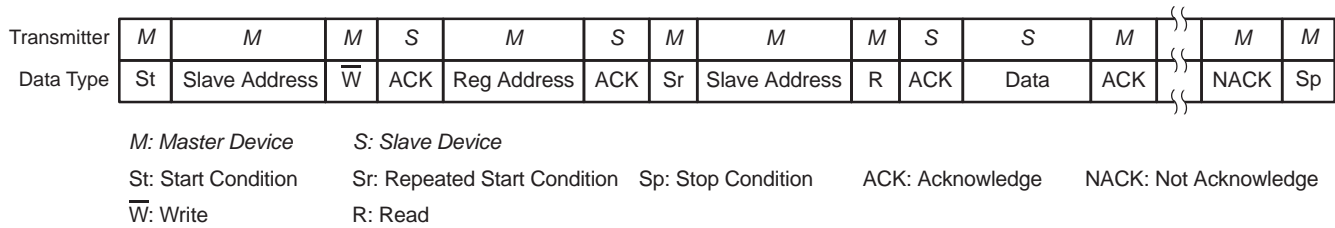
A master can write to any PCM1796 registers using single or multiple accesses. The master sends a PCM1796 slave address with a write bit, a register address, and the data. If multiple access is required, the address is that of the starting register, followed by the data to be transferred. When the data are received properly, the index register is incremented by 1 automatically. When the index register reaches 0x7F, the next value is 0x00. When undefined registers are accessed, the PCM1796 does not send an acknowledgement. Figure 32 is a diagram of the write operation.



**Figure 32. Write Operation**

### Read Register

A master can read the PCM1796 register. The value of the register address is stored in an indirect index register in advance. The master sends a PCM1796 slave address with a read bit after storing the register address. Then the PCM1796 transfers the data which the index register points to. When the data are transferred during a multiple access, the index register is incremented by 1 automatically. (When first going into read mode immediately following a write, the index register is not incremented. The master can read the register that was previously written.) When the index register reaches 0x7F, the next value is 0x00. The PCM1796 outputs some data when the index register is 0x10 to 0x1F, even if it is not defined in Table 4. Figure 33 is a diagram of the read operation.



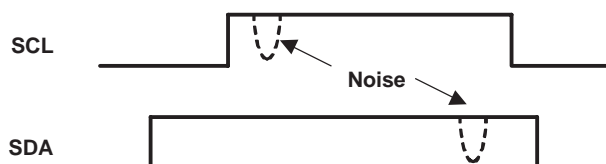
**Figure 33. Read Operation**

## Noise Suppression

The PCM1796 incorporates noise suppression using the system clock (SCK). However, there must be no more than two noise spikes in 600 ns. The noise suppression works for SCK frequencies between 8 MHz and 40 MHz in fast mode. However, it works incorrectly in the following conditions.

### Case 1:

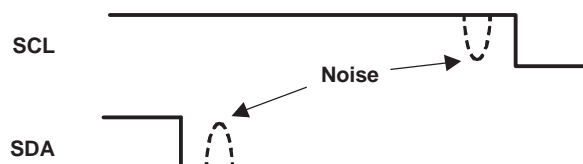
1.  $t_{(SCK)} > 120 \text{ ns}$  ( $t_{(SCK)}$ : period of SCK)
2.  $t_{(HI)} + t_{(D-HD)} < t_{(SCK)} \times 5$
3. Spike noise exists on the first half of the SCL HIGH pulse.
4. Spike noise exists on the SDA HIGH pulse just before SDA goes LOW.



When these conditions occur at the same time, the data is recognized as LOW.

### Case 2:

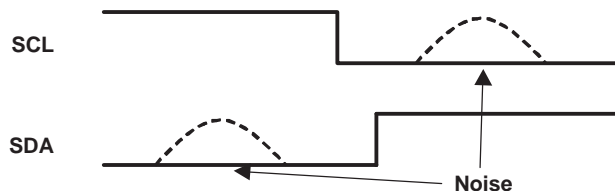
1.  $t_{(SCK)} > 120 \text{ ns}$
2.  $t_{(S-HD)}$  or  $t_{(RS-HD)} < t_{(SCK)} \times 5$
3. Spike noise exists on both SCL and SDA during the hold time.



When these conditions occur at the same time, the PCM1796 fails to detect a start condition.

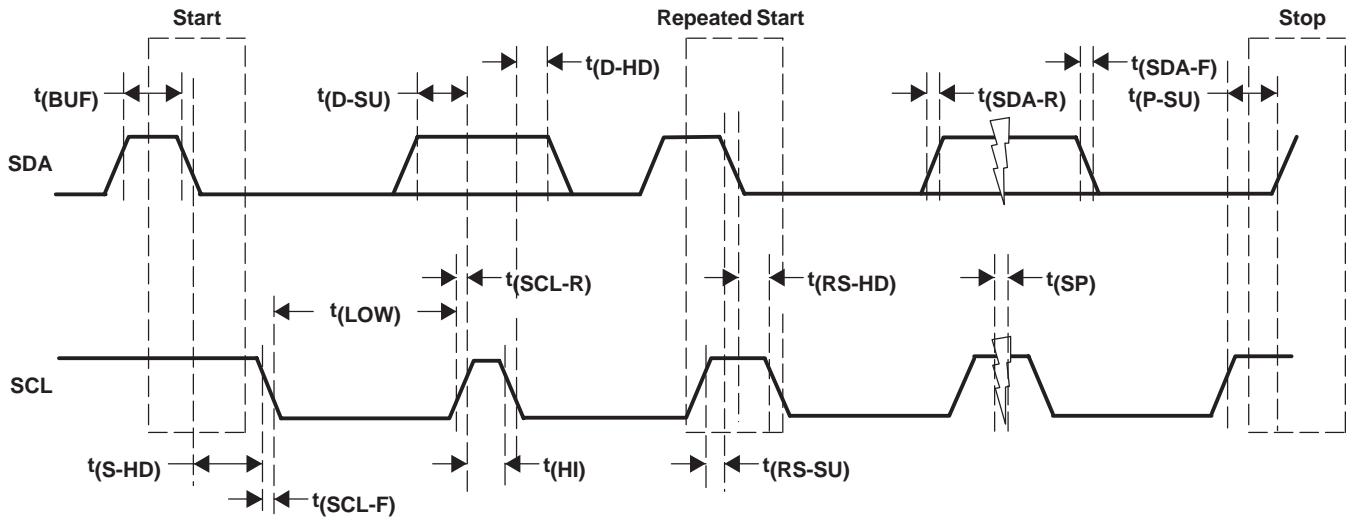
### Case 3:

1.  $t_{(SCK)} < 50 \text{ ns}$
2.  $t_{(SP)} > t_{(SCK)}$
3. Spike noise exists on SCL just after SCL goes LOW.
4. Spike noise exists on SDA just before SCL goes LOW.



When these conditions occur at the same time, the PCM1796 erroneously detects a start or stop condition.

**TIMING DIAGRAM**



**TIMING CHARACTERISTICS**

| PARAMETER        |   | CONDITIONS | MIN                     | MAX                 | UNIT |
|------------------|---|------------|-------------------------|---------------------|------|
| f(SCL)           | SCL clock frequency   | Standard   |                         | 100                 | kHz  |
|                  |   | Fast       |                         | 400                 |      |
| t(BUF)           | Bus free time between stop and start conditions                                       | Standard   | 4.7                     |                     | μs   |
|                  |   | Fast       | 1.3                     |                     |      |
| t(LOW)           | Low period of the SCL clock   | Standard   | 4.7                     |                     | μs   |
|                  |   | Fast       | 1.3                     |                     |      |
| t(HI)            | High period of the SCL clock  | Standard   | 4                       |                     | μs   |
|                  |   | Fast       | 600                     |                     |      |
| t(RS-SU)         | Setup time for (repeated) start condition   | Standard   | 4.7                     |                     | μs   |
|                  |   | Fast       | 600                     |                     |      |
| t(S-HD)          | Hold time for (repeated) start condition  | Standard   | 4                       |                     | μs   |
| t(RS-HD)         |   | Fast       | 600                     |                     |      |
| t(D-SU)          | Data setup time   | Standard   | 250                     |                     | ns   |
|                  |   | Fast       | 100                     |                     |      |
| t(D-HD)          | Data hold time  | Standard   | 0                       | 900                 | ns   |
|                  |   | Fast       | 0                       | 900                 |      |
| t(SCL-R)         | Rise time of SCL signal   | Standard   | 20 + 0.1 C <sub>B</sub> | 1000                | ns   |
|                  |   | Fast       | 20 + 0.1 C <sub>B</sub> | 300                 |      |
| t(SCL-R1)        | Rise time of SCL signal after a repeated start condition and after an acknowledge bit | Standard   | 20 + 0.1 C <sub>B</sub> | 1000                | ns   |
|                  |   | Fast       | 20 + 0.1 C <sub>B</sub> | 300                 |      |
| t(SCL-F)         | Fall time of SCL signal   | Standard   | 20 + 0.1 C <sub>B</sub> | 1000                | ns   |
|                  |   | Fast       | 20 + 0.1 C <sub>B</sub> | 300                 |      |
| t(SDA-R)         | Rise time of SDA signal   | Standard   | 20 + 0.1 C <sub>B</sub> | 1000                | ns   |
|                  |   | Fast       | 20 + 0.1 C <sub>B</sub> | 300                 |      |
| t(SDA-F)         | Fall time of SDA signal   | Standard   | 20 + 0.1 C <sub>B</sub> | 1000                | ns   |
|                  |   | Fast       | 20 + 0.1 C <sub>B</sub> | 300                 |      |
| t(P-SU)          | Setup time for stop condition   | Standard   | 4                       |                     | μs   |
|                  |   | Fast       | 600                     |                     |      |
| C <sub>(B)</sub> | Capacitive load for SDA and SCL line  |            |                         | 400                 | pF   |
| t(SP)            | Pulse duration of suppressed spike  | Fast       |                         | 50                  | ns   |
| V <sub>NH</sub>  | Noise margin at high level for each connected device (including hysteresis)           |            |                         | 0.2 V <sub>DD</sub> | V    |

**Figure 34. Timing Definition on the I<sup>2</sup>C Bus**



## MODE CONTROL REGISTERS

### User-Programmable Mode Controls

The PCM1796 includes a number of user-programmable functions which are accessed via mode control registers. The registers are programmed using the serial control interface, which is previously discussed in the *SPI Interface* and *I<sup>2</sup>C INTERFACE* sections of this data sheet. Table 3 lists the available mode-control functions, along with their default reset conditions and associated register index.

**Table 3. User-Programmable Function Controls**

| FUNCTION  | DEFAULT                           | REGISTER                   | BIT  | PCM | DSD                | DF BYPASS |
|---|-----------------------------------|----------------------------|--|-----|--------------------|-----------|
| Digital attenuation control<br>0 dB to –120 dB and mute, 0.5 dB step  | 0 dB                              | Register 16<br>Register 17 | ATL[7:0] (for L-ch)<br>ATR[7:0] (for R-ch) | yes |                    |           |
| Attenuation load control<br>Disabled, enabled   | Attenuation disabled              | Register 18                | ATLD                                       | yes |                    |           |
| Input audio data format selection<br>16-, 20-, 24-bit standard (right-justified) format<br>24-bit MSB-first left-justified format<br>16-/24-bit I <sup>2</sup> S format | 24-bit I <sup>2</sup> S format    | Register 18                | FMT[2:0]                                   | yes |                    | yes       |
| Sampling rate selection for de-emphasis<br>Disabled, 44.1 kHz, 48 kHz, 32 kHz   | De-emphasis disabled              | Register 18                | DMF[1:0]                                   | yes | yes <sup>(1)</sup> |           |
| De-emphasis control<br>Disabled, enabled  | De-emphasis disabled              | Register 18                | DME  | yes |                    |           |
| Soft mute control<br>Soft mute disabled, enabled  | Mute disabled                     | Register 18                | MUTE                                       | yes |                    |           |
| Output phase reversal<br>Normal, reverse  | Normal                            | Register 19                | REV  | yes | yes                | yes       |
| Attenuation speed selection<br>$\times 1f_s$ , $\times (1/2)f_s$ , $\times (1/4)f_s$ , $\times (1/8)f_s$  | $\times 1f_s$                     | Register 19                | ATS[1:0]                                   | yes |                    |           |
| DAC operation control<br>Enabled, disabled  | DAC operation enabled             | Register 19                | OPE  | yes | yes                | yes       |
| Stereo DF bypass mode select<br>Monaural, stereo  | Monaural                          | Register 19                | DFMS                                       |     |                    | yes       |
| Digital filter rolloff selection<br>Sharp rolloff, slow rolloff   | Sharp rolloff                     | Register 19                | FLT  | yes |                    |           |
| Infinite zero mute control<br>Disabled, enabled   | Disabled                          | Register 19                | INZD                                       | yes |                    | yes       |
| System reset control<br>Reset operation, normal operation   | Normal operation                  | Register 20                | SRST                                       | yes | yes                | yes       |
| DSD interface mode control<br>DSD enabled, disabled   | Disabled                          | Register 20                | DSD  | yes | yes                |           |
| Digital-filter bypass control<br>DF enabled, DF bypass  | DF enabled                        | Register 20                | DFTH                                       | yes |                    | yes       |
| Monaural mode selection<br>Stereo, monaural   | Stereo                            | Register 20                | MONO                                       | yes | yes                | yes       |
| Channel selection for monaural mode data<br>L-channel, R-channel  | L-channel                         | Register 20                | CHSL                                       | yes | yes                | yes       |
| Delta-sigma oversampling rate selection<br>$\times 64f_s$ , $\times 128f_s$ , $\times 32f_s$  | $\times 64f_s$                    | Register 20                | OS[1:0]                                    | yes | yes <sup>(2)</sup> | yes       |
| PCM zero output enable  | Enabled                           | Register 21                | PCMZ                                       | yes |                    | yes       |
| DSD zero output enable  | Disabled                          | Register 21                | DZ[1:0]                                    |     | yes                |           |
| <b>FUNCTION AVAILABLE ONLY FOR READ</b>   |                                   |                            |  |     |                    |           |
| Zero detection flag<br>Not zero, zero detected  | Not zero = 0<br>Zero detected = 1 | Register 22                | ZFGL (for L-ch)<br>ZFGR (for R-ch)         | yes | yes                | yes       |
| Device ID (at TDMCA)  | –                                 | Register 23                | ID[4:0]                                    | yes |                    |           |

<sup>(1)</sup> When in DSD mode, DMF[1:0] is defined as DSD filter (analog FIR) performance selection.

<sup>(2)</sup> When in DSD mode, OS[1:0] is defined as DSD filter (analog FIR) operation rate selection.

## Register Map

The mode control register map is shown in Table 4. Registers 16–21 include an  $R/\overline{W}$  bit, which determines whether a register read ( $R/\overline{W} = 1$ ) or write ( $R/\overline{W} = 0$ ) operation is performed. Registers 22 and 23 are read-only.

**Table 4. Mode Control Register Map**

|             | B15              | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7   | B6   | B5   | B4   | B3   | B2   | B1   | B0   |
|-------------|------------------|-----|-----|-----|-----|-----|----|----|------|------|------|------|------|------|------|------|
| Register 16 | $R/\overline{W}$ | 0   | 0   | 1   | 0   | 0   | 0  | 0  | ATL7 | ATL6 | ATL5 | ATL4 | ATL3 | ATL2 | ATL1 | ATL0 |
| Register 17 | $R/\overline{W}$ | 0   | 0   | 1   | 0   | 0   | 0  | 1  | ATR7 | ATR6 | ATR5 | ATR4 | ATR3 | ATR2 | ATR1 | ATR0 |
| Register 18 | $R/\overline{W}$ | 0   | 0   | 1   | 0   | 0   | 1  | 0  | ATLD | FMT2 | FMT1 | FMT0 | DMF1 | DMF0 | DME  | MUTE |
| Register 19 | $R/\overline{W}$ | 0   | 0   | 1   | 0   | 0   | 1  | 1  | REV  | ATS1 | ATS0 | OPE  | RSV  | DFMS | FLT  | INZD |
| Register 20 | $R/\overline{W}$ | 0   | 0   | 1   | 0   | 1   | 0  | 0  | RSV  | SRST | DSD  | DFTH | MONO | CHSL | OS1  | OS0  |
| Register 21 | $R/\overline{W}$ | 0   | 0   | 1   | 0   | 1   | 0  | 1  | RSV  | RSV  | RSV  | RSV  | RSV  | DZ1  | DZ0  | PCMZ |
| Register 22 | R                | 0   | 0   | 1   | 0   | 1   | 1  | 0  | RSV  | RSV  | RSV  | RSV  | RSV  | RSV  | ZFGR | ZFGL |
| Register 23 | R                | 0   | 0   | 1   | 0   | 1   | 1  | 1  | RSV  | RSV  | RSV  | ID4  | ID3  | ID2  | ID1  | ID0  |

## Register Definitions

|             | B15              | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7   | B6   | B5   | B4   | B3   | B2   | B1   | B0   |
|-------------|------------------|-----|-----|-----|-----|-----|----|----|------|------|------|------|------|------|------|------|
| Register 16 | $R/\overline{W}$ | 0   | 0   | 1   | 0   | 0   | 0  | 0  | ATL7 | ATL6 | ATL5 | ATL4 | ATL3 | ATL2 | ATL1 | ATL0 |
| Register 17 | $R/\overline{W}$ | 0   | 0   | 1   | 0   | 0   | 0  | 1  | ATR7 | ATR6 | ATR5 | ATR4 | ATR3 | ATR2 | ATR1 | ATR0 |

### $R/\overline{W}$ : Read/Write Mode Select

When  $R/\overline{W} = 0$ , a write operation is performed.

When  $R/\overline{W} = 1$ , a read operation is performed.

Default value: 0

### ATx[7:0]: Digital Attenuation Level Setting

These bits are available for read and write.

Default value: 1111 1111b

Each DAC output has a digital attenuator associated with it. The attenuator can be set from 0 dB to –120 dB, in 0.5-dB steps. Alternatively, the attenuator can be set to infinite attenuation (or mute).

The attenuation data for each channel can be set individually. However, the data load control (the ATLD bit of control register 18) is common to both attenuators. ATLD must be set to 1 in order to change an attenuator setting. The attenuation level can be set using the following formula:

$$\text{Attenuation level (dB)} = 0.5 \text{ dB} \cdot (\text{ATx}[7:0]_{\text{DEC}} - 255)$$

where  $\text{ATx}[7:0]_{\text{DEC}} = 0$  through 255

For  $\text{ATx}[7:0]_{\text{DEC}} = 0$  through 14, the attenuator is set to infinite attenuation. The following table shows attenuation levels for various settings:

| ATx[7:0]   | Decimal Value | Attenuation Level Setting      |
|------------|---------------|--------------------------------|
| 1111 1111b | 255           | 0 dB, no attenuation (default) |
| 1111 1110b | 254           | –0.5 dB                        |
| 1111 1101b | 253           | –1.0 dB                        |
| ⋮          | ⋮             | ⋮                              |
| 0001 0000b | 16            | –119.5 dB                      |
| 0000 1111b | 15            | –120.0 dB                      |
| 0000 1110b | 14            | Mute                           |
| ⋮          | ⋮             | ⋮                              |
| 0000 0000b | 0             | Mute                           |

|             |                   |            |            |            |            |            |           |           |           |           |           |           |           |           |           |           |
|-------------|-------------------|------------|------------|------------|------------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
|             | <b>B15</b>        | <b>B14</b> | <b>B13</b> | <b>B12</b> | <b>B11</b> | <b>B10</b> | <b>B9</b> | <b>B8</b> | <b>B7</b> | <b>B6</b> | <b>B5</b> | <b>B4</b> | <b>B3</b> | <b>B2</b> | <b>B1</b> | <b>B0</b> |
| Register 18 | R/ $\overline{W}$ | 0          | 0          | 1          | 0          | 0          | 1         | 0         | ATLD      | FMT2      | FMT1      | FMT0      | DMF1      | DMF0      | DME       | MUTE      |

### R/ $\overline{W}$ : Read/Write Mode Select

When R/ $\overline{W}$  = 0, a write operation is performed.

When R/ $\overline{W}$  = 1, a read operation is performed.

Default value: 0

### ATLD: Attenuation Load Control

This bit is available for read and write.

Default value: 0

|          |  |
|----------|--|
| ATLD = 0 | Attenuation control disabled (default) |
| ATLD = 1 | Attenuation control enabled            |

The ATLD bit is used to enable loading of the attenuation data contained in registers 16 and 17. When ATLD = 0, the attenuation settings remain at the previously programmed levels, ignoring new data loaded from registers 16 and 17. When ATLD = 1, attenuation data written to registers 16 and 17 is loaded normally.

### FMT[2:0]: Audio Interface Data Format

These bits are available for read and write.

Default value: 101

| FMT[2:0] | Audio Data Format Selection                   |
|----------|---|
| 000      | 16-bit standard format, right-justified data  |
| 001      | 20-bit standard format, right-justified data  |
| 010      | 24-bit standard format, right-justified data  |
| 011      | 24-bit MSB-first, left-justified format data  |
| 100      | 16-bit I <sup>2</sup> S format data           |
| 101      | 24-bit I <sup>2</sup> S format data (default) |
| 110      | Reserved                                      |
| 111      | Reserved                                      |

The FMT[2:0] bits are used to select the data format for the serial audio interface.

For the external digital filter interface mode (DFTH mode), this register is operated as shown in the *APPLICATION FOR EXTERNAL DIGITAL FILTER INTERFACE* section of this data sheet.

### DMF[1:0]: Sampling Frequency Selection for the De-Emphasis Function

These bits are available for read and write.

Default value: 00

| DMF[1:0] | De-Emphasis Sampling Frequency Selection |
|----------|--|
| 00       | Disabled (default)                       |
| 01       | 48 kHz                                   |
| 10       | 44.1 kHz                                 |
| 11       | 32 kHz                                   |

The DMF[1:0] bits are used to select the sampling frequency used by the digital de-emphasis function when it is enabled by setting the DME bit. The de-emphasis curves are shown in the *TYPICAL PERFORMANCE CURVES* section of this data sheet.

For the DSD mode, analog FIR filter performance can be selected using this register. A register map and filter response plots are shown in the *APPLICATION FOR DSD FORMAT (DSD MODE) INTERFACE* section of this data sheet.

**DME: Digital De-Emphasis Control**

This bit is available for read and write.

Default value: 0

|         |                                |
|---------|--------------------------------|
| DME = 0 | De-emphasis disabled (default) |
| DME = 1 | De-emphasis enabled            |

The DME bit is used to enable or disable the de-emphasis function for both channels.

**MUTE: Soft Mute Control**

This bit is available for read and write.

Default value: 0

|          |                              |
|----------|------------------------------|
| MUTE = 0 | Soft mute disabled (default) |
| MUTE = 1 | Soft mute enabled            |

The MUTE bit is used to enable or disable the soft mute function for both channels.

Soft mute is operated as a 256-step attenuator. The speed for each step to  $-\infty$  dB (mute) is determined by the attenuation rate selected in the ATS register.

|             |            |            |            |            |            |            |           |           |           |           |           |           |           |           |           |           |
|-------------|------------|------------|------------|------------|------------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
|             | <b>B15</b> | <b>B14</b> | <b>B13</b> | <b>B12</b> | <b>B11</b> | <b>B10</b> | <b>B9</b> | <b>B8</b> | <b>B7</b> | <b>B6</b> | <b>B5</b> | <b>B4</b> | <b>B3</b> | <b>B2</b> | <b>B1</b> | <b>B0</b> |
| Register 19 | R/W        | 0          | 0          | 1          | 0          | 0          | 1         | 1         | REV       | ATS1      | ATS0      | OPE       | RSV       | DFMS      | FLT       | INZD      |

**R/W: Read/Write Mode Select**

When  $R/\overline{W} = 0$ , a write operation is performed.

When  $R/\overline{W} = 1$ , a read operation is performed.

Default value: 0

**REV: Output Phase Reversal**

This bit is available for read and write.

Default value: 0

|         |                         |
|---------|-------------------------|
| REV = 0 | Normal output (default) |
| REV = 1 | Inverted output         |

The REV bit is used to invert the output phase for both channels.

**ATS[1:0]: Attenuation Rate Select**

These bits are available for read and write.

Default value: 00

| ATS[1:0] | Attenuation Rate Selection |
|----------|----------------------------|
| 00       | Every LRCK (default)       |
| 01       | LRCK/2                     |
| 10       | LRCK/4                     |
| 11       | LRCK/8                     |

The ATS[1:0] bits are used to select the rate at which the attenuator is decremented/incremented during level transitions.

**OPE: DAC Operation Control**

This bit is available for read and write.

Default value: 0

|         |                                 |
|---------|---------------------------------|
| OPE = 0 | DAC operation enabled (default) |
| OPE = 1 | DAC operation disabled          |

The OPE bit is used to enable or disable the analog output for both channels. Disabling the analog outputs forces them to the bipolar zero level (BPZ) even if audio data is present on the input.

**DFMS: Stereo DF Bypass Mode Select**

This bit is available for read and write.

Default value: 0

|          |                      |
|----------|----------------------|
| DFMS = 0 | Monaural (default)   |
| DFMS = 1 | Stereo input enabled |

The DFMS bit is used to enable stereo operation in DF bypass mode. In the DF bypass mode, when DFMS is set to 0, the pin for the input data is DATA (pin 5) only, therefore the PCM1796 operates as a monaural DAC. When DFMS is set to 1, the PCM1796 can operate as a stereo DAC with inputs of L-channel and R-channel data on ZEROL (pin 1) and ZEROR (pin 2), respectively.

**FLT: Digital Filter Rolloff Control**

This bit is available for read and write.

Default value: 0

|         |                         |
|---------|-------------------------|
| FLT = 0 | Sharp rolloff (default) |
| FLT = 1 | Slow rolloff            |

The FLT bit is used to select the digital filter rolloff characteristic. The filter responses for these selections are shown in the *TYPICAL PERFORMANCE CURVES* section of this data sheet.

**INZD: Infinite Zero Detect Mute Control**

This bit is available for read and write.

Default value: 0

|          |  |
|----------|--|
| INZD = 0 | Infinite zero detect mute disabled (default) |
| INZD = 1 | Infinite zero detect mute enabled            |

The INZD bit is used to enable or disable the zero detect mute function. Setting INZD to 1 forces muted analog outputs to hold a bipolar zero level when the PCM1796 detects a zero condition in both channels. The infinite zero detect mute function is not available in the DSD mode.

|             | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7  | B6   | B5  | B4   | B3   | B2   | B1  | B0  |
|-------------|-----|-----|-----|-----|-----|-----|----|----|-----|------|-----|------|------|------|-----|-----|
| Register 20 | R/W | 0   | 0   | 1   | 0   | 1   | 0  | 0  | RSV | SRST | DSD | DFTH | MONO | CHSL | OS1 | OS0 |

**R/W: Read/Write Mode Select**

When  $R/\overline{W} = 0$ , a write operation is performed.

When  $R/\overline{W} = 1$ , a read operation is performed.

Default value: 0

**SRST: System Reset Control**

This bit is available for write only.

Default value: 0

|          |   |
|----------|---|
| SRST = 0 | Normal operation (default)                        |
| SRST = 1 | System reset operation (generate one reset pulse) |

The SRST bit is used to reset the PCM1796 to the initial system condition.

**DSD: DSD Interface Mode Control**

This bit is available for read and write.

Default value: 0

|         |                                       |
|---------|---------------------------------------|
| DSD = 0 | DSD interface mode disabled (default) |
| DSD = 1 | DSD interface mode enabled            |

The DSD bit is used to enable or disable the DSD interface mode.

**DFTH: Digital Filter Bypass (or Through Mode) Control**

This bit is available for read and write.

Default value: 0

|          |   |
|----------|---|
| DFTH = 0 | Digital filter enabled (default)                    |
| DFTH = 1 | Digital filter bypassed for external digital filter |

The DFTH bit is used to enable or disable the external digital filter interface mode.

**MONO: Monaural Mode Selection**

This bit is available for read and write.

Default value: 0

|          |                       |
|----------|-----------------------|
| MONO = 0 | Stereo mode (default) |
| MONO = 1 | Monaural mode         |

The MONO function is used to change operation mode from the normal stereo mode to the monaural mode. When the monaural mode is selected, both DACs operate in a balanced mode for one channel of audio input data. Channel selection is available for L-channel or R-channel data, determined by the CHSL bit as described immediately following.

**CHSL: Channel Selection for Monaural Mode**

This bit is available for read and write.

Default value: 0

|          |                              |
|----------|------------------------------|
| CHSL = 0 | L-channel selected (default) |
| CHSL = 1 | R-channel selected           |

This bit is available when MONO = 1.

The CHSL bit selects L-channel or R-channel data to be used in monaural mode.

**OS[1:0]: Delta-Sigma Oversampling Rate Selection**

These bits are available for read and write.

Default value: 00

| OS[1:0] | Operation Speed Select   |
|---------|--------------------------|
| 00      | 64 times $f_S$ (default) |
| 01      | 32 times $f_S$           |
| 10      | 128 times $f_S$          |
| 11      | Reserved                 |

The OS bits are used to change the oversampling rate of delta-sigma modulation. Use of this function enables the designer to stabilize the conditions at the post low-pass filter for different sampling rates. As an application example, programming to set 128 times in 44.1-kHz operation, 64 times in 96-kHz operation, and 32 times in 192-kHz operation allows the use of only a single type (cutoff frequency) of post low-pass filter. The 128  $f_S$  oversampling rate is not available at sampling rates above 100 kHz. If the 128- $f_S$  oversampling rate is selected, a system clock of more than 256  $f_S$  is required.

In DSD mode, these bits are used to select the speed of the bit clock for DSD data coming into the analog FIR filter.

|             | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7  | B6  | B5  | B4  | B3  | B2  | B1  | B0   |
|-------------|-----|-----|-----|-----|-----|-----|----|----|-----|-----|-----|-----|-----|-----|-----|------|
| Register 21 | R/W | 0   | 0   | 1   | 0   | 1   | 0  | 1  | RSV | RSV | RSV | RSV | RSV | DZ1 | DZ0 | PCMZ |

**R/W: Read/Write Mode Select**

When  $R/\overline{W} = 0$ , a write operation is performed.

When  $R/\overline{W} = 1$ , a read operation is performed.

Default value: 0

**DZ[1:0]: DSD Zero Output Enable**

These bits are available for read and write.

Default value: 00

| DZ[1:0] | Zero Output Enable  |
|---------|---------------------|
| 00      | Disabled (default)  |
| 01      | Even pattern detect |
| 1x      | 96h pattern detect  |

The DZ bits are used to enable or disable the output zero flags, and to select the zero pattern in the DSD mode.

**PCMZ: PCM Zero Output Enable**

These bits are available for read and write.

Default value: 1

|          |                                   |
|----------|-----------------------------------|
| PCMZ = 0 | PCM zero output disabled          |
| PCMZ = 1 | PCM zero output enabled (default) |

The PCMZ bit is used to enable or disable the output zero flags in the PCM mode and the external DF mode.

|             | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7  | B6  | B5  | B4  | B3  | B2  | B1   | B0   |
|-------------|-----|-----|-----|-----|-----|-----|----|----|-----|-----|-----|-----|-----|-----|------|------|
| Register 22 | R   | 0   | 0   | 1   | 0   | 1   | 1  | 0  | RSV | RSV | RSV | RSV | RSV | RSV | ZFGR | ZFGL |

**R: Read Mode Select**

Value is always 1, specifying the readback mode.

**ZFGx: Zero-Detection Flag**

Where x = L or R, corresponding to the DAC output channel. These bits are available only for readback.

Default value: 00

|          |               |
|----------|---------------|
| ZFGx = 0 | Not zero      |
| ZFGx = 1 | Zero detected |

These bits show zero conditions. Their status is the same as that of the zero flags at ZEROL (pin 1) and ZEROR (pin 2). See *Zero Detect* in the *FUNCTION DESCRIPTIONS* section.

|             | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7  | B6  | B5  | B4  | B3  | B2  | B1  | B0  |
|-------------|-----|-----|-----|-----|-----|-----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| Register 23 | R   | 0   | 0   | 1   | 0   | 1   | 1  | 1  | RSV | RSV | RSV | ID4 | ID3 | ID2 | ID1 | ID0 |

**R: Read Mode Select**

Value is always 1, specifying the readback mode.

**ID[4:0]: Device ID**

The ID[4:0] bits hold a device ID in the TDMCA mode.



APPLICATION INFORMATION

TYPICAL CONNECTION DIAGRAM IN PCM MODE

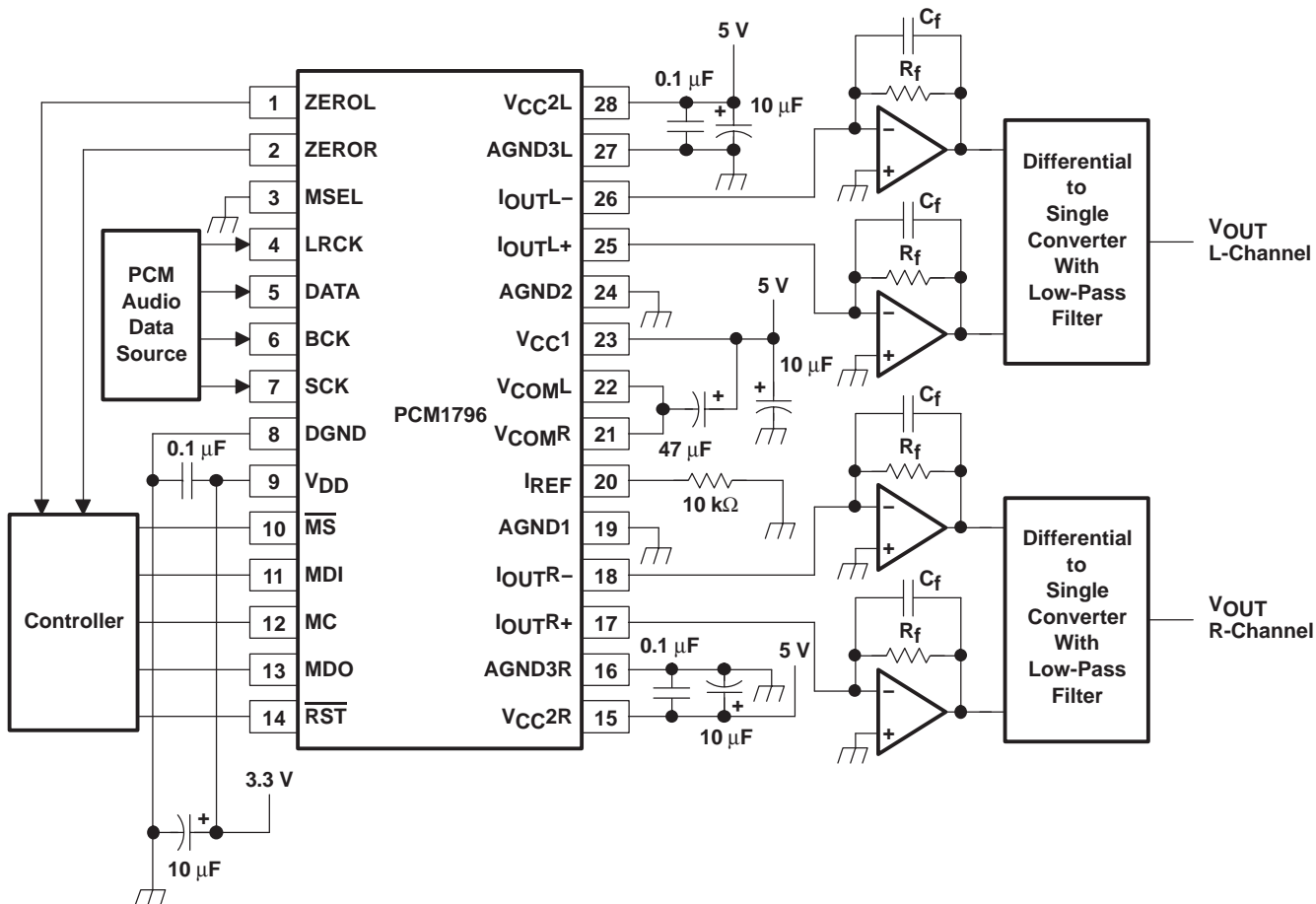


Figure 35. Typical Application Circuit for Standard PCM Audio Operation

APPLICATION CIRCUIT

The design of the application circuit is very important in order to actually realize the high S/N ratio of which the PCM1796 is capable. This is because noise and distortion that are generated in an application circuit are not negligible.

In the third-order LPF circuit of Figure 36, the output level is 2.1 V rms and 123 dB S/N is achieved.

Figure 37 shows a circuit for the DSD mode, which is a fourth-order LPF in order to reduce the out-of-band noise.

I/V Section

The current of the PCM1796 on each of the output pins ( $I_{OUTL+}$ ,  $I_{OUTL-}$ ,  $I_{OUTR+}$ ,  $I_{OUTR-}$ ) is 4 mA p-p at 0 dB (full scale). The voltage output level of the I/V converter ( $V_i$ ) is given by following equation:

$$V_i = 4 \text{ mA p-p} \times R_f \text{ (} R_f \text{ : feedback resistance of I/V converter)}$$

An NE5534 op amp is recommended for the I/V circuit to obtain the specified performance. Dynamic performance such as the gain bandwidth, settling time, and slew rate of the op amp affects the audio dynamic performance of the I/V section.

Differential Section

The PCM1796 voltage outputs are followed by differential amplifier stages, which sum the differential signals for each channel, creating a single-ended I/V op-amp output. In addition, the differential amplifiers provide a low-pass filter function.

The op amp recommended for the differential circuit is the low-noise type.

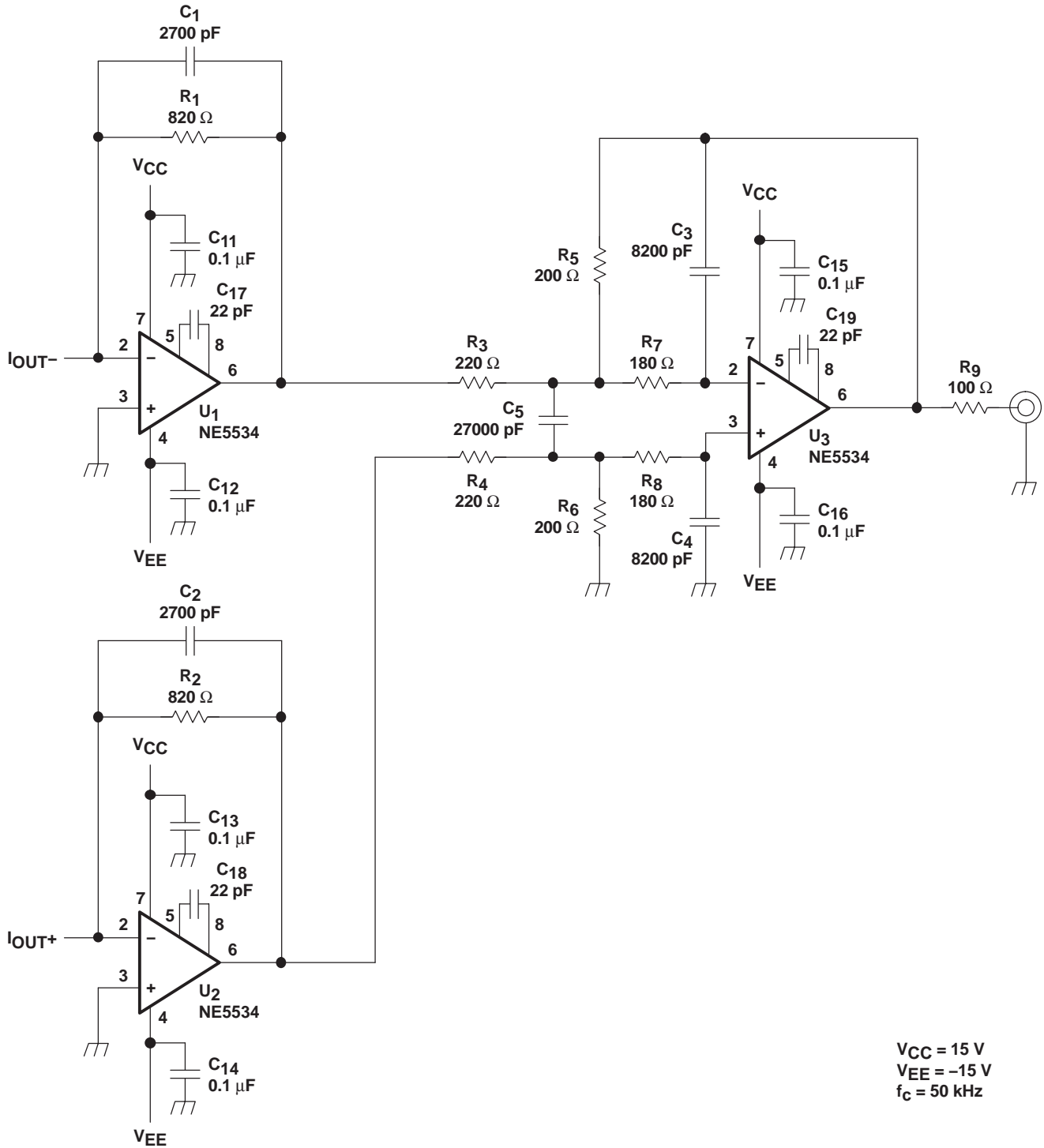


Figure 36. Measurement Circuit for PCM

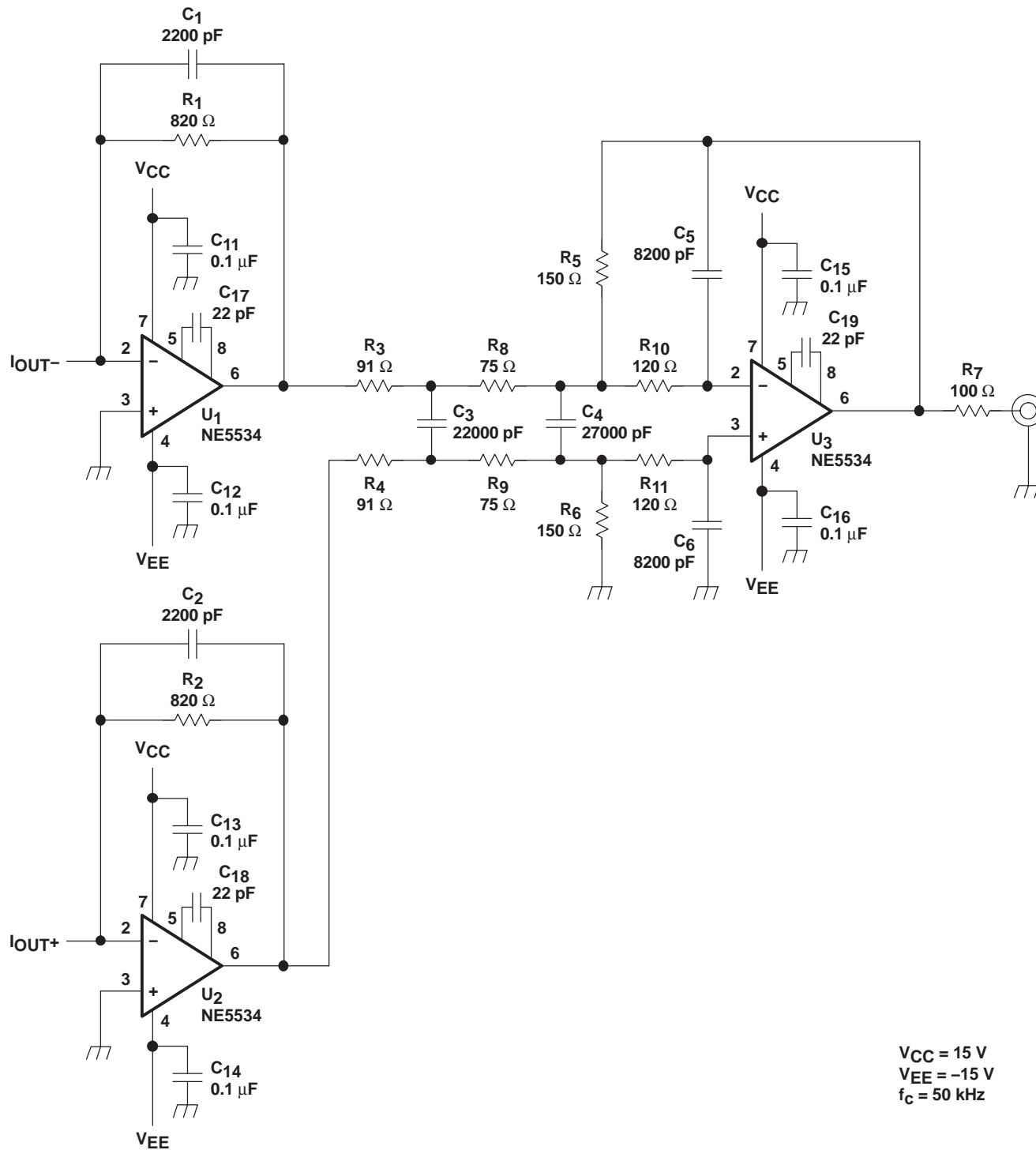


Figure 37. Measurement Circuit for DSD

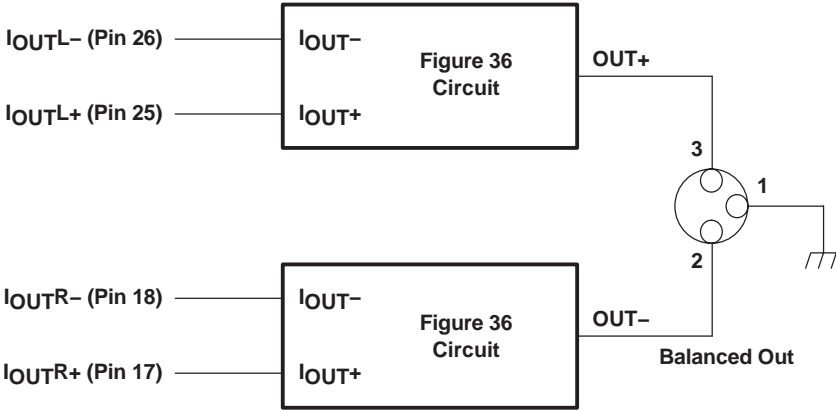
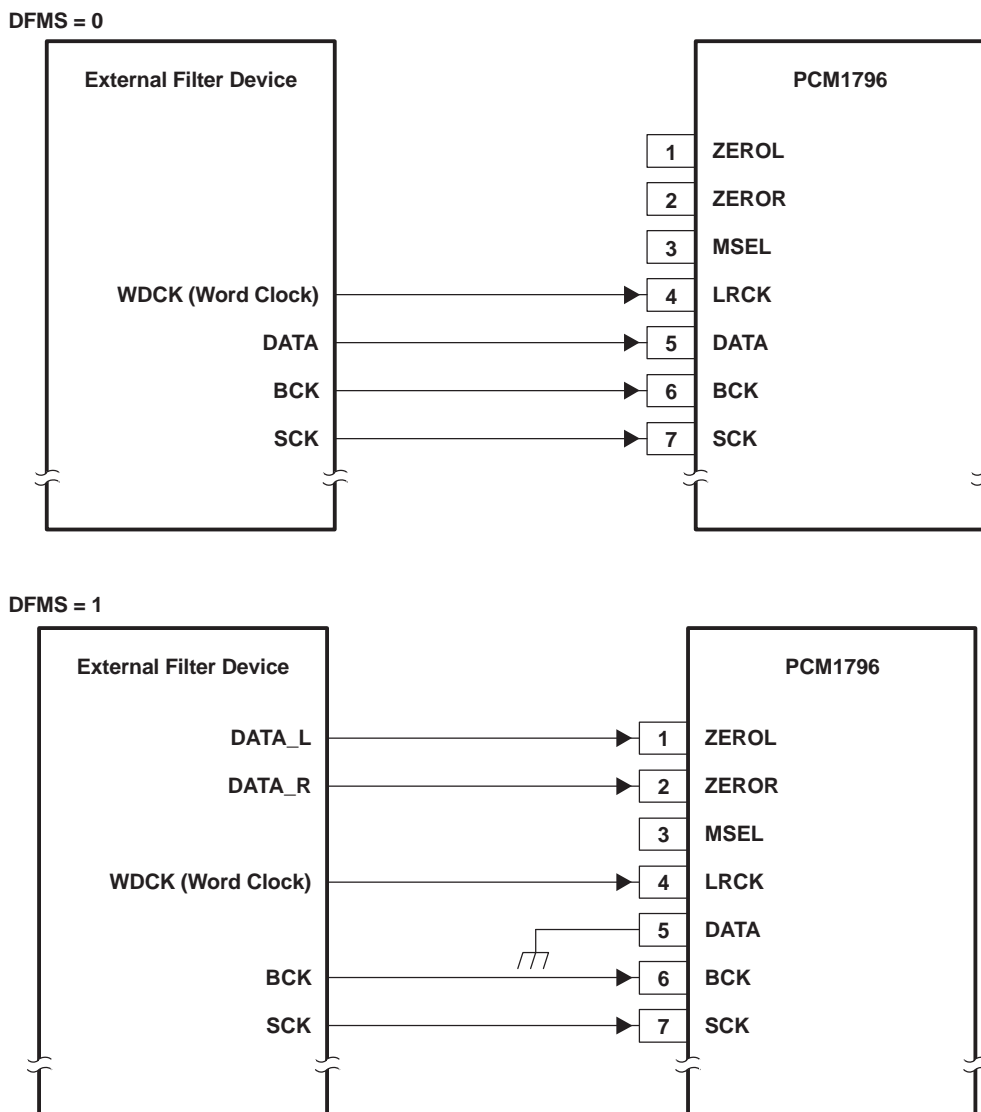


Figure 38. Measurement Circuit for Monaural Mode

**APPLICATION FOR EXTERNAL DIGITAL FILTER INTERFACE**



**Figure 39. Connection Diagram for External Digital Filter (Internal DF Bypass Mode) Application**

### Application for Interfacing With an External Digital Filter

For some applications, it may be desirable to use an external digital filter to perform the interpolation function, as it can provide improved stop-band attenuation when compared to the internal digital filter of the PCM1796.

The PCM1796 supports several external digital filters, including:

- Texas Instruments DF1704 and DF1706
- Pacific Microsonics PMD200 HDCD filter/decoder IC
- Programmable digital signal processors

The external digital filter application mode is accessed by programming the following bits in the corresponding control register:

- DFTH = 1 (register 20)

The pins used to provide the serial interface for the external digital filter are shown in the connection diagram of Figure 39. The word clock (WDCK) signal must be operated at  $8\times$  or  $4\times$  the desired sampling frequency,  $f_s$ .

### Pin Assignment When Using the External Digital Filter Interface

- LRCK (pin 4): WDCK as word clock input
- BCK (pin 6): Bit clock for audio data
- DATA (pin 5): Monaural audio data input when the DFMS bit is not set to 1
- ZEROL (pin 1): DATAL as L-channel audio data input when the DFMS bit is set to 1
- ZEROR (pin 2): DATAR as R-channel audio data input when the DFMS bit is set to 1

## Audio Format

The PCM1796 in the external digital filter interface mode supports right-justified audio formats including 16-bit, 20-bit, and 24-bit audio data, as shown in Figure 40. The audio format is selected by the FMT[2:0] bits of control register18.

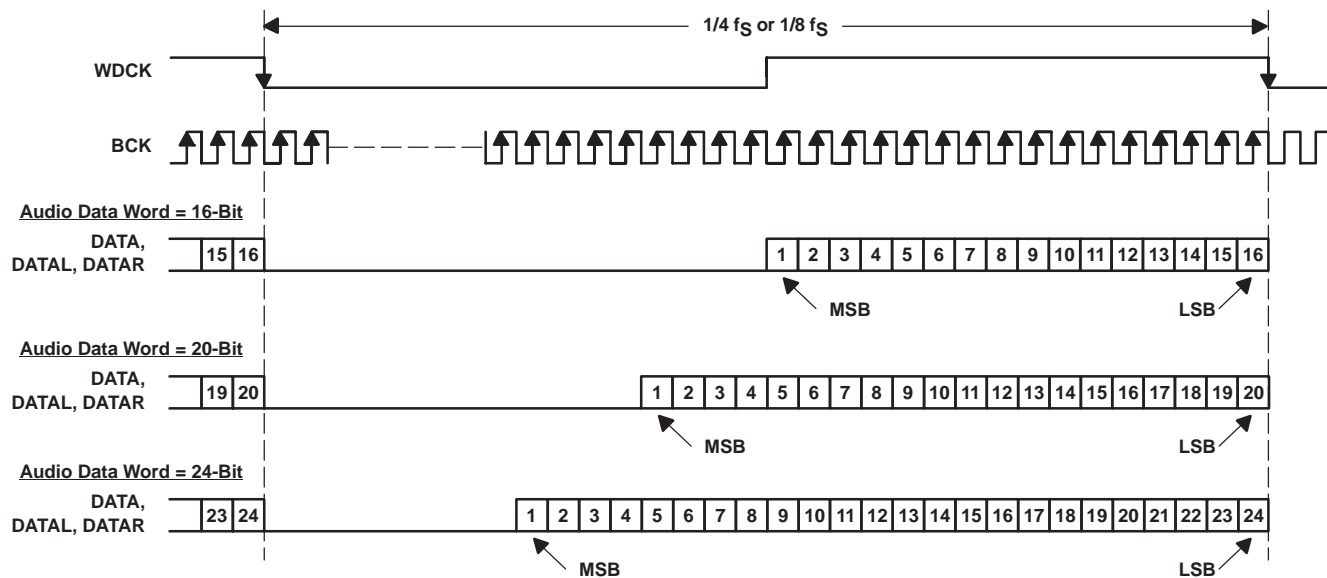
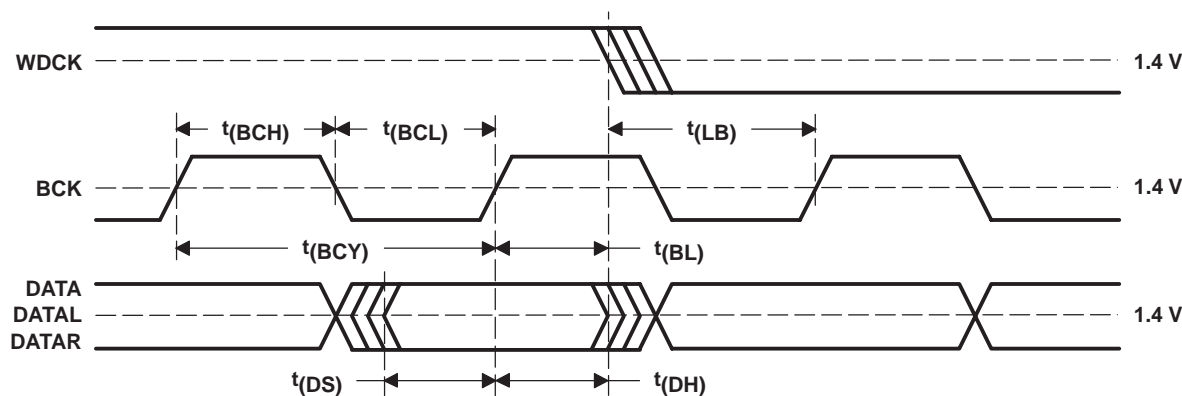


Figure 40. Audio Data Input Format for External Digital Filter (Internal DF Bypass Mode) Application

## System Clock (SCK) and Interface Timing

The PCM1796 in an application using an external digital filter requires the synchronization of WDCK and the system clock. The system clock is phase-free with respect to WDCK. Interface timing among WDCK, BCK, DATA, DATAL, and DATAR is shown in Figure 41.



| PARAMETER                                  | MIN | MAX | UNITS |
|--|-----|-----|-------|
| t(BCY) BCK pulse cycle time                | 20  |     | ns    |
| t(BCL) BCK pulse duration, LOW             | 7   |     | ns    |
| t(BCH) BCK pulse duration, HIGH            | 7   |     | ns    |
| t(BL) BCK rising edge to WDCK falling edge | 5   |     | ns    |
| t(LB) WDCK falling edge to BCK rising edge | 5   |     | ns    |
| t(DS) DATA, DATAL, DATAR setup time        | 5   |     | ns    |
| t(DH) DATA, DATAL, DATAR hold time         | 5   |     | ns    |

Figure 41. Audio Interface Timing for External Digital Filter (Internal DF Bypass Mode) Application

## FUNCTIONS AVAILABLE IN THE EXTERNAL DIGITAL FILTER MODE

The external digital filter mode is selected by setting DSD = 0 (register 20, B5) and DFTH = 1 (register 20, B4).

The external digital filter mode allows access to the majority of the PCM1796 mode control functions.

The following table shows the register mapping available when the external digital filter mode is selected, along with descriptions of functions which are modified when using this mode selection.

|             | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7  | B6   | B5   | B4   | B3   | B2   | B1   | B0   |
|-------------|-----|-----|-----|-----|-----|-----|----|----|-----|------|------|------|------|------|------|------|
| Register 16 | R/W | 0   | 0   | 1   | 0   | 0   | 0  | 0  | –   | –    | –    | –    | –    | –    | –    | –    |
| Register 17 | R/W | 0   | 0   | 1   | 0   | 0   | 0  | 1  | –   | –    | –    | –    | –    | –    | –    | –    |
| Register 18 | R/W | 0   | 0   | 1   | 0   | 0   | 1  | 0  | –   | FMT2 | FMT1 | FMT0 | –    | –    | –    | –    |
| Register 19 | R/W | 0   | 0   | 1   | 0   | 0   | 1  | 1  | REV | –    | –    | OPE  | –    | DFMS | –    | INZD |
| Register 20 | R/W | 0   | 0   | 1   | 0   | 1   | 0  | 0  | –   | SRST | 0    | 1    | MONO | CHSL | OS1  | OS0  |
| Register 21 | R/W | 0   | 0   | 1   | 0   | 1   | 0  | 1  | –   | –    | –    | –    | –    | –    | –    | PCMZ |
| Register 22 | R   | 0   | 0   | 1   | 0   | 1   | 1  | 0  | –   | –    | –    | –    | –    | –    | ZFGR | ZFGL |

NOTE: –: Function is disabled. No operation even if data bit is set

### FMT[2:0]: Audio Data Format Selection

Default value: 000

| FMT[2:0] | Audio Data Format Select                |
|----------|---|
| 000      | 16-bit right-justified format (default) |
| 001      | 20-bit right-justified format           |
| 010      | 24-bit right-justified format           |
| Other    | N/A                                     |

### OS[1:0]: Delta-Sigma Modulator Oversampling Rate Selection

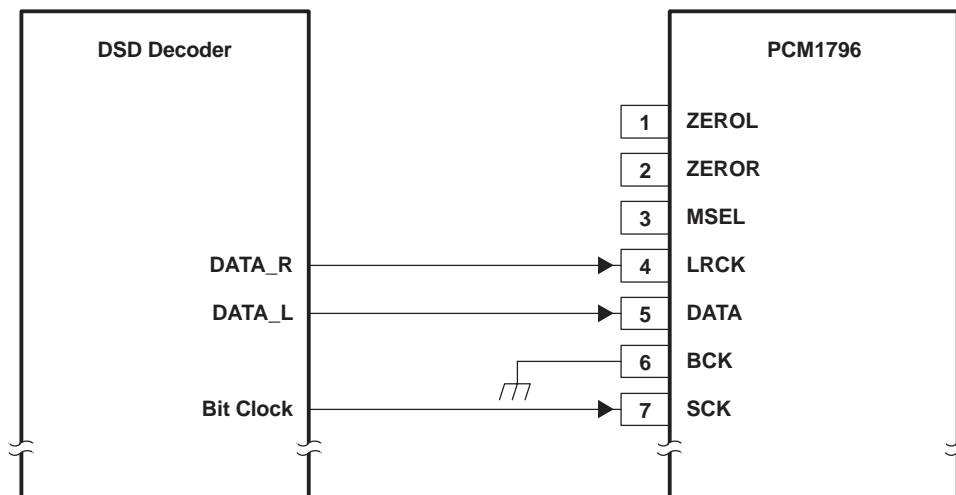
Default value: 00

| OS[1:0] | Operation Speed Select |
|---------|------------------------|
| 00      | 8 times WDCK (default) |
| 01      | 4 times WDCK           |
| 10      | 16 times WDCK          |
| 11      | Reserved               |

The effective oversampling rate is determined by the oversampling performed by both the external digital filter and the delta-sigma modulator. For example, if the external digital filter is 8× oversampling, and the user selects OS[1:0] = 00, then the delta-sigma modulator oversamples by 8×, resulting in an effective oversampling rate of 64×. The 16× WDCK oversampling rate is not available above a 100-kHz sampling rate. If the oversampling rate selected is 16× WDCK, the system clock frequency must be over 256 f<sub>S</sub>.



## APPLICATION FOR DSD FORMAT (DSD MODE) INTERFACE



**Figure 42. Connection Diagram in DSD Mode**

### Feature

This mode is used for interfacing directly to a DSD decoder, which is found in Super Audio CD™ (SACD) applications. The DSD mode is accessed by programming the following bit in the corresponding control register.

DSD = 1 (register 20)

The DSD mode provides a low-pass filtering function. The filtering is provided using an analog FIR filter structure. Four FIR responses are available, and are selected by the DMF[1:0] bits of control register 18.

The DSD bit must be set before inputting DSD data; otherwise, the PCM1796 erroneously detects the TDMCA mode, and commands are not accepted through the serial control interface.

### Pin Assignment When Using DSD Format Interface

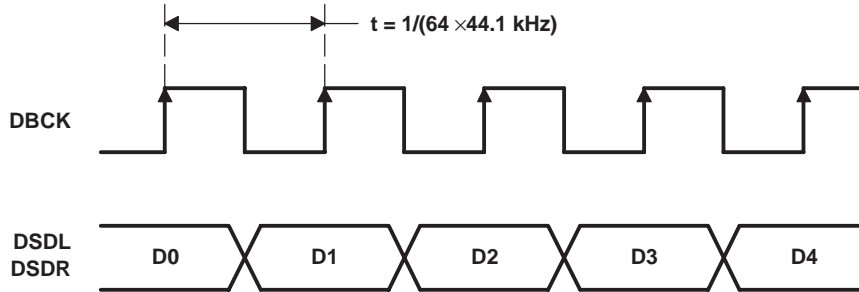
Several pins are redefined for DSD mode operation. These include:

- DATA (pin 5): DSDL as L-channel DSD data input
- LRCK (pin 4): DSDR as R-channel DSD data input
- SCK (pin 7): DBCK as bit clock for DSD data
- BCK (pin 6): Set LOW (N/A)

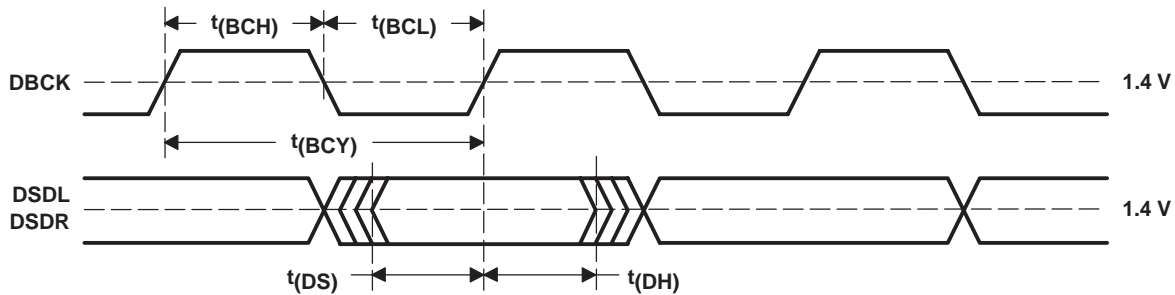
**Requirements for System Clock**

For operation in the DSD mode, the bit clock (DBCK) is required on pin 7 of the PCM1796. The frequency of the bit clock can be N times the sampling frequency. Generally, N is 64 in DSD applications.

The interface timing between the bit clock and DSDL and DSDR is required to meet the setup and hold time specifications shown in Figure 44.



**Figure 43. Normal Data Output Form From DSD Decoder**

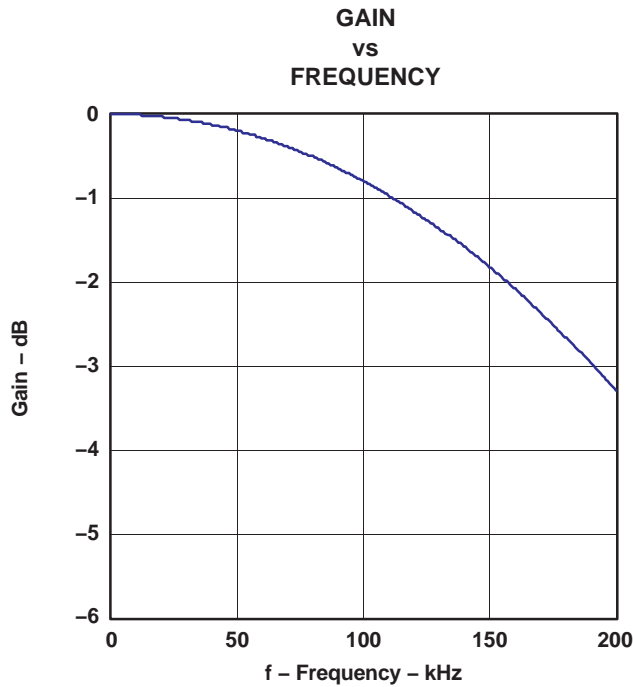


| PARAMETER                    | MIN               | MAX | UNITS |
|------------------------------|-------------------|-----|-------|
| t(BCY) DBCK pulse cycle time | 85 <sup>(1)</sup> |     | ns    |
| t(BCH) DBCK high-level time  | 30                |     | ns    |
| t(BCL) DBCK low-level time   | 30                |     | ns    |
| t(DS) DSDL, DSDR setup time  | 10                |     | ns    |
| t(DH) DSDL, DSDR hold time   | 10                |     | ns    |

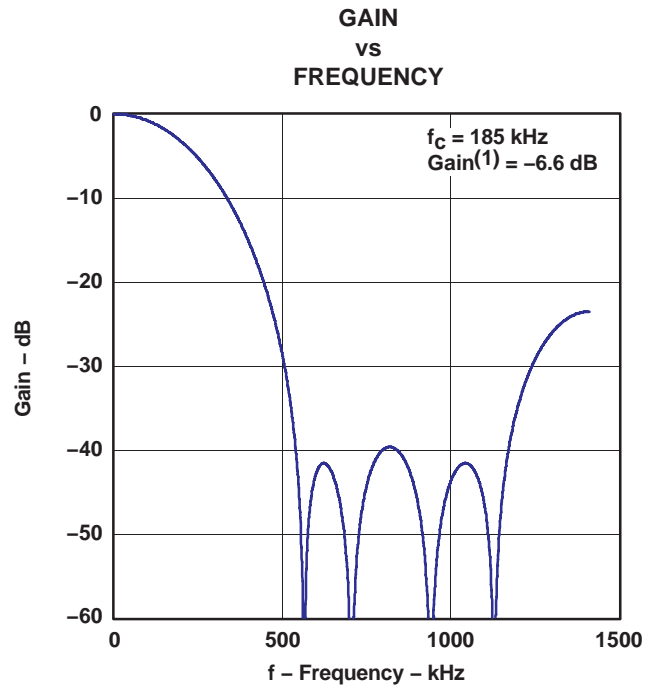
<sup>(1)</sup> 2.8224 MHz × 4. (2.8224 MHz = 64 × 44.1 kHz. This value is specified as a sampling rate of DSD.)

**Figure 44. Timing for DSD Audio Interface**

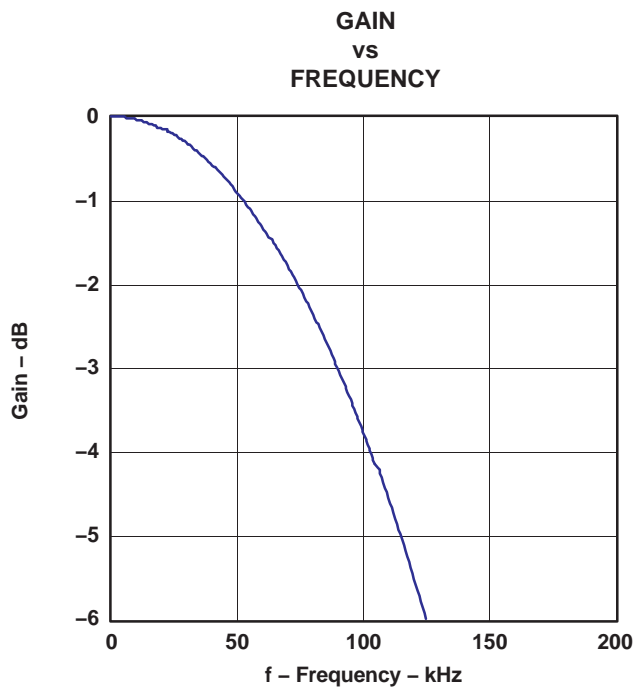
**ANALOG FIR FILTER PERFORMANCE IN DSD MODE**



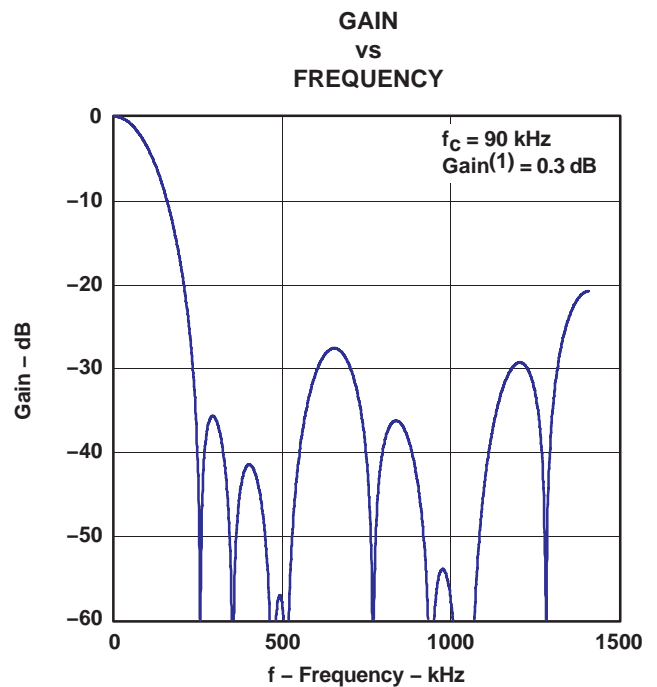
**Figure 45. DSD Filter-1, Low BW**



**Figure 46. DSD Filter-1, High BW**



**Figure 47. DSD Filter-2, Low BW**



**Figure 48. DSD Filter-2, High BW**

(1) This gain is in comparison to PCM 0 dB, when the DSD input signal efficiency is 50%.

ANALOG FIR FILTER PERFORMANCE IN DSD MODE (CONTINUED)

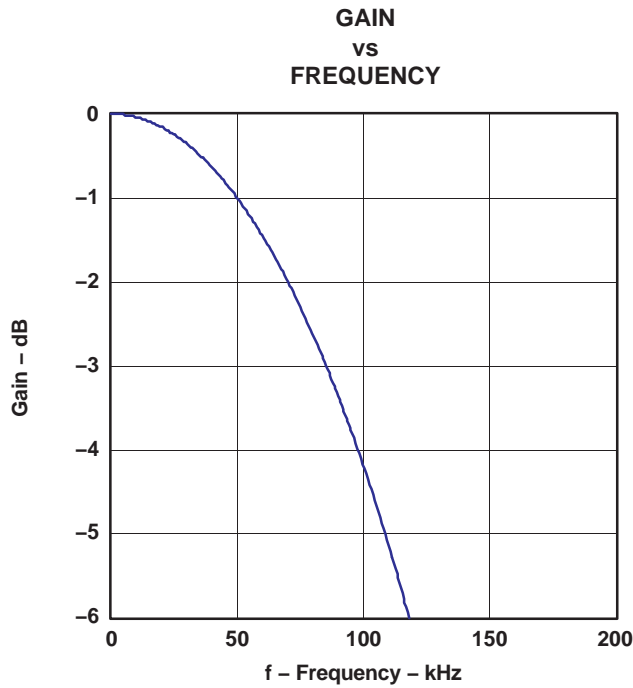


Figure 49. DSD Filter-3, Low BW

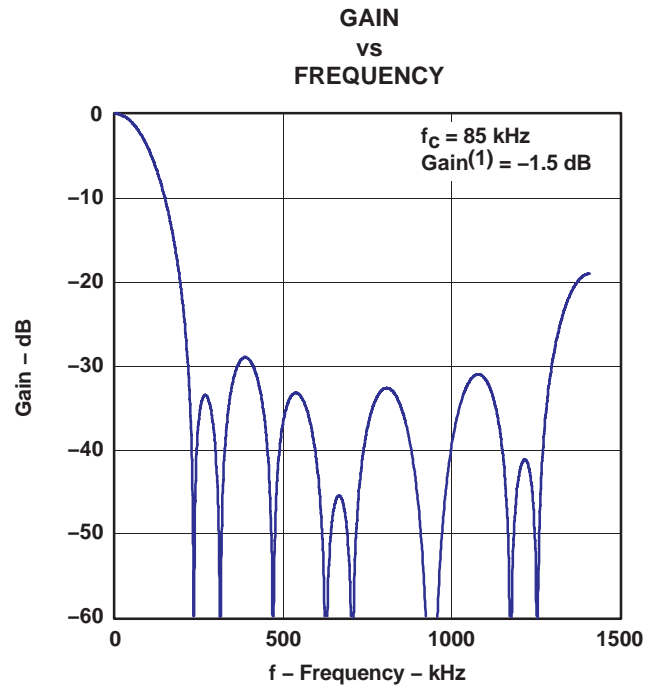


Figure 50. DSD Filter-3, High BW

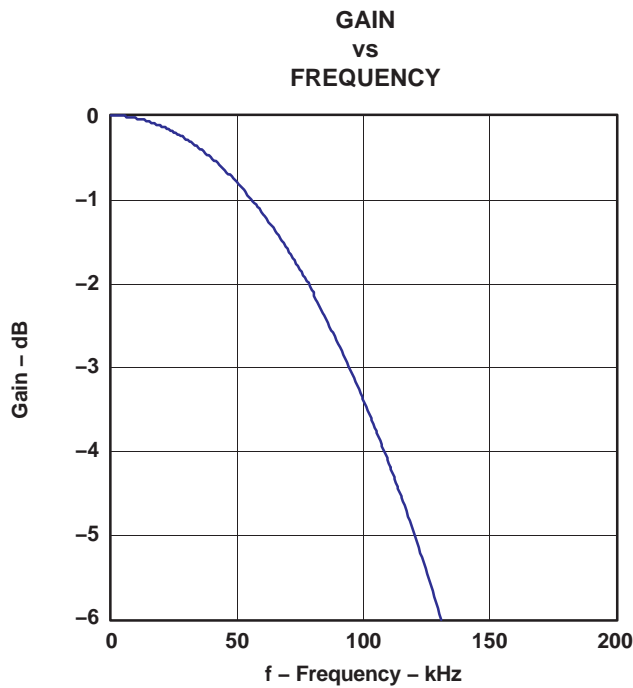


Figure 51. DSD Filter-4, Low BW

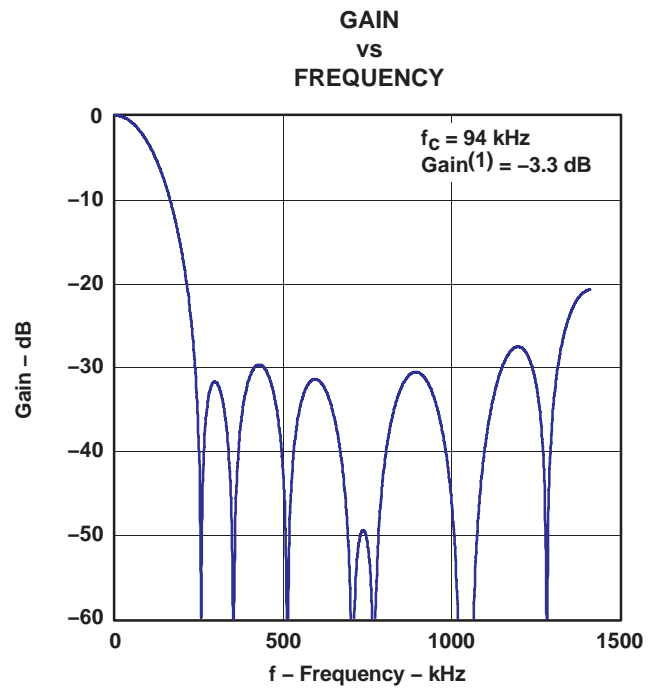


Figure 52. DSD Filter-4, High BW

(1) This gain is in comparison to PCM 0 dB, when the DSD input signal efficiency is 50%.

## DSD MODE CONFIGURATION AND FUNCTION CONTROLS

### Configuration for the DSD Interface Mode

The DSD interface mode is selected by setting DSD = 1 (register 20, B5).

|                    | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7  | B6   | B5 | B4  | B3   | B2   | B1   | B0   |
|--------------------|-----|-----|-----|-----|-----|-----|----|----|-----|------|----|-----|------|------|------|------|
| <b>Register 16</b> | R/W | 0   | 0   | 1   | 0   | 0   | 0  | 0  | –   | –    | –  | –   | –    | –    | –    | –    |
| <b>Register 17</b> | R/W | 0   | 0   | 1   | 0   | 0   | 0  | 1  | –   | –    | –  | –   | –    | –    | –    | –    |
| <b>Register 18</b> | R/W | 0   | 0   | 1   | 0   | 0   | 1  | 0  | –   | –    | –  | –   | DMF1 | DMF0 | –    | –    |
| <b>Register 19</b> | R/W | 0   | 0   | 1   | 0   | 0   | 1  | 1  | REV | –    | –  | OPE | –    | –    | –    | –    |
| <b>Register 20</b> | R/W | 0   | 0   | 1   | 0   | 1   | 0  | 0  | –   | SRST | 1  | –   | MONO | CHSL | OS1  | OS0  |
| <b>Register 21</b> | R   | 0   | 0   | 1   | 0   | 1   | 0  | 1  | –   | –    | –  | –   | –    | DZ1  | DZ0  | –    |
| <b>Register 22</b> | R   | 0   | 0   | 1   | 0   | 1   | 1  | 0  | –   | –    | –  | –   | –    | –    | ZFGR | ZFGL |

NOTE: –: Function is disabled. No operation even if data bit is set

### DMF[1:0]: Analog-FIR Performance Selection

Default value: 00

| DMF[1:0] | Analog-FIR Performance Select |
|----------|-------------------------------|
| 00       | FIR-1 (default)               |
| 01       | FIR-2                         |
| 10       | FIR-3                         |
| 11       | FIR-4                         |

Plots for the four analog FIR filter responses are shown in the *ANALOG FIR FILTER PERFORMANCE IN DSD MODE* section of this data sheet.

### OS[1:0]: Analog-FIR Operation-Speed Selection

Default value: 00

| OS[1:0] | Operation-Speed Select |
|---------|------------------------|
| 00      | $f_{DBCK}$ (default)   |
| 01      | $f_{DBCK}/2$           |
| 10      | Reserved               |
| 11      | $f_{DBCK}/4$           |

The OS bit in the DSD mode is used to select the operating rate of the analog FIR. The OS bits must be set before setting the DSD bit to 1.

## TDMCA INTERFACE FORMAT

The PCM1796 supports the time-division-multiplexed command and audio (TDMCA) data format to simplify the host control serial interface. The TDMCA format is designed not only for the McBSP of TI DSPs but also for any programmable devices. The TDMCA format can transfer not only audio data but also command data, so that it can be used together with any kind of device that supports the TDMCA format. The TDMCA frame consists of a command field, extended command field, and some audio data fields. Those audio data are transported to IN devices (such as a DAC) and/or from OUT devices (such as an ADC). The PCM1796 is an IN device. LRCK and BCK are used with both IN and OUT devices so that the sample frequency of all devices in a system must be the same. The TDMCA mode supports a maximum of 30 device IDs. The maximum number of audio channels depends on the BCK frequency.

### TDMCA Mode Determination

The PCM1796 recognizes the TDMCA mode automatically when it receives an LRCK signal with a pulse duration of two BCK clocks. If the TDMCA mode operation is not needed, the duty cycle of LRCK must be 50%. Figure 53 shows the LRCK and BCK timing that determines the TDMCA mode. The PCM1796 enters the TDMCA mode after two continuous TDMCA frames. Any TDMCA commands can be issued during the next TDMCA frame after the TDMCA mode is entered.

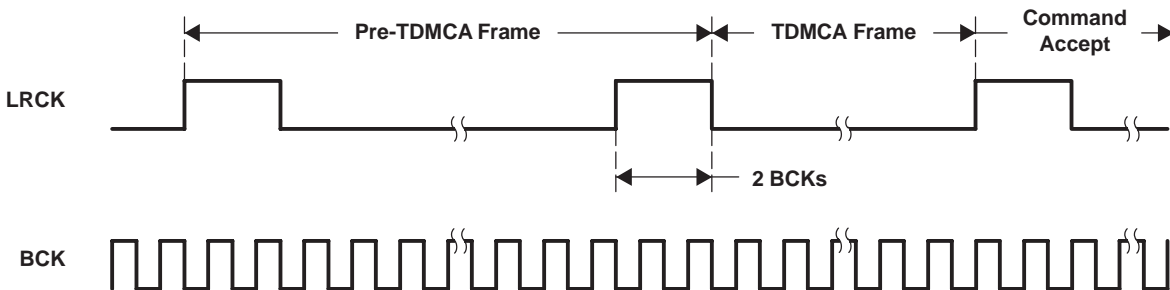


Figure 53. LRCK and BCK Timing for Determination of TDMCA Mode

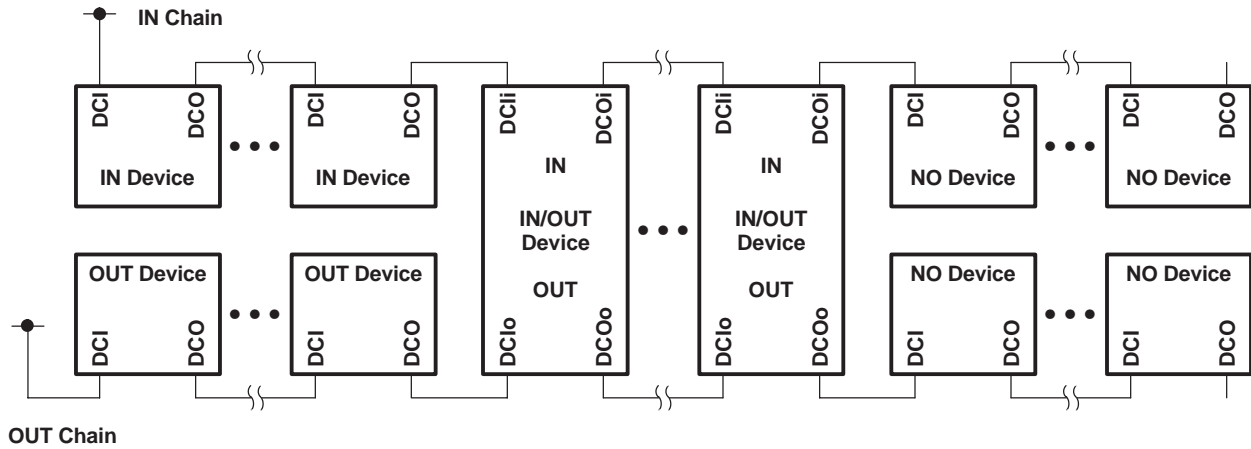
### TDMCA Terminals

TDMCA requires six signals, of which four signals are for command and audio data interface, and one pair for daisy chaining. Those signals can be shared as in the following table. The DO signal has a 3-state output so that it can be connected directly to other devices.

| TERMINAL NAME          | TDMCA NAME | PROPERTY | DESCRIPTION   |
|------------------------|------------|----------|---|
| LRCK                   | LRCK       | input    | TDMCA frame start signal. It must be the same as the sampling frequency.                          |
| BCK                    | BCK        | input    | TDMCA clock. Its frequency must be high enough to communicate a TDMCA frame within an LRCK cycle. |
| DATA                   | DI         | input    | TDMCA command and audio data input signal   |
| MDO                    | DO         | output   | TDMCA command data 3-state output signal  |
| MC                     | DCI        | input    | TDMCA daisy-chain input signal  |
| $\overline{\text{MS}}$ | DCO        | output   | TDMCA daisy-chain output signal   |

### Device ID Determination

The TDMCA mode also supports a multichip implementation in one system. This means a host controller (DSP) can simultaneously support several TDMCA devices, which can be of the same type or different types, including PCM devices. The PCM devices are categorized as IN device, OUT device, IN/OUT device, and NO device. The IN device has an input port to receive audio data, the OUT device has an output port to supply audio data, the IN/OUT device has both input and output ports for audio data, and the NO device has no port for audio data but needs command data from the host. A DAC is an IN device, an ADC is an OUT device, a codec is an IN/OUT device, and a PLL is a NO device. The PCM1796 is an IN device. For the host controller to distinguish the devices, each device is assigned its own device ID by the daisy chain. The devices obtain their own device IDs automatically by connecting their DCI to the DCO of the preceding device and their DCO to the DCI of the following device in the daisy chain. The daisy chains are categorized as the IN chain and the OUT chain, which are completely independent and equivalent. Figure 54 shows an example daisy chain connection. If a system needs to chain the PCM1796 and a NO device in the same IN or OUT chain, the NO device must be chained at the back end of the chain because it does not require any audio data. Figure 55 shows an example of TDMCA system including an IN chain and an OUT chain with a TI DSP. For a device to get its own device ID, the DID signal must be set to 1 (see the *Command Field* section for details), and LRCK and BCK must be driven in the TDMCA mode for all PCM devices that are chained. The device at the top of the chain knows its device ID is 1 because its DCI is fixed HIGH. Other devices count the BCK pulses and observe their own DCI signal to determine their position and ID. Figure 56 shows the initialization of each device ID.



**Figure 54. Daisy Chain Connection**

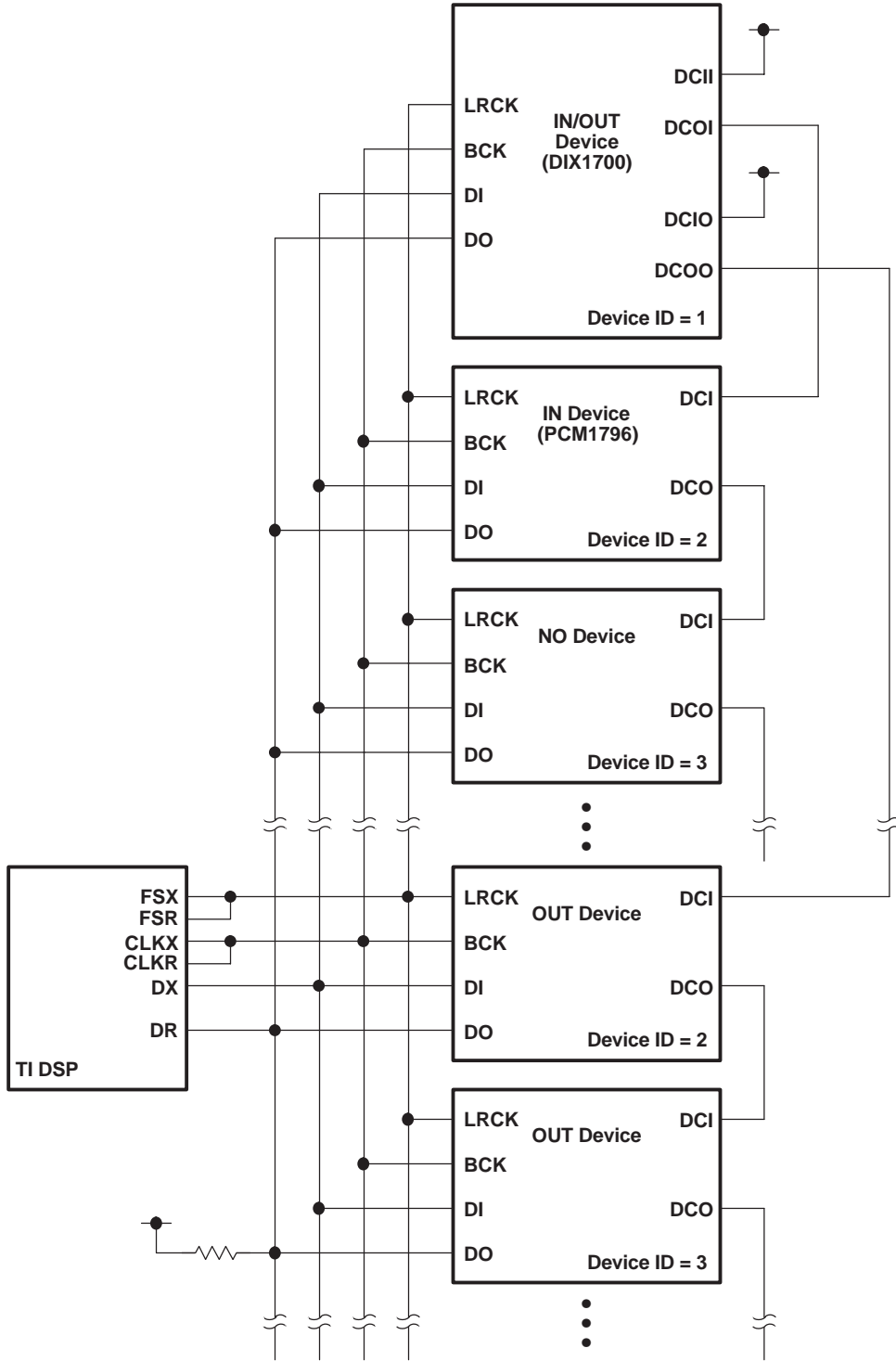


Figure 55. IN Daisy Chain and OUT Daisy Chain Connection for a Multichip System



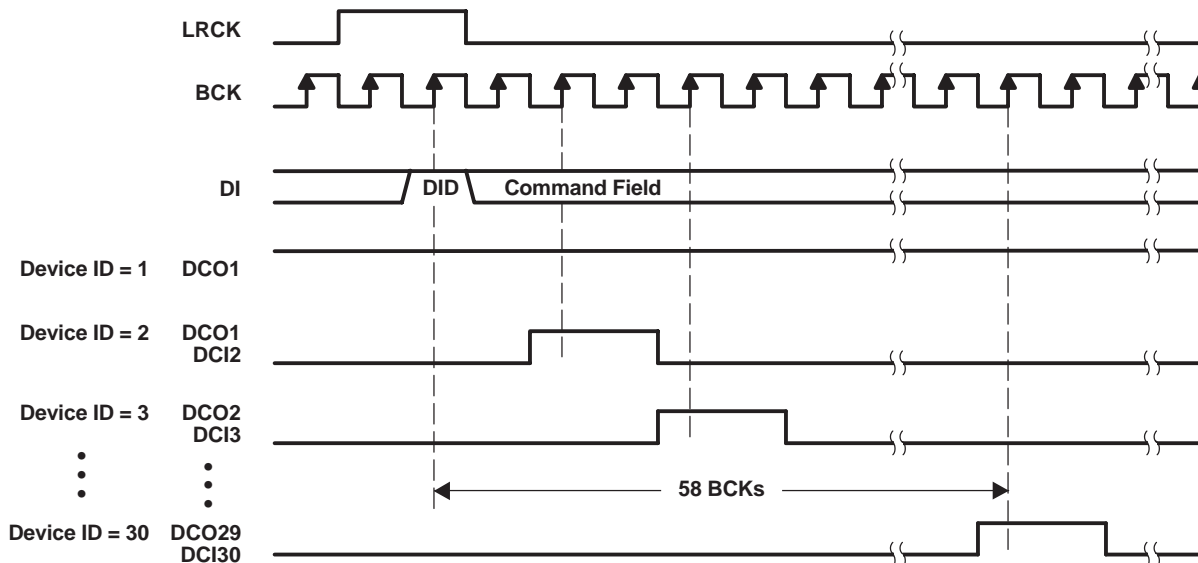


Figure 56. Device ID Determination Sequence

### TDMCA Frame

In general, the TDMCA frame consists of the command field, extended command (EMD) field, and audio data fields. All of them are 32 bits in length, but the lowest byte has no meaning. The MSB is transferred first for each field. The command field is always transferred as the first packet of the frame. The EMD field is transferred if the EMD flag of the command field is HIGH. If any EMD packets are transferred, no audio data follows the EMD packets. This frame is for quick system initialization. All devices of a daisy chain should respond to the command field and extended command field. The PCM1796 has two audio channels that can be selected by OPE (register 19). If the OPE bit is not set to HIGH, those audio channels are transferred. Figure 57 shows the general TDMCA frame. If some DACs are enabled, but corresponding audio data packets are not transferred, the analog outputs are unpredictable.



Figure 57. General TDMCA Frame

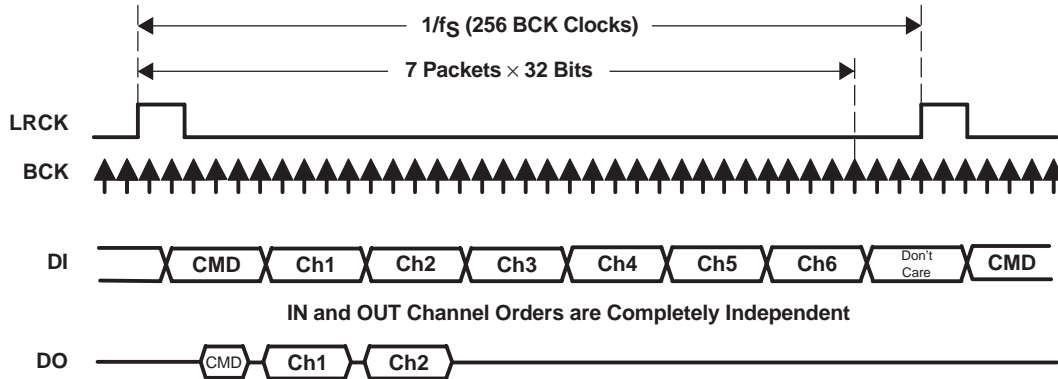


Figure 58. TDMCA Frame Example of 6-Ch DAC and 2-Ch ADC With Command Read

**Command Field**

The normal command field is defined as follows. When the DID bit (MSB) is 1, this frame is used only for device ID determination, and all remaining bits in the field are ignored.

|         |     |     |     |           |     |             |    |      |    |   |   |          |
|---------|-----|-----|-----|-----------|-----|-------------|----|------|----|---|---|----------|
|         | 31  | 30  | 29  | 28        | 24  | 23          | 22 | 16   | 15 | 8 | 7 | 0        |
| command | DID | EMD | DCS | device ID | R/W | register ID |    | data |    |   |   | not used |

**Bit 31: Device ID enable flag**

The PCM1796 operates to get its own device ID for TDMCA initialization if this bit is HIGH.

**Bit 30: Extended command enable flag**

The EMD packet is transferred if this bit is HIGH, otherwise skipped. Once this bit is HIGH, this frame does not contain any audio data. This is for system initialization.

**Bit 29: Daisy chain selection flag**

HIGH designates OUT-chain devices, LOW designates IN-chain devices. The PCM1796 is an IN device, so the DCS bit must be set to LOW.

**Bits[28:24]: Device ID**

The device ID is 5 bits length, and it can be defined. These bits identify the order of a device in the IN or OUT daisy chain. The top of the daisy chain defines device ID 1 and successive devices are numbered 2, 3, 4, etc. All devices for which the DCI is fixed HIGH are also defined as ID 1. The maximum device ID is 30 each in the IN and OUT chains. If a device ID of 0x1F is used, all devices are selected as broadcast when in the write mode. If a device ID of 0x00 is used, no device is selected.

**Bit 23: Command Read/Write flag**

If this bit is HIGH, the command is a read operation.

**Bits[22:16]: Register ID**

It is 7 bits in length.

**Bits[15:8]: Command data**

It is 8 bits in length. Any valid data can be chosen for each register.

**Bits[7:0]: Not used**

These bits are never transported when a read operation is performed.

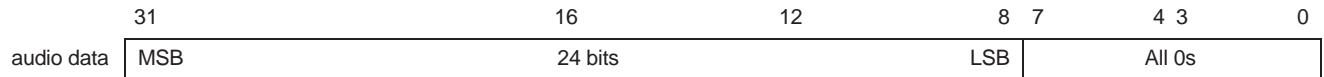
**Extended command field**

The extended command field is the same as the command field, except that it does not have a DID flag.

|                  |      |     |     |           |     |             |    |      |    |   |   |          |
|------------------|------|-----|-----|-----------|-----|-------------|----|------|----|---|---|----------|
|                  | 31   | 30  | 29  | 28        | 24  | 23          | 22 | 16   | 15 | 8 | 7 | 0        |
| extended command | rsvd | EMD | DCS | device ID | R/W | register ID |    | data |    |   |   | not used |

### Audio Fields

The audio field is 32 bits in length and the audio data is transferred MSB first, so the other fields must be stuffed with 0s as shown in the following example.



### TDMCA Register Requirements

TDMCA mode requires device ID and audio channel information, previously described. The OPE bit in register 19 indicates audio channel availability and register 23 indicates the device ID. Register 23 is used only in the TDMCA mode. See the mode control register map (Table 4).

### Register Write/Read Operation

The command supports register write and read operations. If the command requests to read one register, the read data is transferred on DO during the data phase of the timing cycle. The DI signal can be retrieved at the positive edge of BCK, and the DO signal is driven at the negative edge of BCK. DO is activated one BCK cycle early to compensate for the output delay caused by high impedance. Figure 59 shows the TDMCA write and read timing.

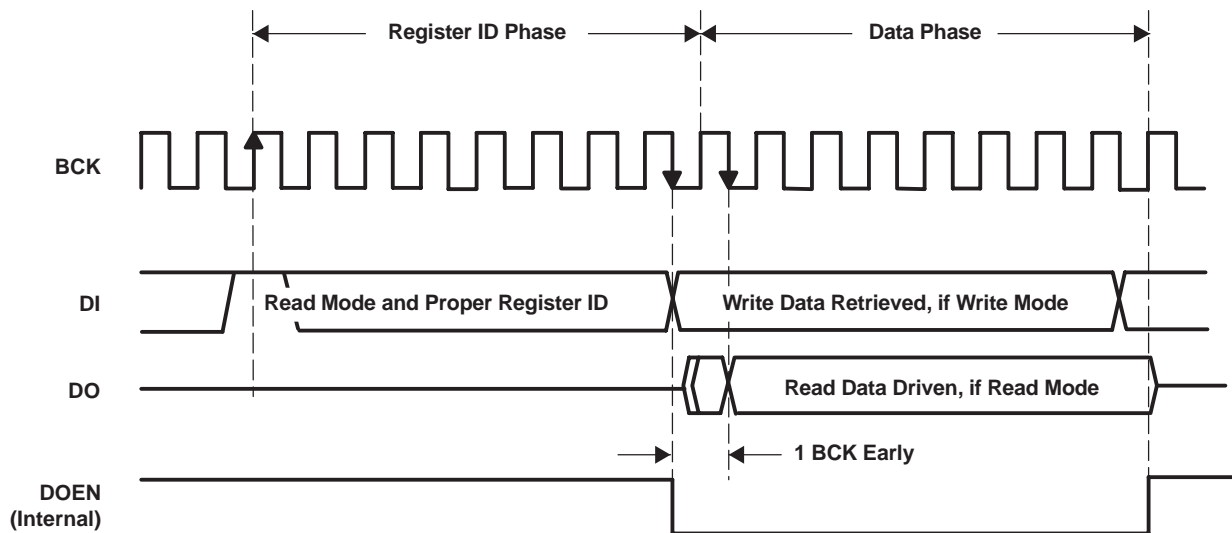


Figure 59. TDMCA Write and Read Operation Timing

### TDMCA-Mode Operation

DCO specifies the owner of the next audio channel in TDMCA-mode operation. When a device retrieves its own audio channel data, DCO goes HIGH during the last audio channel period. Figure 60 shows the DCO output timing in TDMCA-mode operation. The host controller ignores the behavior of DCI and DCO. DCO indicates the last audio channel of each device. Therefore, DCI means the next audio channel is allocated.

If some devices are skipped due to no active audio channel, the skipped devices must notify the next device that the DCO will be passed through the next DCI. Figure 61 and Figure 62 show DCO timing with skip operation. Figure 63 shows the ac timing of the daisy chain signals.

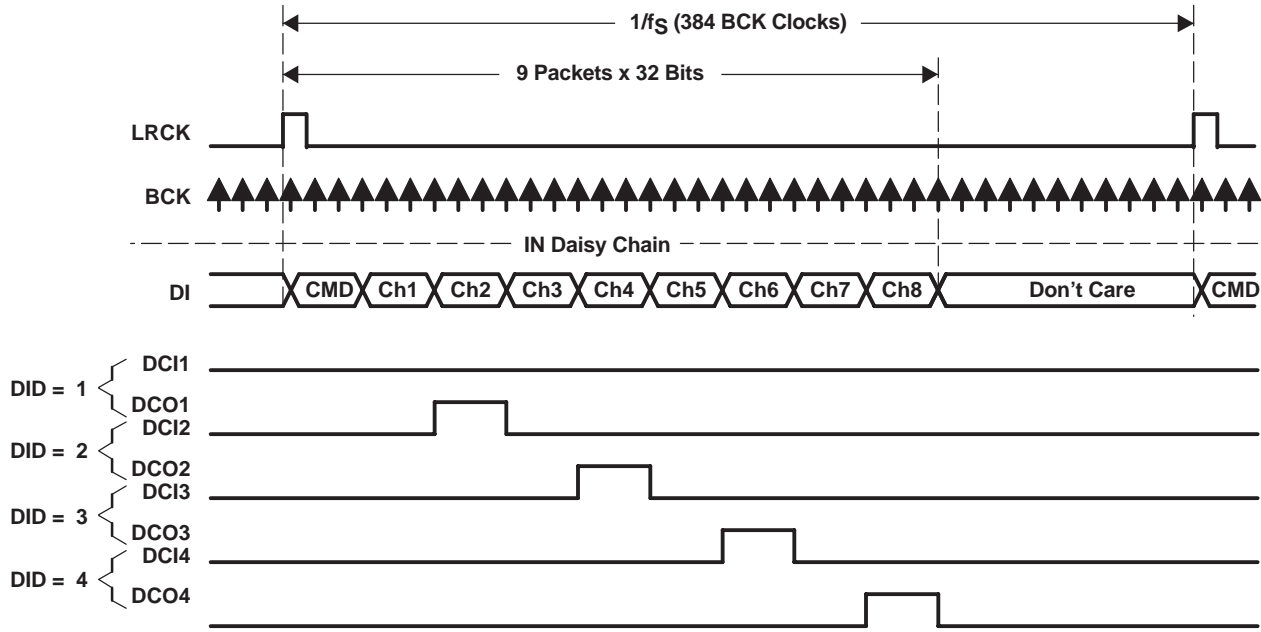


Figure 60. DCO Output Timing of TDMCA Mode Operation

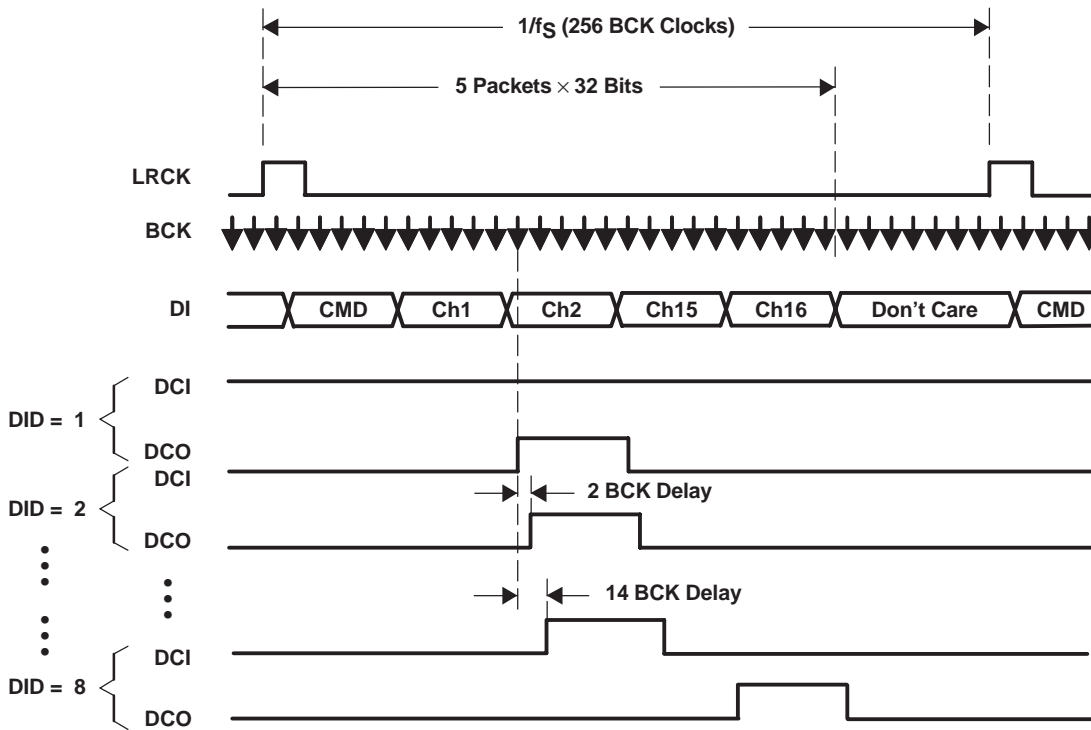


Figure 61. DCO Output Timing With Skip Operation

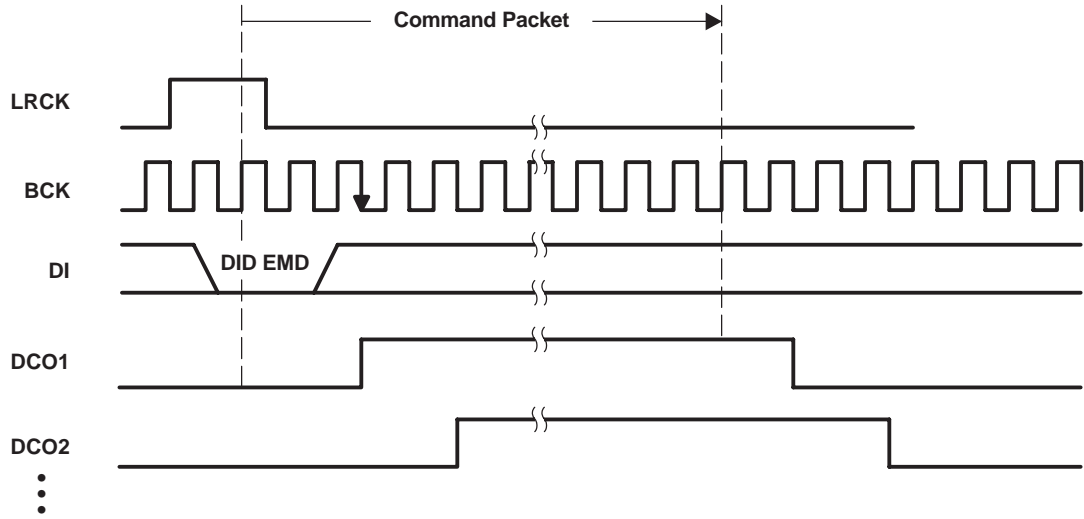
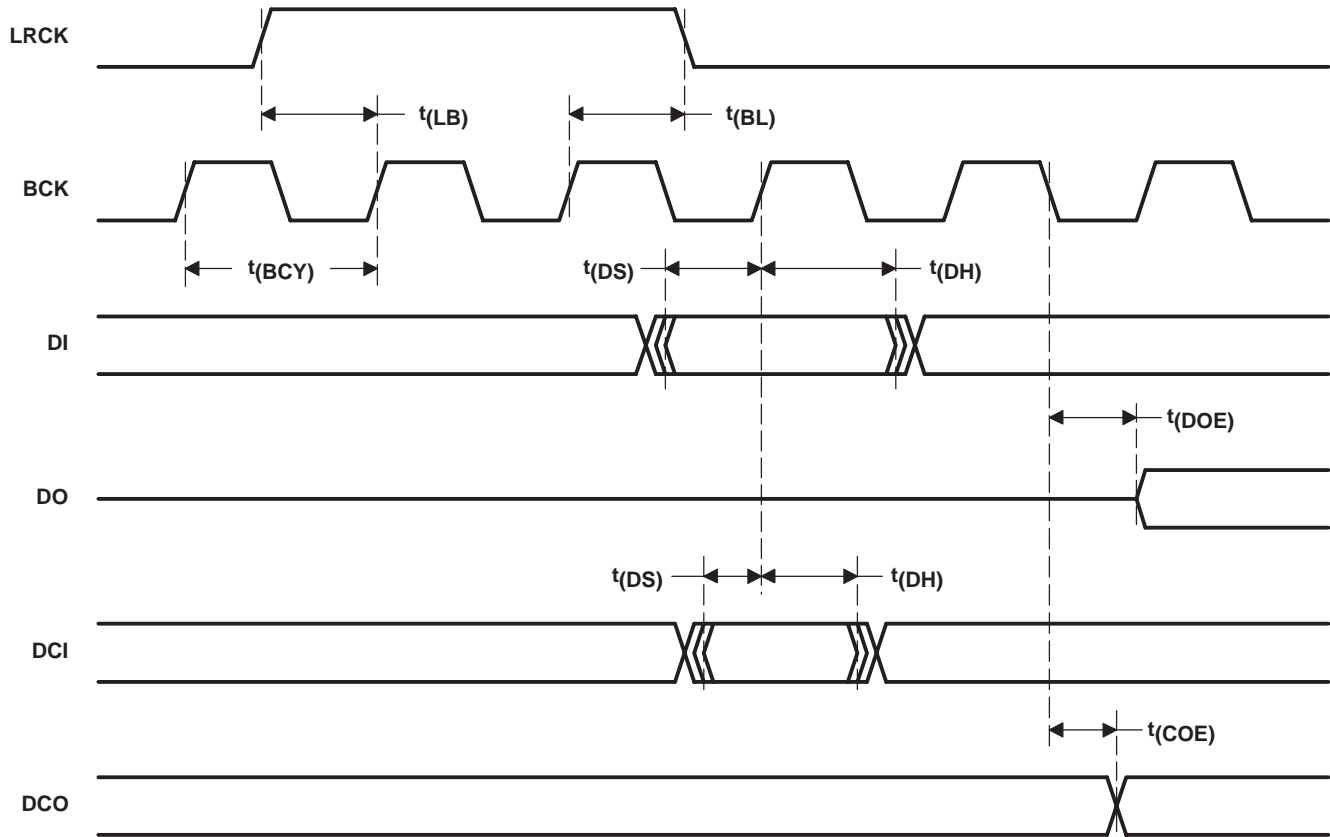


Figure 62. DCO Output Timing With Skip Operation (for Command Packet 1)



| PARAMETER |                                 | MIN | MAX | UNITS |
|-----------|---------------------------------|-----|-----|-------|
| t(BCY)    | BCK pulse cycle time            | 20  |     | ns    |
| t(LB)     | LRCK setup time                 | 0   |     | ns    |
| t(BL)     | LRCK hold time                  | 3   |     | ns    |
| t(DS)     | DI setup time                   | 0   |     | ns    |
| t(DH)     | DI hold time                    | 3   |     | ns    |
| t(DS)     | DCI setup time                  | 0   |     | ns    |
| t(DH)     | DCI hold time                   | 3   |     | ns    |
| t(DOE)    | DO output delay <sup>(1)</sup>  |     | 8   | ns    |
| t(COE)    | DCO output delay <sup>(1)</sup> |     | 6   | ns    |

<sup>(1)</sup> Load capacitance is 10 pF.

Figure 63. AC Timing of Daisy Chain Signals

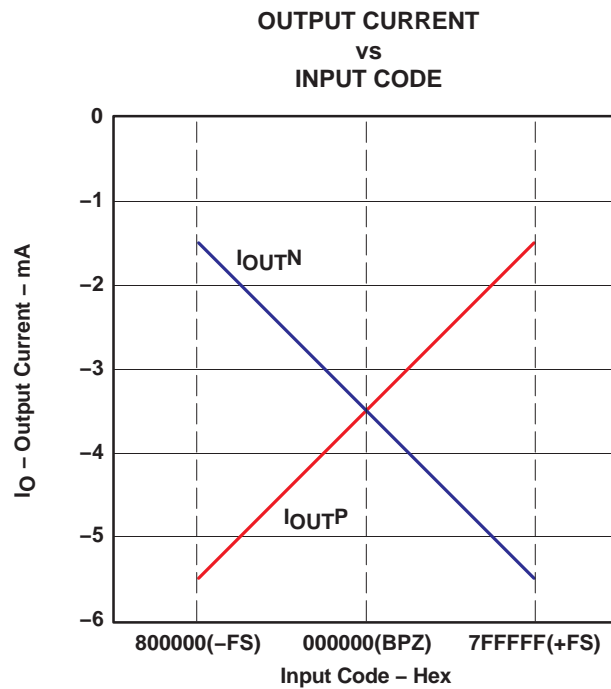
## ANALOG OUTPUT

Table 5 and Figure 64 show the relationship between the digital input code and analog output.

**Table 5. Analog Output Current and Voltage**

|                        | 800000 (-FS) | 000000 (BPZ) | 7FFFFFFF (+FS) |
|------------------------|--------------|--------------|----------------|
| I <sub>OUTN</sub> [mA] | -1.5         | -3.5         | -5.5           |
| I <sub>OUTP</sub> [mA] | -5.5         | -3.5         | -1.5           |
| V <sub>OUTN</sub> [V]  | -1.23        | -2.87        | -4.51          |
| V <sub>OUTP</sub> [V]  | -4.51        | -2.87        | -1.23          |
| V <sub>OUT</sub> [V]   | -2.98        | 0            | 2.98           |

NOTE: V<sub>OUTN</sub> is the output of U1, V<sub>OUTP</sub> is the output of U2, and V<sub>OUT</sub> is the output of U3 in the measurement circuit of Figure 36.



**Figure 64. The Relationship Between Digital Input and Analog Output**

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150



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