Ultra Low-Noise, 24-Bit Analog-to-Digital Converter

FEATURES

- **Up to 23.5 Effective Bits**
- **RMS Noise:**
  - **17nV at 10Hz**
  - **44nV at 80Hz**
- **On-Board Low Noise Gain-Amp**
- **19.2-Bit Noise-Free Resolution at Gain = 64**
- **Simultaneous 50Hz and 60Hz Rejection:**
  - **Internal Clock: 110 dB**
  - **External Clock: 130 dB**
- **±1% Low-Drift On-Board Oscillator**
- **Selectable Gains of 1, 2, 64, and 128**
- **Selectable 10/80SPS Conversion Rates**
- **2-Channel Differential Input with Built-In Temp sensor (ADS1232)**
- **4-Channel Differential Input (ADS1234)**
- **External Reference up to AVDD**
- **Simple Serial Digital Interface**
- **Supply Range: 2.7V to 5.3V**
- **–40°C to +105°C Temperature Range**

APPLICATIONS

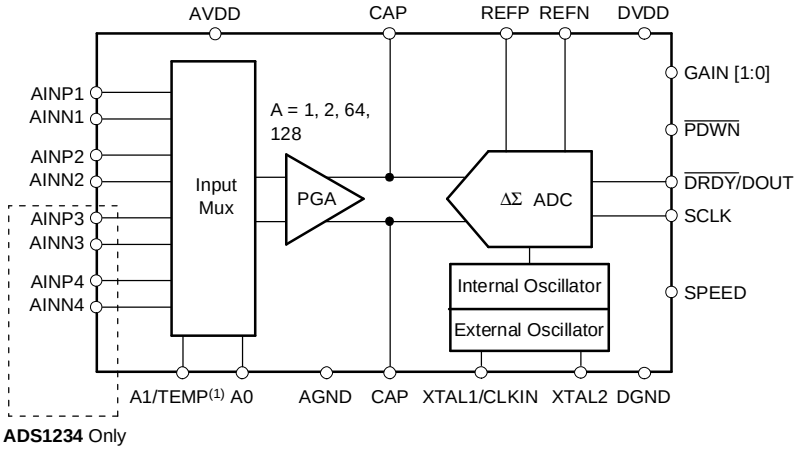
- **Weigh Scales**
- **Strain Gauges**
- **Bridge Sensors**
- **Industrial Process Control**

DESCRIPTION

The ADS1232 and ADS1234 are precision analog-to-digital (A/D) converters featuring true 23.5 effective-bit performance and exceptional ease of use. Selectable gains of 1, 2, 64, or 128 allow full-scale differential input ranges of ±2.5V to ±19.5mV with a +5V reference. While the ADS1232 offers a two-channel differential input and a built-in temperature sensor, the ADS1234 features a four-channel differential input multiplexer. A very low-noise Gain-Amp features low differential input current to minimize errors when using high-impedance transducers. An on-board oscillator is provided for excellent 50Hz and 60Hz rejection without an external clock source. The devices also feature a low current driver to accommodate an external crystal; they also accept external clock sources for all applications.

All of the features of the ADS1232/ADS1234 are hard-wire selected, without software programming. Data is accessed over a simple serial interface compatible with popular microcontrollers such as the MSP430. The ADS1232 is available in the 24-pin TSSOP package, and the ADS1234 is available in the 28-pin TSSOP.

PRODUCT PREVIEW



NOTE: (1) A1 for ADS1234, TEMP for ADS1232.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS1232	TSSOP-24	PW	–40°C to 105°C	ADS1232	ADS1232IPWT	Tape and Reel, 250
					ADS1232IPWR	Tape and Reel, 2500
ADS1234	TSSOP-28	PW	–40°C to 105°C	ADS1234	ADS1234IPWT	Tape and Reel, 250
					ADS1234IPWR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

	ADS1232, ADS1234	UNIT
AVDD to AGND	–0.3 to +6	V
DVDD to DGND	–0.3 to +6	V
AGND to DGND	–0.3 to +0.3	V
Input Current	100, Momentary	mA
Input Current	10, Continuous	mA
Analog Input Voltage to AGND	–0.3 to AVDD + 0.3	V
Digital Input Voltage to DGND	–0.3 to DVDD + 0.3	V
Maximum Junction Temperature	+150	°C
Operating Temperature Range	–40 to +105	°C
Storage Temperature Range	–60 to +150	°C
Lead Temperature (soldering, 10s)	+300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_{REF} = +5V

All specifications T_A = –40°C to +105°C, AVDD = DVDD = VREFP = +5V, VREFN = AGND, Internal Oscillator, SPEED = Low, Gain = 64 (unless otherwise specified).

PARAMETER	CONDITIONS	ADS1232, ADS1234 MIN	TYP	MAX	UNIT
Analog Inputs					
Full-Scale Input Voltage (AIN_P - AIN_N)			±0.5V_{REF}/Gain		V
Common-mode Input Range	AINxP or AINxN with respect to GND, Gain = 1	AGND – 0.1		AVDD + 0.1	V
	Gain = 64, 128	(0.5)AVDD – 1		(0.5)AVDD + 1	V
Differential Input Current	Gain = 1, 2		500		nA
	Gain = 64, 128		50		nA
System Performance					
Resolution	No missing codes	24			Bits
Conversion Rate	Internal Oscillator, SPEED = High	***TBD***	80	***TBD***	SPS
	Internal Oscillator, SPEED = Low	***TBD***	10	***TBD***	SPS
	External Oscillator, SPEED = High		f_{CLK} / 61440		SPS
	External Oscillator, SPEED = Low		f_{CLK} / 491520		SPS
Digital Filter Settling Time	Full Settling		4		Conversions
Integral Non-Linearity (INL)	Differential input, End point fit Gain = 1, 2		±0.0002	±0.0015	% of FSR(1)
	Differential input, End point fit Gain = 64, 128		±0.0010	***TBD***	% of FSR
Input Offset Error(2)	Gain = 1		±0.2	***TBD***	ppm of FS
	Gain = 64		±2	***TBD***	ppm of FS
Input Offset Error Drift	Gain = 1		1		µV/°C
	Gain = 64		15		nV/°C
Gain Error(3)	Gain = 1		0.001	***TBD***	%
	Gain = 64		0.001	***TBD***	%
Gain Error Drift	Gain = 1		0.5		ppm/°C
	Gain = 64		±4		ppm/°C
Normal-mode Rejection(4)	Internal oscillator, 50Hz and 60Hz	100	110		dB
	External oscillator, 50Hz and 60Hz, ±1Hz	120	130		dB
Common-mode Rejection	at DC, Gain = 1, ΔVDD = 1V	***TBD***	100		dB
	at DC, Gain = 64, ΔVDD = 0.1V	***TBD***	75		dB
Input-Referred Noise		See Noise Performance Tables			
Power-Supply Rejection	at DC, Gain = 1, ΔVDD = 1V	***TBD***	100		dB
	at DC, Gain = 64, ΔVDD = 0.1V	***TBD***	85		dB
Voltage Reference Input					
Voltage Reference Input (V_{REF})	V_{REF} = VREFP - VREFN	1	AVDD	AVDD + 0.1V	V
Negative Reference Input (VREFN)		AGND – 0.1		VREFP – 1.0	V
Positive Reference Input (VREFP)		VREFN + 1.0		AVDD + 0.1	V
Voltage Reference Input Current			50		nA

(1) FSR = full scale range = V_{REF}/Gain
(2) Offset calibration can minimize these errors to the level of noise at any temperature.
(3) Gain errors are calibrated at the factory (AVDD = +5V, all gains, T_A = +25°C).
(4) Specification is assured by the combination of design and final production test.

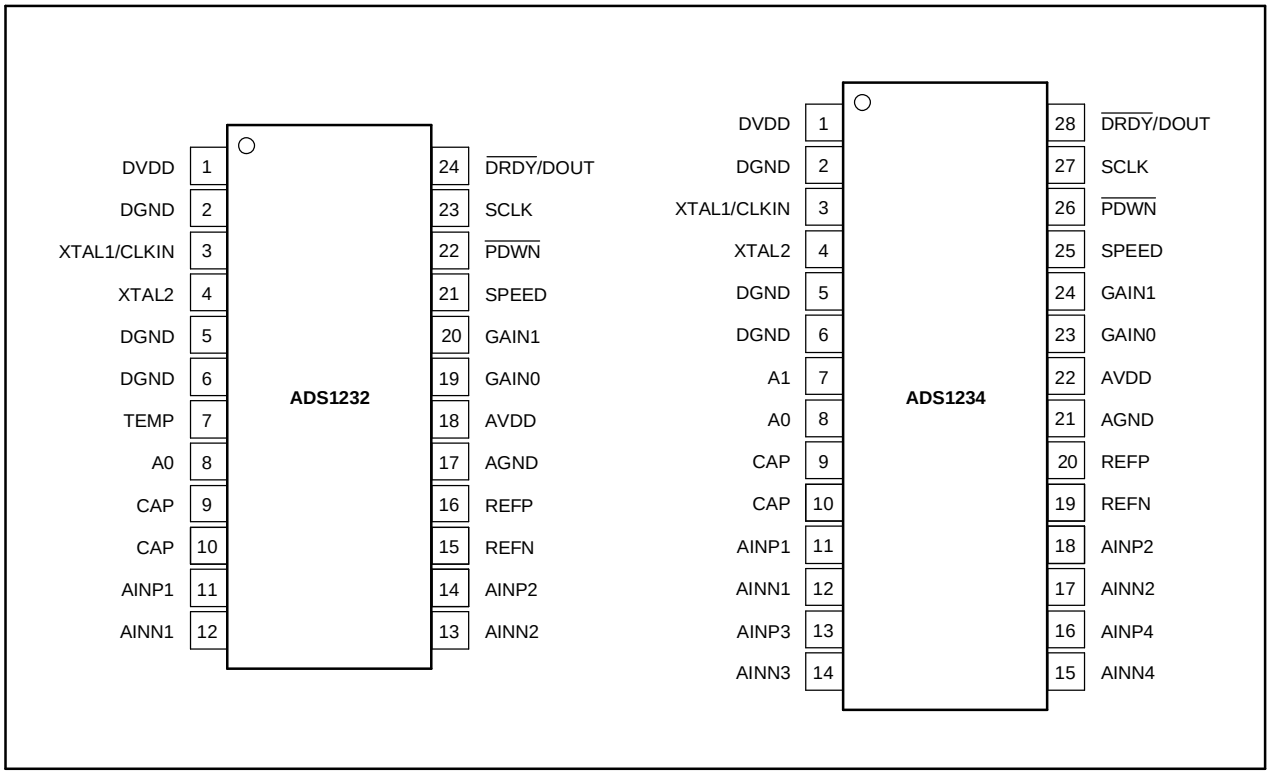
PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS: V_{REF} = +5V (continued)

All specifications T_A = –40°C to +105°C, AVDD = DVDD = VREFP = +5V, VREFN = AGND, Internal Oscillator, SPEED = Low, Gain = 64 (unless otherwise specified).

PARAMETER	CONDITIONS	ADS1232, ADS1234			UNIT
		MIN	TYP	MAX	
Digital					
Logic Levels					
V_{IH}		0.6 DVDD		DVDD + 0.1	V
V_{IL}		DGND		0.3 DVDD	V
V_{OH}	I_{OH} = 1mA	DVDD – 0.4			V
V_{OL}	I_{OL} = 1mA		0.2 DVDD		V
Input Leakage	0 < V_{IN} < DVDD			±10	µA
Power Supply					
Power Supply Voltage (AVDD, DVDD)		2.7		5.3	V
Analog Supply Current	Normal mode, AVDD = 3V, Gain = 1, 2		600	***TBD***	µA
	Normal mode, AVDD = 3V, Gain = 64, 128		1500	***TBD***	µA
	Normal mode, AVDD = 5V, Gain = 1, 2		700	***TBD***	µA
	Normal mode, AVDD = 5V, Gain = 64, 128		1600	***TBD***	µA
	Standby mode		0.1	***TBD***	µA
	Power-down		0.1	***TBD***	µA
Digital Supply Current	Normal mode, DVDD = 3V, Gain = 1, 2		90	***TBD***	µA
	Normal mode, DVDD = 3V, Gain = 64, 128		90	***TBD***	µA
	Normal mode, DVDD = 5V, Gain = 1, 2		110	***TBD***	µA
	Normal mode, DVDD = 5V, Gain = 64, 128		110	***TBD***	µA
	Standby mode, SCLK = High		50	***TBD***	µA
	Power-down		0.1	***TBD***	µA
Power Dissipation, Total	Normal mode, AVDD = DVDD = 3V, Gain = 1, 2		2.1	***TBD***	mW
	Normal mode, AVDD = DVDD = 5V, Gain = 1, 2		4	***TBD***	mW
	Normal mode, AVDD = DVDD = 3V, Gain = 64, 128		4.8	***TBD***	mW
	Normal mode, AVDD = DVDD = 5V, Gain = 64, 128		8.6	***TBD***	mW
	Standby		***TBD***	***TBD***	mW
	Power-down		***TBD***	***TBD***	mW

DEVICE INFORMATION



PRODUCT PREVIEW

DEVICE INFORMATION (continued)

PIN DESCRIPTIONS

NAME	TERMINAL ADS1232	TERMINAL ADS1234	ANALOG/DIGITAL INPUT/OUTPUT	DESCRIPTION
DVDD	1	1	Digital	Digital Power Supply: 2.7V to 5.3V
DGND	2	2	Digital	Digital Ground
XTAL1/ CLKIN	3	3	Digital/Digital Input	External Clock Input: Typically 4.9152MHz. Ties low to activate Internal Oscillator. Can also use external Crystal Oscillator across XTAL1/CLKIN and XTAL2 pins. See text for more details.
XTAL2	4	4	Digital	External Clock Output pin. See text for more details.
DGND	5	5	Digital	Digital Ground
DGND	6	6	Digital	Digital Ground
TEMP	7	–	Digital Input	Onboard Temperature Diode Enable Input pin
A1	–	7	Digital Input	Input Mux Select Input pin (MSB)
A0	8	8	Digital Input	Input Mux Select Input pin (LSB):

A1	A0	Channel
0	0	AIN1
0	1	AIN2
1	0	AIN3
1	1	AIN4

CAP	9	9	Analog	Gain Amp Bypass Capacitor Connection
CAP	10	10	Analog	Gain Amp Bypass Capacitor Connection
AINP1	11	11	Digital Input	Positive Analog Input Channel 1
AINN1	12	12	Digital Input	Negative Analog Input Channel 1
AINP3	–	13	Digital Input	Positive Analog Input Channel 3
AINN3	–	14	Digital Input	Negative Analog Input Channel 3
AINN4	–	15	Digital Input	Negative Analog Input Channel 4
AINP4	–	16	Digital Input	Positive Analog Input Channel 4
AINN2	13	17	Digital Input	Negative Analog Input Channel 2
AINP2	14	18	Digital Input	Positive Analog Input Channel 2
REFN	15	19	Digital Input	Negative Reference Input pin
REFP	16	20	Digital Input	Positive Reference Input pin
AGND	17	21	Analog	Analog Ground
AVDD	18	22	Analog	Analog Power Supply, 2.7V to 5.3V
GAIN0	19	23	Digital Input	Gain Select Input pin (LSB)
GAIN1	20	24	Digital Input	Gain Select Input pin (MSB):

GAIN1	GAIN0	PGA
0	0	1
0	1	2
1	0	64
1	1	128

SPEED	21	25	Digital Input	Output Data Rate Select Input pin:

SPEED	DATA RATE
0	10Hz
1	80Hz

$\overline{\text{PDWN}}$	22	26	Digital Input	Power Down Input pin: Holding this pin low powers down the entire converter and resets the A/D converter.
SCLK	23	27	Digital Input	Serial Clock Input pin: Clock out data on the rising edge. Used to initiate Offset Calibration and Sleep modes. See text for more details.
$\overline{\text{DRDY}}$/ DOUT	24	28	Digital Input	Dual-Purpose Output: Data Ready: Indicates valid data by going low. Data Output: Outputs data, MSB first, on the first rising edge of SCLK.

PRODUCT PREVIEW

NOISE PERFORMANCE

The ADS1232/1234 offer outstanding noise performance that can be optimized for a givven full-scale range using the on-chip programmable gain amplifier, Table 1, Table 2, Table 3, and Table 4 summarize the typical noise performance with inputs shorted externally for different gains, data rates and voltage reference values.

The RMS and Peak-to-Peak noise are referred to the input. The Effective Number of Bits (ENOB) is defined as:

- ENOB = ln (FSR/RMS noise)/ln(2)

The Noise Free Bits are defined as:

- Noise-Free Bits = ln (FSR/Peak-to-Peak Noise)/ln(2)

Where FSR (Full-Scale Range) = V_{REF}/Gain

Table 1. AVDD = 5V, V_{REF} = 5V, Data Rate = 10SPS

GAIN	RMS NOISE	PEAK-TO-PEAK NOISE	ENOB (rms)	NOISE-FREE BITS
1	420nV	1.79µV	23.5	21.4
2	270nV	900nV	23.1	21.4
64	19nV	125nV	22.0	19.2
128	17nV	110nV	21.1	18.4

Table 2. AVDD = 5V, V_{REF} = 5V, Data Rate = 80SPS

GAIN	RMS NOISE	PEAK-TO-PEAK NOISE	ENOB (rms)	NOISE-FREE BITS
1	1.36µV	8.3µV	21.8	19.2
2	850nV	5.5µV	21.5	18.8
64	48nV	307nV	20.6	18
128	44nV	247nV	19.7	17.2

Table 3. AVDD = 3V, V_{REF} = 3V, Data Rate = 10SPS

GAIN	RMS NOISE	PEAK-TO-PEAK NOISE	ENOB (rms)	NOISE-FREE BITS
1	450nV	2.8µV	22.6	20
2	325nV	1.8µV	22.1	19.7
64	20nV	130nV	21.2	18.5
128	18nV	115nV	20.3	17.6

Table 4. AVDD = 3V, V_{REF} = 3V, Data Rate = 80SPS

GAIN	RMS NOISE	PEAK-TO-PEAK NOISE	ENOB (rms)	NOISE-FREE BITS
1	2.2µV	12µV	20.4	17.9
2	1.2µV	6.8µV	20.2	17.8
64	54nV	340nV	19.7	17.1
128	48nV	254nV	18.9	16.5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS1232IPW	PREVIEW	TSSOP	PW	24	60	TBD	Call TI	Call TI
ADS1232IPWR	PREVIEW	TSSOP	PW	24	2000	TBD	Call TI	Call TI
ADS1234IPW	PREVIEW	TSSOP	PW	28	50	TBD	Call TI	Call TI
ADS1234IPWR	PREVIEW	TSSOP	PW	28	2000	TBD	Call TI	Call TI

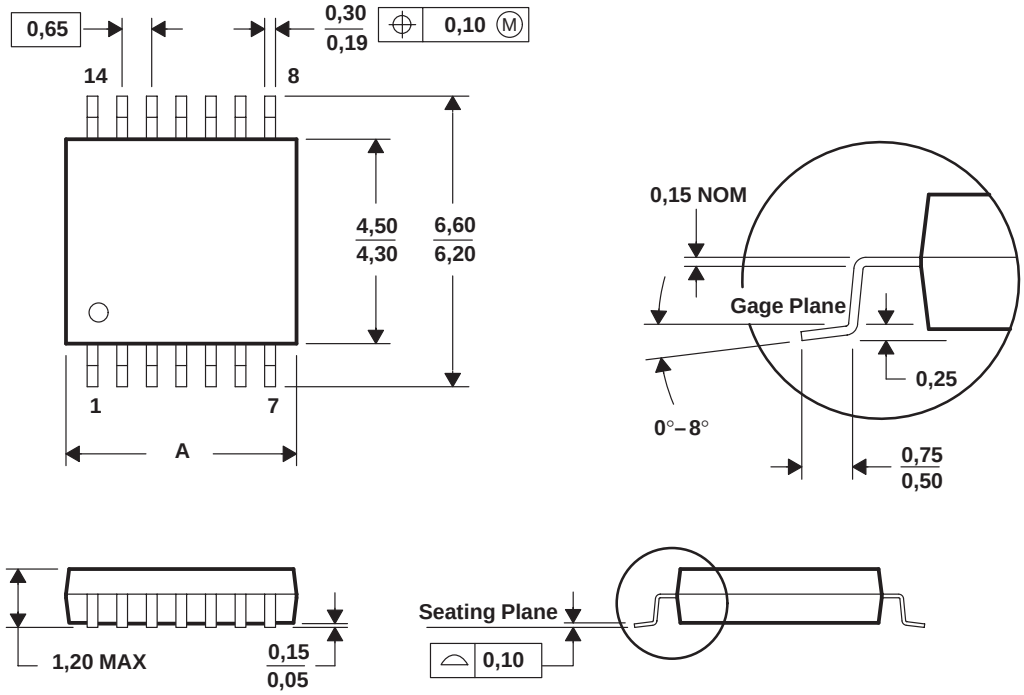
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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