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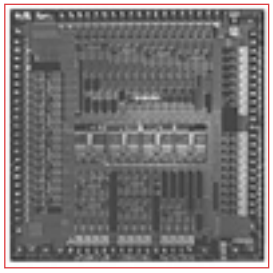
BCM8118
PRODUCT Brief



DIFFERENTIAL 10.7 Gbps LIMITING AMPLIFIER

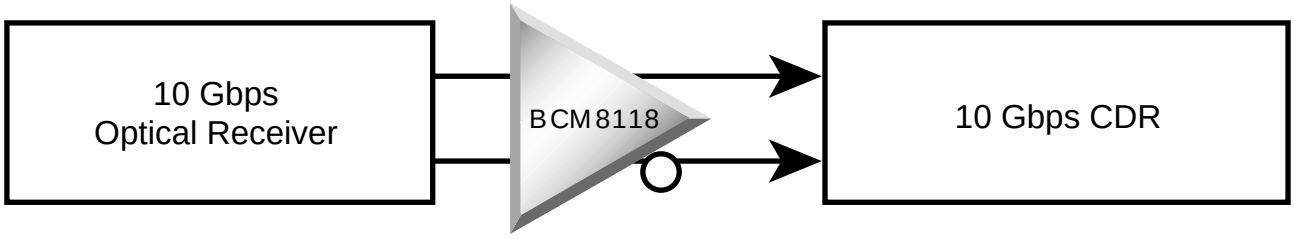
BCM8118 FEATURES

- **30 dB gain**
- **550 mVpp output swing**
- **6 x 6 mm BGA package**
- **1.8V power supply**
- **Standard CMOS fabrication process**
- **Power dissipation: 150 mW typical at 1.8V**

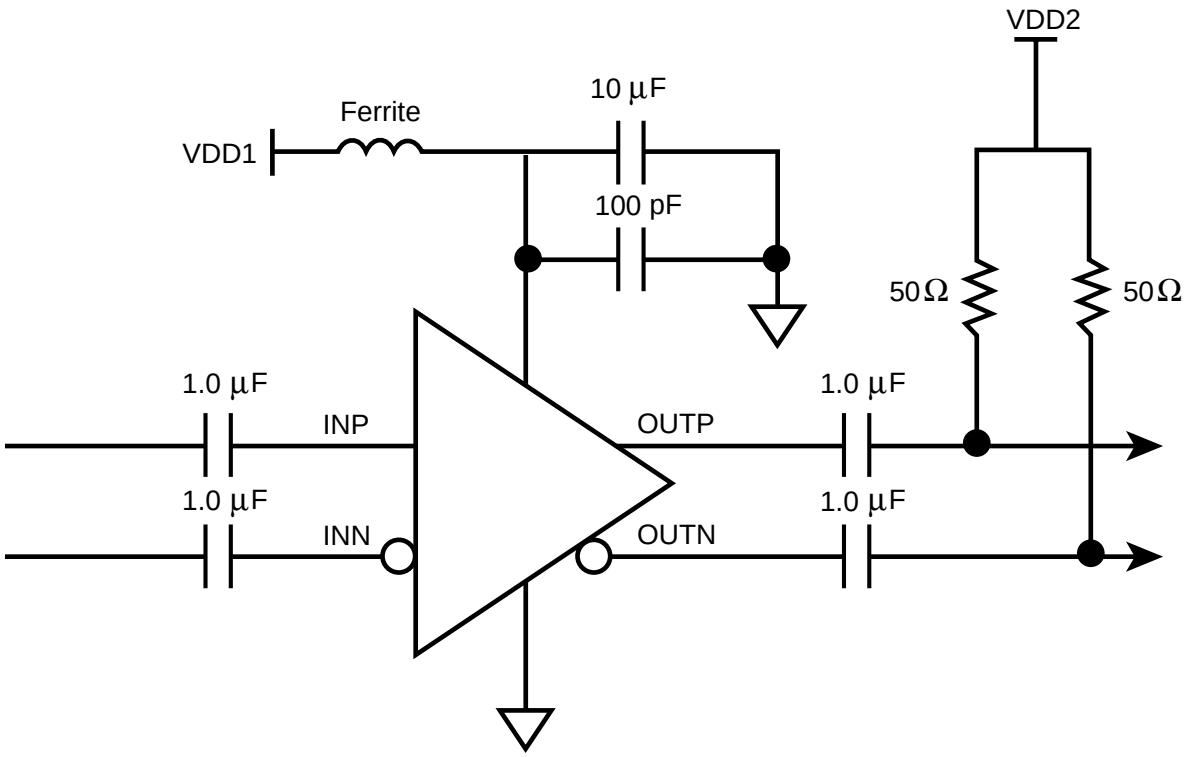
SUMMARY OF BENEFITS

- **Delivers superior 10.7-Gbps performance for OC-192/STM-64 and 802.3ae applications.**
- **Features a small footprint for high-density applications.**
- **Includes low-power operation for increased system reliability.**
- **Uses the most effective silicon economy of scale for CMOS-based devices.**
- **Exceeds SONET jitter requirements.**
- **Target applications:**
  - Optical transceiver modules
  - SONET and Ethernet optical interfaces

Application Block Diagram



Application Schematic



The **BCM8118** differential 10.7 Gbps limiting amplifier provides post-amplification of low-level signals between an optical receiver and the CDR inputs. It provides a typical differential output voltage of 550 mVpp for input signals between 20 and 2000 mVpp, differential.

The differential input stage of the device contains internal DC biasing, which allows AC coupling of the input signals. The **BCM8118** is packaged in a 6 x 6 mm, 36-pin BGA.

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