Features

- **Comprehensive Library of Standard Logic Cells**
- **MH2RT I/O Cells Designed to Operate With VDD 2.5V ± 0.2V as Main Target Operating Conditions**
- **IO33 Pad Library Provides Interface to 3.3V Environment**
- **Memory Cells Compiled to Precise Design Requirements**
- **Processed on Radiation Hard 0.25 µm CMOS Process, 5 Metal Layers**
- **Cold Sparing Buffers**
- **Pre-defined Pads Frames**
- **SEU Free Cells**
- **Latch-up Immune**
- **200 Krads Total Dose**
- **LVDS, LVTTL, PCI, PECL Buffers**
- **75 µm Buffer Pitch Allowing up to 750 pads**
- **High Speed: <100 ps Typical Propagation Gate Delay (NAND2 with FO = 2)**
- **Integration Capability With up to 5 Mgates**
- **Up to 2.25-Mbit Memory Compiler**
- **MQFP Package With Pin Count up to 352**
- **CLGA Packages With 1.25 mm and 1 mm Column Pitches and Pin Count up to 613**

Description

The Atmel MH2RT cell-based ASIC series are fabricated on a 0.25 micron CMOS process, with up to five levels of metal. This family allows up to 5 million gates and 800 pads. The high density and high pin count capabilities of the MH2RT family, coupled with the ability to embed processor cores or memories on the same silicon, make the MH2RT series an ideal choice for System Level Integration.

The MH2RT series is supported by an advanced software environment based on industry standards linking proprietary and commercial tools. Verilog®, DFT, Synopsys® and Vital are the reference front-end tools. The Cadence™ "Logic Design Planner" floor planning associated with timing driven layout provides an efficient back-end cycle.

The MH2RT series comes as a dual use of the MH2 series adding:

- through process changes, the 100 MeV latch up immunity and the 200 Krads+ total dose capability as required by most of the space programs,
- through cells layout, an SEU immunity allowing to SEU harden only where it is actually necessary with respect to function requirements.

The MH2RT series comes as the Atmel 8th generation of ASIC series designed for radiation hardened applications in 19 years.

It will be made available to any of the currently available quality grades, including QML Q and V.

The Atmel MH2RT family is fabricated on a proprietary 0.25 micron five-layer-metal CMOS process intended for use with a supply voltage of 2.5V ± 0.2V.

The MH2RT Series is offered with a mutli-project wafer service.

Rad. Hard 5M Gates 0.25 µm CMOS Cell-based

MH2RT

Advance Information

Rev. 4142B–AERO–06/02

The following table shows the range for which Atmel library cells have been characterized.

Table 1. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	DC Supply Voltage	Core and Standard I/Os	2.3	2.5	2.7	V
V_{DD3}	DC Supply Voltage	3V Interface I/Os	3	3.3	3.6	V
V_I	DC Input Voltage		0		V_{DD}	V
V_O	DC Output Voltage		0		V_{DD}	V
TEMP	Operating Free Air Temperature Range	Military	-55		+125	°C

The Atmel cell libraries and megacell compilers have been designed to be compatible with each other. Simulation representations exist for three types of operating conditions. They correspond to three characterization conditions defined as follows:

- MIN conditions:

  TJ = -55°C
  VDD (cell) = 2.7V
  Process = fast (military best case)

- TYP conditions:

  TJ = +25°C
  VDD (cell) = 2.5V
  Process = typ (military typical case)

- MAX conditions:

  TJ = +125°C
  VDD (cell) = 2.3V
  Process = slow (military worst case)

Delays to tri-state are defined as delays to turn off (VGS < VT) the driving devices. Output pad drain current corresponds to the output current of the pad when the output voltage is VOL or VOH. The output resistor of the pad and the voltage drop due to access resistors (in and out of the die) are taken into account. In order to have accurate timing estimates, all characterization has been run on electrical netlists extracted from the layout database.

Standard Cell Library

The Atmel Standard Cell Library, contains a comprehensive set of combinational logic and storage cells. The library includes cells which belong to the following categories:

- Buffers and Gates
- Multiplexers
- Flip-flops
- Scan Flip-flops
- Latches
- Adders and Subtractors

Decoding the Cell Name

The table below shows the naming conventions for the cells in the library. Each cell name begins with either a two-, three-, or four-letter code that defines the type of cell. This indicates the range of standard cells available.

Table 2. Cell Codes

Code	Description	Code	Description
AD	Adder	INVT	Inverting 3-State Buffer
AH	Half Adder	JK	JK Flip-Flop
AS	Adder/Subtractor	LA	D Latch
AN	AND Gate	MI	Inverting Multiplexer
AOI	AND-OR-Invert Gate	MX	Multiplexer
AON	AND-OR-AND-Invert Gates	ND	NAND Gate
AOR	AND-OR Gate	NR	NOR Gate
BH	Bus Holder	OAI	OR-AND-Invert Gate
BUFB	Balanced Buffer	OAN	OR-AND-OR-Invert Gates
BUFF	Non-Inverting Buffer	OR	OR Gate
BUFT	Non-Inverting 3-State Buffer	ORA	OR-AND Gate
CG	Carry Generator	SD	Multiplexed Scan D Flip-Flop
CLK2	Clock Buffer	SE	Multiplexed Scan Enable D Flip-Flop
DE	D-Enabled Flip-Flop	SRLA	Set/Reset Latches with NAND input
DF	D Flip-Flop	SU	Subtractor
INV0	Inverter	XN	Exclusive NOR Gate
INVB	Balanced Inverter	XR	Exclusive OR Gate

Cell Matrices

The following three tables provide a quick reference to the storage elements in the library. Note that all storage elements feature buffered clock inputs and buffered output.

Table 3. JK Flip-flops

Macro Name	Set	Clear	1x Drive	2 x Drive
JKBRBx	•	•	•	•

Table 4. D Flip-flops

Macro Name	Set	Clear	Enabled D Input	1 x Drive	2 x Drive	Single Output
DFBRBx	•	•		•	•	
DFCRBx		•		•	•	
DFCRQx		•		•	•	•
DFCRNx		•		•	•	
DFNRBx				•	•	
DFNRQx				•	•	•
DFPRBx	•			•	•	
DEPRQx	•		•	•	•	•
DENRQx			•	•	•	•
DENRBx			•	•	•	
DECRQx		•	•	•	•	•

Table 5. Scan Flip-flops

Macro Name	Set	Clear	1x Drive	2x Drive	Single Output
SDBRBx	•	•	•	•	
SDCRBx		•	•	•	
SDCRNx		•	•	•	•
SDCRQx		•	•	•	•
SDNRBx			•	•	
SDNRNx			•	•	•
SDNRQx			•	•	•
SDPRBx	•		•	•	
SECRQx		•	•	•	•
SENRQx			•	•	•
SEPRQx	•		•	•	•

Input/Output Pad Cell Libraries IO25lib and IO33lib

The Atmel Input/Output Cell Library, IO25lib, contains a comprehensive list of input, output, bi-directional and tri-state cells. The MH2RT (2.5V) cell library includes a special set of I/O cells, IO33lib, for interfacing with external 3.3V devices.

Voltage Levels

The IO25lib library is made up exclusively of low-voltage chip interface circuits powered by a voltage in the range of 2.3V to 2.7V. The library is compatible with the 2.5V standard cells library.

Power and Ground Pads

Designers are strongly encouraged to provide three kinds of power pairs for the IO25lib library. These are “AC”, “DC” and core power pairs. AC power is used by the I/O to switch its output from one state to the other. This switching generates noise in the AC power buses on the chip. DC power is used by the I/O to maintain its output in a steady state. The best noise performance is achieved when the DC power buses on the chip are free of noise; designers are encouraged to use separate power pairs for AC and DC power to prevent most of the noise in the AC power buses from reaching the DC power buses. The same power pairs can be used to supply both DC power to the I/Os and power to the core without affecting noise performance.

Table 6. VSS Power Pad Combinations

Core	Switching I/O	Quiet I/O		
Vssi	**VssAC**	**VssDC**	**Library Cell Name**	**Signal Name**
•			pv25i00	VSS
	•		pv25a00	VSS
		•	pv25d00	VSS
	•	•	pv25e00	VSS
•		•	pv25b00	VSS
•	•	•	pv25f00	VSS

Table 7. VDD Power Pad Combinations

Core	Switching I/O	Quiet I/O		
Vddi	**VddAC**	**VddDC**	**Library Cell Name**	**Signal Name**
•			pv25i25	VDD
	•		pv25a25	VDD
		•	pv25d25	VDD
	•	•	pv25e25	VDD
•		•	pv25b25	VDD
•	•	•	pv25f25	VDD

Cell Matrices

Table 8. CMOS Pads

CMOS Cell Name	3-State I/O	Output Only	3-State Output Only	Drive Strength	Pad Sites Used
PC25B01	•			1x	1
PC25B02	•			2x	1
PC25B03	•			3x	1
PC25B04	•			4x	1
PC25B05	•			5x	1
PC25O01		•		1x	1
PC25O02		•		2x	1
PC25O03		•		3x	1
PC25O04		•		4x	1
PC25O05		•		5x	1
PC25T01			•	1x	1
PC25T02			•	2x	1
PC25T03			•	3x	1
PC25T04			•	4x	1
PC25T05			•	5x	1

Table 9. TTL Pads

TTL Cell Name	3-State I/O	Output Only	3-State Output Only	Drive Strength	Pad Sites Used
PT25B01	•			2 mA	1
PT25B02	•			4 mA	1
PT25B03	•			8 mA	1
PT25O01		•		2 mA	1
PT25O02		•		4 mA	1
PT25O03		•		8 mA	1
PT25T01			•	2 mA	1
PT25T02			•	4 mA	1
PT25T03			•	8 mA	1

Table 10. CMOS/TTL Input Only Pad

CMOS Cell Name	Input Levels	Schmitt Input Level Shifter	Non-Inverting	Inverting	Pad Sites Used
PC25D01	CMOS		•		1
PC25D11	CMOS			•	1
PC25D21	CMOS	•	•		1
PC25D31	CMOS	•		•	1

Note: 1. All 3-state I/Os, 3-state output only and input pads are also available with pull-up and pull-down device.

IO33lib Low Slew Rate Cells

The IO33lib cells comprise a series of 2.5V/3.3V input/output pads developed for low supply voltage processes in order to interface 2.5V ASICs to 3.3V environments.

All IO33lib cells are slew rate controlled. Advantage has been taken of the 2.5V to 3.3V level shifter (slow by construction) to reduce the slew rate without reducing speed.

Table 11. IO33lib Pads

3V Interface Pad Name	3-State I/O	Output Only	3-State Output Only	Input Only	Drive Strength	Pad Sites Used
pc33b0x	•				2 mA, 4 mA, 8 mA, 16 mA	1
pc33d00				•		1
pc33o0x		•			2 mA, 4 mA, 8 mA, 16 mA	1
pc33t0x			•		2 mA, 4 mA, 8 mA, 16 mA	1

Note: 1. All 3-state I/Os, 3-state output only and input pads are also available with pull-up and pull-down device.

Table 12. IO33lib Power Pads

Cell Name	Power Bus Connections				Pad Sites Used
	vssi	mixvss	vddi	mixvdd	
pv33e00		•			1
pv33i00	•				1
pv33i25			•		1
pv33e33				•	1
pv33ecrn		•		•	2

Atmel Compiled Megacell Library

The Atmel Compiled Megacell Library enables compilation of megacells for the functions Synchronous RAM, High-range Synchronous RAM, Asynchronous RAM, Asynchronous Dual-port RAM, Asynchronous Two-port RAM and Synchronous ROM, according to the user's precise requirements.

General Characteristics of the Atmel Megacell Compilers

The Atmel megacells can be instanced as often as required in designs and can be used in parallel with cells from all other Atmel libraries. All the megacell representations required for schematic entry, simulation, place and route, layout generation, and verification are created automatically.

Compiled Synchronous RAM Megacells

General Synchronous RAM Characteristics

The Atmel Synchronous RAM compiler has bi-directional or separate I/O ports, and can be configured in multi-bank form, with a maximum of four banks.

Synchronous RAM Configurations

The range of permitted Synchronous RAM megacell configurations is as follows:

Number of bits:128,...144K bits

Number of words:32,... 8K

Word Size: 4,... 36 bits

Synchronous RAM Example Characteristics

The following table shows the range of performances for particular Synchronous RAM configurations under typical conditions.

Configuration	1K x 8 (8K bits)	2K x 16 (32K bits)	4K x 32 (128K bits)
Density (Kbits/mm^2)	51	58	62
Frequency (MHz)	255	205	145
Dynamic Power (mW/MHz)	0.17	0.36	0.73

Compiled High-range Synchronous RAM Megacells

General High-range Synchronous RAM Characteristics

The Atmel High-range Synchronous RAM compiler has bi-directional or separate I/O ports, and can be configured in multi-bank form, with a maximum of four banks.

High-range Synchronous RAM Configurations

The range of permitted High-range Synchronous RAM megacell configurations is as follows:

Number of bits: 16K,... 2.25M bits

Number of words: 2K,... 32K

Word Size: 8,... 72 bits

High-range Synchronous RAM Example Characteristics

The following table shows the range of performances for particular High-range Synchronous RAM configurations under typical conditions.

Configuration	8K x 8 (64K bits)	16K x 16 (256K bits)	32K x 32 (1M bits)
Density (Kbits/mm^2)	80	84	87
Frequency (MHz)	150	100	60
Dynamic Power (mW/MHz)	0.29	0.55	1.22

Compiled Asynchronous RAM Megacells

General Asynchronous RAM Characteristics

The Atmel Asynchronous RAM compiler has bi-directional or separate I/O ports, and can be configured in multi-bank form, with a maximum of four banks.

Asynchronous RAM Configurations

The range of permitted Asynchronous RAM megacell configurations is as follows:

Number of bits:128,... 128K bits

Number of words:16,... 4K

Word Size: 8,... 36 bits

Asynchronous RAM Example Characteristics

The following table shows the range of performances for particular Asynchronous RAM configurations under typical conditions.

Configuration	1K x 8 (8K bits)	2K x 16 (32K bits)	4K x 32 (128K bits)
Density (Kbits/mm^2)	40	40	50
Frequency (MHz)	415	405	265
Dynamic Power (mW/MHz)	0.24	0.38	0.63

Compiled Asynchronous Dual-port RAM Megacells

General Asynchronous Dual-port RAM Characteristics

The Atmel Asynchronous Dual-port RAM has bi-directional or separate I/O ports, and can be configured in multi-bank form, with a maximum of four banks.

Asynchronous Dual-port RAM Configurations

The range of permitted Asynchronous Dual-port RAM Megacell configurations is as follows:

Number of bits: 128,... 16K

Number of words(1): 64,... 2K

Word Size(1): 2,... 36 bits

Note: 1. Must be the same for both ports.

Asynchronous Dual-port RAM Example Characteristics

The following table shows the range of performances for particular Asynchronous Dual-port RAM configurations under typical conditions.

Configuration	128 x 8 (1K bits)	256 x 16 (4K bits)	512 x 32 (16K bits)
Density (Kbits/mm^2)	22	32	36
Frequency (MHz)	245	220	200
Dynamic Power (mW/MHz)	0.09	0.31	0.41

Compiled Two-port RAM Megacells

General Two-port RAM Characteristics

The Atmel Asynchronous Two-port RAM can be configured in multi-bank form, with a maximum of four banks, and can be used to achieve FIFO functions.

Two-port RAM Configurations

The range of permitted Asynchronous Two-port RAM Megacell configurations is as follows:

Number of bits: 128,... 36K

Number of words(1): 64,... 2K

Word Size(1): 2,... 36 bits

Note: 1. Must be the same for both ports.

Two-port RAM Example Characteristics

The following table shows the range of performances for particular Asynchronous Two-port RAM configurations under typical conditions.

Configuration	256 x 8 (2K bits)	512 x 16 (8K bits)	1K x 32 (32K bits)
Density (Kbits/mm^2)	20	24	27
Frequency (MHz)	315	290	235
Dynamic Power (mW/MHz)	0.06	0.10	0.18

Compiled Synchronous ROM Megacells

General Synchronous ROM Characteristics

The Atmel Synchronous ROM is diffusion programmable and is applicable in low power solutions. It can be configured in multi-bank form, with a maximum of four banks.

Synchronous ROM Configurations

The range of permitted Synchronous ROM Megacell configurations is as follows:

Number of bits: 256,... 512K

Number of words: 64,... 8K

Word Size: 4,... 64 bits

Synchronous ROM Example Characteristics

The following table shows the range of performances for particular Synchronous ROM configurations under typical conditions.

Configuration	2K x 8 (16K bits)	4K x 16 (64K bits)	8K x 32 (256K bits)
Density (Kbits/mm^2)	400	568	669
Frequency (MHz)	240	230	165
Dynamic Power (mW/MHz)	0.13	0.26	0.54

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