Features

- 1.1 - 3.6 V Operating Voltage Range
- 4 Non-inverting, Tristatable Drivers for the Following Applications:
  - Motor Driver for Bipolar Stepper Motors in Watch/Clock Applications
  - Driver for Piezoelectric Transducers (Buzzer)
  - LED Driver
  - Line Driver for Medium Speed Applications

Applications

- Motor Driver
- Radio Controlled Clock/Watch
- Line Driver for Mini Computer, Laptop
- LED Driver
- Relay Driver

Benefits

- High Load Current at Low Supply Voltage
- Replaces Several Discrete Transistors
- Tri-state Operation Possible

Description

The e5130 contains 4 independent driver outputs with an ON resistance of typically 25 Ω (15 Ω) for the P-channel output transistors and typically 20 Ω (13 Ω) for the N-channel output transistors at a supply voltage of 1.5 V (3 V). To obtain a fast transition of the outputs even for slow rise/fall time input signals, all digital inputs (IN1 to IN4) have a Schmitt-trigger characteristic with a hysteresis of typically 50 mV. If a higher driving capability is needed, all inputs and outputs may be connected in parallel. In this case the rise/fall time of the input signals IN1 to IN4 must be less than 200 ns. Due to the fast switching characteristic of the tri-statable output drivers, the circuit is also suited as a low-voltage bus driver.

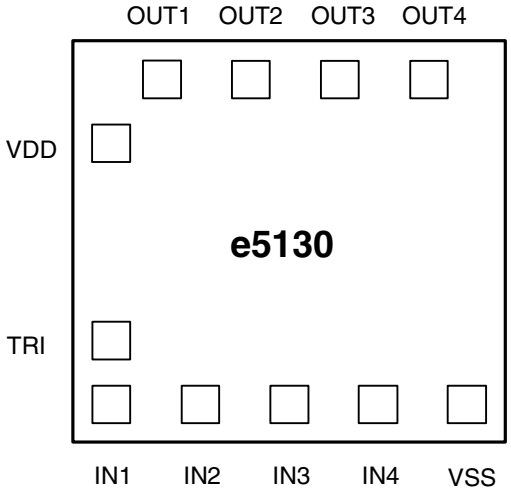
Low Voltage CMOS Driver Circuit

e5130

4730A–CLOCK–07/03

Pad Configuration

Figure 1. Pinning



Chip size: x = 1.08 mm, y = 1.42 mm,

Pad window: 90 × 90 µ

Pin Description

Symbol	Description
VDD	Positive supply voltage
VSS	Negative supply voltage
IN1 ... IN4	Digital inputs
TRI	Tri-state input
OUT1 ... OUT4	Drive outputs

Absolute Maximum Ratings

Absolute maximum ratings define parameter limits which, if exceeded, may permanently change or damage the device.
All inputs and outputs on circuits are highly protected against electrostatic discharges.
However, precautions to minimize build-up of electrostatic charges during handling are recommended.
The circuits are protected against supply voltage reversal for typically 5 minutes, if the current is limited to 120 mA.

Parameters	Symbol	Value	Unit
Supply voltage	V_{DD} - V_{SS}	-0.3 to +5	V
Input voltage range, all inputs	V_I	V_{SS} - 0.3 to V_{DD} + 0.3	V
Operating ambient temperature range		-20 to +70	°C
Storage temperature range		-40 to +125	°C
Lead temperature during soldering at 2 mm distance, 10 s		260	°C

Electrical Characteristics

V_{SS} = 0 V, V_{DD} = +1.5 V, T_{amb} = +25°C, unless otherwise specified. All voltage levels are measured with reference to V_{SS}.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Operating voltage		V_{DD}	1.1		3.6	V
Operating temperature		T_{amb}	-10		60	°C
Operating current (standby)	V_{DD} = 3.6 V, R_{L12} = R_{L34} = R IN1 to IN4 at V_{DD} or V_{SS}, TRI at V_{SS}	I_{DD}		0.05	1	µA
Drive Output OUT1 to OUT4						
Output current	V_{DD} = 1.2 V, R_{L12} = R_{L34} = 200 Ω	I_{OUT}	±4.3	±4.75		mA
Output current	V_{DD} = 1.5 V, R_{L12} = R_{L34} = 200 Ω	I_{OUT}	±5.7	±6.20		mA
Output current	V_{DD} = 3.0 V, R_{L12} = R_{L34} = 200 Ω	I_{OUT}	±12	±13		mA
Delay time	V_{DD} = 3 V, C_L = 50 pF	T_{Dr}, T_{Df}		35	60	ns
Delay time	V_{DD} = 1.5 V, C_L = 50 pF see Figure 3, note 1	T_{Dr}, T_{Df}		80	150	ns
Rise-/fall time	V_{DD} = 3 V, C_L = 50 pF	t_r, t_f		8	15	ns
Rise-/fall time	V_{DD} = 1.5 V, C_L = 50 pF see Figure 3, note 2	t_r, t_f		12	25	ns
Digital Input IN1 to IN4						
Input current	V_{IL} = 0 V	I_{IL}			-100	nA
Input current	V_{IH} = V_{DD}	I_{IH}			100	nA
Threshold	V	V_{TH}		V_{DD}/2		V
Hysteresis	mV	V_{HYST}		50		mV
Tristate Input TRI						
Input current TRI	V_{IH} = V_{DD}	I_{IH}	0.15	0.4	1.2	µA

Figure 2. Test Circuit

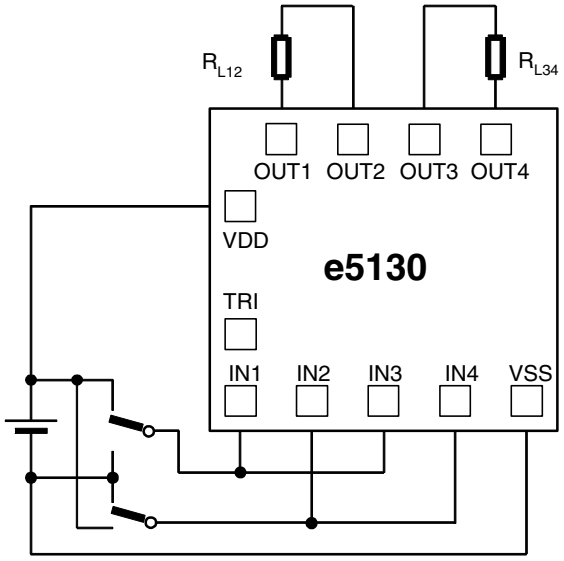
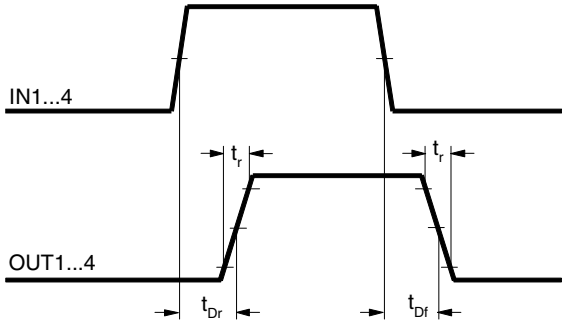


Figure 3. Drive Output Delay Time



Notes: 1. t_{Dr}, t_{Df} is defined at 50% of supply voltage
2. t_r, t_f is defined from 10% to 90%, resp. 90% to 10% of supply voltage

Figure 4. Typical Current into 200 Ω Load Resistor, Condition as per Figure 2

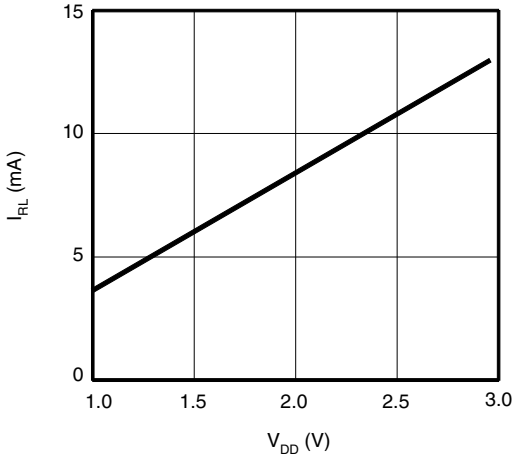


Figure 5. Typical Output ON-resistance versus Supply Voltage at V_{DS} = 0.2 V

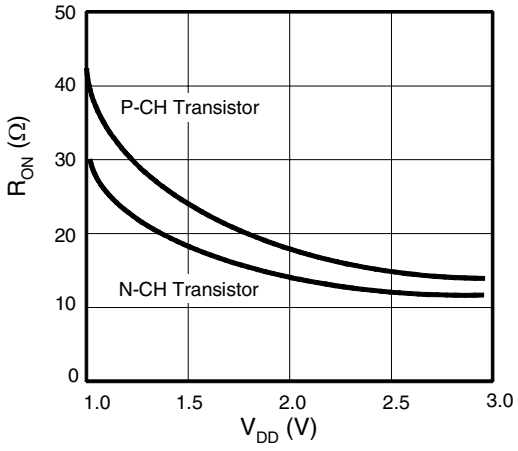


Figure 6. Pad Coordinates

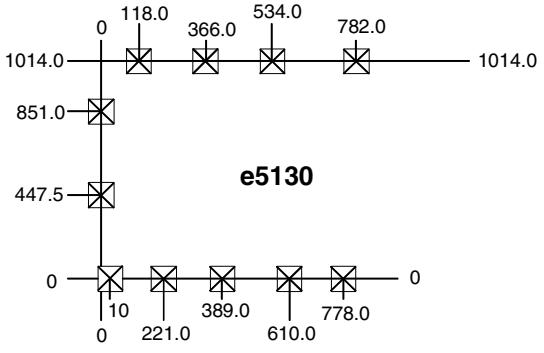
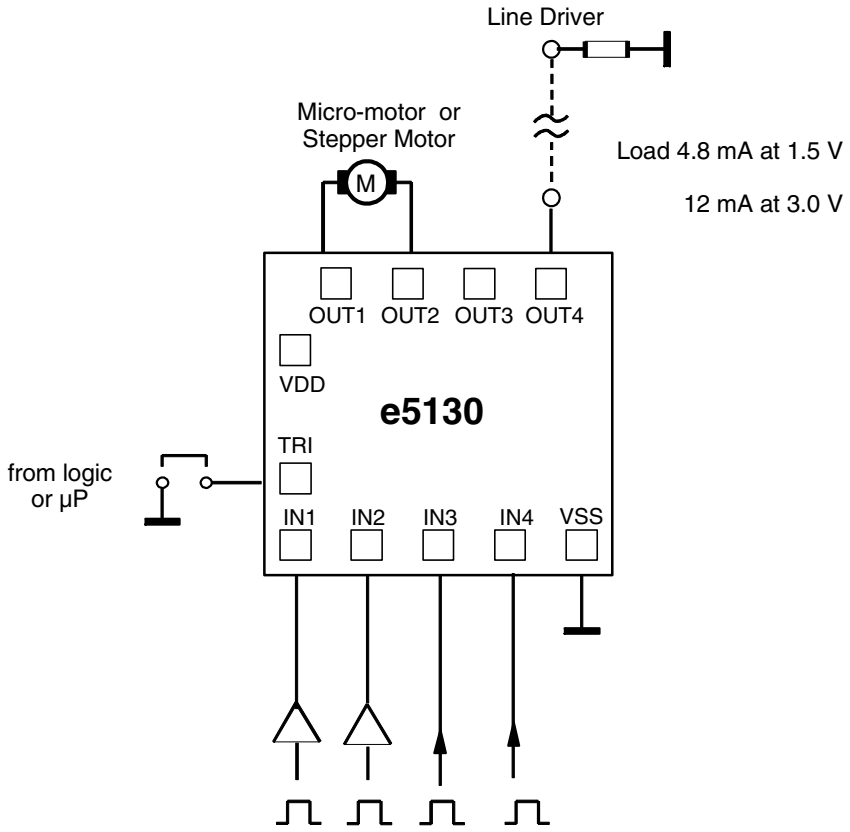


Figure 7. Application Circuit



Ordering Information

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