Features

- **High Sensitivity and High SNR Performance Linear CCD**
- **1024, 2048 or 4096 Resolution with 10 µm Square Pixels**
- **512, 1024 or 2048 Resolution with 14 µm Square Pixels**
- **100% Aperture, Built-in Anti-Blooming, No Lag**
- **CameraLink Data Format (Base Configuration)**
- **High Data Rate up to 60 Mpixels/s**
- **Flexible and Easy to Operate via RS232 Control:**
  - **Gain: 0 dB to 40 dB by Step of 0.05 dB**
  - **Output Format: 8-, 10- or 12-bit Data**
  - **Offset (for Contrast Expansion)**
  - **Trigger Mode: Free Run or External Trigger Modes**
  - **Data Output Mode (Dual, Single)**
- **Multi Camera Synchronization**
- **Single Power Supply: DC 12V to 24V**
- **Very Compact Design: 56 x 60 x 39.4 mm (w, h, l)**
- **High Reliability – CE and FCC Compliant**
- **C or F (Nikon) Mount Adapter (Lens Not Supplied)**
- **T2 (M42 x 0.75) or M42 x 1 Mount Adapter (Lens Not Supplied)**

Description

This camera is designed with three concepts in mind: accuracy, versatility and easy implementation.

- The same compact mechanical design incorporates all the sensors, from 512 to 4096 pixels.
- Atmel manages the whole chain, from the sensor to the camera. The result is a camera able to work up to 12-bit, with a dedicated electronics offering an excellent signal to noise ratio.
- The programmable settings let the user work at different integration time, gain and offset. The external clock and trigger synchronize several cameras.

Applications

Performance and reliability of this camera make it well suited for the most demanding industrial applications, from web inspection to document scanning, from surface inspection to metrology.

AViiVA™ M2 CL

CameraLink™ Linescan Camera

CAMERA Link™

CE

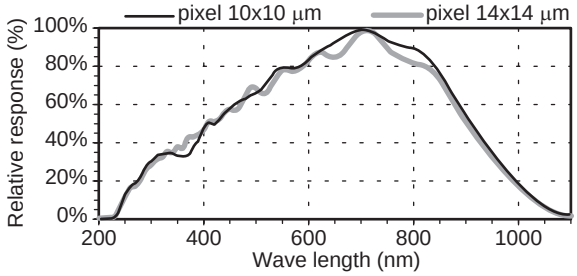
Rev. 2160B–IMAGE–04/03

Typical Performances

Table 1. Typical Performances

Parameter	Value				Unit
Sensor Characteristics at Maximum Pixel Rate					
Resolution	512	1024	2048	4096	pixels
Pixel size (square) –	14 –	14 10	14 10	– 10	µm µm
Max Line rate	98	53	28	14	kHz
Anti blooming	x 150				–
Radiometric Performances (maximum Pixel Rate, Tamb = 25°C)					
Output format	12 (also configurable in 8 or 10)				bit
Spectral range	250 - 1100				nm
Linearity	< 1				%
Gain range (step of 0.047 dB)	Gmin 0	Gnom 18	Gmax 30		 dB
Peak response(1)(2) with 14 µm pitch 10 µm pitch	130 50	1040 400	4180 1600		LSB/(nJ/cm^2) LSB/(nJ/cm^2)
SNR Effective bit	67.4 11.2	49 8.2	37 6.2		dB bit
Input RMS Noise with 14 µm pitch 10 µm pitch	14 37				pJ/cm^2 pJ/cm^2
PRNU (Pixel Response Non Uniformity)	± 3% (± 10% max)				%
Mechanical and Electrical Interface					
Size (w x h x l)	56 x 60 x 39.4				mm
Lens mount	C, F, T2, M42 x 1				–
Sensor alignment (See “Sensor Alignment” on page 14)	$\Delta x,y = \pm 50 - \Delta z = \pm 30 - \Delta tilt_z = 0\text{-}35$ $\Delta\theta x,y = \pm 0.2$				µm °
Power supply	DC, single 12 to 24V				V
Power dissipation	< 7				W
Operating temperature(3)	0 to 65 (non condensing)				°C
Storage temperature	-40 to 75 (non condensing)				°C

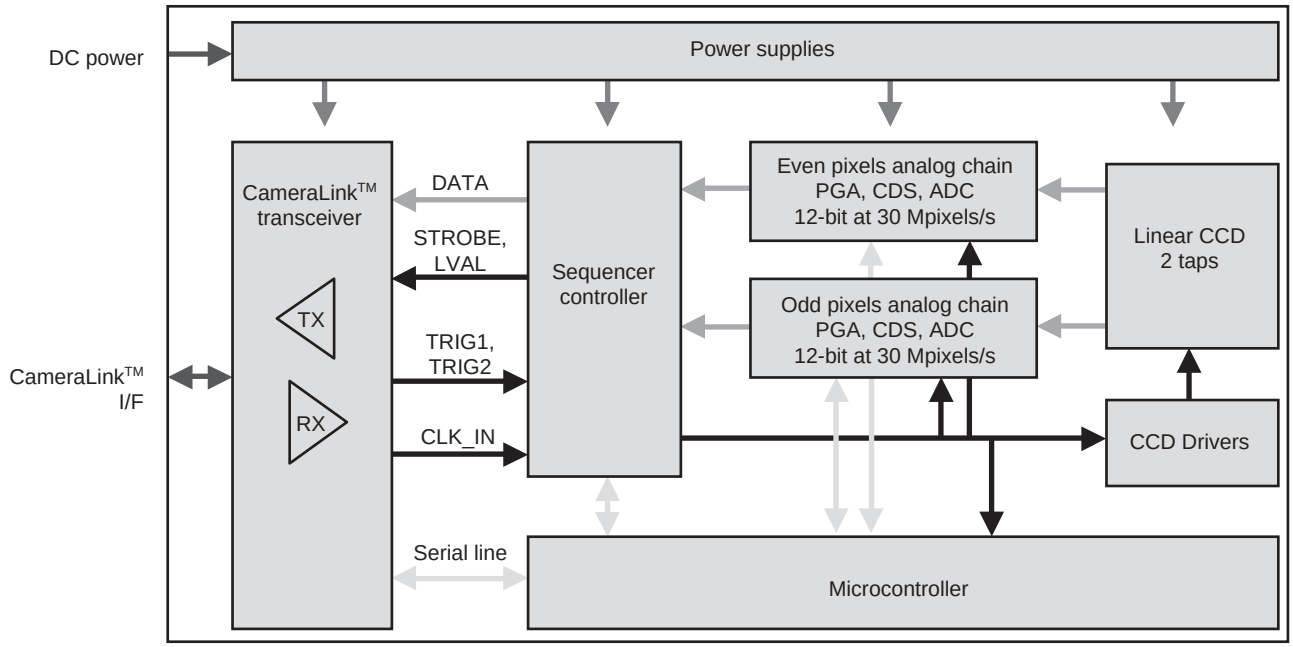
Spectral Response



Notes: 1. LSB are given for 12-bit configuration
2. nJ/cm^2 measured on the sensor
3. Camera front face temperature

Camera Description

Figure 1. Camera Synoptic



The CameraLink linescan is based on a two-tap linear CCD. Therefore, two analog chains process odd and even pixel outputs of the linear sensor. The CCD signal processing encompasses the correlated double sampling (CDS), the dark level correction (dark pixel clamping), the gain (PGA) and offset correction and finally the analog to digital conversion on 12-bit.

Note: PGA stands for Programmable Gain Array.

The camera is powered by a single DC power supply from 12V to 24V.

The functional interface (data and control) is provided with the CameraLink interface. The camera uses the base configuration of Cameralink standard.

Note: DVAL = 1 and FVAL = 0

The data can be delivered either on two channels or on a single multiplexed channel. The data format can be configured in 8-, 10- or 12-bit.
The camera can be used with external triggers (TRIG1 and TRIG2 signals) in different trigger modes (see “Synchronization Mode” on page 6). The camera can be also clocked externally, allowing system synchronization and/or multi-camera synchronization.

The camera configuration and settings are performed via a serial line.

This interface is used for:

- Gain, offset setting.
- Dynamic range, data rate setting.
- Trigger mode setting: free run or external trigger modes.
- Integration time setting: in free running and external trigger mode.

Standard Conformity

The cameras have been tested in the following conditions:

- Shielded power supply cable.
- CameraLink™ data transfer cable ref. 14B26-SZLB-500-OLC (3M).
- Linear AC-DC power supply.
- Atmel recommends using the same configuration to ensure the compliance with the following standards.

CE Conformity

AViiVA Cameras comply with the requirements of the EMC (European) directive 89/336/CEE (EN 50081-2, EN 61000-6-2).

FCC Conformity

AViiVA Cameras comply with Part 15 of FCC rules.

Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Warning: Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

Camera Command and Control

Camera configuration is set through the serial interface. Please refer to “Serial Communication” on page 10 for the detailed protocol of the serial line.

Table 2. Camera Command and Control

Setting	Command	Parameter	Description
Configuration record[1]	E=	0	The camera configuration is recorded on each change
		1	The camera configuration is recorded only on request
Gain[2]	G=	0 to 851	Gain setting from 0 to 40 dB (~0.047dB steps)
Even Gain[2]	A=	0 to 20	Even pixels gain adjustment (odd – even mismatch adjustment)
Odd Gain[2]	B=	0 to 20	Odd pixels gain adjustment (odd – even mismatch adjustment)
Data transfer[3]	H=	0	Two outputs on external clock
		1	One output (multiplexed) on external clock
		3	One output (multiplexed) at 20 MHz data rate
		5	One output (multiplexed) at 30 MHz data rate
		6	Two outputs at 20 MHz data rate
		7	One output (multiplexed) at 40 MHz data rate
		8	Two outputs at 30 MHz data rate
		9	One output (multiplexed) at 60 MHz data rate
		10	One output (multiplexed) on external clock (data frequency / 2)[7]
Output format[4]	S=	0	12-bit Output data
		1	10-bit Output data
		2	8-bit Output data
Pattern[5]	T=	0	Standard
		1	Test pattern
Integration Time	I=	5 to 13000	Integration time (µs) in free run or external triggered mode
Trigger mode	M=	1	Free run with integration time setting (see Figure 2)
		2	External trigger with integration time setting (see Figure 3)
		3	Trigger and Integration time controlled (see Figure 4)
		4	Trigger and integration time controlled by two inputs (see Figure 5)
Even data Offset[6]	O=	0 to 15	Even Offset setting from 0 to approx. 200 LSB
Odd data Offset[6]	P=	0 to 15	Odd Offset setting from 0 to approx. 200 LSB
Special commands	!=	0	Camera identification readout
		1	User camera identification readout
		2	Software version readout
		3	Camera configuration readout
		4	Current camera configuration record
		5	Default camera configuration restoration
User camera ID	$=	String of Char.	Writing and record of the user camera identification

Notes:
1. ATMEL commends to use E = 1 because of the limited EEPROM write cycles refer on page 10.
2. Camera gain (dB) = G x 0.047. A and B gain value are set in manufacturing but can be adjust if necessary.
3. Commands “H=2” and “H=4” will give 10 and 15 MHz data rate which are not compatible with CameraLink standard. Please don’t use it.
4. The pinout corresponding to this option is fully compatible with the CameraLink standard.
5. The test pattern is useful to check if the interfacing is well done. The user should see a jagged image of 256 pixels steps.

6. The offset is set in manufacturing to balance both the channels. The initial setting is about 8 (~ 130 LSB). In some cases, the user may have to change it (for example if the ambient temperature is very high).
7. To be used for multi-camera synchronisation. Refer to Figure 6.

Timing

Synchronization Mode

Four different modes may be defined under user control. The TRIG1 and TRIG2 signals may be used to trigger external events and to control the integration time. The Master clock is either external or internal clock.

Free Run Mode with Integration Time Setting

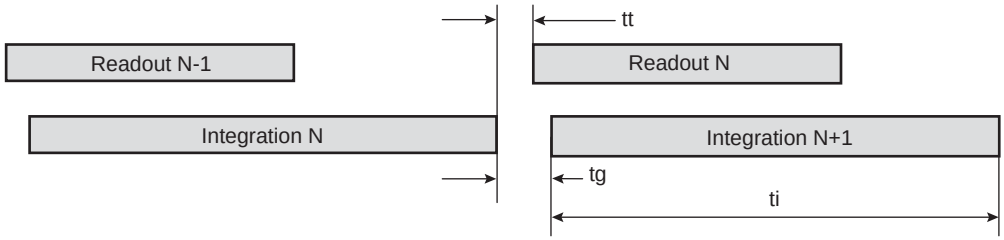
The integration and readout periods start automatically and immediately after the previous period. The read-out time depends on pixel number and pixel rate.

Table 3. Free Run Mode with Integration Time Setting

Label	Description	Min	Typ	Max
ti	Integration time duration	(1)	–	13 ms
tg	Consecutive integration period gap (at maximum frequency)	–	6 µs	–
tt	Integration period stop to read-out start delay	–	1 µs	–

Note: 1. The integration time is set by the serial line and should be higher than the read-out time (otherwise it is adjusted to the readout time).

Figure 2. Timing Diagram



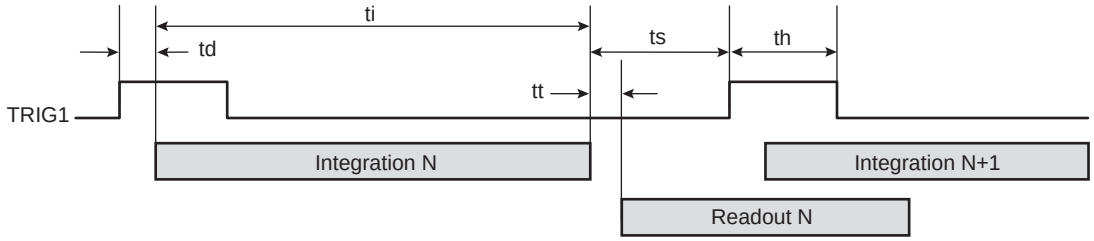
Triggered Mode with Integration Time Setting

The integration period starts immediately after the rising edge of TRIG1 input signal. The Integration time is set by the serial line. This integration period is immediately followed by a readout period. The read-out time depends on pixel number and the pixel rate.

Table 4. Triggered Mode with Integration Time Setting

Label	Description	Min	Typ	Max
ti	Integration time duration	5 µs	–	13 ms
td	TRIG1 rising to integration period start delay	–	5.5 µs	–
tt	Integration period stop to read-out start delay	–	1 µs	–
ts	Integration period stop to TRIG1 rising set-up time	4 µs	–	–
th	TRIG1 hold time (pulse high duration)	1 µs	–	–

Figure 3. Timing Diagram



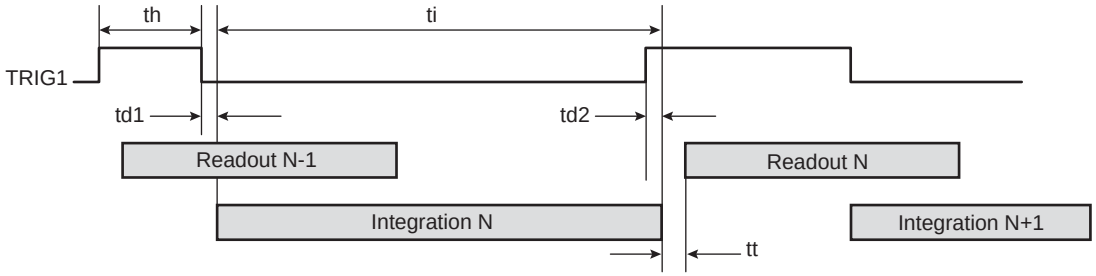
Trigger and Integration Time Controlled by One Input

The integration period starts immediately after the falling edge of TRIG1 input signal, stops immediately after the rising edge of TRIG1 input signal, and is immediately followed by a read-out period. The read-out time depends on pixel number and pixel rate.

Table 5. Trigger and Integration Time Controlled by One Input

Label	Description	Min	Typ	Max
ti	Integration time duration	5 µs	–	–
td1	TRIG1 falling to integration period start delay	–	100 ns	–
td2	TRIG1 rising to integration period stop delay	–	1.3 µs	–
tt	Integration period stop to read-out start delay	–	1 µs	–
th	TRIG1 hold time (pulse high duration)	1 µs	–	–

Figure 4. Timing Diagram



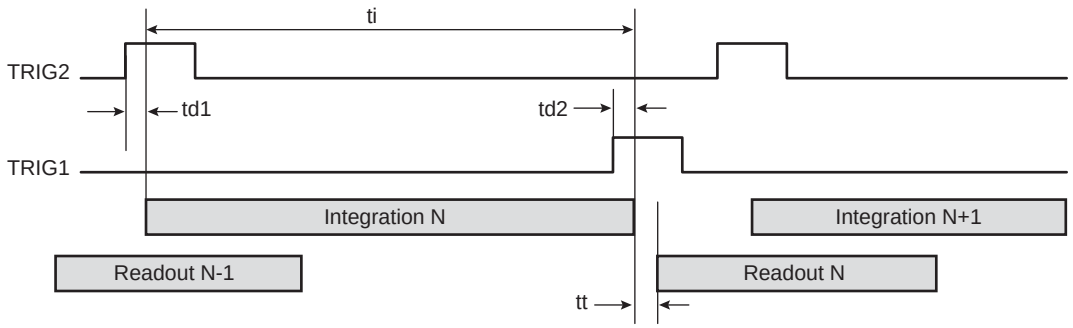
Trigger and Integration Time Controlled by Two Inputs

TRIG2 rising edge start the integration period. TRIG1 rising edge stop the integration period. This period is immediately followed by a readout period.

Table 6. Trigger and Integration Time Controlled by Two Inputs

Label	Description	Min	Typ	Max
ti	Integration time duration	5 µs	–	–
td1	TRIG2 rising to integration period start delay	–	100 ns	–
td2	TRIG1 rising to integration period stop delay	–	1.3 µs	–
tt	Integration period stop to read-out start delay	–	1 µs	–
th	TRIG1 and TRG2 hold time (pulse high duration)	1 µs	–	–

Figure 5. Timing Diagram



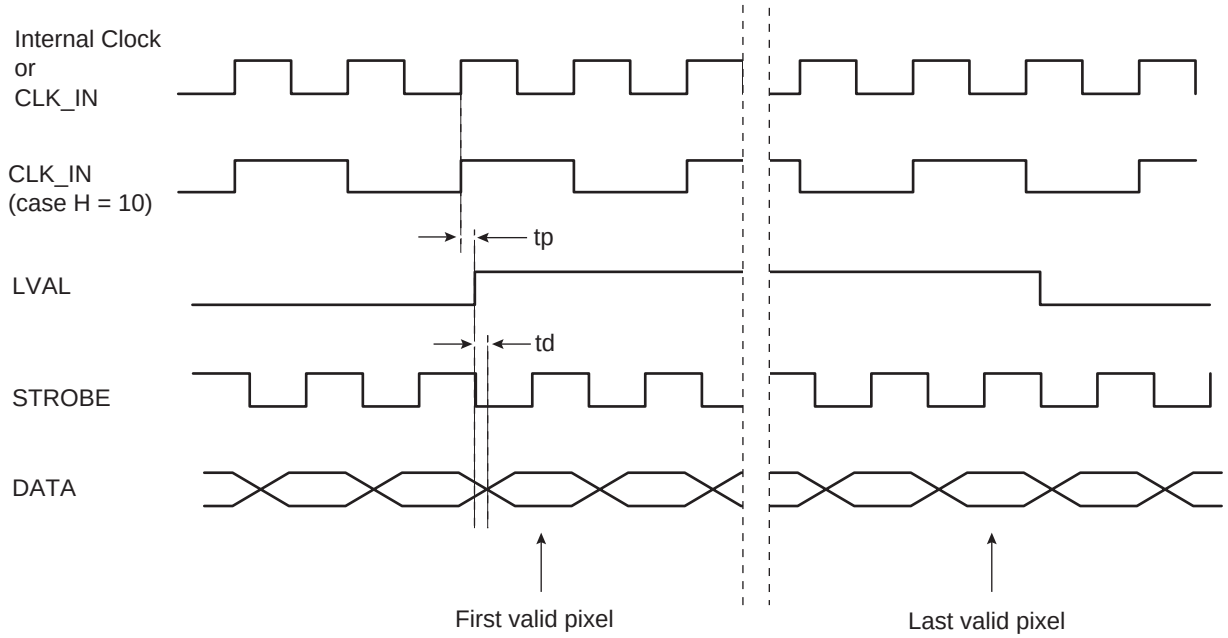
Output Data Timing

This timing corresponds to the input data of the “Chanel Link” interface. The camera output data are not detailed here because fully compliant with the CameraLink™ standard (serial high speed interface).

Table 7. Output Data Timing

Label	Description	Min	Typ	Max
tp	Input falling edge to output clock propagation delay	–	7 ns	–
td	STROBE to synchronized signals delay	-5 ns	–	+5 ns

Figure 6. Timing Diagram



Note: CLK_IN input frequency must be in the range 5 to 60 MHz. Out of this range, the performances may be decreased.

In case of **multi-cameras synchronisation** (means more than one camera on one acquisition board):

- the "master" camera will provide DATA, STROBE and LVAL signals to the acquisition board. The others will only provide DATA.
- the external clock CLK_IN must be input on each cameras to guaranty perfect data synchronisation.
- the trigger(s) input (TRIG1 and/or TRIG2) must be input on each cameras. It is recommended to synchronise the rising edge of these signals on the CLK_IN falling edge.
- cables must be balanced between each cameras (same quality, same length) to ensure perfect cameras synchronisation.
- the CLK_IN frequency must be equal to the two CCD register frequency. It means that the user shall use either H=2 (2 taps at CLK_IN data rate) or H=10 (1 tap at 2xCLK_IN data rate). **Using H=1 clock mode will provide LVAL jitter on the "slave" camera.**
- Only "trigged and integration time controlled" (M=3 or M=4) can be used. These modes ensure perfect readout phase starting for each cameras.

Electrical Interface

Power Supply

It is recommended to insert a 1A fuse between the power supply and the camera.

Table 8. Power Supply

Signal Name	I/O	Type	Description
PWR	P	–	DC power input: +12V to +24V (±0.5V)
GND	P	–	Electrical and Mechanical ground

I = input, O = output, IO = bi-directional signal, P = power/ground, NC = not connected

Camera Control

The CameraLink interface provides four LVDS signals dedicated to camera control (CC1 to CC4). On the AViiVA, three of them are used to synchronize the camera on external events.

Table 9. Camera Control

Signal Name	I/O	Type	Description
TRIG1	I	RS644	CC1 – Synchronization input (refer to “Synchronization Mode” on page 6)
TRIG2	I	RS644	CC2 – Start Integration period in dual synchro mode (refer to “Synchronization Mode” on page 6)
CLK_IN	I	RS644	CC4 – External clock for (multi-)camera synchronization (refer to “Synchronization Mode” on page 6)

I = input, O = output, IO = bi-directional signal, P = power/ground, NC = not connected

Note: CC3 is not used.

Video Data

Data and enable signals are provided on the CameraLink interface.

Table 10. Video Data

Signal Name	I/O	Type	Description
ODD[11-0]	O	RS644	Odd pixel data (refer to “Output Data Timing” on page 8), ODD-00 = LSB, ODD-11 = MSB
EVEN[11-0]	O	RS644	Even pixel data (refer to “Output Data Timing” on page 8), EVEN-00 = LSB, EVEN-11 = MSB
STROBE	O	RS644	Output data clock (refer to “Output Data Timing” on page 8), data valid on the rising edge
LVAL	O	RS644	Line valid (refer to “Output Data Timing” on page 8), active high signal

I = input, O = output, IO = bi-directional signal, P = power/ground, NC = not connected

Notes: FVAL, as defined in the CameraLink standard, is not used. FVAL is permanently tied to 0 (low) level.
DVAL is not used. DVAL is permanently tied to 1 (high) level.
In case of Single output, the data (multiplexed) are output in place of Odd data.

Serial Communication

The CameraLink interface provides two LVDS signal pairs for the communication between the camera and the frame grabber. This is an asynchronous serial communication based on RS-232 protocol.

The configuration of the serial line is:

- Full duplex/without handshaking
- 9600 bauds, 8-bit data, no parity bit, 1 stop bit.

Table 11. Serial Communication

Signal Name	I/O	Type	Description
SerTFG	O	RS644	Differential pair for serial communication to the frame grabber
SerTC	I	RS644	Differential pair for serial communication from the frame grabber

Command Syntax

The valid syntax is "S = n(CR)" with:

- S: command identification as per “Camera Command and Control” on page 4. S is a single character in upper case.
- n: setting value.
- (CR): means "carriage return".

no space, nor tab may be inserted between S, =, n and (CR).

Example of a valid command:

- G = 3(CR): sets the camera to gain 3 (refer to “Camera Command and Control” on page 4 for exact value calculation).

Example of non valid commands:

- G = 3(CR): spaces.
- g = 3(CR): g instead of G.
- G = 1040(CR): 1040 is outside of range.

Command Processing

Each command received by the camera is processed:

- If the command is valid:
  - the setting is done in case of a write command.
  - the camera returns the data separated by (CR) in case of the read command.
  - the camera returns: >OK(CR).
- If the command is not valid:
  - nothing is done.
  - the camera returns: >1 = out of range; >2 = syntax error; >3 = command too long; >4,>6,>7 = internal error; >5 undefined function.

Example: when receiving "! = 3(CR)’’ the camera returns its current settings:

- A = 0(CR); B = 0(CR); ....; E = 0(CR); >OK(CR).

Storage of the Settings in EEPROM

ATMEL recommends to use "E = 1" for settings that are often changed (check the maximum number of write cycles above) and when the time required by the camera to process a command is critical. The maximum number of write cycles allowed for the EEPROM is: 100 000.

Connector Description

All connectors are on the rear panel.

Note: Cables for digital signals shall be shielded twisted pairs.

Power Supply

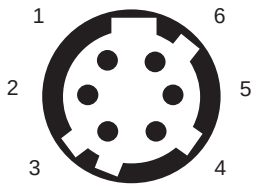
Camera connector type: Hirose HR10A-7R-6PB (male).

Cable connector type: Hirose HR10A-7P-6S (female).

Table 12. Power Supply Connector Pin-out

Signal	Pin	Signal	Pin
PWR	1	GND	4
PWR	2	GND	5
PWR	3	GND	6

Figure 7. Receptacle Viewed from Camera Back



CameraLink Connector

Standard CameraLink cable shall be used to ensure the full electrical compatibility.

Camera connector type: MDR-26 (female) ref. 10226-2210VE.

Cable connector type: Standard CameraLink cable shall be used (ex. 3M - 14B26-SZLB-x00-OLC).

Table 13. CameraLink Connector Pin-out

Signal	Pin	Signal	Pin	Signal	Pin
GND	1	CC2+	10	X3+	19
X0-	2	CC3-	11	SerTC-	20
X1-	3	CC4+	12	SerTFG+	21
X2-	4	GND	13	CC1+	22
Xclk-	5	GND	14	CC2-	23
X3-	6	X0+	15	CC3+	24
SerTC+	7	X1+	16	CC4-	25
SerTFG-	8	X2+	17	GND	26
CC1-	9	Xclk+	18		

Bit Assignments

This bit assignment is compliant with the CameraLink Specification in the Base Configuration.

In "single output" mode (multiplexed), the data are output on ODD-xx bit.

Table 14. Bit Assignments when used in 12-bit data (S = 0)

Bit	DS90CR285 Pin Name	Bit	DS90CR285 Pin Name	Bit	DS90CR285 Pin Name	Bit	DS90CR285 Pin Name
ODD-00	Tx0	ODD-07	Tx5	EVEN-02	Tx19	EVEN-09	Tx14
ODD-01	Tx1	ODD-08	Tx7	EVEN-03	Tx20	EVEN-10	Tx10
ODD-02	Tx2	ODD-09	Tx8	EVEN-04	Tx21	EVEN-11	Tx11
ODD-03	Tx3	ODD-10	Tx9	EVEN-05	Tx22	STROBE	TxCLK
ODD-04	Tx4	ODD-11	Tx12	EVEN-06	Tx16	LVAL	Tx24
ODD-05	Tx6	EVEN-00	Tx15	EVEN-07	Tx17		
ODD-06	Tx27	EVEN-01	Tx18	EVEN-08	Tx13		

Table 15. Bit Assignments when used in 10-bit data (S = 1)

Bit	DS90CR285 Pin Name	Bit	DS90CR285 Pin Name	Bit	DS90CR285 Pin Name	Bit	DS90CR285 Pin Name
ODD-00	Tx0	ODD-07	Tx5	EVEN-02	Tx19	EVEN-09	Tx14
ODD-01	Tx1	ODD-08	Tx7	EVEN-03	Tx20	NC	Tx10
ODD-02	Tx2	ODD-09	Tx8	EVEN-04	Tx21	NC	Tx11
ODD-03	Tx3	NC	Tx9	EVEN-05	Tx22	STROBE	TxCLK
ODD-04	Tx4	NC	Tx12	EVEN-06	Tx16	LVAL	Tx24
ODD-05	Tx6	EVEN-00	Tx15	EVEN-07	Tx17		
ODD-06	Tx27	EVEN-01	Tx18	EVEN-08	Tx13		

Table 16. Bit Assignments when used in 8-bit data (S = 2)

Bit	DS90CR285 Pin Name	Bit	DS90CR285 Pin Name	Bit	DS90CR285 Pin Name	Bit	DS90CR285 Pin Name
ODD-00	Tx0	ODD-07	Tx5	NC	Tx19	EVEN-05	Tx14
ODD-01	Tx1	EVEN-00	Tx7	NC	Tx20	EVEN-06	Tx10
ODD-02	Tx2	EVEN-01	Tx8	NC	Tx21	EVEN-07	Tx11
ODD-03	Tx3	EVEN-02	Tx9	NC	Tx22	STROBE	TxCLK
ODD-04	Tx4	EVEN-03	Tx12	NC	Tx16	LVAL	Tx24
ODD-05	Tx6	NC	Tx15	NC	Tx17		
ODD-06	Tx27	NC	Tx18	EVEN-04	Tx13		

Mechanical Characteristics

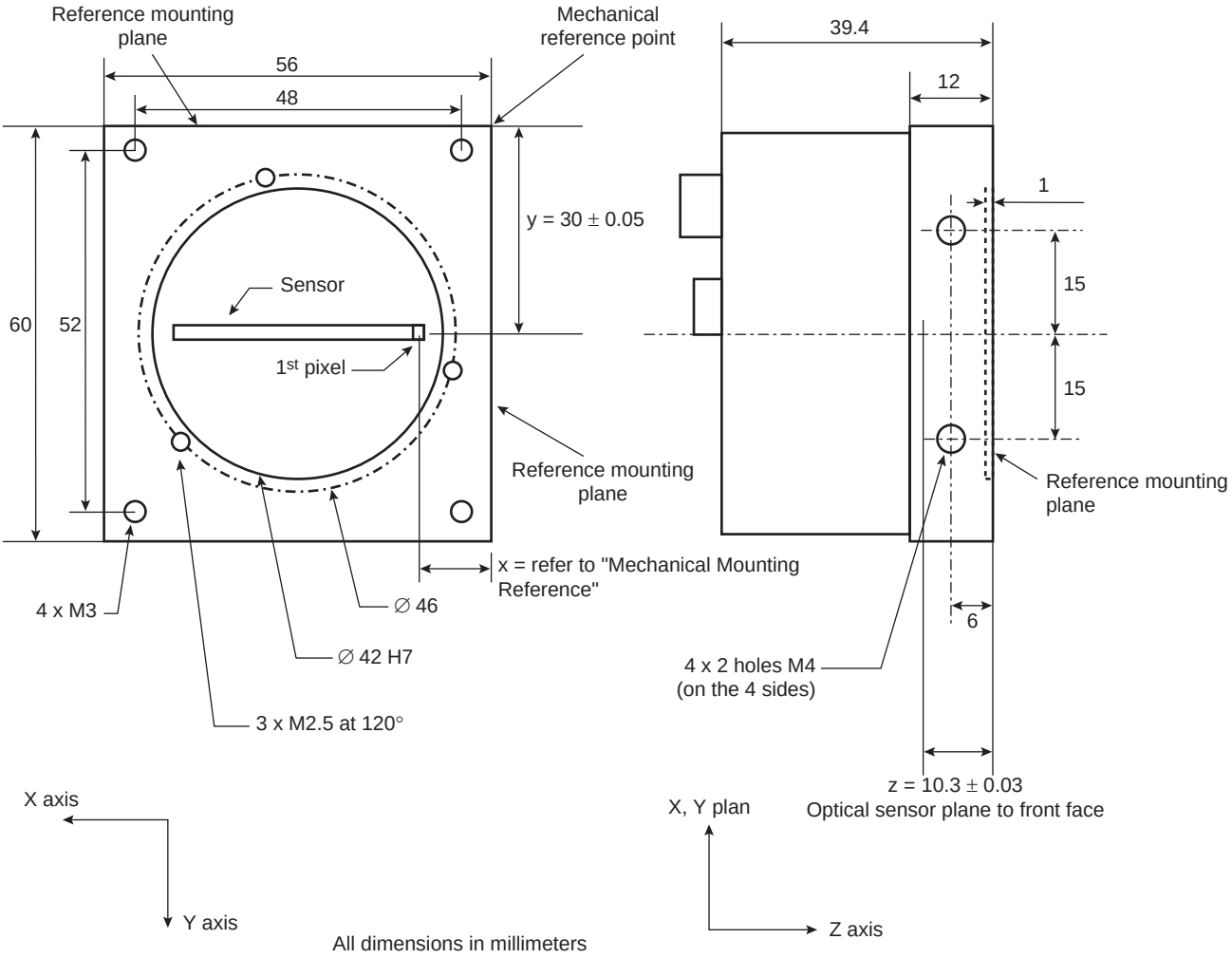
Weight

The camera typical weight (without lens nor lens adapter) is 220 g/7.7 ounces (typical).

Dimensions

The camera dimensions (without lens) are W = 56 mm, H = 60 mm, L = 39.4 mm.

Figure 8. Mechanical Box Drawing and Dimensions



Mechanical Mounting Reference

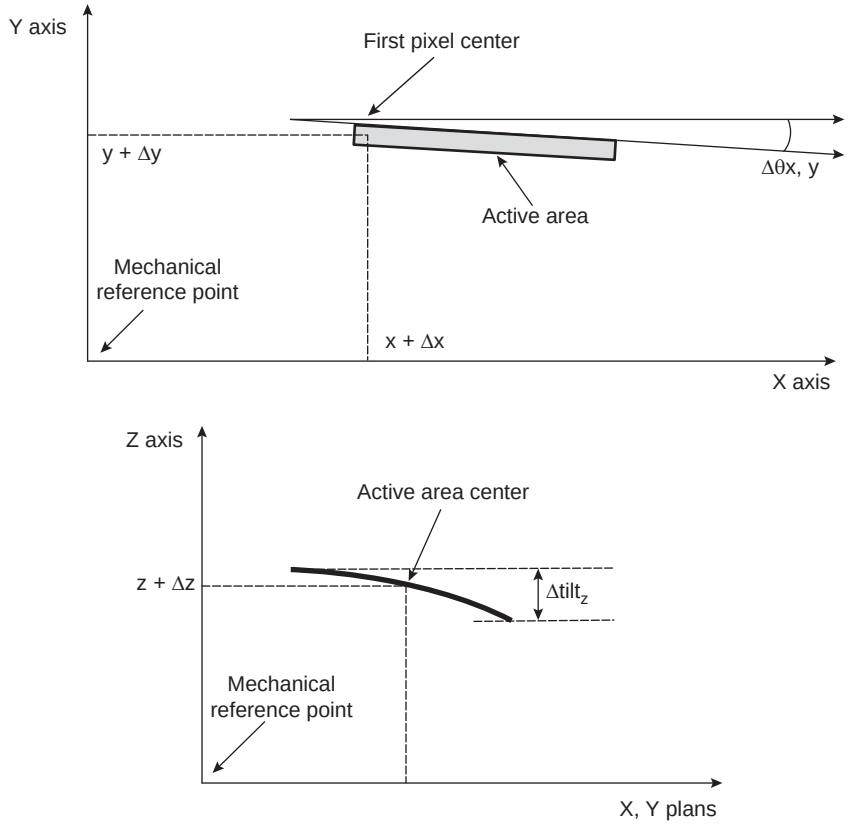
The front panel mechanical part is designed to support the mounting of the camera. On this mechanical part, three surfaces are considered as mounting reference surface: i.e. the distance between these surfaces and the first active pixel are known very precisely (better than ±50 µm).

Table 17. Mechanical Mounting Reference

Number of Pixels	512	1024	2048	4096
x with 14 µm sensor (nm)	24.416	20.832	13.664	–
x with 10 µm sensor (nm)	–	22.880	17.760	7.520

Sensor Alignment

Figure 9. Sensor Alignment Diagram



Lens Mounting (Lens Not Supplied)

The camera can be provided with three different lens adapter, corresponding to three different options. The user has to selected the correct adapter. The following table gives recommendations according to the sensor size.

Table 18. Lens Mounting

Number of Pixels	512/14 µm	1024/10 µm	1024/14 µm	2048/10 µm	2048/14 µm	4096/10 µm
C mount	OK	OK	~OK(1)	~OK(1)	not usable	not usable
F mount	OK	OK	OK	OK	OK	OK

Note: 1. Depends on the lens quality.

Heat-sink Mounting

In order to improve the power dissipation, the camera can be delivered with heat-sink to be mounted by the user on the side faces of the camera. The delivery of the heat-sinks corresponds to a dedicated option.

Ordering Code

Table 19. Ordering Code

Part Number	Resolution	Pixels Size	Description
AT71M2CL1010-BA0	1K	10 µm	AViiVA M2 CL 1010
AT71M2CL2010-BA0	2K	10 µm	AViiVA M2 CL 2010
AT71M2CL4010-BA0	4K	10 µm	AViiVA M2 CL 4010
AT71M2CL0514-BA0	512	14 µm	AViiVA M2 CL 0514
AT71M2CL1014-BA0	1K	14 µm	AViiVA M2 CL 1014
AT71M2CL2014-BA0	2K	14 µm	AViiVA M2 CL 2014
AT71KFPAVIVA-ABA	–	–	F mount (NIKON)
AT71KFPAVIVA-AKA	–	–	T2 mount (M42 x 0.75)
AT71KFPAAVIVA-ADA	–	–	M42 x 1 mount
AT71KFPAVIVA-ACA	–	–	C mount
AT71KAVIVAP2C0D3A0	–	–	Cables kit: 10m power supply and 5m CameraLink cables

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