Features

- 64K x 32-bit Flash Embedded Memory Cell
- Fast Read Access Time
  - Random Access Time: 70 ns Worst Case (Process, Voltage, Temperature)
  - Page Access Time: 40 ns Worst Case (Process, Voltage, Temperature)
- Single Supply Voltage: 1.8V ±10%
- Page Program Operation
  - 1024 Pages (64 Words/Page)
  - Internal Data Latches For 64 Words
  - Read Capability During Data Load
- Program Cycle Time: 4 ms per Page Including Auto-erase
- Full Chip Erase Available in 10 ms
- rdybsyn Signal For End of Program Detection
- Very Low Power Dissipation
  - 8 mA Active Current in Write and Erase
  - 4 mA Active Current in Random Read
  - 30 µA Stand-by Current
- High Reliability CMOS Technology
  - Typical Endurance: 100K Write/Word
  - Data Retention: 10 Years
- Erased State (Charged Gate) Is a Logic "1"

Description

The 64K x 32-bit cell is an embedded 2-Mbit Flash electrically erasable and programmable read only memory with a power supply of 1.8V ±10%. The memory is organized as 1024 pages of 64 32-bit words each. The device uses the Atmel ATC18 0.18 µm silicon process. For easy reprogrammability, it does not require a high input voltage for programming: the embedded Flash can be operated with a single 1.8V ±10% power supply.

Re-programming the cell is performed on a page basis: the words to be written (from a minimum of 1 word to a maximum of 64 words) are loaded into the device and then simultaneously written into the targeted page after the full page has been erased during the auto-erase phase. 2 ms are necessary to erase the page, followed by 2 ms to write the words, independent of the number of words that are written in parallel into the targeted page. Thus the write time after the auto-erase varies from a maximum of 2 ms per word if only 1 word is written to a minimum of 32 µs per word if the entire page is written at a time. Memory read is allowed during data loading and forbidden once programming has started. The signal rdybsyn pulses low at the beginning of the program cycle to indicate that the memory is not ready for a read operation. Programming the entire memory can be done using a full chip erase followed by 1024 page write without auto-erase. Compared to full-memory programming using auto-erase on each page, the programming time is reduced by half. At the end of each program cycle, the rdybsyn signal pulses high to indicate that programming is completed and the memory available for a new program or read cycle. Reading data out of the device can be done in an asynchronous and random manner, with 70 ns access time.

Embedded ASIC Memory Cell

ATC18 64K x 32-bit Low-power Flash

Advance Information

Rev. 2680A–CASIC–11/02

DC and AC Operating Range

Conditions are:

- Operating temperature: -40°C to 85°C

Table 1. Parameters

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Power Supply	1.6	1.8	2.0	
t_{ACC}	Read Access Time			70	ns
t_{BACC}	Page Access Time			40	
t_{WC}	Write Cycle Time[1]			4	ms

Note: 1. The max value includes auto-erase.

Table 2. DC Characteristics

Symbol	Parameter	Condition	Max
I_{SB}	Standby Current	V_{DD} = 2.0V	30 uA
I_{CC}	Active Current	Random Read: V_{DD} = 2.0V, 10 MHz	4.0 mA
		Write: V_{DD} = 2.0V	8.0 mA

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