

SmartSwitch™

General Description

The AAT4650 SmartSwitch™ is a single channel PC Card (PCMCIA) power switch. It is used to select between two different voltage inputs, each between 2.7V and 5.5V. An internal switch powers the circuitry from whichever input voltage is higher. The device's output, V_{CC}, is slew rate controlled and current limited, in compliance with PC Card specifications. The current limit response time to a short circuit is typically 1µs. The internal P-Channel MOS-FET switches are configured to break before make, that is, both switches cannot be closed at the same time. Controlled by a 2 bit parallel interface, the four states for V_{CC} are $V_{CC}5$, $V_{CC}3$, Hi-impedance, or Ground. When in the ground state, V_{CC} is pulled to ground by a $5k\Omega$ resistor. An open drain FAULT output is asserted during over-current conditions. During power up slewing, FAULT also signals that V_{CC} is out of tolerance. An internal over temperature sensor forces V_{CC} to a high impedance state when an over-temperature condition exists. Quiescent current is typically a low 15µA, as long as I_{CC} is less than approximately 500mA. Above this load current, the guiescent current increases to 200µA.

The AAT4650 is available in 8-pin SOP and TSSOP packages specified over -40 to 85°C.

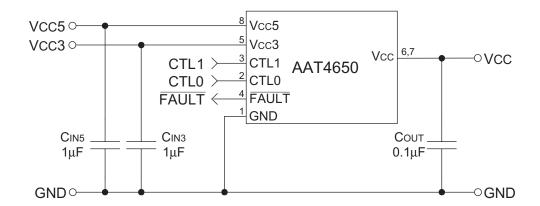
Features

- 2.7V to 5.5V Input voltage range
- 85m Ω (5V) typical R_{DS(ON)}
- Low quiescent current 15µA (typ)
- Reverse-blocking switches
- · Short-circuit protection
- Over-temperature protection
- FAULT flag output
- Temp range -40 to 85°C
- 8 pin SOP or TSSOP package

Applications

- Notebook Computer
- PDA, Subnotebook
- Power Supply Multiplexer Circuit

Typical Application



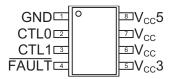


Pin Descriptions

Pin #	Symbol	Function
1	GND	Ground connection
2	CTL0	Control input (see Control Logic Table below)
3	CTL1	Control input (see Control Logic Table below)
4	FAULT	Open drain output signals over-current condition
5	V _{CC} 3	3V supply
6	V _{cc}	Output (see Control Logic Table below)
7	V _{cc}	Output (see Control Logic Table below)
8	V _{CC} 5	5V supply

Pin Configuration

SO-8 / TSSOP-8 (Top View)



Control Logic Table

CTL1	CTL0	Function	Result
0	0	OFF	5k V _{CC} to GND
0	1	5v	V _{CC} =V _{CC} 5
1	0	3v	V _{CC} =V _{CC} 3
1	1	HiZ	Both FETs OFF



Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Symbol	Description	Value	Units
V _{CC} 3, V _{CC} 5	IN to GND	-0.3 to 6	V
V _{CC}	OUT to GND	-0.3 to 6	V
I _{MAX}	Maximum Continuous Switch Current	Current Limited	А
T _J	Operating Junction Temperature Range	-40 to 150	°C
T _{LEAD}	Maximum Soldering Temperature (at Leads)	300	°C
V _{ESD}	ESD Rating ¹ — HBM	4000	V

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

Note 1: Human body model is a 100pF capacitor discharged through a 1.5k Ω resistor into each pin.

Thermal Characteristics

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance (SOP-8) ²	100	°C/W
P _D	Power Dissipation (SOP-8) ²	1.25	W

Note 2: Mounted on an FR4 board.

Electrical Characteristics ($V_{IN} = 5V$, $T_A = -40$ to 85°C unless otherwise noted. Typical values are at $T_A = 25$ °C; **bold** values designate full temperature range)

Symbol	Description	Conditions	Min	Тур	Max	Units
V _{CC} Outpu	V _{CC} Output					!
I _{CC} Hi-Z	High impedance Output Leakage Current	OFF mode, V _{CC} =0V			1	μА
Iccsc	Short Circuit Current Limit	V_{CC} = V_{CCIN} -0.5V, ON mode V_{CC} 3 or V_{CC} 5 selected, T_A =25°C	1.0		2.0	Α
D	On-Resistance	V _{CC} =3.0v, T _A =25°C		85	110	mΩ
$R_{DS(ON)}$	On-Resistance	V _{CC} =5.0v, T _A =25°C		80	100	mΩ
Tcrds	Switch Resistance Tempco			2800		ppm/°C
V _{CC} Switcl	ning Time (Refer to Figure 1)			•	•	•
t1	Output Turn-On Delay Time	V_{CC} =0v to 10% of 3.3V, R_{OUT} =10 Ω		500	2000	μs
t2	Output Turn-On Delay Time	V_{CC} =0v to 10% of 5.0V, R_{OUT} =10 Ω		500	1500	μs
t3	Output Rise Time	V_{CC} =10% to 90% of 3.3V, R_{LOAD} =10 Ω	300	1000	3000	μs
t4	Output Rise Time	V_{CC} =10% to 90% of 5.0V, R_{LOAD} =10 Ω	300	1000	3000	μs
t5	Output Turn-Off Delay Time	V_{CC} =3.3 to 90% of 3.3V, R_{LOAD} =10 Ω			400	μs
t6	Output Turn-Off Delay Time	V_{CC} =5.0 to 90% of 5.0V, R_{LOAD} =10 Ω			400	μs
t7	Output Fall Time to OFF State	V_{CC} =90% to 10% of 3.3V, R_{LOAD} =10 Ω			200	μs
t8	Output Fall Time to OFF State	V_{CC} =90% to 10% of 5.0V, R_{LOAD} =10 Ω			200	μs
t9	Output Fall Time to Hi-Z State	V_{CC} =90% to 10% of 3.3V, R_{LOAD} =10 Ω			1500	μs
t10	Output Fall Time to Hi-Z State	V_{CC} =90% to 10% of 5.0V, R_{LOAD} =10 Ω			2000	μs



Description	Conditions	Min	Тур	Max	Units
ply					
V _{CC} 3 Operation Voltage		2.7		5.5	V
V _{CC} 5 Operation Voltage		2.7		5.5	V
	V _{CC} =5V or HiZ or OFF,			1	μA
V _{CC} 3 Supply Current	V _{CC} 3 <v<sub>CC5, I_{CC} Out=0</v<sub>				
	V_{CC} =3.3v, V_{CC} 3< V_{CC} 5, I_{CC} Out=0		5	20	μA
	V _{CC} =Off, V _{CC} 5>V _{CC} 3, I _{CC} Out=0			1	μA
V F Supply Current	V _{CC} =HiZ, V _{CC} 5>V _{CC} 3, I _{CC} Out=0		10	40	μΑ
V _{CC} 3 Supply Current	V _{CC} =3.3v, V _{CC} 5>V _{CC} 3 ,I _{CC} Out=0		10	40	μΑ
	V _{CC} =5v, V _{CC} 5>V _{CC} 3, I _{CC} Out=0		15	40	μA
erface					
CTL Input Low Voltage				0.8	V
CTL Input High Voltage	V _{CC} 3 or V _{CC} 5=2.7 to 3.6V	2.0			V
	V _{CC} 3 or V _{CC} 5=4.5 to 5.5V	2.4			V
CTL Input leakage	V _{CTL} = 5.5V		0.01	1	μA
FAULT Logic Output Low	I _{SINK} =1mA			0.4	V
Voltage					
FAULT Logic Output High	V _{FAULT} = 5.5V		0.05	1	μA
Leakage Current					
Over Temperature Shutdown			125		degC
	V _{CC} 3 Operation Voltage V _{CC} 5 Operation Voltage V _{CC} 5 Operation Voltage V _{CC} 3 Supply Current V _{CC} 5 Supply Current erface CTL Input Low Voltage CTL Input High Voltage CTL Input leakage FAULT Logic Output Low Voltage FAULT Logic Output High Leakage Current	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$

Timing Diagram

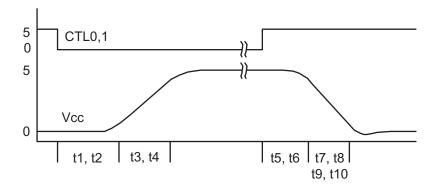


Figure 1: V_{CC} Switching Time Diagram

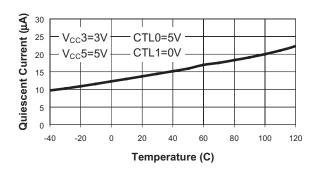
Refer to V_{CC} Switching Time specifications under the Electrical Characteristics section for definitions of t1 to t10.



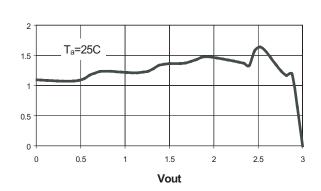
Typical Characteristics

(Unless otherwise noted, $T_A = 25^{\circ}C$)

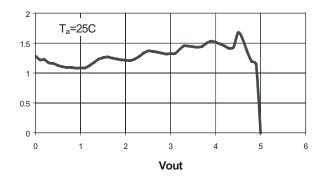
Quiescent Current vs. Temperature (I_{CC}5)



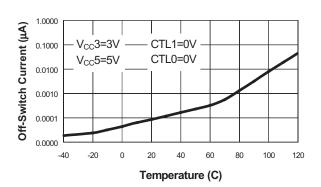
Current Limit V_{CC}=V_{CC}3



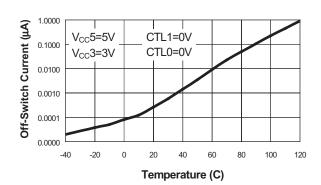
Current Limit V_{CC}=V_{CC}5



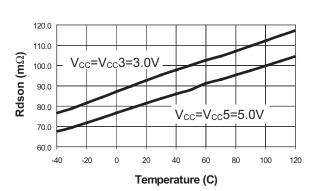
Off-Switch Current vs. Temperature (I_{CC}3)



Off-Switch Current vs. Temperature I_{CC}5



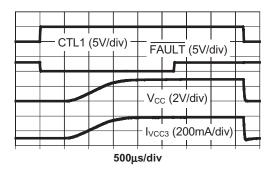
Rdson vs. Temperature



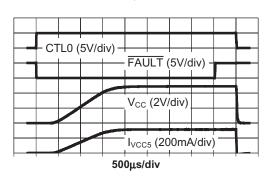


(Unless otherwise noted, $T_A = 25$ °C)

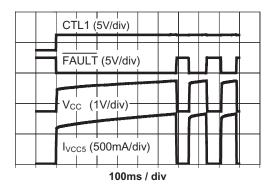
Turn-ON/OFF Response with 10 Ohm 1μF load



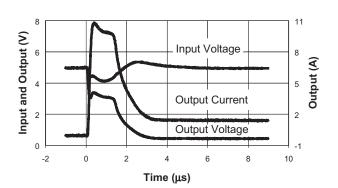
Turn-ON/OFF Response with 15 Ohm 1μF load



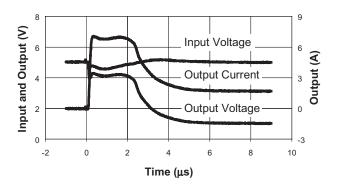
Thermal Shutdown Response



Short Circuit Through 0.3 Ohm



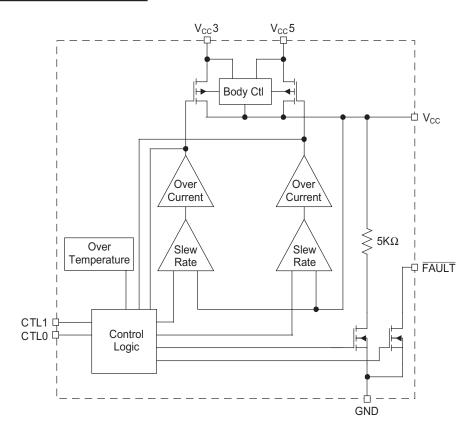
Short Circuit Through 0.6 Ohm



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Functional Block Diagram



Functional Description

The AAT4650 is a single channel power switch that can be used in any application where dual power supply multiplexing is required. Typical applications for this include PC card applications not requiring a 12 volt power supply, or applications where power is switched, for example, between 5 volts for operation and 3.3 volts for standby mode. The AAT4650 operates with input voltages ranging from 2.7 to 5.5 volts in any combination and automatically powers its internal circuitry off of whichever input voltage is higher. Two identical low R_{DS} P-channel MOSFETS serve as the power multiplexing circuit with a common drain as the Vcc output and independent sources as the two Vcc3 and Vcc5 inputs. A two bit parallel interface determines the state of the multiplexer: Vcc=Vcc3, Vcc=Vcc5, Vcc with resistive pull down to ground, or Vcc hi-impedance. When the state is set to either of the two inputs, the multiplexing circuit will slowly slew the V_{CC} output to the new voltage level which protects the upstream power supply from sudden load transients. When the resistive pull down is chosen for V_{CC} , the V_{CC} output is quickly discharged by the resistive pull down. The AAT4650 always serves as an electronic fuse by limiting the load current if it exceeds the current limit threshold. During power up into a short, the current will gradually increase until the current limit is reached. During a sudden short circuit on the output, the current limit will respond in 1 µs to isolate and protect the upstream power supply from the load short circuit. In most applications, because the response time is so fast, a short circuit to V_{CC} will not affect the upstream supply, so system functionality will not be affected. In the case of an over current condition, an open drain FAULT flag output will signal the event. The FAULT output is also active during output voltage slew, and becomes inactive once the output is within regulation.



Applications Information

Input Capacitor

Typically a 1µF or larger capacitor is recommended for C_{IN} . A C_{IN} capacitor is not required for basic operation, however, it is useful in preventing load transients from affecting up stream circuits. C_{IN} should be located as close to the device V_{IN} pin as practically possible. Ceramic, tantalum or aluminum electrolytic capacitors may be selected for C_{IN} . There is no specific capacitor ESR requirement for C_{IN} . However, for higher current operation, ceramic capacitors are recommended for C_{IN} due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

A 0.1 μ F or greater capacitor is generally required between Vcc and GND. Likewise, with the output capacitor, there is no specific capacitor ESR requirement. If desired, C_{OUT} may be increased to accommodate any load transient condition.

Parallel Interface / Break Before Make

A two bit parallel interface determines the state of the Vcc output. The logic levels are compatible with CMOS or TTL logic. A logic low value must be less than 0.8 volts, and a logic high value must be greater than 2.4 volts. In cases where the interface pins rapidly change state directly from 3v to 5v (or vice versa), internal break before make circuitry prevents any back flow of current from one input power supply to the other. In addition, the body connections of the internal P-channel MOSFET switches are always set to the highest potential of Vcc3, Vcc5, or Vcc, which prevents any body diode conduction, power supply backflow, or possible device damage.

FAULT Output

The FAULT output is pulled to ground by an open drain N-channel MOSFET during an over current or output slew condition. It should be pulled up to the reference power supply of the controller IC via a nominal $100 \text{K}\Omega$ resistor.

Voltage Regulation

The PC Card Specification calls for a regulated 5 volt supply tolerance of +/-5%. Of this, a typical power supply will drop less than 2%, and the PCB traces will drop another 1%. This leaves 2% for the AAT4650 as the PC card switch. In the PC card application, the maximum allowable current for the

AAT4650 is dominated by voltage regulation rather than by thermal considerations, and is set by either the current limit or the maximum R_{DS} of the P-channel MOSFET. The maximum R_{DS} at 85°C is calculated by applying the R_{DS} Tempco to the maximum room temperature R_{DS} :

$$R_{DS(MAX)}$$
 = R_{DS25} x (1 + TC x ΔT), or $R_{DS(MAX)}$ = 105m Ω x (1 + 0.0028 x 60) = 122m Ω

The maximum current is equal to the 2% tolerance of the 5 volt supply (100mV) across the AAT4650 divided by $R_{\rm DS(MAX)}$. Or

$$I_{MAX5} = 100 \text{mV} / 122 \text{m}\Omega = 820 \text{mA}$$

For the 3.3 volt supply in the PC card application, the conditions are a bit relaxed, with the allowable voltage regulation drop equal to 300mV. With a 2% supply, and 1% PCB trace regulation, the PC card switch can have a 200mV drop. So

$$I_{MAX3} = 200 \text{mV} / 134 \text{m}\Omega = 1.5 \text{A}$$

Since 1.5A is the nominal current limit value, the AAT4650 will current limit before I_{MAX3} is reached.

Thermal issues are not a problem in the SO-8 package since Θ_{JA} , the package thermal resistance, is only 120°C/W. At any given ambient temperature (T_A) the maximum package power dissipation can be determined by the following equation:

$$P_{D(MAX)} = [T_{J(MAX)} - T_A] / \Theta_{JA}$$

Constants for the AAT4650 are maximum junction temperature, $T_{J(MAX)}$ = 125°C, and package thermal resistance, Θ_{JA} = 120°C/W. Worst case conditions are calculated at the maximum operating temperature where T_A = 85°C. Typical conditions are calculated under normal ambient conditions where T_A = 25°C. At T_A = 85°C, $P_{D(MAX)}$ = 333mW. At T_A = 25°C, $P_{D(MAX)}$ = 833mW.

Maximum current is given by the following equation:

$$I_{OUT(MAX)} = (P_{D(MAX)} / R_{DS})^{1/2}$$

For the AAT4650 at 85°C, $I_{OUT(MAX)} = 1.65A$, a value greater than the internal minimum current limit specification.

Overcurrent and Overtemperature Protection

Because many AAT4650 applications provide power to external devices, it is designed to protect its host device from malfunctions in those peripherals

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through slew rate control, current limiting, and thermal limiting. The AAT4650 current limit and thermal limit serve as an immediate and reliable electronic fuse without any increase in $R_{\rm DS}$ for this function. Other solutions such as a poly fuse do not protect the host power supply and system from mishandling, or short circuited peripherals, they will only prevent a fire. The AAT4650 high speed current limit and thermal limit not only prevent fires, they also isolate the power supply and entire system from any activity at the external port, and report a mishap by means of a $\overline{\rm FAULT}$ signal.

Overcurrent and overtemperature go hand in hand. Once an overcurrent condition exists, the current supplied to the load by the AAT4650 is limited to the overcurrent threshold. This results in a voltage drop across the AAT4650 which causes excess power dissipation and a package temperature increase. As the die begins to heat up, the overtemperature circuit is activated. If the temperature reaches the maximum level, the AAT4650 automatically switches off the P-channel MOSFETs. While they are off, the overtemperature circuit remains active. Once the temperature has cooled by approximately 10°C, the P-channel MOSFETs are switched back on. In this manner, the AAT4650 is thermally cycled on and off until the short circuit is removed. Once the short is removed, normal operation automatically resumes.

To save power, the full high speed overcurrent circuit is not activated until a lower threshold of current (approximately 700mA) is exceeded in the power device. When the load current exceeds this

crude threshold, the AAT4650 quiescent current increases from 15µA to 150µA. The high speed overcurrent circuit works by linearly limiting the current when the current limit is reached. As the voltage begins to drop on Vcc due to current limiting, the current limit magnitude varies, and generally decreases as the Vcc voltage drops to 0 volts.

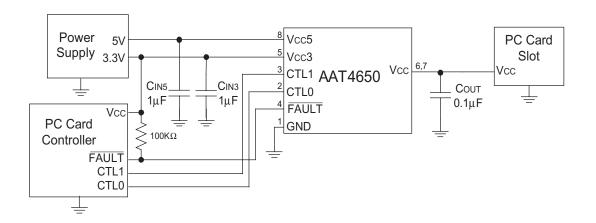
Switching Vcc Voltage

The AAT4650 meets PC card standards for switching the Vcc output by providing a ground path for Vcc as well as a hi impedance state. The PC card protocol for determining low voltage operations is to first power the peripheral with 5 volts and poll for 3.3 volt operation. When transitioning from 5 volts to 3.3 volts, Vcc must be discharged to less than 0.8 volts to provide a hard reset. The resistive ground state (CTL1=0, CTL0=0) will accommodate this. The ground state will also guarantee the Vcc voltage to be discharged within the specified 100ms amount of time.

Printed Circuit Board Layout Recommendations

For proper thermal management, to minimize PCB trace resistance, and to take advantage of the low $R_{\rm DS(ON)}$ of the AAT4650, a few circuit board layout rules should be followed: Vcc3, Vcc5, and Vcc should be routed using wider than normal traces, the two Vcc pins (6 and 7) should be connected to the same wide PCB trace, and GND should be connected to a ground plane. For best performance, $C_{\rm IN}$ and $C_{\rm OLIT}$ should be placed close to the package pins.

Typical PC Card Application Circuit





Evaluation Board Layout

The AAT4650 evaluation layout follows the printed circuit board layout recommendations, and can be used for good applications layout.

Note: Board layout shown is not to scale.

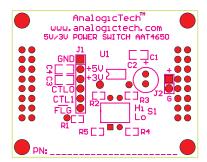


Figure 2: Evaluation board top side silk screen layout / assembly drawing

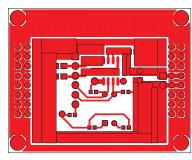


Figure 3: Evaluation board component side layout

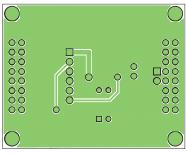


Figure 4: Evaluation board solder side layout

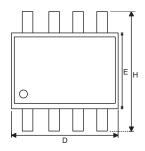


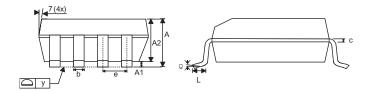
Ordering Information

Doolsogo	Marking	Part Number			
Package		Bulk	Tape and Reel		
SO-8		AAT4650IAS-B1	AAT4650IAS-T1		
TSSOP-8		AAT4650IHS-B1	AAT4650IHS-T1		

Package Information

SOP-8





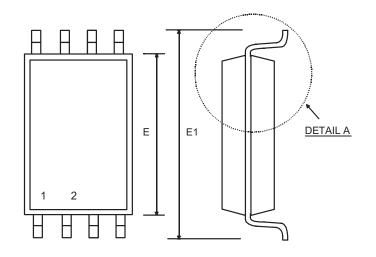
Dim	Millimeters		Inches	
	Min	Max	Min	Max
Α	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.4	5	0.0	57
В	0.33	0.51	0.013	0.020
С	0.19	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
Е	3.80	4.00	0.150	0.157
е	1.2	7	0.050	
Н	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
Υ	0.00	0.10	0.000	0.004
θ1	0°	8°	0°	8°

Note

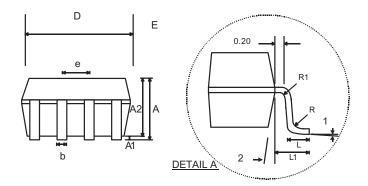
- 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.
- 2. TOLERANCE 0.1000mm (4mil) UNLESS OTHERWISE SPECIFIED
- 3. COPLANARITY: 0.1000mm
- 4. DIMENSION L IS MEASURED IN GAGE PLANE.
- 5. CONTROLLING DIMENSION IS MILLIMETER; CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.



TSSOP-8



Dim	Millimeters		Inches		
	Min	Max	Min	Max	
Α	1.05	1.20	0.041	0.047	
A1	0.05	0.15	0.002	0.006	
A2	-	1.05	-	0.041	
b	0.25	0.30	0.010	0.012	
С	0.12	27	0.00)5	
D-8	2.90	3.10	0.114	0.122	
D-28	9.60	9.80	0.378	0.386	
E	4.30	4.50	0.170	0.177	
E1	6.20	6.60	0.244	0.260	
е	0.65 E	BSC	0.025 BSC		
L	0.50	0.70	0.20	0.028	
L1	1.0)	0.039		
R	0.09	-	0.004	-	
R1	0.09	-	0.004	-	
θ1	0°	8°	0°	8°	
θ2	12°				



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