Rx module specification

MD7101_A01

General Description

The receiver module is designed for 2.4GHz ISM band wireless applications using AMIC A7101 FSK transceiver. This module features a fully programmable frequency synthesizer, which is base on 100KHz reference frequency and 300uA charge pump output current. The data rate is 57.6Kbps or 64Kbps.

Electrical specification

Item	Specification	Remark
Supply voltage	3 - 5V	
Current consumption	6uA(typical) @sleep mode (regulator off) 10mA(typical) @sleep mode (regulator on) 12mA(typical) @stand-by mode 40mA(typical) @Rx mode	
Frequency	2416 – 2478 MHz	
Rx sensitivity	-80 dBm (max)	BER≦1E-3
Modulation	FSK	
Channel spacing	2 MHz	
Channel number	32	
Interface	6 & 3 pin 1.27mm header	
Dimension	35(L) x 19(W) x 10(H) mm^3	
Operating temperature	0 – 50 ℃	

Interface

Pin Number	Pin Name	Description	Note
J1-3	VIN	Supply voltage.	
J1-4	EN_REG	Voltage regulator enable input, active high (VIN).	Option.
J1-5	SPI_LATCH	Latch for SPI interface.	
J1-6	SPI_CLOCK	Clock for SPI interface.	
J1-7	SPI_DATA	Data for SPI interface.	
J1-8	GND	Ground.	
J2-1	MUTE	Receiver mute control output, active low (open drain).	Option.
J2-2	EN_AFC	AFC circuit control input, active high.	Option.
J2-3	RXDATA	Receiver data output.	

Serial to Parallel Interface (SPI)

The SPI bus consists of three signals: SPI_DATA, SPI_CLOCK, and SPI_LATCH. This interface is used for external base-band controller to communicate with internal registers. The contents of the registers are shown in the following register description sections.

After setting SPI_LATCH signal to "Low" state, data on SPI_DATA is shifted into the internal shift register on the rising edge of SPI_CLOCK with MSB going in first. SPI_LATCH should be asserted at the end to latch the data packet into the register according to the address bits, bit 0 through bit 3, for each of the registers. All registers can only be written into except the Status Register which can only be read.

When the content of the Status Register need to be fetched by external controller, external baseband controller need to make sure that the address bits are pointing to address location 0x0 for proper read operation. After the address bits are shifted into the SPI interface and latched by asserting SPI_LATCH, the SPI interface will be in Read Mode and the content of the Status Register will be shifted out on SPI_DATA pin. When all 12 status bits have been shifted out, the SPI bus will be put back to Write Mode automatically.

A. Register Description

Note: Convention used:

1: Logic level "ONE".
0: Logic level "ZERO".
X: Don't care.

Synthesizer Configuration Register I (Write only / Address 0xf)

Bit 15	Bit 14	Bit 13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit 1	Bit 0
MB6	MB5	MB4	MB3	MB2	MB1	MB0	**MA4**	**MA3**	**MA2**	**MA1**	**MA0**	1	1	1	1

Synthesizer Configuration Register II (Write only / Address 0x7)

Bit 15	Bit 14	Bit 13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit 1	Bit 0
X	MB9	MB8	MB7	**R7**	**R6**	**R5**	**R4**	**R3**	**R2**	**R1**	**R0**	0	1	1	1

Synthesizer Configuration Register I and Synthesizer Configuration Register II control synthesizer frequency settings where

MA[4:0]: A counter[4:0] . Valid range is from 0 to 31.
MB[9:0]: B counter[9:0] . Valid range is from 0 to 1023.
R[7:0]: R counter[7:0] . Valid range is from 2 to 255, for this module must be set to 0x78 for proper operation.

The content of A, B and R registers are in unsigned binary format (i.e., $11111_2 = 31_{10}$).

The equation for setting the synthesizer frequency is:

$f_{vco} = f_{crystal} * (32*B + A) / R, \quad (B > A)$.

For example :

If f_{vco} = 2450MHz , f_{crysta} = 12MHz , $f_{reference}$ = 100KHz.
Then R = $f_{crysta} / f_{reference}$ = 120 =01111000_2 , B = 765 = 1011111101_2 , A = 20 = 10100_2.

Crystal Control Register (Write only / Address 0xb)

Bit 15	Bit 14	Bit 13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit 1	Bit 0
0	DP	TXH2	TXH1	TXH0	TXL2	TXL1	TXL0	FX3	FX2	FX1	FX0	1	0	1	1

DP: Data Polarity. This control bit sets data output polarity.
0: Data is inverted.
1: Normal.

TXH[2:0]: Must be set to 0x0 for proper operation.
TXL[2:0]: Must be set to 0x0 for proper operation.
FX[3:0]: Must be set to 0x0 for proper operation.

VCO Control Register (Write only / Address 0x3)

Bit 15	Bit 14	Bit 13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit 1	Bit 0
VTH2	VTH1	VTH0	T1	T0	HP0	CP2	CP1	CP0	VC2	VC1	VC0	0	0	1	1

VTH[2:0]: Set VCO tuning voltage range, for this module must be set to 0x6 for proper operation.

0x0 = 0.3 to VDD-0.3V , 0x1 = 0.4 to VDD-0.4V ,
0x2 = 0.5 to VDD-0.5V , 0x3 = 0.6 to VDD-0.6V ,
0x4 = 0.7 to VDD-0.7V , 0x5 = 0.8 to VDD-0.8V ,
0x6 = 0.9 to VDD-0.9V , 0x7 = 1.0 to VDD-1.0V ,

T[1:0]: Reserved. Must be set to 0x0 for proper operation.

HP0: RF output power level control.

0: Low power output (-16 dBm).
1: High power output (-6 dBm).

CP[2]: Reserved. Must be set to 0x0 for proper operation.

CP[1:0]: Charge pump output current control, for this module must be set to 0x1(300uA) for proper operation.

0x0 = 100uA , 0x1 = 300uA ,
0x2 = 500uA , 0x3 = 700uA ,

VC[2:0]: Reserved. Must be set to 0x4 for proper operation.

RX Control Register (Write only / Address 0xd)

Bit 15	Bit 14	Bit 13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit 1	Bit 0
T2	T1	T0	MT2	MT1	MT0	MTC	DM4	DM3	DM2	DMI	DM0	1	1	0	1

T[2:0]: Reserved. Must be set to 0x0 for proper operation.

MT[2:0]: Internal voltage threshold level for mute output (pin 37).

0x0 = 0.581*VDD , 0x1 = 0.516*VDD ,
0x2 = 0.452*VDD , 0x3 = 0.387*VDD ,
0x4 = 0.323*VDD , 0x5 = 0.258*VDD ,
0x6 = 0.194*VDD , 0x7 = 0.129*VDD ,

MTC: RXDATA mute function enable.
0: Disable mute function.
1: Enable mute function. When RSSI output voltage level is higher than the threshold set by MT[2:0], RXDATA becomes inactive and pull high.

DM[4:0]: Reference voltage level for demodulator tank center frequency tuning.
Valid range is from 0x1f to 0x6. The setting of DM varies with the voltage reference level such that when DM = 0x6 voltage reference = 0.9V and when DM = 0x1f voltage reference = 2.4V.

For this module must be set to 0x0 for proper operation.

Mode Select Register (Write only / Address 0x5)

Bit 15	Bit 14	Bit 13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit 1	Bit 0
X	X	X	X	X	SC1	SC0	XOE	CM	EXTB	MD1	MD0	0	1	0	1

SC[1:0]: Status Register bit 6 control. Depends on the setting of SC[1:0], bit 6 of the Status Register can represent system error flag, Battery-low detect or PLL lock detect.

[1:0] = 10: System Error.
[1:0] = 11: Battery-low detect.
[1:0] = 0X: PLL lock detect.

XOE: Crystal oscillator buffer output enable.
0: Output enable.
1: Output disable. The output will be forced to low level at this setting.

CM: Reserved. Must be set to 1 for proper operation.

EXTB: Operating mode selection.
0: external mode. Operation mode is determined by external pin MODSEL0 and MODSEL1.
1: internal mode. Operation mode is determined by setting of MD[1:0].

MD[1:0]: Internal mode selection.
[1:0] = 00: Sleep mode. Transceiver circuit is turned off.
[1:0] = 01: Stand-by mode. X'TAL oscillator is turned on.
[1:0] = 10: Transmit mode.
[1:0] = 11: Receive mode.

Status Register (Read only / Address 0x0)

SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
X	X	X	X	X	X	X	X	X	S/B/P	X	X	0	0	0	0

S/B/P: Depends on the setting of SC[1:0] in Mode Select Register, this bit can be used to reflect the status of System Error, Battery-low detect .

System Error: 0: Normal; 1: Error.
Battery-low detect: 0: Battery supply voltage below threshold. 1: Normal.
PLL lock detect: 0: Unlock. 1: Lock.

SR[3:0]: Address bits.

B. SPI Timing Diagram

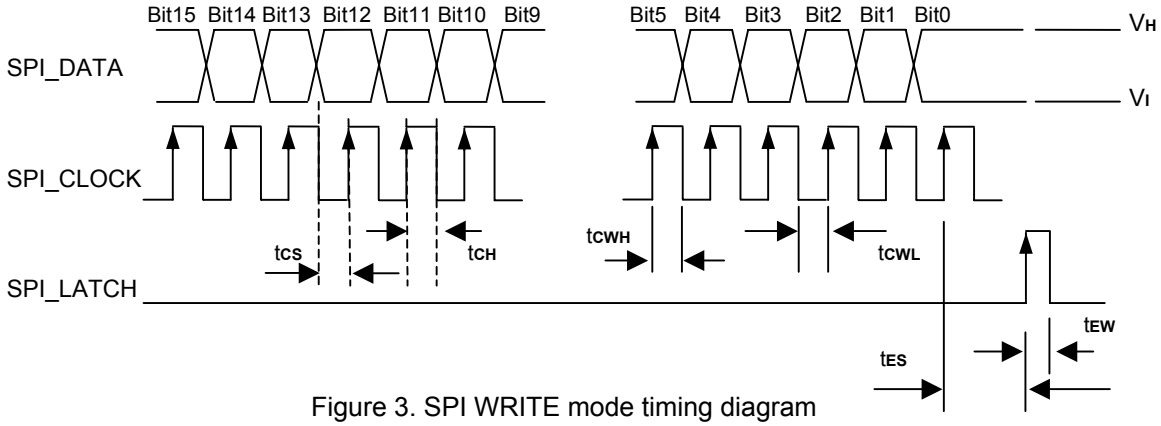

Figure 3. SPI WRITE mode timing diagram

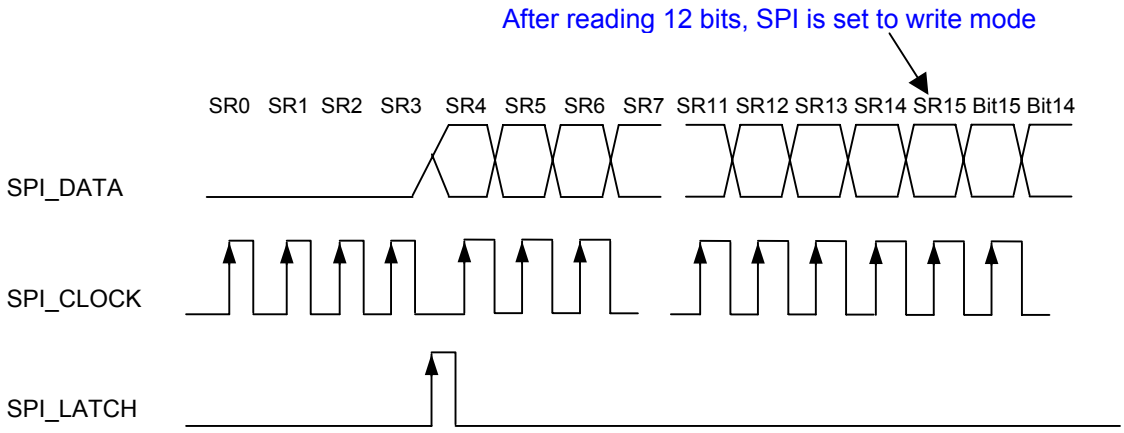

Figure 4. SPI READ mode timing diagram

C. SPI Timing Specification

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
V_H	The High level of voltage	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram	VCC-0.4			V
V_I	The low level of voltage	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram			0.4	V
t_{CE}	SPI_DATA to SPI_CLOCK setup time	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram	50			ns
t_{CH}	SPI_CLOCK to SPI_DATA hold time	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram	10			ns
t_{CWH}	SPI_CLOCK pulse width high	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram	50			ns
t_{CWL}	SPI_CLOCK pulse width low	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram	50			ns
t_{ES}	SPI_CLOCK to SPI_LATCH setup time	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram	50			ns
t_{EW}	SPI_LATCH pulse width	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram	50			ns

Table 5.

Module setup procedure:

Step 1: Supply DC voltage to VIN.

Step 2: Reset IC by setting SPI_CLOCK and SPI _LATCH to logic high simultaneously for more than **1 us**.

Step 3: Setup IC's internal control registers by configuring the followings: Synthesizer Configuration Register I, Synthesizer Configuration Register II, VCO Control Register, RX Control Register, and the Mode Select Register. All registers should be written to in the order specified above.

a. Synthesizer Configuration Register I and II: Set VCO center frequency.
b. VCO Control Register: Set VCO tuning range and charge pump output current.
c. RX Control Register: Set mute threshold level, RXDATA mute function and reference voltage for demodulator tank center frequency tuning. When **AFC** function is used, DM[4:0] must be set to **0x0** for proper operation.

Step 4: Set IC to Stand-by mode.
For internal mode operation, set Mode Select Register to **0x05D5,** then wait about 10mS.

Step 5: Set IC to RX mode.
For internal mode operation, set Mode Select Register to **0x05F5**.

Whenever frequency is to be changed, or system error has been detected (by reading from the Status Register) the IC must be reset by repeating step **2, 3-a, 4** and **5**.

PC board layout and dimension drawing

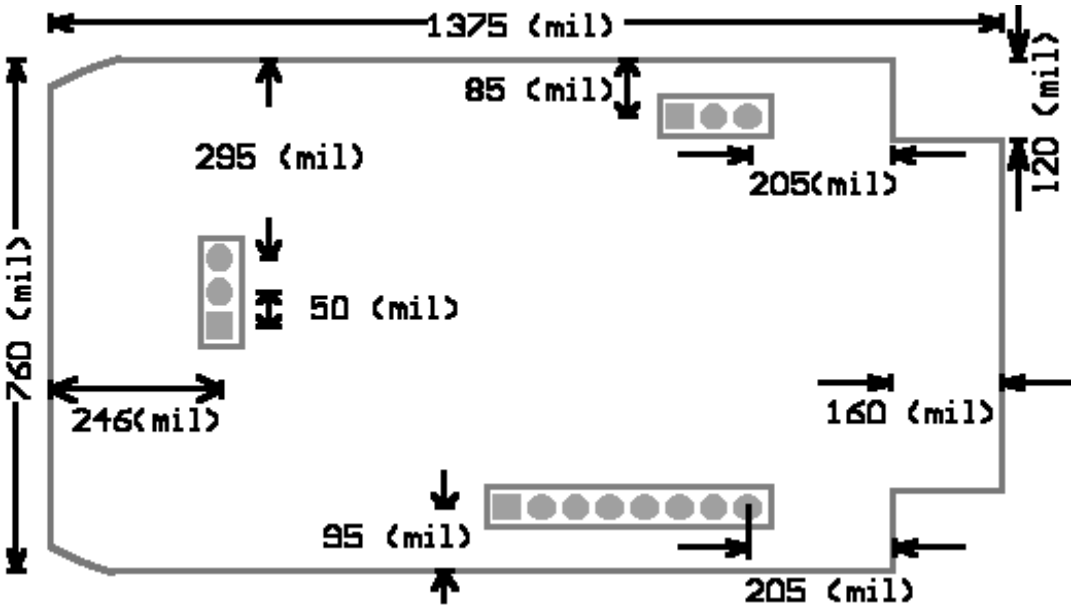

Figure 1: Dimension Drawing

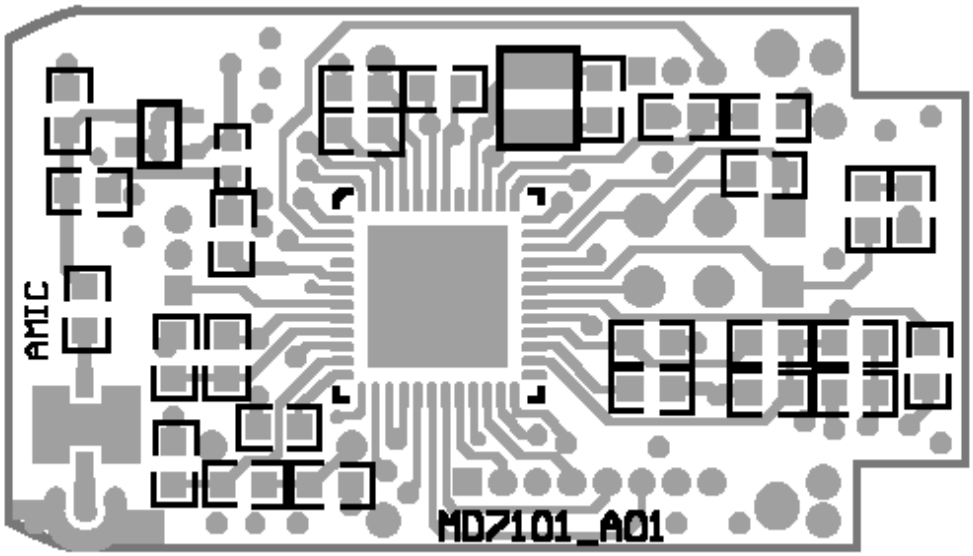

Figure 2: Top Layer Layout

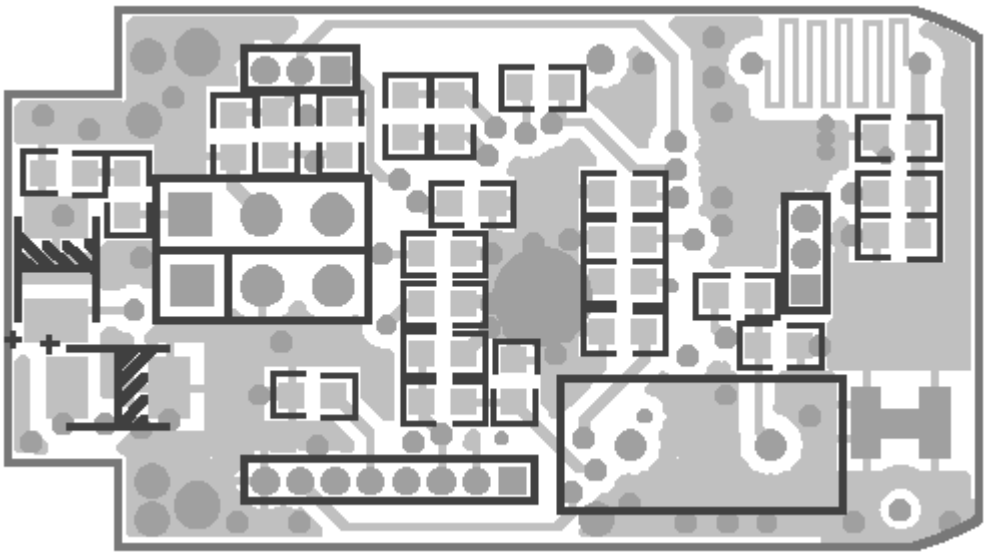

Figure 3: Bottom Layer Layout

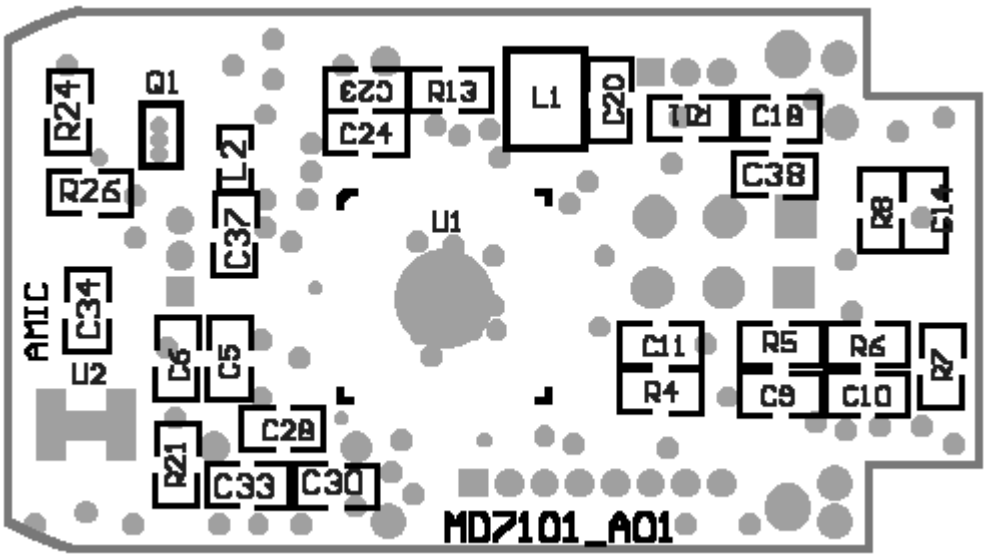

Figure 4: Top Layer Placement

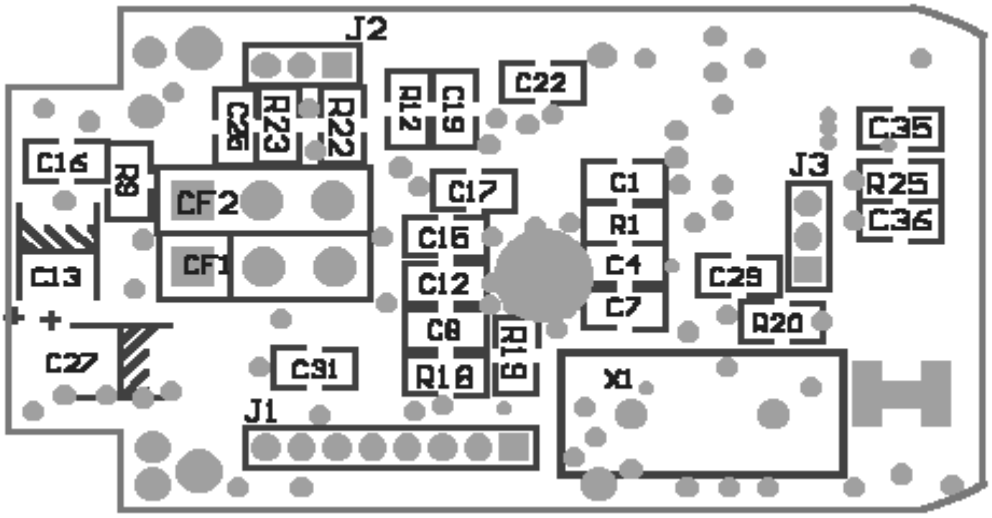

Figure 5: Bottom layer Placement