Document Title

1M X 16 Bit Low Voltage Super RAM™

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	November 30, 2001	Preliminary
0.1	Add t_{ASC}, t_{AHC}, t_{CEH}, t_{WEH}	July 31, 2002	
0.2	Change VCCmax from 3.1V to 3.3V Change t_{CW} from 60ns to 70ns for -70 and from 70ns to 85ns for -85 Change t_{WP} from 50ns to 55ns for -70 and from 55ns to 60ns for -85 Change t_{WHZ} from 20ns to 25ns for -70 and from 20ns to 25ns for -85	October 21, 2002	
0.3	Change power on $\overline{CE1}$=50ns Change avoid timing	November 7, 2002	
0.4	Change t_{OHZ} from 25ns to 14ns	March 4, 2003	

Preliminary — *1M X 16 Bit Low Voltage Super RAM™*

Features

- Operating voltage: 2.7V to 3.3V
- Access times: 70 ns (max.)
- Current:
  A64S0616 series: Operating: 35mA (max.)
  Power Down Standby: 10µA (max.)
- Fully SRAM compatible operation
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Industrial operating temperature range: -25°C to +85°C for -I
- Available in 48-ball Mini BGA (6X8) package.

General Description

The A64S0616 is a low operating current 16,777,216-bit Super RAM organized as 1,048,576 words by 16 bits and operates on low power supply voltage from 2.7V to 3.3V. It is built using AMIC's high performance CMOS DRAM process.
Using hidden refresh technique, the A64S0616 provides a 100% compatible asynchronous interface.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.
The chip enable input is provided for POWER-DOWN, device enable. Two byte enable inputs and an output enable input are included for easy interfacing.
This A64S0616 is suited for low power application such as mobile phone and PDA or other battery-operated handheld device.

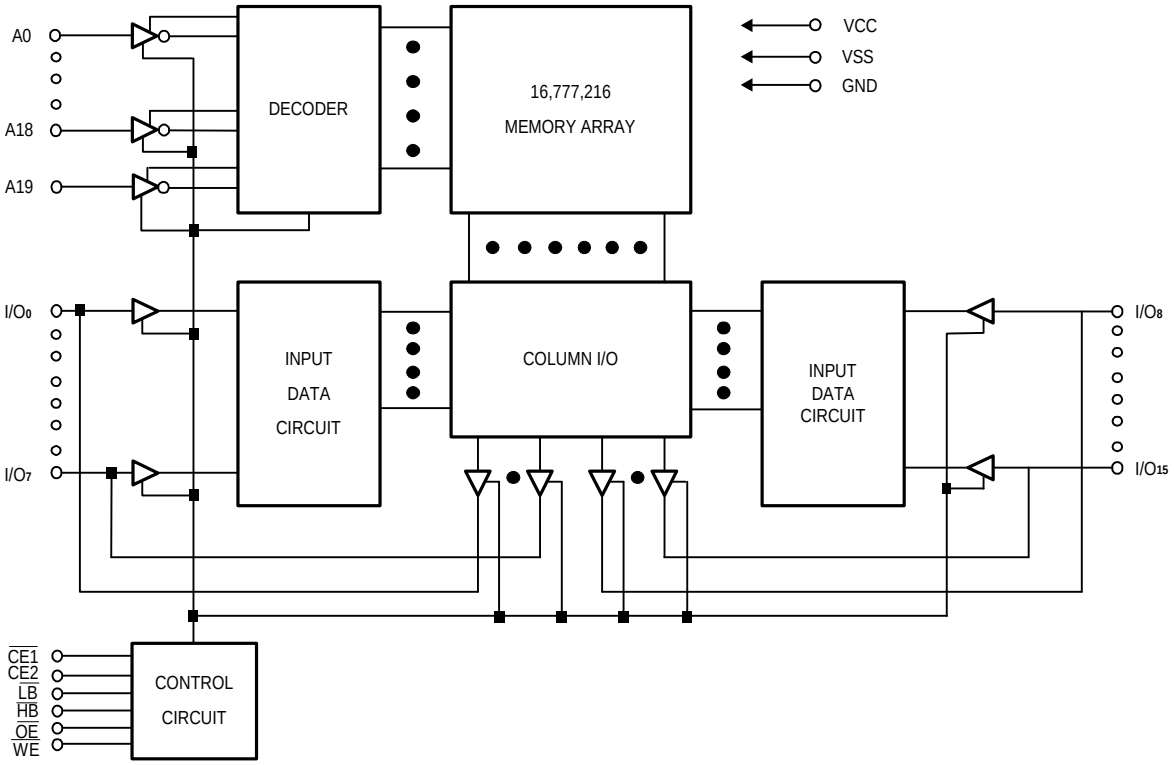
Pin Configuration

■ **Mini BGA (6X8) Top View**

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	CE2
B	I/O_8	$\overline{HB}$	A3	A4	$\overline{CE1}$	I/O_0
C	I/O_9	I/O_{10}	A5	A6	I/O_1	I/O_2
D	VSS	I/O_{11}	A17	A7	I/O_3	VCC
E	VCC	I/O_{12}	GND	A16	I/O_4	VSS
F	I/O_{14}	I/O_{13}	A14	A15	I/O_5	I/O_6
G	I/O_{15}	A19	A12	A13	$\overline{WE}$	I/O_7
H	A18	A8	A9	A10	A11	NC

A64S0616G

Block Diagram



Pin Description

Symbol	Description
A0 - A19	Address Inputs
$\overline{CE1}$	Chip Enable 1 Input
CE2	Chip Enable 2 Input
I/O_0 - I/O_{15}	Data Input/Outputs
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Byte Enable Input (I/O_0 to I/O_7)
$\overline{HB}$	Byte Enable Input (I/O_8 to I/O_{15})
$\overline{OE}$	Output Enable Input
VCC	Power
VSS	Ground
GND	Ground
NC	No Connection

Recommended DC Operating Conditions

(T_A = 0°C to + 70°C or -25°C to 85°C)

Symbol	Parameter	Min.	Max.	Unit
VCC	Supply Voltage	2.7	3.3	V
VSS	Ground	0	0	V
GND	Ground	0	0	V
V_{IH}	Input High Voltage	2.4	VCC + 0.3	V
V_{IL}	Input Low Voltage	-0.3	+0.6	V
C_L	Output Load	-	30	pF
TTL	Output Load	-	1	-

Absolute Maximum Ratings*

VCC to GND . . . . . -0.5V to +4.6V
IN, IN/OUT Volt to GND . . . . . -0.5V to VCC + 0.5V
Storage Temperature, Tstg . . . . . -55°C to +125°C
Power Dissipation, P_T 0.7W
Soldering Temp. & Time . . . . . 260°C, 10 sec

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(T_A = 0°C to + 70°C or -25°C to 85°C, VCC = 2.7V to 3.3V, GND = 0V)

Symbol	Parameter	-70		-85		Unit	Conditions
		Min.	Max.	Min.	Max.		
$\lvert I_{LI} \rvert$	Input Leakage Current	-	1	-	1	µA	V_{IN} = GND to VCC
$\lvert I_{LO} \rvert$	Output Leakage Current	-	1	-	1	µA	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to VCC
I_{CC1}	Dynamic Operating Current	-	35	-	30	mA	Min. Cycle, Duty = 100% $\overline{CE1}$ = V_{IL}, CE2 = V_{IH} $I_{I/O}$ = 0mA
I_{CC2}		-	5	-	5	mA	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} V_{IH} = VCC, V_{IL} = 0V, f = 1MHz, $I_{I/O}$ = 0mA

DC Electrical Characteristics (continued)

Symbol	Parameter	-70		-85		Unit	Conditions
		Min.	Max.	Min.	Max.		
I_{SB1}	Standby Power Supply Current	-	100	-	100	µA	$\overline{CE1} \geq VCC - 0.2V$ $CE2 \geq VCC - 0.2V$ $V_{IN} \geq 0V$
I_{SB2}	Power Down Mode Standby Current	-	10	-	10	µA	$CE2 \leq 0.2V$
V_{OL}	Output Low Voltage	-	0.4	-	0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4	-	2.4	-	V	I_{OH} = -1.0mA

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{HB}$	I/O_0 to I/O_7 Mode	I/O_8 to I/O_{15} Mode	VCC Current
H	H	X	X	X	X	Not selected	Not selected	I_{SB1}
X	H	X	X	H	H	Not selected	Not selected	I_{SB1}
X	L	X	X	X	X	Not selected	Not selected	I_{SB2}
L	H	L	H	L	L	Read	Read	I_{CC1}, I_{CC2}
				L	H	Read	High - Z	I_{CC1}, I_{CC2}
				H	L	High - Z	Read	I_{CC1}, I_{CC2}
L	H	X	L	L	L	Write	Write	I_{CC1}, I_{CC2}
				L	H	Write	Not Write/Hi - Z	I_{CC1}, I_{CC2}
				H	L	Not Write/Hi - Z	Write	I_{CC1}, I_{CC2}
L	H	H	H	X	X	High - Z	High - Z	I_{CC1}, I_{CC2}
						High - Z	High - Z	I_{CC1}, I_{CC2}

Note: X = H or L

Capacitance (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance	-	10	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance	-	10	pF	$V_{I/O}$ = 0V

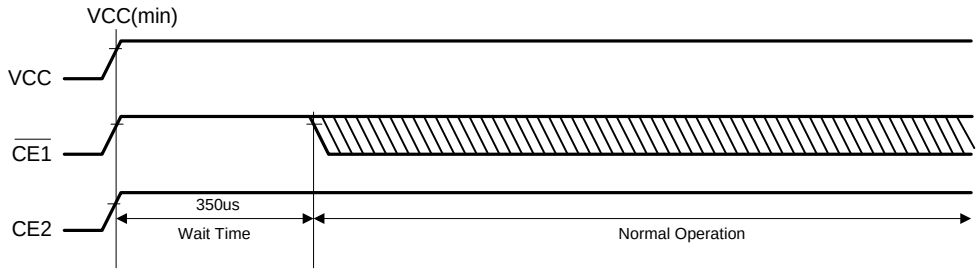
* These parameters are sampled and not 100% tested.

Initialization

The A64S0616 is initialized in the power-on sequence according to the following.

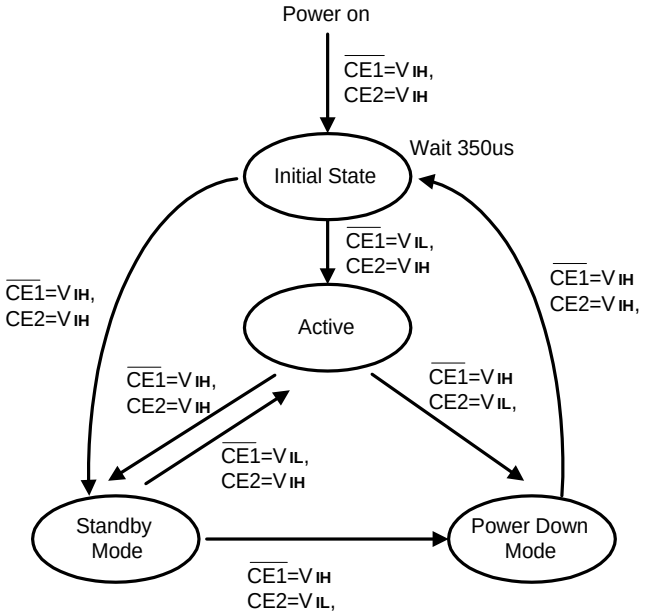
1. To stabilize internal circuits, after turning on the power, a 350µs or longer wait time must precede any signal toggling.
2. After the wait time, it can be normal operation.

Power on Chart



Notes: 1. Following power application, make CE2 and $\overline{CE1}$ high level during the wait time interval.
2. After power on sequence, the normal operating CE2 must keep at high.

Power on / Depower down State Machine



Standby Mode Characteristics

Standby Mode	Memory Cell Data Hold	Standby Supply Current (µA)
Standby	Valid	100 (I_{SB1})
Power down	Invalid	10 (I_{SB2})

Avoid Timing

Following figure 1 is show you an abnormal timing which is not supported on Super RAM.

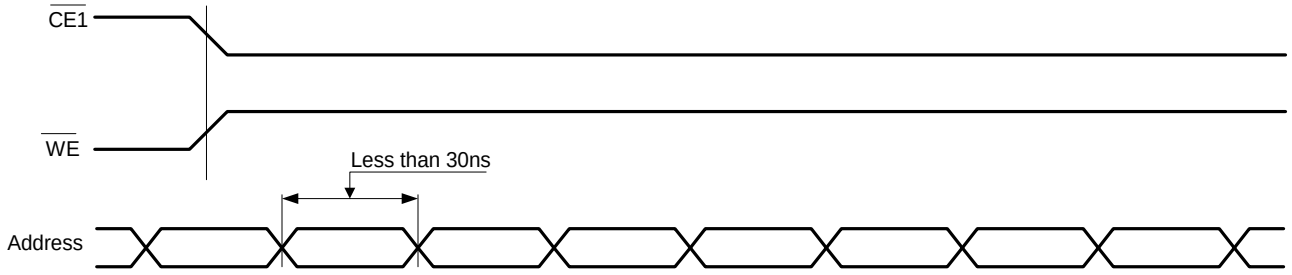


Figure 1

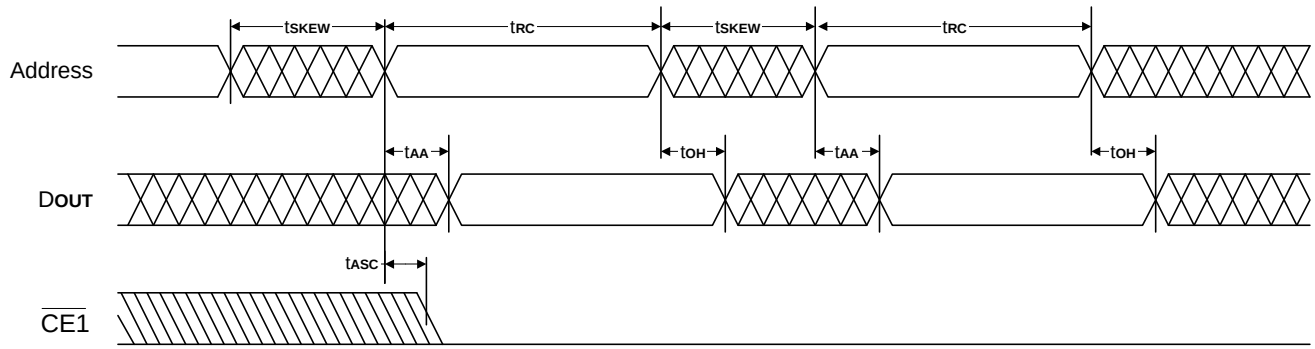
AC Characteristics (T_A = 0°C to +70°C or -25°C to 85°C, VCC = 2.7V to 3.3V)

Symbol	Parameter	-70		-85		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	70	-	85	-	ns
t_{SKEW}	Address Skew	-	10	-	10	ns
t_{AA}	Address Access Time	-	70	-	85	ns
t_{ACE}	Chip Enable Access Time	-	70	-	85	ns
t_{BE}	Byte Enable Access Time	-	70	-	85	ns
t_{OE}	Output Enable to Output Valid	-	35	-	45	ns
t_{CLZ}	Chip Enable to Output in Low Z	10	-	10	-	ns
t_{BLZ}	Byte Enable to Output in Low Z	5	-	5	-	ns
t_{OLZ}	Output Enable to Output in Low Z	5	-	5	-	ns
t_{CHZ}	Chip Disable to Output in High Z	0	25	0	35	ns
t_{BHZ}	Byte Disable to Output in High Z	0	25	0	35	ns
t_{OHZ}	Output Disable to Output in High Z	0	14	0	14	ns
t_{OH}	Output Hold from Address Change	10	-	10	-	ns
t_{ASC}	Address Setup to $\overline{CE1}$ Low	0	-	0	-	ns
t_{AHC}	Address Hold Time from $\overline{CE1}$ High	0	-	0	-	ns
t_{CEH}	$\overline{CE1}$ High Pulse With	10	-	10	-	ns
Write Cycle						
t_{WC}	Write Cycle Time	70	-	85	-	ns
t_{SKEW}	Address Skew	-	10	-	10	ns
t_{CW}	Chip Enable to End of Write	70	-	85	-	ns
t_{BW}	Byte Enable to End of Write	60	-	70	-	ns
t_{AS}	Address Setup Time	0	-	0	-	ns
t_{AW}	Address Valid to End of Write	60	-	70	-	ns
t_{WP}	Write Pulse Width	55	-	60	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	ns
t_{WHZ}	Write to Output in High Z	-	25	-	25	ns
t_{DW}	Data to Write Time Overlap	30	-	35	-	ns
t_{DH}	Data Hold from Write Time	0	-	0	-	ns
t_{OW}	Output Active from End of Write	5	-	5	-	ns
t_{ASC}	Address Setup to $\overline{CE1}$ Low	0	-	0	-	ns
t_{AHC}	Address Hold Time from $\overline{CE1}$ High	0	-	0	-	ns
t_{CEH}	$\overline{CE1}$ High Pulse With	10	-	10	-	ns
t_{WEH}	$\overline{WE}$ High Pulse With	10	-	10	-	ns

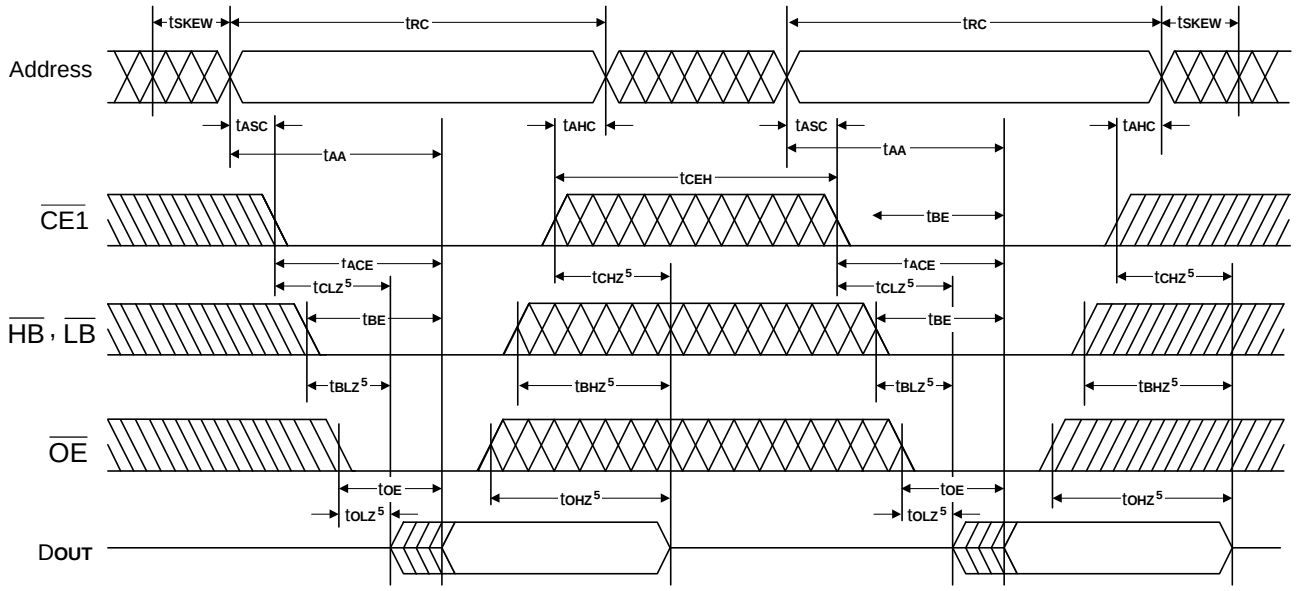
Note: t_{CHZ}, t_{BHZ} and t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms

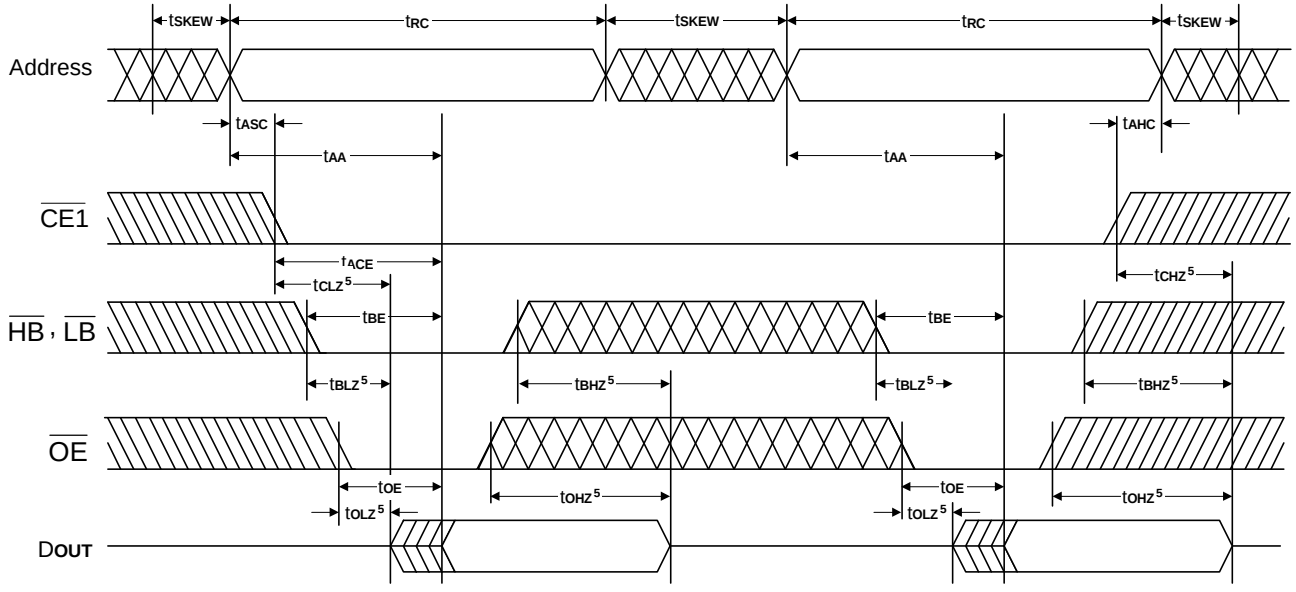
Read Cycle 1[1, 2, 4, 6]



Read Cycle 2-1[1, 3, 6]



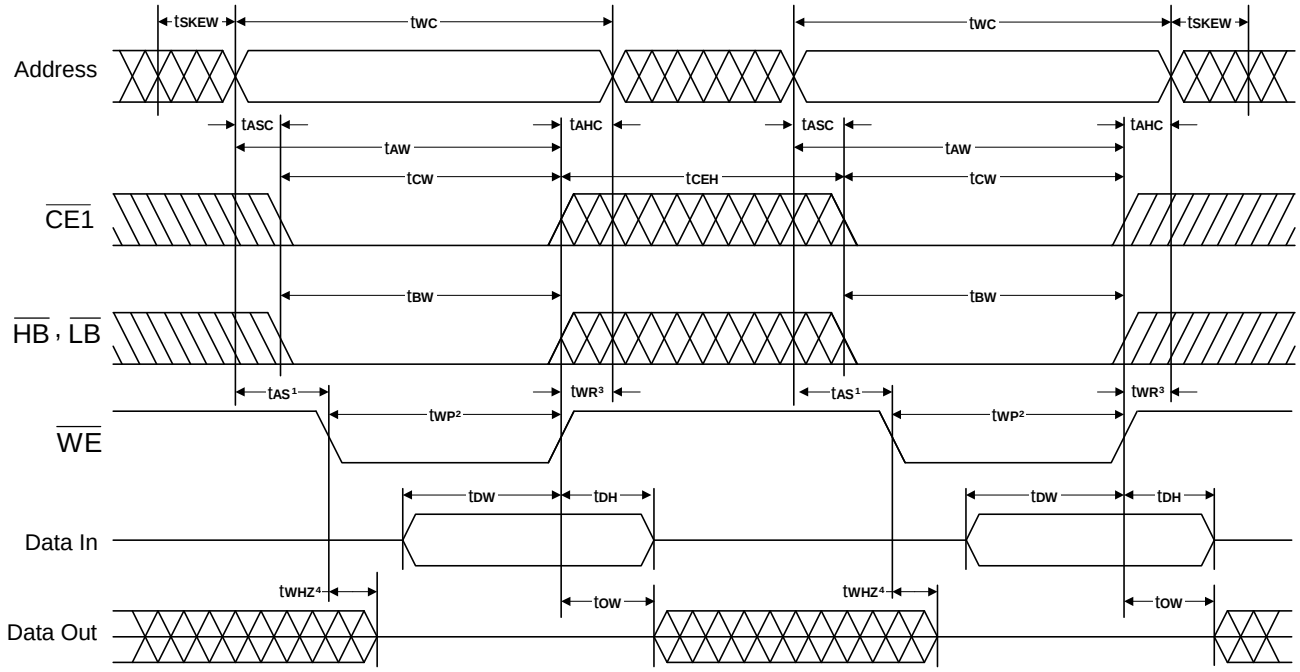
Read Cycle 2-2[1, 3, 6]



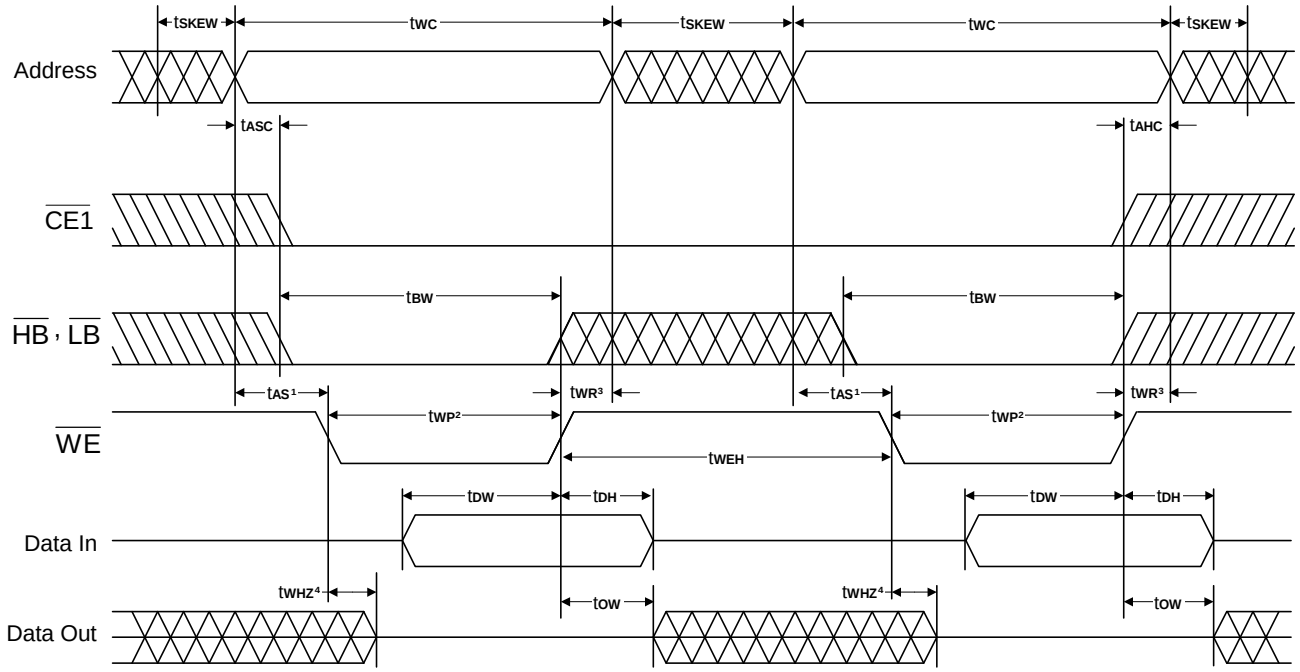
Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled $\overline{CE1}$ = V_{IL}, $\overline{HB}$ = V_{IL} and, or $\overline{LB}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CE1}$ and ($\overline{HB}$ and, or $\overline{LB}$) transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
6. CE2 is high for Read Cycle.

Timing Waveforms (continued)

Write Cycle 1-1[6]
(Write Enable Controlled)

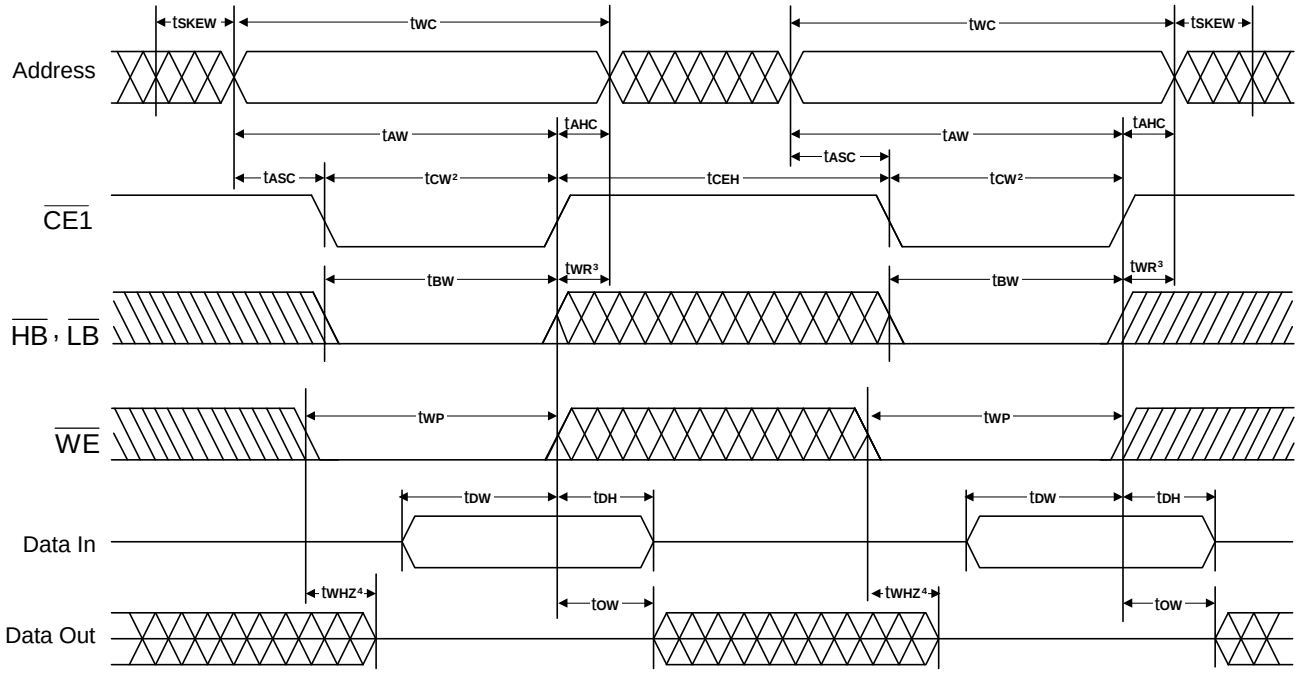


Write Cycle 1-2[6]
(Write Enable Controlled)

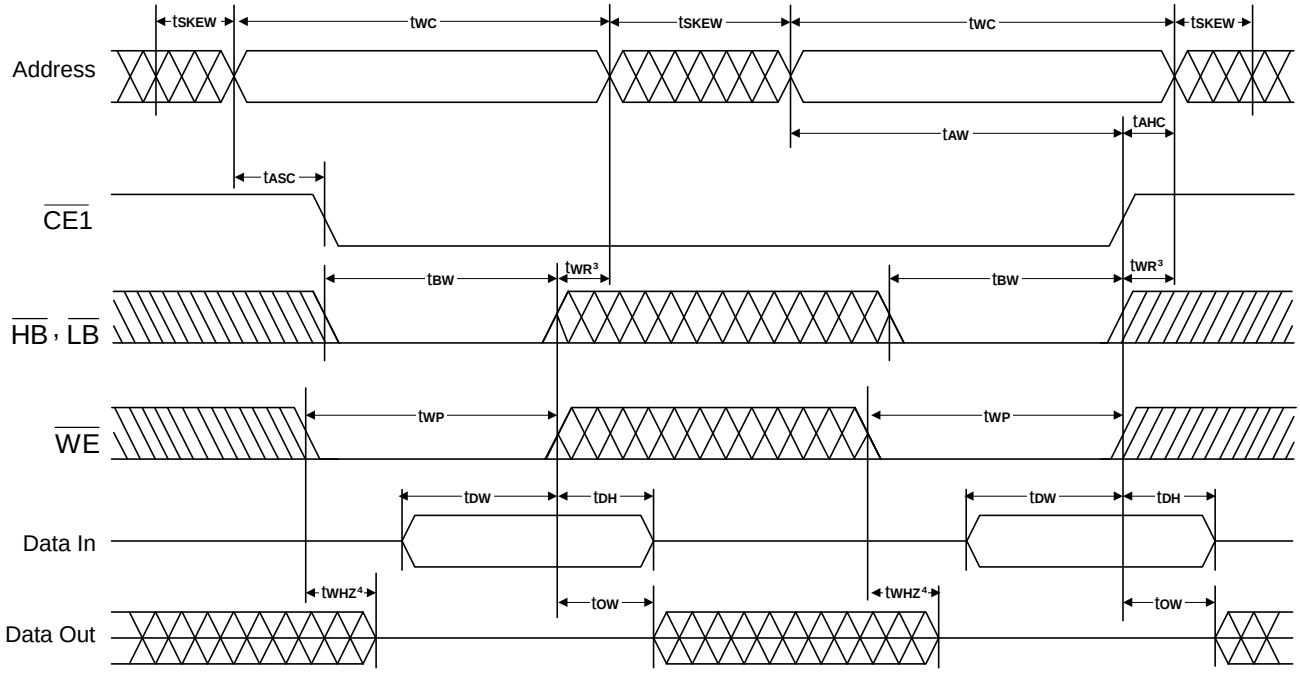


Timing Waveforms (continued)

Write Cycle 2-1[6]
(Chip Enable Controlled)

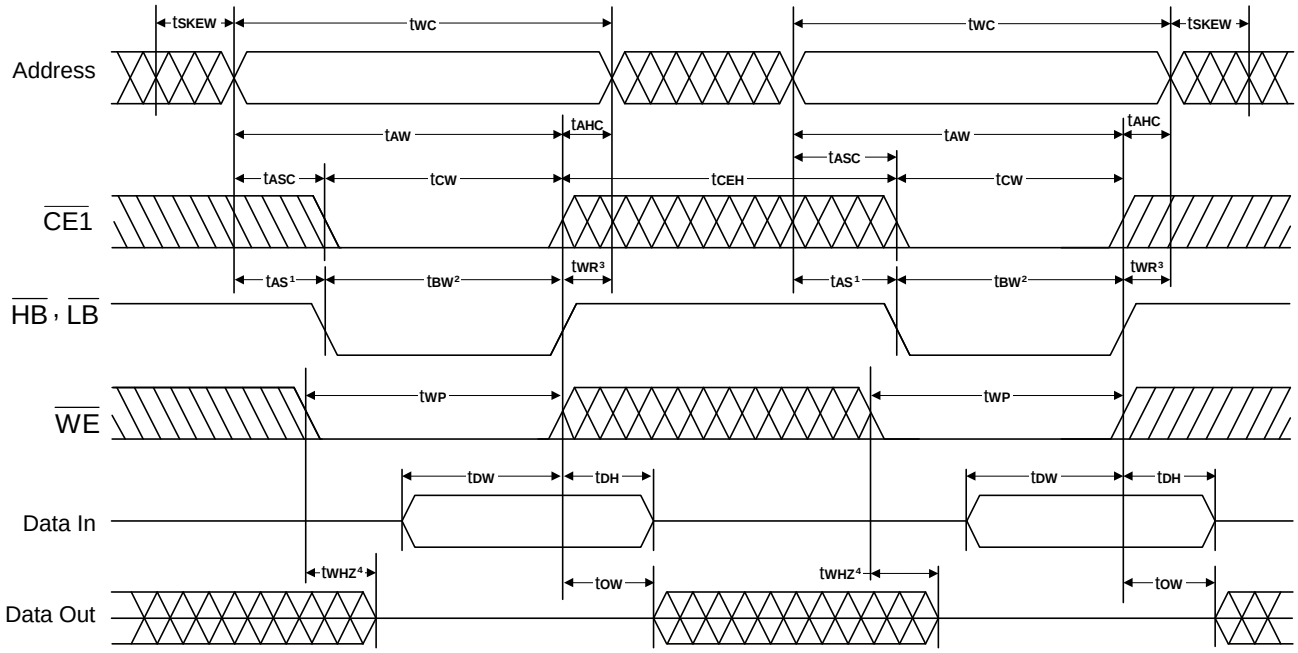


Write Cycle 2-2[6]
(Chip Enable Controlled)

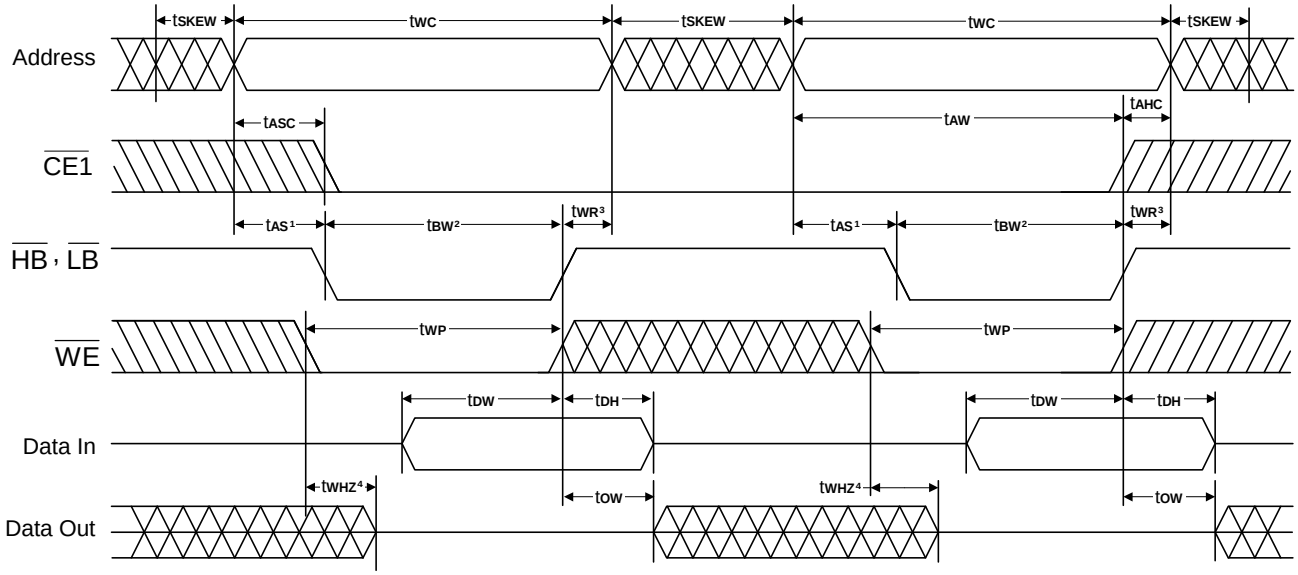


Timing Waveforms (continued)

Write Cycle 3-1[6]
(Byte Enable Controlled)



Write Cycle 3-2[6]
(Byte Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap (t_{WP}, t_{BW}) of a low $\overline{CE1}$, $\overline{WE}$ and ($\overline{HB}$ and, or $\overline{LB}$).
3. t_{WR} is measured from the earliest of $\overline{CE1}$ or $\overline{WE}$ or ($\overline{HB}$ and, or $\overline{LB}$) going high to the end of the Write cycle.
4. $\overline{OE}$ level is high or low.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
6. CE2 is high for Write Cycle.

AC Test Conditions

Input Pulse Levels	0.4V to 2.4V
Input Rise And Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 3 and 4

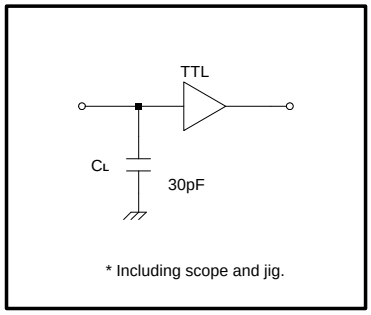


Figure 3. Output Load

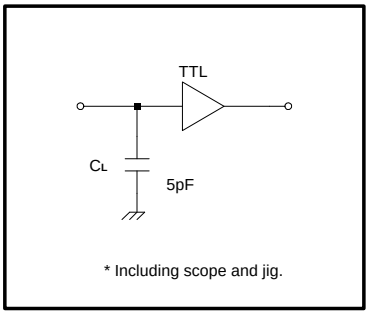


Figure 4. Output Load for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW}

Ordering Information

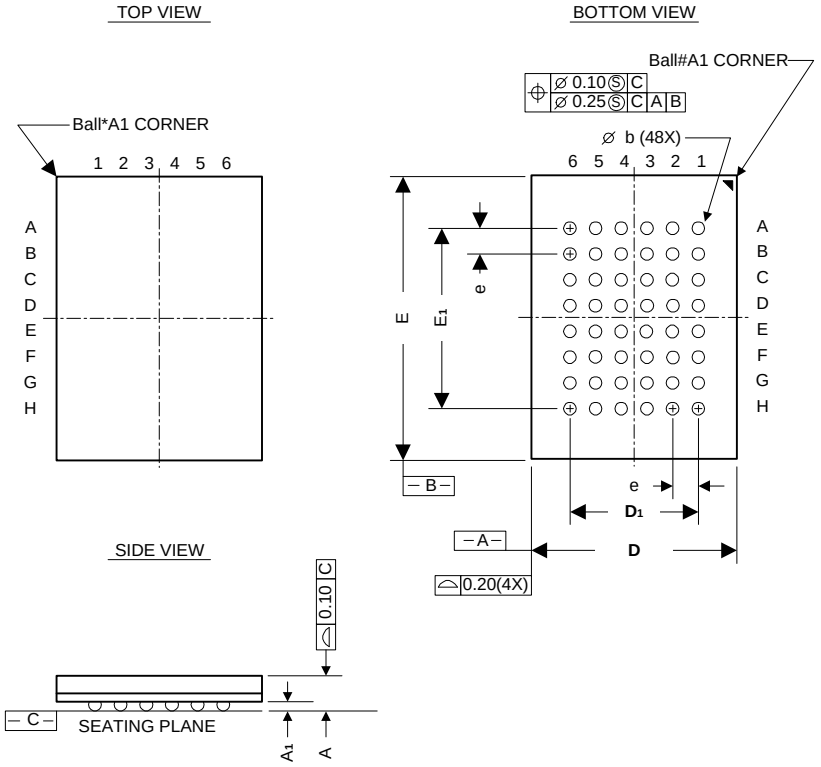
Part No.	Access Time (ns)	Operating Current Max. (mA)	Power Down Mode Standby Current Max. (mA)	Package
A64S0616G-70	70	35	10	48B Mini BGA
A64S0616G-85	85	30	10	48B Mini BGA
A64S0616G-70I	70	35	10	48B Mini BGA
A64S0616G-85I	85	30	10	48B Mini BGA

Note: -I is for industrial operating temperature range

Package Information

48LD CSP (6 x 8 mm) Outline Dimensions
(48TFBGA)

unit: mm



Symbol	Dimensions in mm		
	MIN.	NOM.	MAX.
A	---	---	1.20
A_1	0.20	0.25	0.30
D	5.90	6.00	6.10
E	7.90	8.00	8.10
D_1	---	3.75	---
E_1	---	5.25	---
e	---	0.75	---
b	0.30	0.35	0.40

Note:

1. THE BALL DIAMETER, BALL PITCH, STAND-OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC MO192 (LOW PROFILE BGA FAMILY).
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM.

   THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
4. BALL PAD OPENING OF SUBSTRATE IS Φ 0.3mm (SMD)
   SUGGEST TO DESIGN THE PCB LAND SIZE AS Φ 0.3mm (NSMD)