Document Title

64K X 16 BIT LOW VOLTAGE CMOS SRAM

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	March 30, 2000	Preliminary

Preliminary — *64K X 16 BIT LOW VOLTAGE CMOS SRAM*

Features

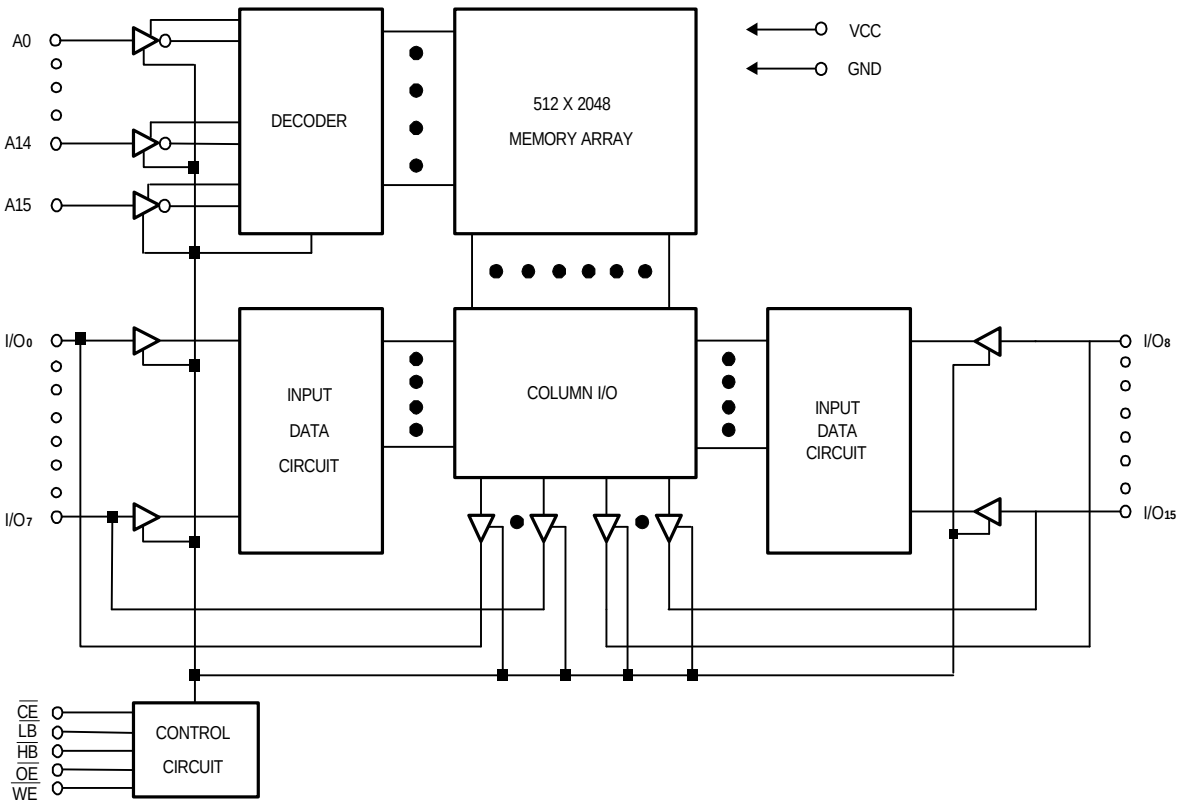
- Operating voltage: 2.7V to 3.3V
- Access times: 70ns (max.)
- Current:
  A62S6316H: Operating: 50mA (max.)
  Standby: 15µA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Data retention voltage: 2V (min.)

General Description

The A62S6316H is a low operating current 1,048,576-bit static random access memory organized as 65,536 words by 16 bits and operates on low power supply voltage from 2.7V to 3.3V. It is built using AMIC's high performance CMOS process.
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

The chip enable input is provided for POWER-DOWN, device enable. Two byte enable inputs and an output enable input are included for easy interfacing.
Data retention is guaranteed at a power supply voltage as low as 2V.

Block Diagram



Pin Configurations

Symbol	Description
A0 - A15	Address Inputs
$\overline{CE}$	Chip Enable Input
I/O_0 - I/O_{15}	Data Input/Outputs
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Byte Enable Input (I/O_0 to I/O_7)
$\overline{HB}$	Byte Enable Input (I/O_8 to I/O_{15})
$\overline{OE}$	Output Enable Input
VCC	Power
GND	Ground
NC	No Connection

Recommended DC Operating Conditions

(T_A = 0°C to + 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	2.7	3.0	3.3	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	VCC + 0.3	V
V_{IL}	Input Low Voltage	-0.3	-	+0.6	V
C_L	Output Load	-	-	30	pF
TTL	Output Load	-	-	1	-

Absolute Maximum Ratings*

VCC to GND . . . . . -0.5V to +4.6V
IN, IN/OUT Volt to GND . . . . . -0.5V to VCC + 0.5V
Operating Temperature, Topr . . . . . 0°C to +70°C
Storage Temperature, Tstg . . . . . -55°C to +125°C
Power Dissipation, P_T 0.7W
Soldering Temp. & Time . . . . . 260°C, 10 sec

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to + 70°C, VCC = 2.7V to 3.3V, GND = 0V)

Symbol	Parameter	A62S6316H		Unit	Conditions
		Min.	Max.		
$\|I_{LI}\|$	Input Leakage Current	-	1	µA	V_{IN} = GND to VCC
$\|I_{LO}\|$	Output Leakage Current	-	1	µA	$\overline{CE}$ = V_{IH} or $\overline{LB}$ = V_{IH} or $\overline{HB}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IH} $V_{I/O}$ = GND to VCC
I_{CC}	Active Power Supply Current	-	5	mA	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA
I_{CC1}	Dynamic Operating Current	-	50	mA	Min. Cycle, Duty = 100% $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA
I_{CC2}		-	20	mA	$\overline{CE}$ = V_{IL}, V_{IH} = VCC, V_{IL} = 0V, f = 1MHz, $I_{I/O}$ = 0 mA
I_{SB}	Standby Power Supply Current	-	0.5	mA	$\overline{CE}$ = V_{IH}
I_{SB1}		-	15	µA	$\overline{CE}$ ≥ VCC - 0.2V V_{IN} ≥ 0V
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.2	-	V	I_{OH} = -1.0mA

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{HB}$	I/O_0 to I/O_7 Mode	I/O_8 to I/O_{15} Mode	VCC Current
H	X	X	X	X	Not selected	Not selected	I_{SB1}, I_{SB}
L	L	H	L	L	Read	Read	I_{CC1}, I_{CC2}, I_{CC}
			L	H	Read	High - Z	I_{CC1}, I_{CC2}, I_{CC}
			H	L	High - Z	Read	I_{CC1}, I_{CC2}, I_{CC}
L	X	L	L	L	Write	Write	I_{CC1}, I_{CC2}, I_{CC}
			L	H	Write	Not Write/Hi - Z	I_{CC1}, I_{CC2}, I_{CC}
			H	L	Not Write/Hi - Z	Write	I_{CC1}, I_{CC2}, I_{CC}
L	H	H	L	X	High - Z	High - Z	I_{CC1}, I_{CC2}, I_{CC}
			X	L	High - Z	High - Z	I_{CC1}, I_{CC2}, I_{CC}
X	X	X	H	H	Not selected	Not selected	I_{SB1}, I_{SB}

Note: X = H or L

Capacitance (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance	-	6	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance	-	8	pF	$V_{I/O}$ = 0V

* These parameters are sampled and not 100% tested.

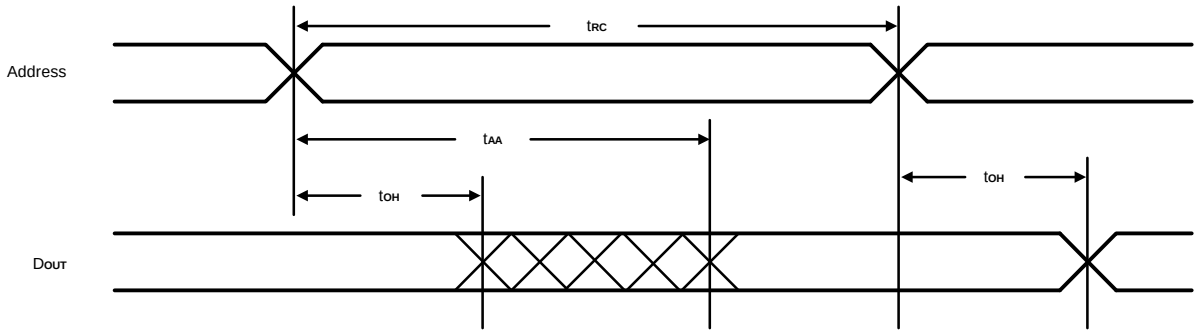
AC Characteristics (T_A = 0°C to +70°C, VCC = 2.7V to 3.3V)

Symbol	Parameter	A62S6316H		Unit
		Min.	Max.	
Read Cycle				
t_{RC}	Read Cycle Time	70	-	ns
t_{AA}	Address Access Time	-	70	ns
t_{ACE}	Chip Enable Access Time	-	70	ns
t_{BE}	Byte Enable Access Time	-	70	ns
t_{OE}	Output Enable to Output Valid	-	35	ns
t_{CLZ}	Chip Enable to Output in Low Z	10	-	ns
t_{BLZ}	Byte Enable to Output in Low Z	5	-	ns
t_{OLZ}	Output Enable to Output in Low Z	5	-	ns
t_{CHZ}	Chip Disable to Output in High Z	-	25	ns
t_{BHZ}	Byte Disable to Output in High Z	-	25	ns
t_{OHZ}	Output Disable to Output in High Z	-	25	ns
t_{OH}	Output Hold from Address Change	10	-	ns
Write Cycle				
t_{WC}	Write Cycle Time	70	-	ns
t_{CW}	Chip Enable to End of Write	60	-	ns
t_{BW}	Byte Enable to End of Write	60	-	ns
t_{AS}	Address Setup Time	0	-	ns
t_{AW}	Address Valid to End of Write	60	-	ns
t_{WP}	Write Pulse Width	50	-	ns
t_{WR}	Write Recovery Time	0	-	ns
t_{WHZ}	Write to Output in High Z	-	30	ns
t_{DW}	Data to Write Time Overlap	30	-	ns
t_{DH}	Data Hold from Write Time	0	-	ns
t_{OW}	Output Active from End of Write	5	-	ns

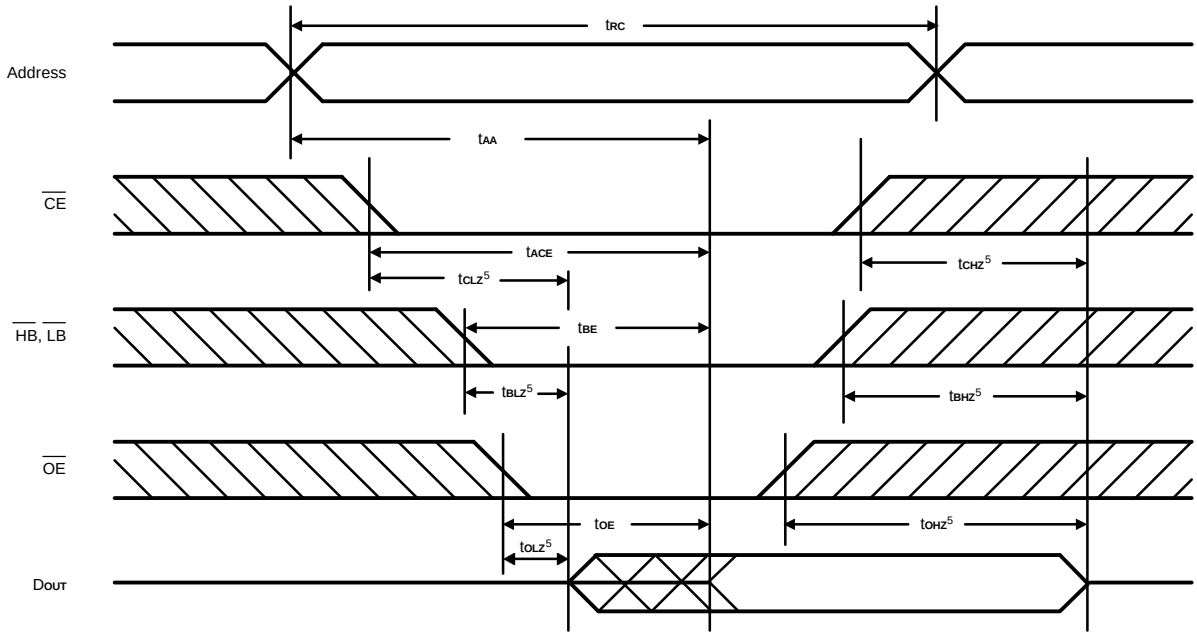
Note: t_{CHZ}, t_{BHZ} and t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms

Read Cycle 1 (1, 2, 4)



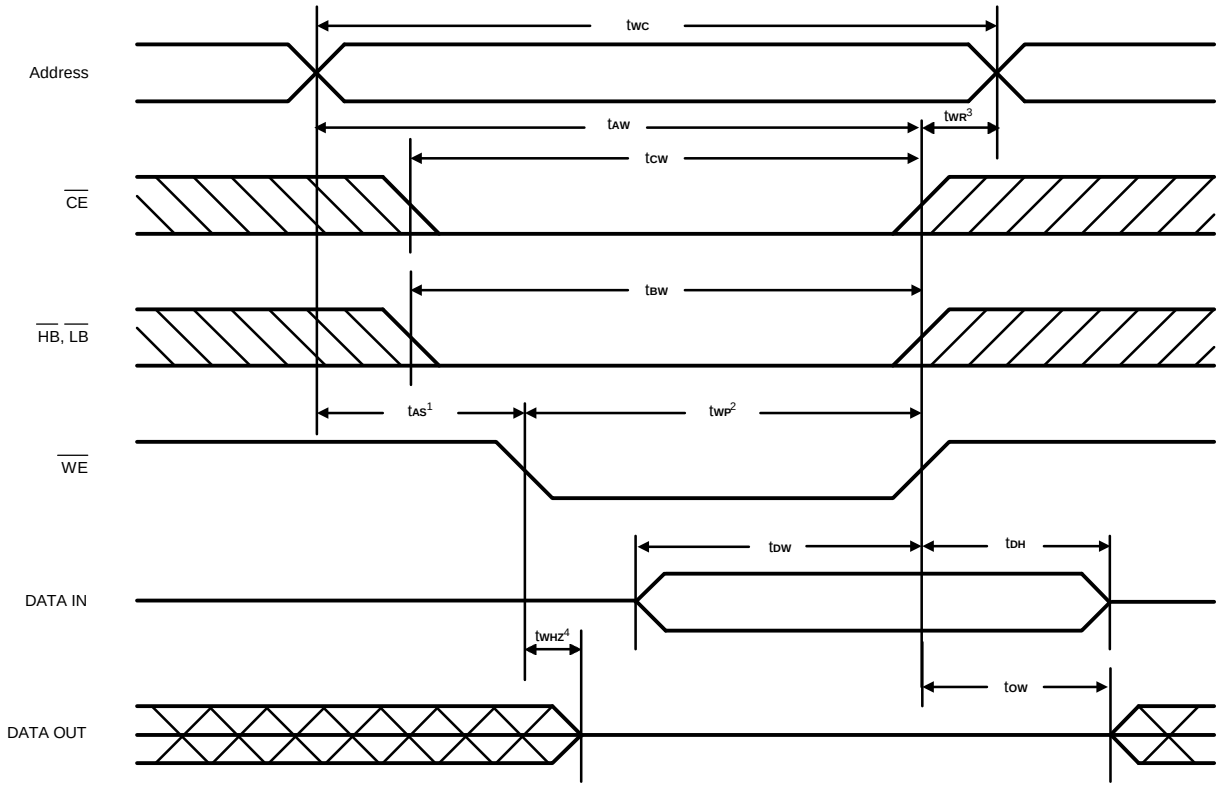
Read Cycle 2 (1, 2, 3)



Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled $\overline{CE}$ = V_{IL}, $\overline{HB}$ = V_{IH} and, or $\overline{LB}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CE}$ and ($\overline{HB}$ and, or $\overline{LB}$) transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

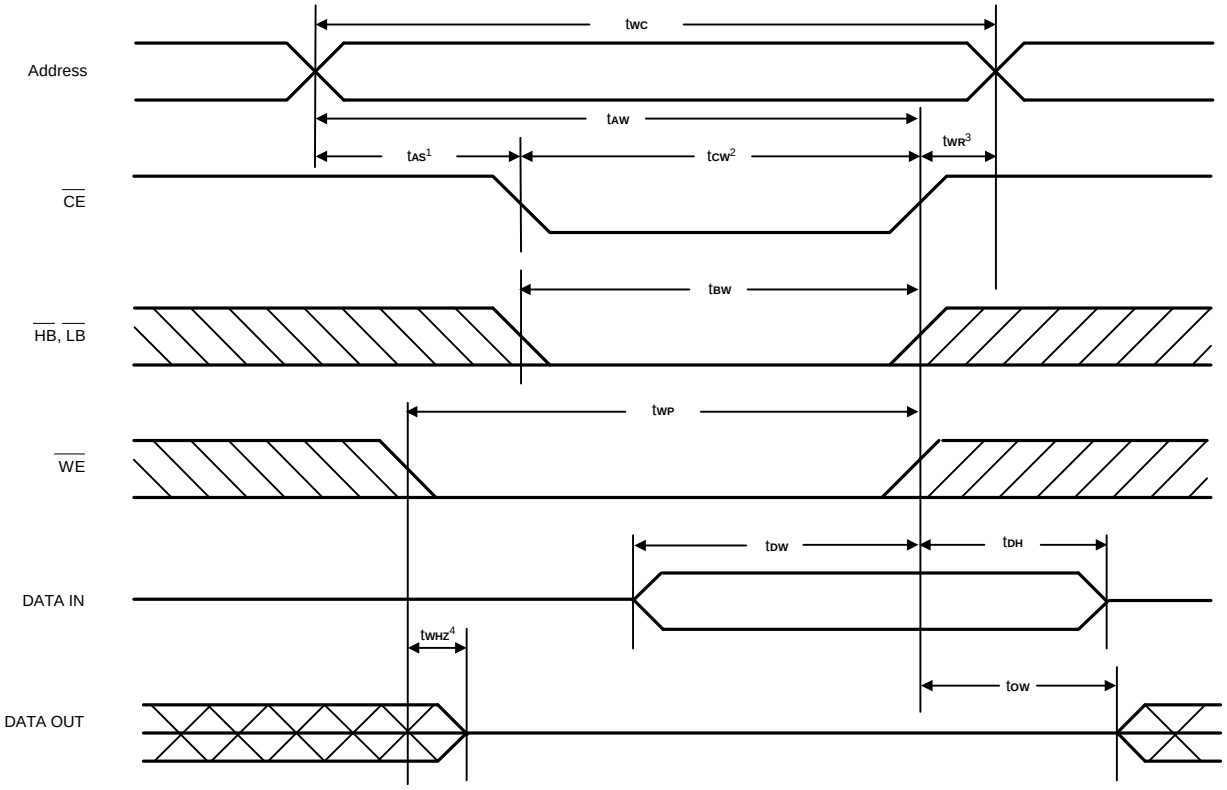
Timing Waveforms (continued)

Write Cycle 1
(Write Enable Controlled)



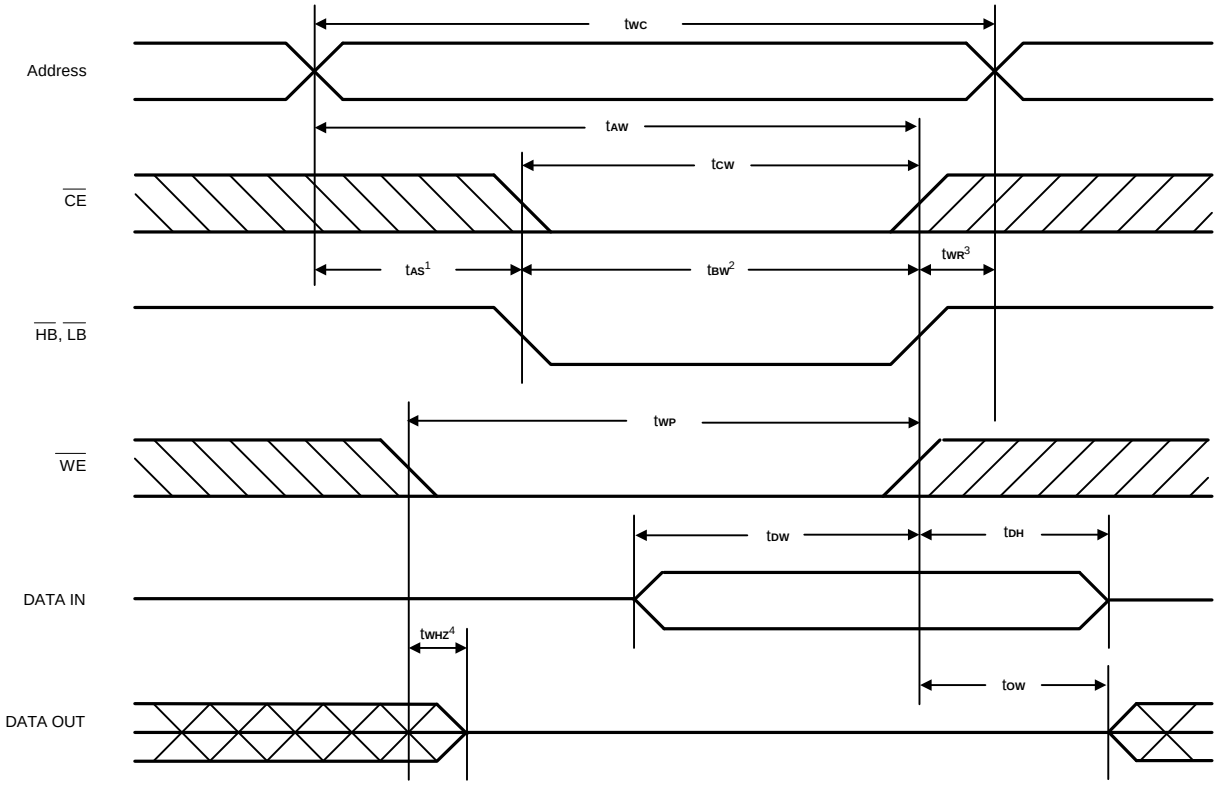
Timing Waveforms (continued)

Write Cycle 2
(Chip Enable Controlled)



Timing Waveforms (continued)

Write Cycle 3
(Byte Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap (t_{WP}, t_{BW}) of a low $\overline{CE}$, $\overline{WE}$ and ($\overline{HB}$ and, or $\overline{LB}$).
3. t_{WR} is measured from the earliest of $\overline{CE}$ or $\overline{WE}$ or ($\overline{HB}$ and, or $\overline{LB}$) going high to the end of the Write cycle.
4. $\overline{OE}$ level is high or low.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0V to 2.4V
Input Rise And Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2

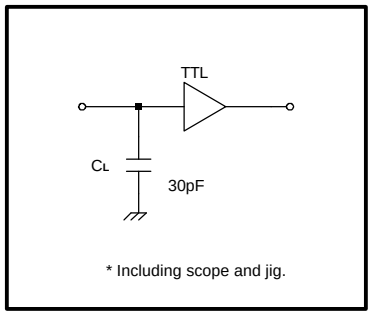


Figure 1. Output Load

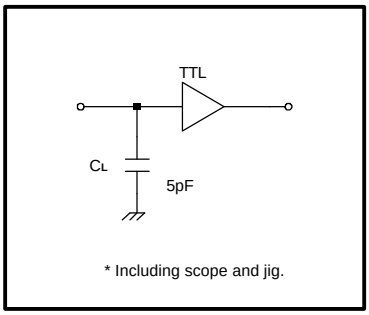
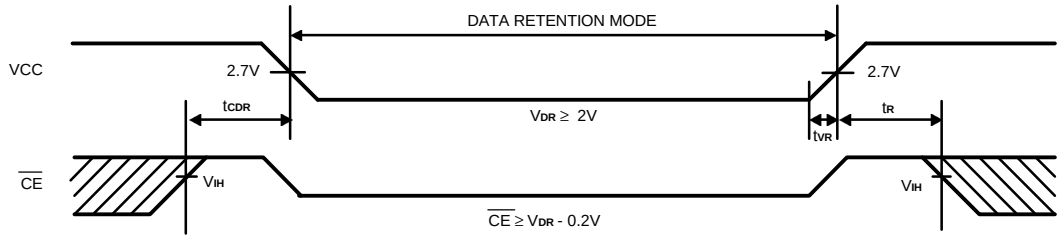


Figure 2. Output Load for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW}

Data Retention Characteristics (T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{DR}	VCC for Data Retention	2.0	3.3	V	$\overline{CE} \geq$ VCC - 0.2V
I_{CCDR}	Data Retention Current	-	5	µA	VCC = 2.0V, $\overline{CE} \geq$ VCC - 0.2V
t_{CDR}	Chip Disable to Data Retention Time	0	-	ns	See Retention Waveform
t_R	Operation Recovery Time	T_{RC}	-	ns	
t_{VR}	VCC Rise Time from Data Retention Voltage to Operating Voltage	5	-	ms	

Low VCC Data Retention Waveform

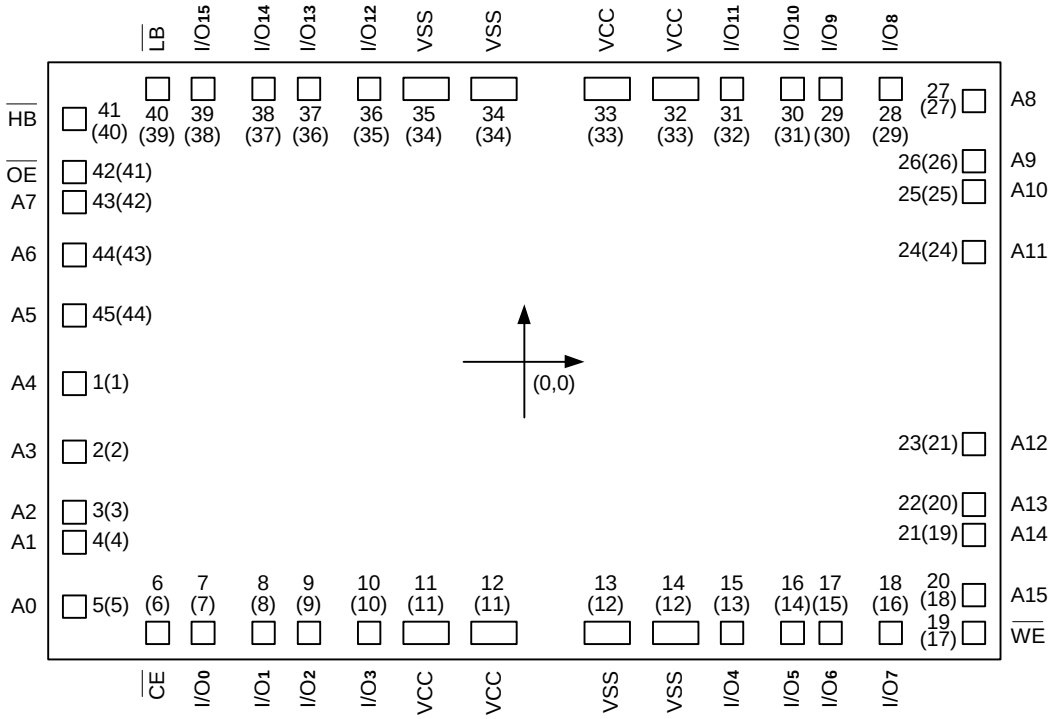


Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (µA)	Package
A62S6316H	70	50	15	Chip Form

Pad Configurations

PIN OUT (NN) is pin no. of standard package type.
NN is pad no. viewed by die form.



Pad Location

Pad No.	Pin No.	Pad Name	Coordinate (um)	
			X	Y
1	(1)	A4	-2239.85	-266.98
2	(2)	A3	-2239.85	-467.88
3	(3)	A2	-2239.85	-759.67
4	(4)	A1	-2239.85	-912.56
5	(5)	A0	-2239.85	-1209.04
6	(6)	$\overline{CE}$	-2038.56	-1356.50
7	(7)	I/O_0	-1820.49	-1356.19
8	(8)	I/O_1	-1436.33	-1356.19
9	(9)	I/O_2	-1266.73	-1356.19
10	(10)	I/O_3	-882.37	-1356.19
11	(11)	VCC	-659.05	-1351.10
12	(11)	VCC	-425.98	-1351.55
13	(12)	VSS	477.26	-1359.96
14	(12)	VSS	761.33	-1350.42
15	(13)	I/O_4	1008.96	-1356.19
16	(14)	I/O_5	1393.32	-1356.19
17	(15)	I/O_6	1562.92	-1356.19
18	(16)	I/O_7	1947.28	-1356.19
19	(17)	$\overline{WE}$	2175.78	-1356.50
20	(18)	A15	2239.84	-1123.99
21	(19)	A14	2239.84	-832.20
22	(20)	A13	2239.84	-679.31
23	(21)	A12	2239.84	-387.52

Pad No.	Pin No.	Pad Name	Coordinate (um)	
			X	Y
24	(24)	A11	2239.84	545.03
25	(25)	A10	2239.84	836.82
26	(26)	A9	2239.84	989.71
27	(27)	A8	2239.84	1287.90
28	(29)	I/O_8	1916.62	1356.18
29	(30)	I/O_9	1532.26	1356.18
30	(31)	I/O_{10}	1362.66	1356.18
31	(32)	I/O_{11}	978.30	1356.18
32	(33)	VCC	749.82	1351.09
33	(33)	VCC	516.75	1351.54
34	(34)	VSS	-312.40	1359.95
35	(34)	VSS	-596.47	1350.41
36	(35)	I/O_{12}	-884.27	1356.18
37	(36)	I/O_{13}	-1268.63	1356.18
38	(37)	I/O_{14}	-1438.23	1356.18
39	(38)	I/O_{15}	-1822.39	1356.18
40	(39)	$\overline{LB}$	-2040.46	1356.49
41	(40)	$\overline{HB}$	-2239.85	1185.54
42	(41)	$\overline{OE}$	-2239.85	934.60
43	(42)	A7	-2239.85	784.02
44	(43)	A6	-2239.85	558.28
45	(44)	A5	-2239.85	266.49