Document Title

64K X 16 BIT LOW VOLTAGE CMOS SRAM

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	October 8, 1998	Preliminary
0.1	Change access times from 70/100 ns to 55/70 ns(max.) Change dynamic operating current from 80/70mA to 40mA Modify TSOP 44L (Type II) package outline drawing	February 12, 1999	
0.2	Modify truth table	June 9, 1999	
0.3	Change dynamic operating current from 40mA to 50mA(max.)	June 21, 1999	
0.4	Modify TSOP 44L (Type II) package outline drawing and Dimensions	November 9, 1999	
0.5	Add mini BGA package outline dimensions symbol E_2 min. and max.	August 12, 2002	

Preliminary

64K X 16 BIT LOW VOLTAGE CMOS SRAM

Features

- Operating voltage: 2.7V to 3.3V
- Access times: 55/70 ns (max.)
- Current:
  - A62S6316-S series: Operating: 50mA (max.)
    Standby: 15µA (max.)
  - A62S6316-SI series: Operating: 50mA (max.)
    Standby: 30µA (max.)
- Extended operating temperature range : -25°C to 85°C for -SI series
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Data retention voltage: 2V (min.)
- Available in 44-pin TSOP and 48-ball Mini BGA (6X8) packages.

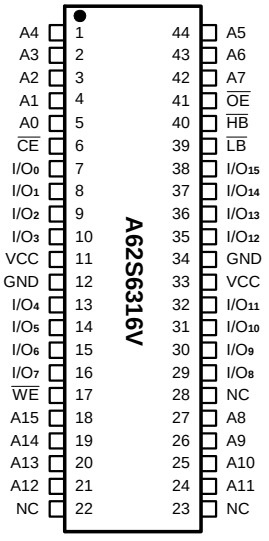
General Description

The A62S6316 is a low operating current 1,048,576-bit static random access memory organized as 65,536 words by 16 bits and operates on low power supply voltage from 2.7V to 3.3V. It is built using AMIC's high performance CMOS process.
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

The chip enable input is provided for POWER-DOWN, device enable. Two byte enable inputs and an output enable input are included for easy interfacing.
Data retention is guaranteed at a power supply voltage as low as 2V.

Pin Configuration

■ **TSOP (Type II)**

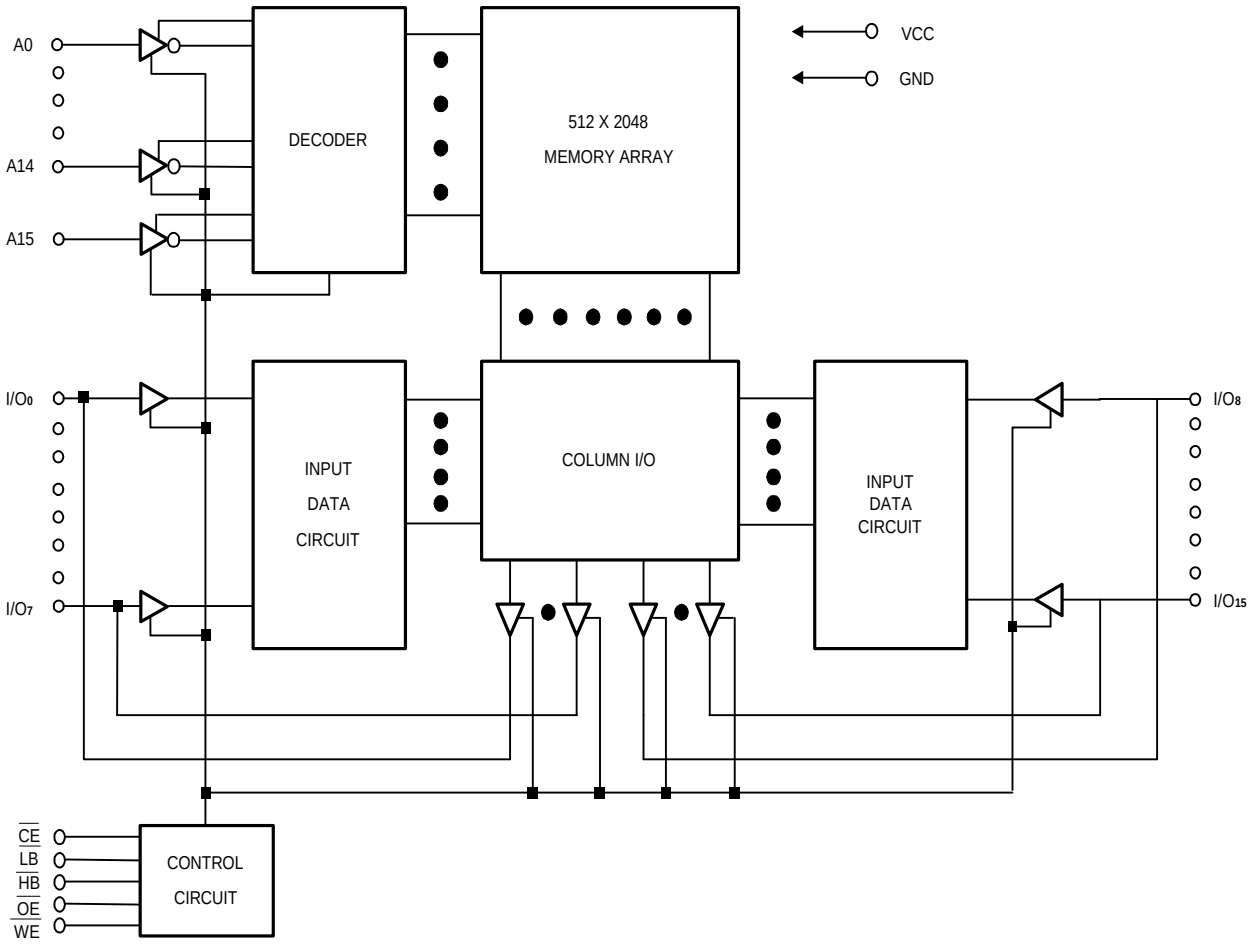


■ **Mini BGA (6X8) Top View**

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	NC
B	I/O_8	$\overline{HB}$	A3	A4	$\overline{CS}$	I/O_0
C	I/O_9	I/O_{10}	A5	A6	I/O_1	I/O_2
D	VSS	I/O_{11}	NC	A7	I/O_3	VCC
E	VCC	I/O_{12}	NC	NC	I/O_4	VSS
F	I/O_{14}	I/O_{13}	A14	A15	I/O_5	I/O_6
G	I/O_{15}	NC	A12	A13	$\overline{WE}$	I/O_7
H	NC	A8	A9	A10	A11	NC

A62S6316G

Block Diagram



Pin Description - TSOP

Pin No.	Symbol	Description
1 - 5, 18 - 21, 24 - 27,42 - 44	A0 - A15	Address Inputs
6	$\overline{CE}$	Chip Enable Input
7 - 10, 13 - 16, 29 - 32, 35 - 38	I/O_0 - I/O_{15}	Data Input/Outputs
17	$\overline{WE}$	Write Enable Input
39	$\overline{LB}$	Byte Enable Input (I/O_0 to I/O_7)
40	$\overline{HB}$	Byte Enable Input (I/O_8 to I/O_{15})
41	$\overline{OE}$	Output Enable Input
11, 33	VCC	Power
12, 34	GND	Ground
22 , 23, 28	NC	No Connection

Recommended DC Operating Conditions

(T_A = 0°C to + 70°C or -25°C to 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	2.7	3.0	3.3	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	VCC + 0.3	V
V_{IL}	Input Low Voltage	-0.3	-	+0.6	V
C_L	Output Load	-	-	30	pF
TTL	Output Load	-	-	1	-

Absolute Maximum Ratings*

VCC to GND . . . . . -0.5V to +4.6V
IN, IN/OUT Volt to GND . . . . . -0.5V to VCC + 0.5V
Operating Temperature, Topr . . . . . -25°C to +85°C
Storage Temperature, Tstg . . . . . -55°C to +125°C
Power Dissipation, P_T 0.7W
Soldering Temp. & Time . . . . . 260°C, 10 sec

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to + 70°C or -25°C to 85°C, VCC = 2.7V to 3.3V, GND = 0V)

Symbol	Parameter	A62S6316-55S/70S		A62S6316-55SI/70SI		Unit	Conditions
		Min.	Max.	Min.	Max.		
$\lvert I_{LI} \rvert$	Input Leakage Current	-	1	-	1	µA	V_{IN} = GND to VCC
$\lvert I_{LO} \rvert$	Output Leakage Current	-	1	-	1	µA	$\overline{CE}$ = V_{IH} or $\overline{LB}$ = V_{IH} or $\overline{HB}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IH} $V_{I/O}$ = GND to VCC
I_{CC}	Active Power Supply Current	-	5	-	5	mA	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA
I_{CC1}	Dynamic Operating Current	-	50	-	50	mA	Min. Cycle, Duty = 100% $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA
I_{CC2}		-	20	-	20	mA	$\overline{CE}$ = V_{IL}, V_{IH} = VCC, V_{IL} = 0V, f = 1MHz, $I_{I/O}$ = 0 mA
I_{SB}	Standby Power Supply Current	-	0.5	-	0.5	mA	$\overline{CE}$ = V_{IH}
I_{SB1}		-	15	-	30	µA	$\overline{CE}$ ≥ VCC - 0.2V V_{IN} ≥ 0V
V_{OL}	Output Low Voltage	-	0.4	-	0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.2	-	2.2	-	V	I_{OH} = -1.0mA

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{HB}$	I/O_0 to I/O_7 Mode	I/O_8 to I/O_{15} Mode	VCC Current
H	X	X	X	X	Not selected	Not selected	I_{SB1}, I_{SB}
L	L	H	L	L	Read	Read	I_{CC1}, I_{CC2}, I_{CC}
			L	H	Read	High - Z	I_{CC1}, I_{CC2}, I_{CC}
			H	L	High - Z	Read	I_{CC1}, I_{CC2}, I_{CC}
L	X	L	L	L	Write	Write	I_{CC1}, I_{CC2}, I_{CC}
			L	H	Write	Not Write/Hi - Z	I_{CC1}, I_{CC2}, I_{CC}
			H	L	Not Write/Hi - Z	Write	I_{CC1}, I_{CC2}, I_{CC}
L	H	H	L	X	High - Z	High - Z	I_{CC1}, I_{CC2}, I_{CC}
			X	L	High - Z	High - Z	I_{CC1}, I_{CC2}, I_{CC}
X	X	X	H	H	Not selected	Not selected	I_{SB1}, I_{SB}

Note: X = H or L

Capacitance (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance	-	6	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance	-	8	pF	$V_{I/O}$ = 0V

* These parameters are sampled and not 100% tested.

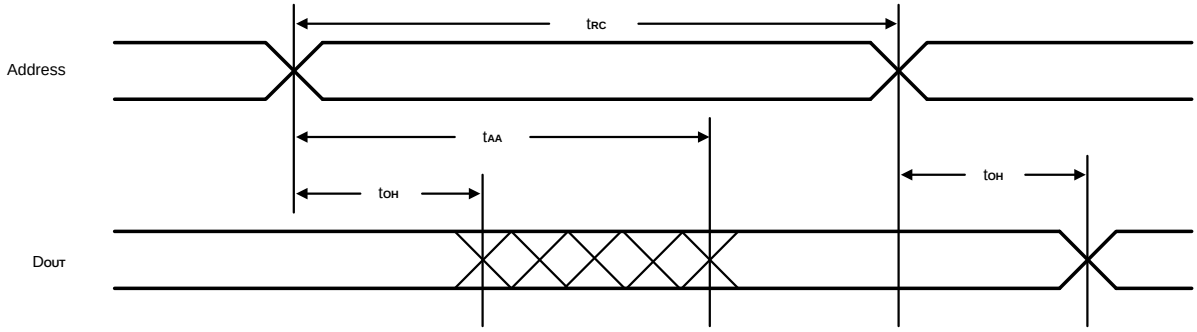
AC Characteristics (T_A = 0°C to +70°C or -25°C to 85°C, VCC = 2.7V to 3.3V)

Symbol	Parameter	A62S6316-55S/SI		A62S6316-70S/SI		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	55	-	70	-	ns
t_{AA}	Address Access Time	-	55	-	70	ns
t_{ACE}	Chip Enable Access Time	-	55	-	70	ns
t_{BE}	Byte Enable Access Time	-	55	-	70	ns
t_{OE}	Output Enable to Output Valid	-	30	-	35	ns
t_{CLZ}	Chip Enable to Output in Low Z	10	-	10	-	ns
t_{BLZ}	Byte Enable to Output in Low Z	5	-	5	-	ns
t_{OLZ}	Output Enable to Output in Low Z	5	-	5	-	ns
t_{CHZ}	Chip Disable to Output in High Z	-	20	-	25	ns
t_{BHZ}	Byte Disable to Output in High Z	-	20	-	25	ns
t_{OHZ}	Output Disable to Output in High Z	-	20	-	25	ns
t_{OH}	Output Hold from Address Change	5	-	10	-	ns
Write Cycle						
t_{WC}	Write Cycle Time	55	-	70	-	ns
t_{CW}	Chip Enable to End of Write	50	-	60	-	ns
t_{BW}	Byte Enable to End of Write	50	-	60	-	ns
t_{AS}	Address Setup Time	0	-	0	-	ns
t_{AW}	Address Valid to End of Write	50	-	60	-	ns
t_{WP}	Write Pulse Width	40	-	50	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	ns
t_{WHZ}	Write to Output in High Z	-	25	-	30	ns
t_{DW}	Data to Write Time Overlap	25	-	30	-	ns
t_{DH}	Data Hold from Write Time	0	-	0	-	ns
t_{OW}	Output Active from End of Write	5	-	5	-	ns

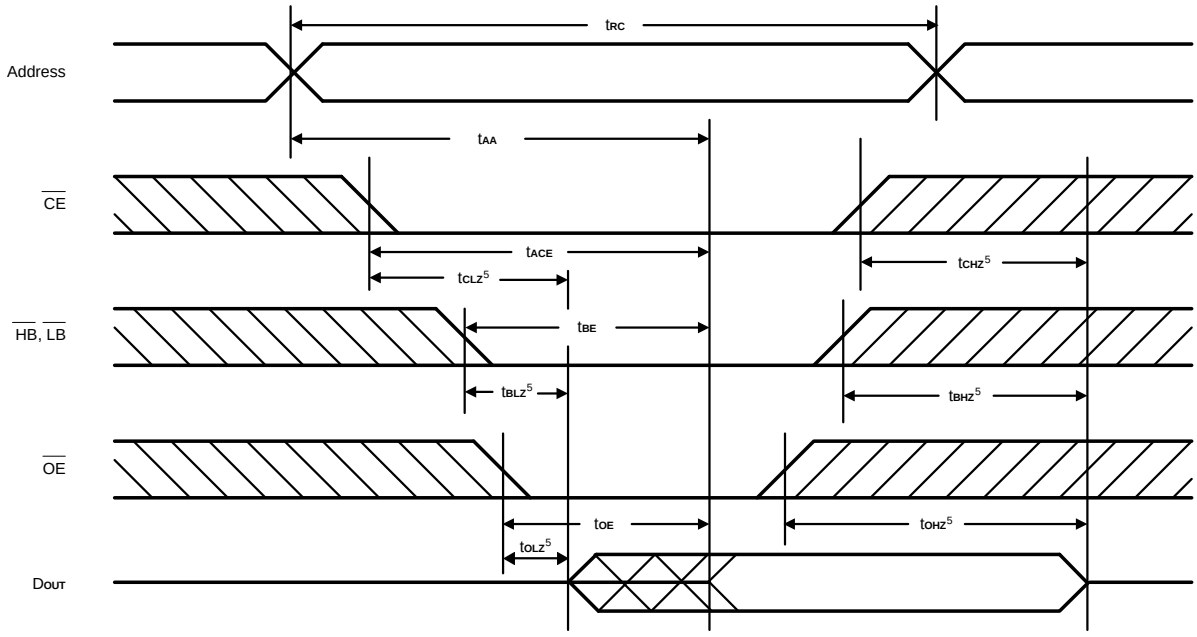
Note: t_{CHZ}, t_{BHZ} and t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms

Read Cycle 1[1, 2, 4]



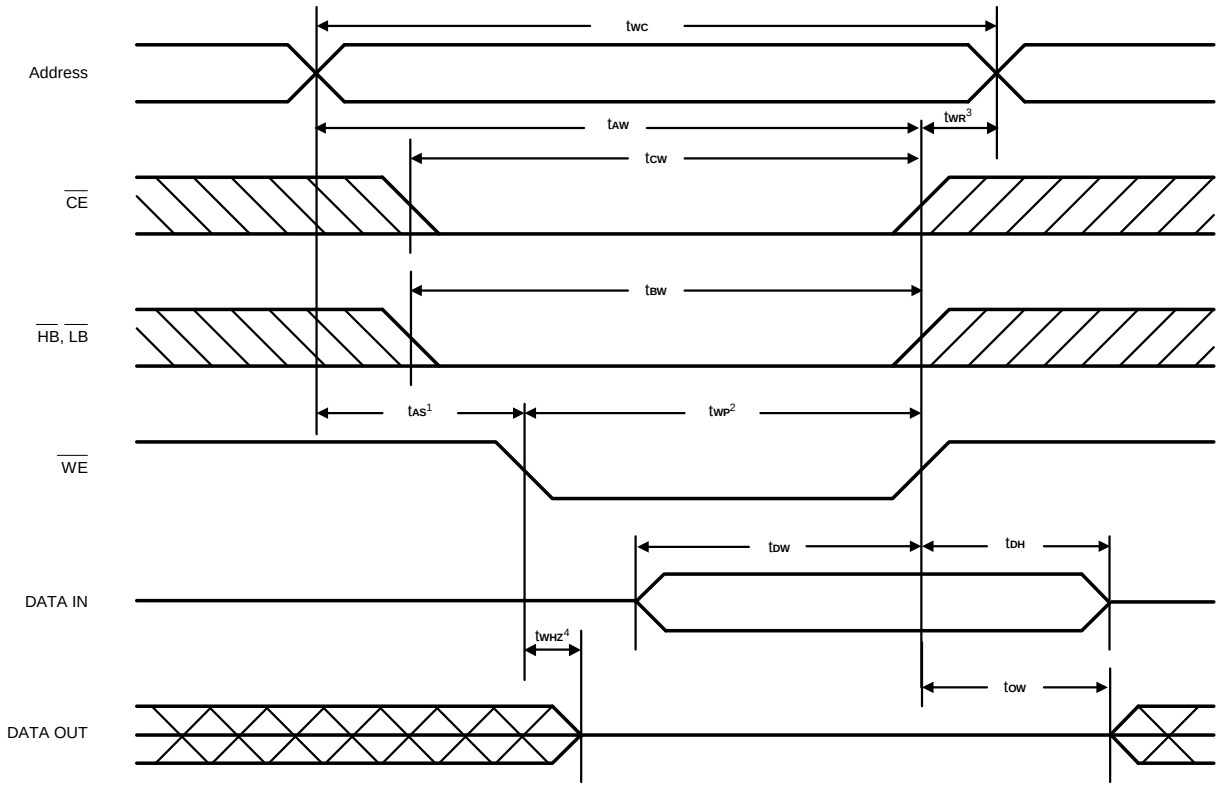
Read Cycle 2[1, 2, 3]



Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled $\overline{CE}$ = V_{IL}, $\overline{HB}$ = V_{IL} and, or $\overline{LB}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CE}$ and ($\overline{HB}$ and, or $\overline{LB}$) transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

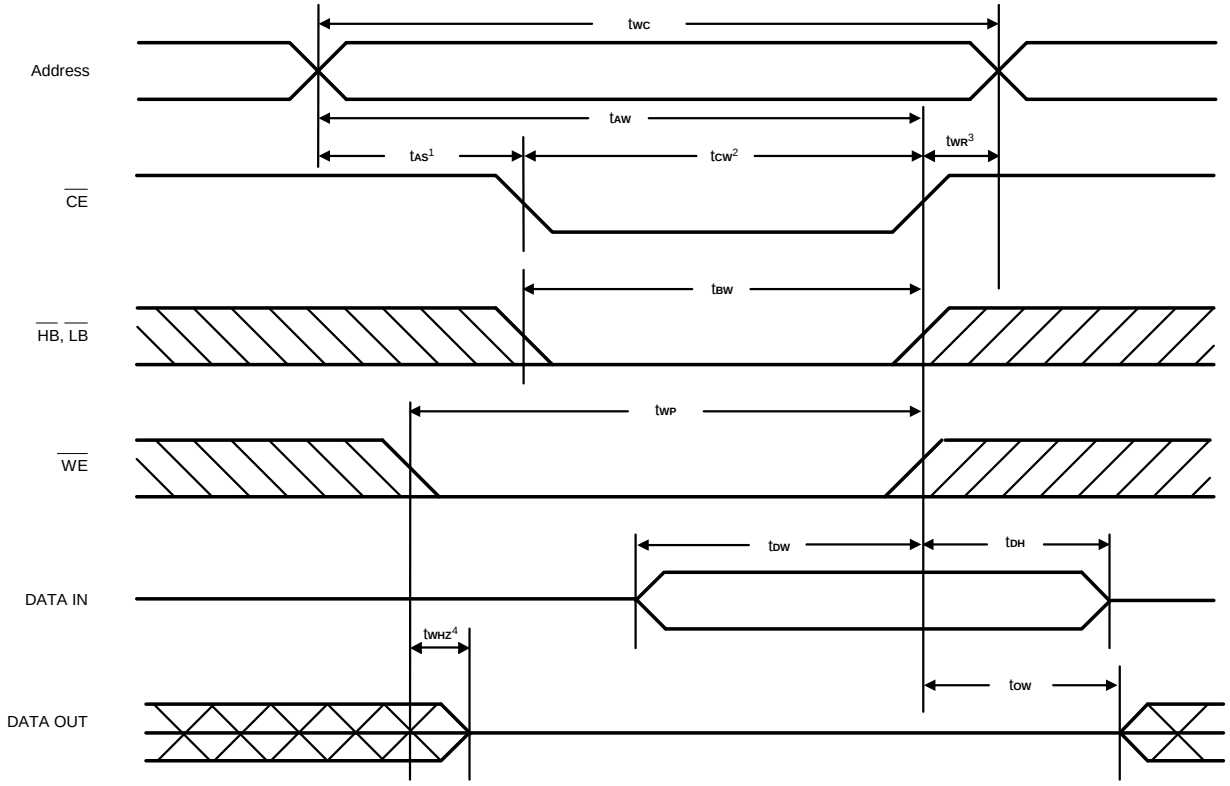
Timing Waveforms (continued)

Write Cycle 1
(Write Enable Controlled)



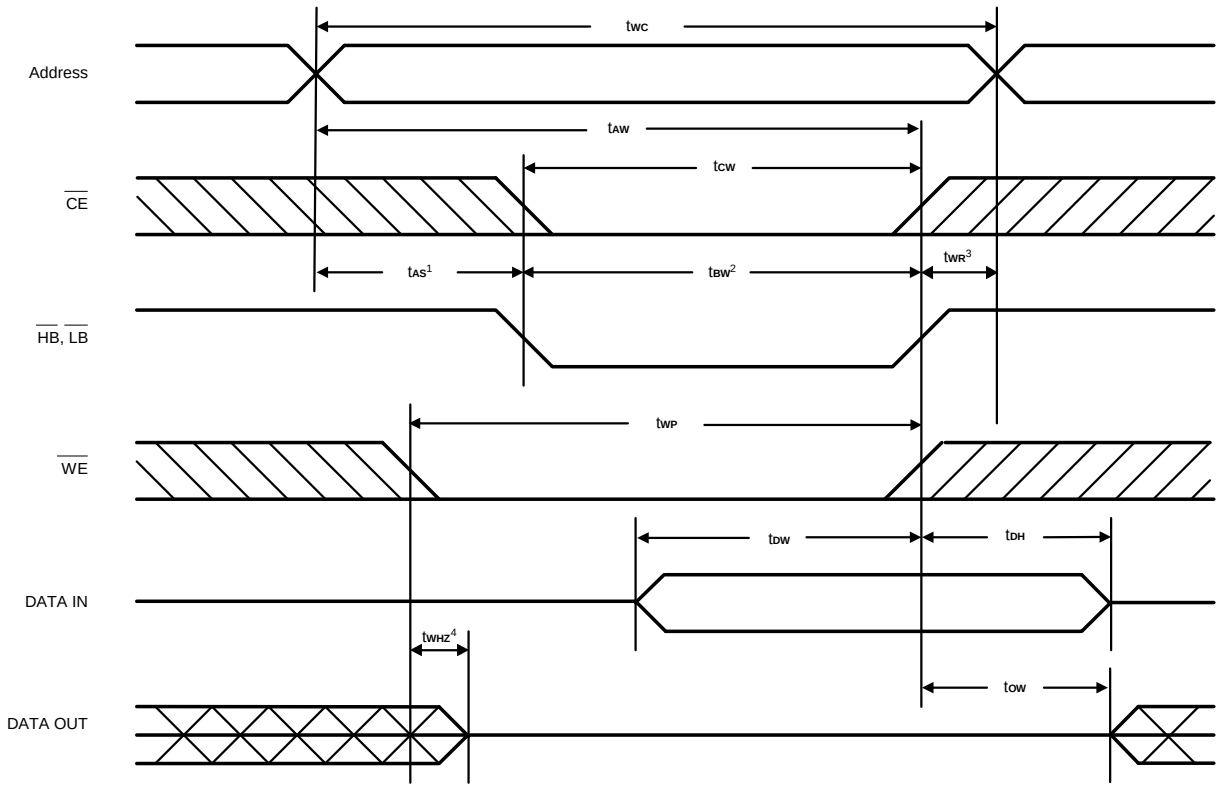
Timing Waveforms (continued)

Write Cycle 2
(Chip Enable Controlled)



Timing Waveforms (continued)

Write Cycle 3
(Byte Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap (t_{WP}, t_{BW}) of a low $\overline{CE}$, $\overline{WE}$ and ($\overline{HB}$ and, or $\overline{LB}$).
3. t_{WR} is measured from the earliest of $\overline{CE}$ or $\overline{WE}$ or ($\overline{HB}$ and, or $\overline{LB}$) going high to the end of the Write cycle.
4. $\overline{OE}$ level is high or low.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0V to 2.4V
Input Rise And Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2

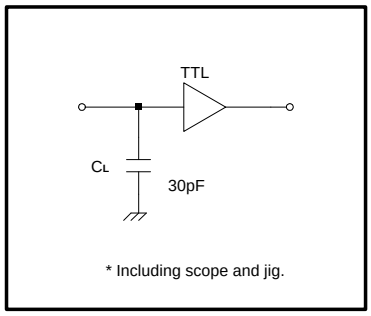


Figure 1. Output Load

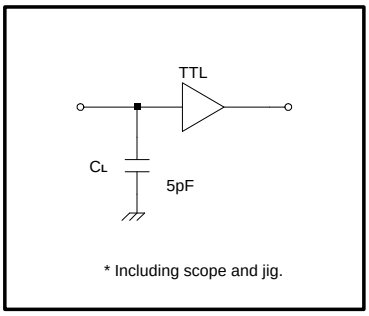


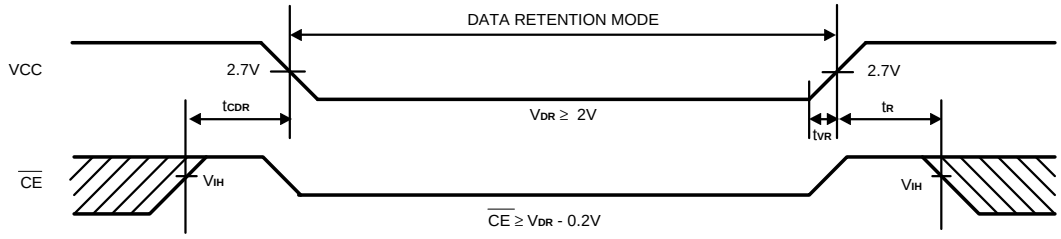
Figure 2. Output Load for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW}

Data Retention Characteristics (TA = 0°C to 70°C or -25°C to 85°C)

Symbol	Parameter		Min.	Max.	Unit	Conditions
V_{DR}	VCC for Data Retention		2.0	3.3	V	$\overline{CE} \geq$ VCC - 0.2V
I_{CCDR}	Data Retention Current	S-Version	-	10*	µA	VCC = 2.0V, $\overline{CE} \geq$ VCC - 0.2V, $V_{IN} \geq$ 0V
		SI-Version	-	20**		
t_{CDR}	Chip Disable to Data Retention Time		0	-	ns	See Retention Waveform
t_R	Operation Recovery Time		T_{RC}	-	ns	
t_{VR}	VCC Rise Time from Data Retention Voltage to Operating Voltage		5	-	ms	

* A62S6316-55S/70S I_{CCDR}: max. 3µA at T_A = 0°C to + 40°C
** A62S6316-55SI/70SI I_{CCDR}: max. 3µA at T_A = 0°C to + 40°C

Low VCC Data Retention Waveform



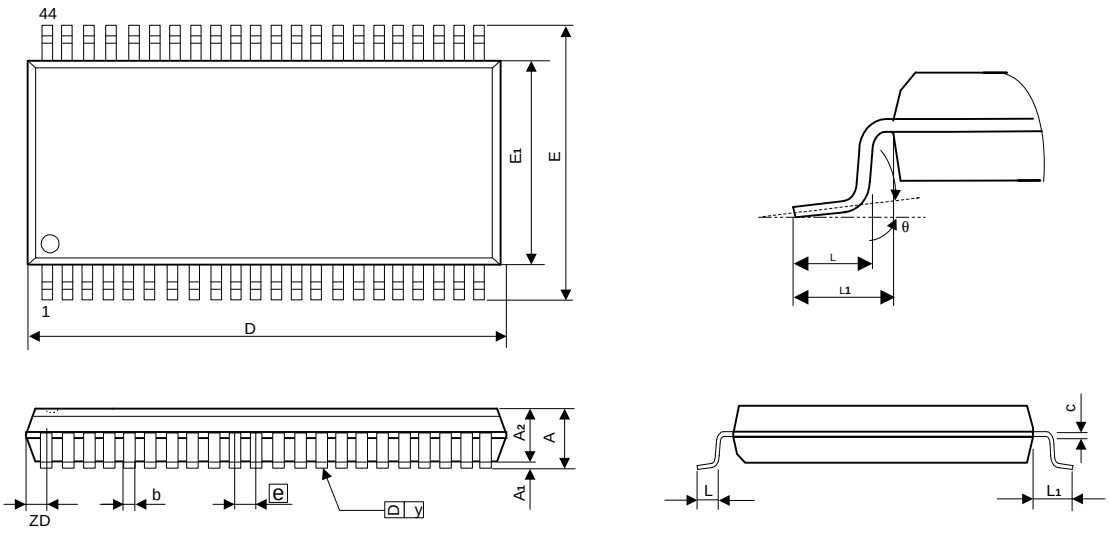
Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package
A62S6316V-55S	55	50	15	44L TSOP
A62S6316V-55SI		50	30	44L TSOP
A62S6316G-55S		50	15	48B Mini BGA
A62S6316G-55SI		50	30	48B Mini BGA
A62S6316V-70S	70	50	15	44L TSOP
A62S6316V-70SI		50	30	44L TSOP
A62S6316G-70S		50	15	48B Mini BGA
A62S6316G-70SI		50	30	48B Mini BGA

Package Information

TSOP 44L (Type II) Outline Dimensions

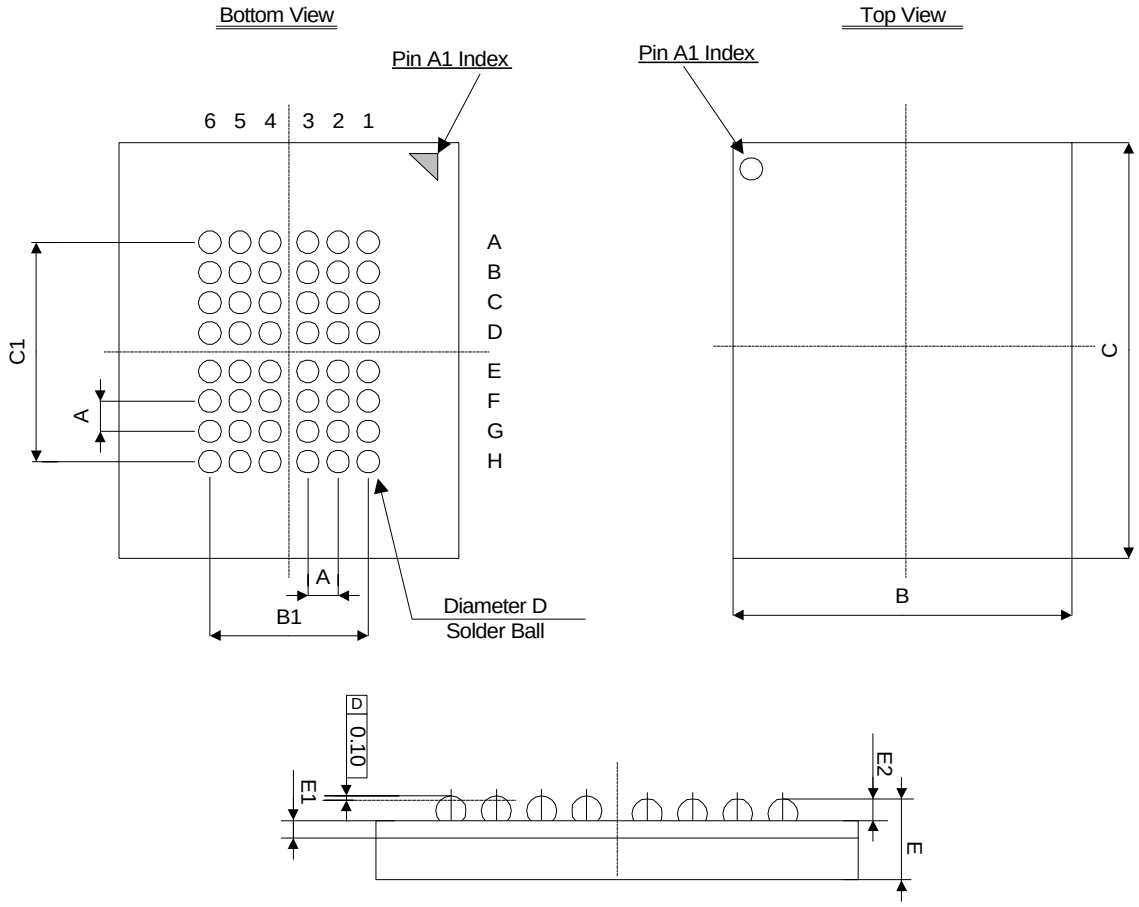
unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.012	-	0.018	0.30	-	0.45
c	0.005	-	0.008	0.12	-	0.21
D	0.720	0.725	0.730	18.28	18.41	18.54
ZD	0.032 REF			0.805 REF		
E	0.455	0.463	0.471	11.56	11.76	11.96
E_1	0.395	0.400	0.405	10.03	10.16	10.29
L	0.019	0.023	0.027	0.49	0.59	0.69
L_1	0.031 REF			0.80 REF		
e	0.031 BSC			0.80 BSC		
y	-	-	0.004	-	-	0.10
θ	0°	-	5°	0°	-	5°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension ZD includes end flash.

Mini BGA 6X8 (48 BALLS) Outline Dimensions unit : millimeter(mm)



Symbol	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	1.00	1.10	1.20
E1	-	0.36	-
E2	0.17	0.22	0.27