S7IPLI27/I29JB0

Stacked Multi-Chip Package (MCP) Flash Memory and pSRAM
I28 Megabit (8M x I6-Bit) CMOS 3.0 Volt-only Simultaneous Operation Flash Memory and 32 Megabit (2M x I6-Bit) CMOS Pseudo Static RAM with Page Mode

ADVANCE

Distinctive Characteristics

MCP Features

- **Power supply voltage of 2.7 to 3.1 volt**
- **High performance**
  - 70 ns maximum access time (Flash)
  - 30 ns maximum page access time (Flash)
  - 70 ns maximum access time (PSRAM)
  - 30 ns maximum page access time (PSRAM)
- **Package**
  - 64-Ball FBGA
- **Operating Temperature**
  - –25°C to +85°C

Flash Memory Features

ARCHITECTURAL ADVANTAGES

- **128 Mbit Page Mode device**
  - Page size of 8 words: Fast page read access from random locations within the page
- **Single power supply operation**
  - Full Voltage range: 2.7 to 3.1 volt read, erase, and program operations for battery-powered applications
- **Dual Chip Enable inputs (PL129J)**
  - Two CE# inputs control selection of each half of the memory space
- **Simultaneous Read/Write Operation**
  - Data can be continuously read from one bank while executing erase/program functions in another bank
  - Zero latency switching from write to read operations
- **FlexBank Architecture**
  - 4 separate banks, with up to two simultaneous operations per device
  - Bank A:
    16Mbit (4Kw x 8 and 32Kw x 31)
  - Bank B:
    48Mbit (32Kw x 96)
  - Bank C:
    48 Mbit (32Kw x 96)
  - Bank D:
    16Mbit (4Kw x 8 and 32Kw x 31)
- **SecSi™ (Secured Silicon) Sector region**
  - Up to 128 words accessible through a command sequence
  - Up to 64 factory-locked words
  - Up to 64 customer-lockable words
- **Both top and bottom boot blocks in one device**
- **Manufactured on 0.11 µm process technology**
- **Data retention: 20 years typical**
- **Cycling Endurance: 1 million cycles per sector typical**

SOFTWARE FEATURES

- **Software command-set compatible with JEDEC 42.4 standard**
  - Backward compatible with Am29F and Am29LV families
- **CFI (Common Flash Interface) compliant**
  - Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- **Erase Suspend / Erase Resume**
  - Suspends an erase operation to allow read or program operations in other sectors of same bank
- **Unlock Bypass Program command**
  - Reduces overall programming time when issuing multiple program command sequences

HARDWARE FEATURES

- **Ready/Busy# pin (RY/BY#)**
  - Provides a hardware method of detecting program or erase cycle completion
- **Hardware reset pin (RESET#)**
  - Hardware method to reset the device to reading array data
- **WP#/ ACC (Write Protect/Acceleration) input**
  - At V_{IL}, hardware level protection for the first and last two 4K word sectors.
  - At V_{HH}, provides accelerated programming in a factory setting
- **Persistent Sector Protection**
  - A command sector protection method to lock combinations of individual sectors and sector groups

to prevent program or erase operations within that sector

— Sectors can be locked and unlocked in-system at V_{CC} level

- **Password Sector Protection**
  — A sophisticated sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector using a user-defined 64-bit password

PSRAM Features

- **Power dissipation**
  — Operating: 40 mA maximum
  — Standby: 135 µA maximum
- **CE1#r and CE2r Chip Select**
- **Power down features using CE1#r and CE2r**
- **Data retention supply voltage: 1.5 to 3.1 volt**
- **Byte data control: LB# (DQ0–DQ7), UB#(DQ8–DQ15)**

Product Selector Guide

Part Number	**S7IPLI27JB0BAW9Z# S7IPLI27JB0BAW9U# S7IPLI27JB0BAW9P# S7IPLI27JB0BFW9Z# S7IPLI27JB0BFW9U# S7IPLI27JB0BFW9P# S7IPLI29JB0BAW9Z# S7IPLI29JB0BAW9U# S7IPLI29JB0BAW9P# S7IPLI29JB0BFW9Z# S7IPLI29JB0BFW9U# S7IPLI29JB0BFW9P#**	
Supply Voltage	V_{CC} = 2.7–3.1 V	V_{CC} = 2.7–3.1 V
Supply Voltage	Flash	PSRAM
Max Access Time, ns	70	70
Max CE# Access, ns	70	70
Max Page Access, ns	30	30
Max OE# Access, ns	30	40

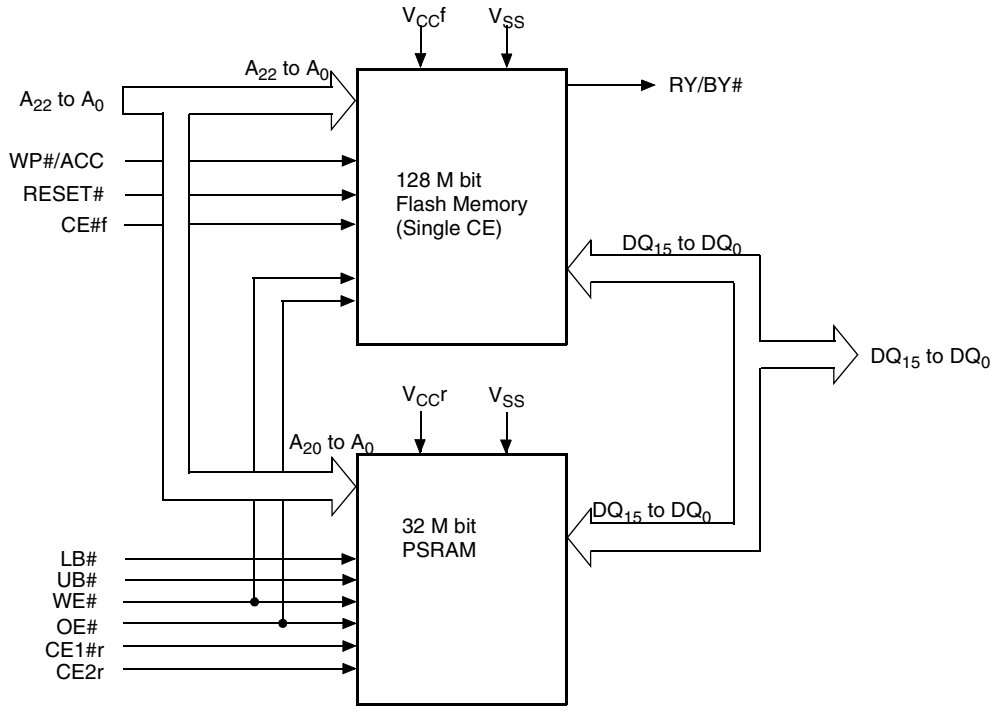
Note:*Both VCCf and VCCr must be the same level when either part is being accessed.*

S7IPLI27/I29JB0

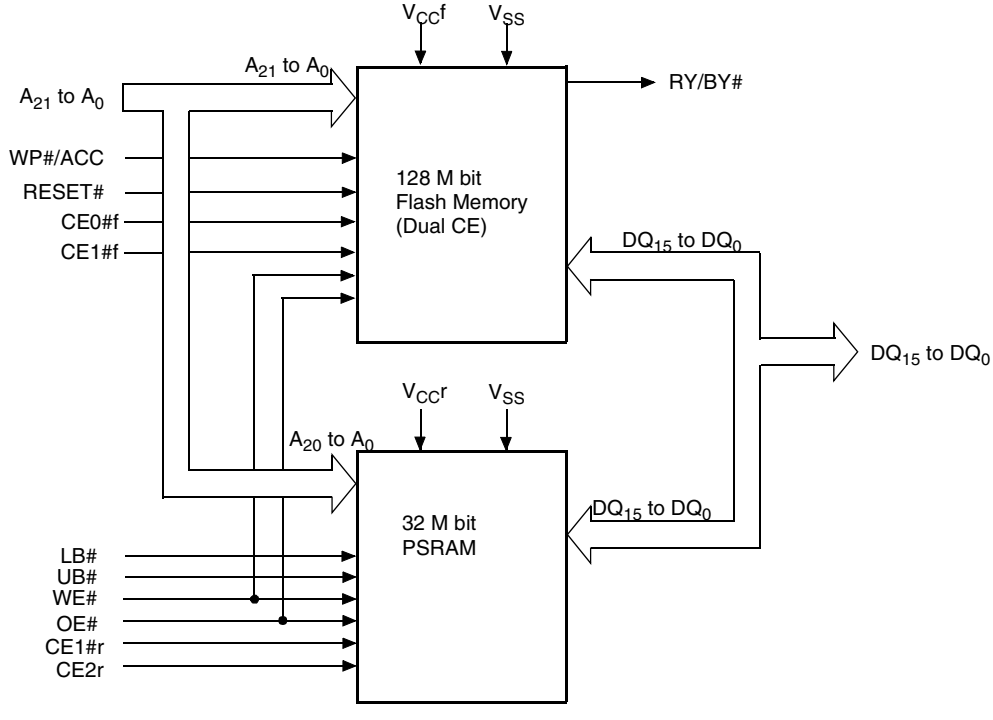
32Mb pSRAM (Supplier I)

Revision Summary

MCP Block Diagram (S71PLI27JB0)

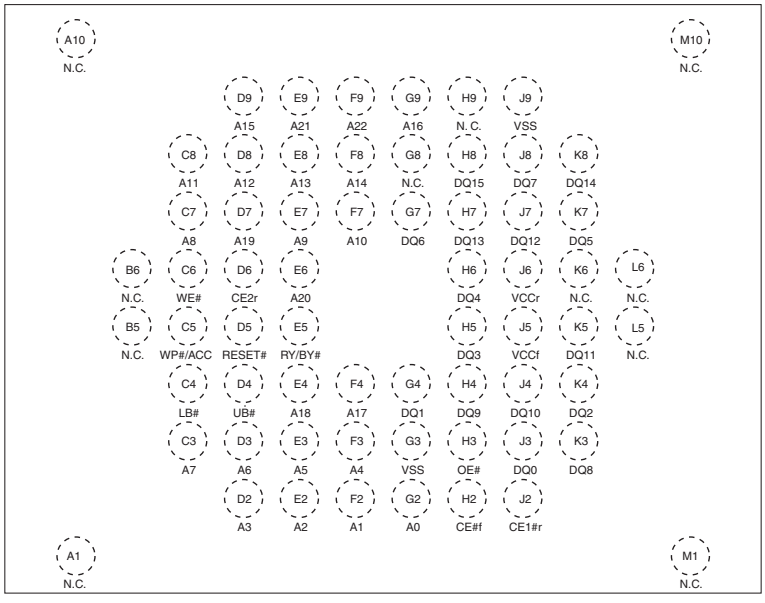


MCP Block Diagram (S71PLI29JB0)



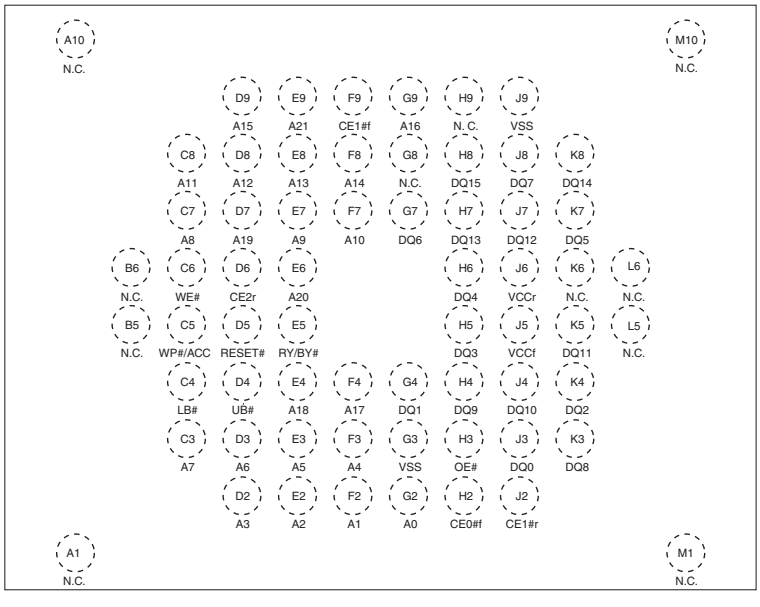
Connection Diagram (S7IPLI27JB0)

64-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)



Connection Diagram (S7IPLI29JB0)

64-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)



Special Handling Instructions For FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

Input/Output Descriptions (S71PLI27JB0)

Pin Name	Input / Output	Description
A19to A0	I	Address inputs (Common)
A22 to A20	I	Address inputs (Flash)
DQ15-DQ0	I/O	Data input/output
CE#f	I	Chip Enable (Flash)
CE1#r	I	Chip Enable (PSRAM)
CE2r	I	Chip Enable (PSRAM
OE#	I	Output Enable (Common)
WE#	I	Write Enable (Common)
RY/BY#	O	Ready/Busy Output (Flash) Open Drain Output
UB#	I	Upper Byte Control
LB#	I	Lower Byte Control
RESET#	I	Hardware Reset Pin / Sector Protection Unlock (Flash)
WP#/ACC	I	Write Protect / Acceleration (Flash)
N.C.	–	No Internal Connection
V_{SS}	Power	Device Ground (Common)
V_{CC}f	Power	Device Power Supply (Flash)
V_{CC}r	Power	Device Power Supply (Flash)

Input/Output Descriptions (S71PLI29JB0)

Pin Name	Input / Output	Description
A19to A0	I	Address inputs (Common)
A21 to A20	I	Address inputs (Flash)
DQ15-DQ0	I/O	Data input/output
CE0#f, CE1#f	I	Chip Enable (Flash)
CE1#r	I	Chip Enable (PSRAM)
CE2r	I	Chip Enable (PSRAM
OE#	I	Output Enable (Common)
WE#	I	Write Enable (Common)
RY/BY#	O	Ready/Busy Output (Flash) Open Drain Output
UB#	I	Upper Byte Control
LB#	I	Lower Byte Control
RESET#	I	Hardware Reset Pin / Sector Protection Unlock (Flash)
WP#/ACC	I	Write Protect / Acceleration (Flash)
N.C.	–	No Internal Connection
V_{SS}	Power	Device Ground (Common)
V_{CC}f	Power	Device Power Supply (Flash)
V_{CC}r	Power	Device Power Supply (Flash)

Ordering Information

Valid Combinations								
Order Number	**Flash**	**Flash Initial/Page Speed (ns)**	**pSRAM**	**pSRAM Supplier**	**pSRAM Initial/Page Speed (ns)**	**Pb-free Compliant or Pb-free**	**MCP Package Size (mm)**	**Ball Count**
S71PL127JB0BAW9Z#	S29PL127J	70/30	32Mb	Supplier 1	70/30	Pb-free Compliant	8 x 11.6 x 1.2	64
S71PL127JB0BAW9U#				Supplier 2				
S71PL127JB0BAW9P#				Supplier 3				
S71PL127JB0BFW9Z#				Supplier 1		Pb-free		
S71PL127JB0BFW9U#				Supplier 2				
S71PL127JB0BFW9P#				Supplier 3				
S71PL129JB0BAW9Z#	S29PL129J	70/30	32Mb	Supplier 1	70/30	Pb-free Compliant	8 x 11.6 x 1.2	64
S71PL129JB0BAW9U#				Supplier 2				
S71PL129JB0BAW9P#				Supplier 3				
S71PL129JB0BFW9Z#				Supplier 1		Pb-free		
S71PL129JB0BFW9U#				Supplier 2				
S71PL129JB0BFW9P#				Supplier 3				

Notes:
1. # = 0 (Tray), 1 (7" Tape and Reel), or 3 (13" Tape and Reel)

Device Bus Operations (S7IPLI27B0)

Operation (1), (2)	CEf#	CE1r#	CE2r	OE#	WE#	LB#	UB#	A_{22} to A_0	DQ_7 to DQ_0	DQ_{15} to DQ_8	RESET	WP/ ACC (7)
Full Standby	H	H	H	X	X	X	X	X	High-Z	High-Z	H	X
Output Disable	H	L	H	H	H	X	X	X(6)	High-Z	High-Z	H	X
	L	H						X				
Read from Flash (3)	L	H	H	L	H	X	X	Valid	D_{OUT}	D_{OUT}	H	X
Write to Flash	L	H	H	H	L	X	X	Valid	D_{IN}	D_{IN}	H	X
Read from PSRAM	H	L	H	L	H	L	L	Valid	D_{IN}	D_{IN}	H	X
						H	L		High-Z	D_{IN}		
						L	H		D_{IN}	High-Z		
PSRAM No Read	H	L	H	L	H	H	H	Valid	High-Z	High-Z	H	X
Write to PSRAM	H	L	H	H(5)	L	L	L	Valid	D_{IN}	D_{IN}	H	X
						H	L		High-Z	D_{IN}		
						L	H		D_{IN}	High-Z		
PSRAM No Write	H	L	H	H(5)	L	H	H	Valid	High-Z	High-Z	H	X
Flash Temporary Sector Group Unprotection(4)	X	X	X	X	X	X	X	X	X	X	V_{ID}	X
Flash Hardware Reset	X	H	H	X	X	X	X	X	High-Z	High-Z	L	X
Flash Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	L
PSRAM Power Down	X	X	L	X	X	X	X	X	X	X	X	X

Legend:*Legend: L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, Hihe-Z = High Impedance. See DC Characteristics for voltage levels.*

Note:

1. *Other operations except for indicated this column are inhibited.*
2. *Do not apply for a following state two or more on the same time;*
   1) CEf# = V_{IL}, 2) CE1r# = V_{IL} and CE2r = V_{IH},
3. *WE# can be V_{IL} if OE# is V_{IL}, OE# at V_{IH} initiates the write operations.*
4. *It is also used for the extended sector group protections.*
5. *OE# can be V_{IL} during Write operation if the following conditions are satisfied;*
   1) Write pulse is initiated by CE1r# (refer to CE1r# Controlled Write timing), or cycle time of the previous operation cycle is satisfied.
   2) OE# stays V_{IL} during Write cycle.
6. *Can be either V_{IL} or V_{IH} but must be valid before Read or Write.*
7. *Protect " outer most " 2×8K bytes (4 words) on both ends of the boot block sectors.*

Device Bus Operations (S71PLI29B0)

Operation (1), (2)	CE0#f	CE1#f	CE1#r	CE2r	OE	WE#	LB#	UB#	A_{21} to A_0	DQ_7 to DQ_0	DQ_{15} to DQ_8	RESET#	WP/ ACC (7)
Full Standby	H	H	H	H	X	X	X	X	X	High-Z	High-Z	H	X
Output Disable	H	H	L	H	H	H	X	X	X(6)	High-Z	High-Z	H	X
	L	H	H						X				
	H	L	H										
Read from Flash (3)	L	H	H	H	L	H	X	X	Valid	D_{OUT}	D_{OUT}	H	X
	H	L											
Write to Flash	L	H	H	H	H	L	X	X	Valid	D_{IN}	D_{IN}	H	X
	H	L	H	H	H	L	X	X	Valid	D_{IN}	D_{IN}	H	X
Read from PSRAM	H	H	L	H	L	H	L	L	Valid	D_{IN}	D_{IN}	H	X
							H	L		High-Z	D_{IN}		
							L	H		D_{IN}	High-Z		
PSRAM No Read	H	H	L	H	L	H	H	H	Valid	High-Z	High-Z	H	X
Write to PSRAM	H	H	L	H	H(5)	L	L	L	Valid	D_{IN}	D_{IN}	H	X
							H	L		High-Z	D_{IN}		
							L	H		D_{IN}	High-Z		
PSRAM No Write	H	H	L	H	H(5)	L	H	H	Valid	High-Z	High-Z	H	X
Flash Temporary Sector Group Unprotection(4)	X	X	X	X	X	X	X	X	X	X	X	V_{ID}	X
Flash Hardware Reset	X	X	H	H	X	X	X	X	X	High-Z	High-Z	L	X
Flash Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	X	L
PSRAM Power Down	X	X	X	L	X	X	X	X	X	X	X	X	X

Legend: *L = VIL, H = VIH, X can be either VIL or VIH, Hihe-Z = High Impedance. See DC Characteristics for voltage levels.*

Note:

1. *Other operations except for indicated this column are inhibited.*
2. *Do not apply for a following state two or more on the same time;*
   1) CEf# = V_{IL}, 2) CE1r# = V_{IL} and CE2r = V_{IH},
3. *WE# can be V_{IL} if OE# is V_{IL}, OE# at V_{IH} initiates the write operations.*
4. *It is also used for the extended sector group protections.*
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operation cycle is satisfied.
2) OE# stays V_{IL} during Write cycle.

6. *Can be either V_{IL} or V_{IH} but must be valid before Read or Write.*
7. *Protect " outer most " 2×8K bytes (4 words) on both ends of the boot block sectors.*

Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Storage Temperature	Tstg	−55	+125	°C
Ambient Temperature with Power Applied	T_A	−25	+85	°C
Voltage with Respect to Ground All pins except $\overline{RESET}$,$\overline{WP}$/ACC *[1]	V_{IN}, V_{OUT}	−0.3	V_{CC}f +0.3	V
			V_{CC}r +0.3	V
V_{CC}f/V_{CC}r Supply *[1]	V_{CC}f,V_{CC}r	−0.3	+3.3	V
$\overline{RESET}$ *[2]	V_{IN}	−0.5	+ 13.0	V
$\overline{WP}$/ACC *[3]	V_{IN}	−0.5	+10.5	V

Notes:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. See Figure 1. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 2.*
2. *Minimum DC input voltage on pins RESET#, and WP#/ACC is −0.5 V. During voltage transitions, WP#/ACC, and RESET# may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. See Figure 1. Maximum DC input voltage on pin RESET# is +12.5 V which may overshoot to +14.0 V for periods up to 20 ns. Maximum DC input voltage on WP#/ACC is +9.5 V which may overshoot to +12.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

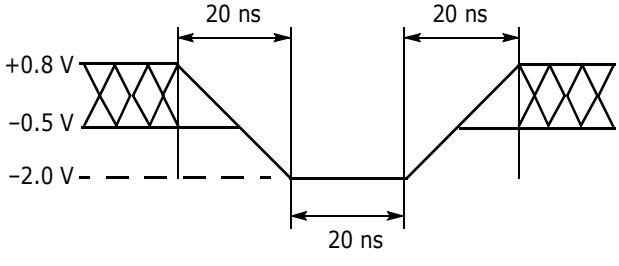


Figure I. Maximum Negative Overshoot Waveform

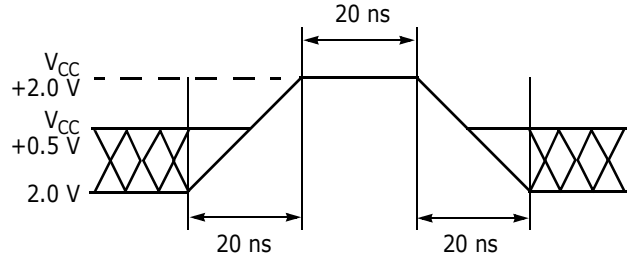


Figure 2. Maximum Positive Overshoot Waveform

Operating Ranges

Parameter	Symbol	Value		Unit
		Min.	Max.	
Ambient Temperature	T_A	−25	+85	°C
V_{CC}f/V_{CC}r Supply Voltages	V_{CC}f,V_{CC}r	+2.7	+3.1	V

Note:*Operating ranges define those limits between which the functionality of the device is guaranteed.*

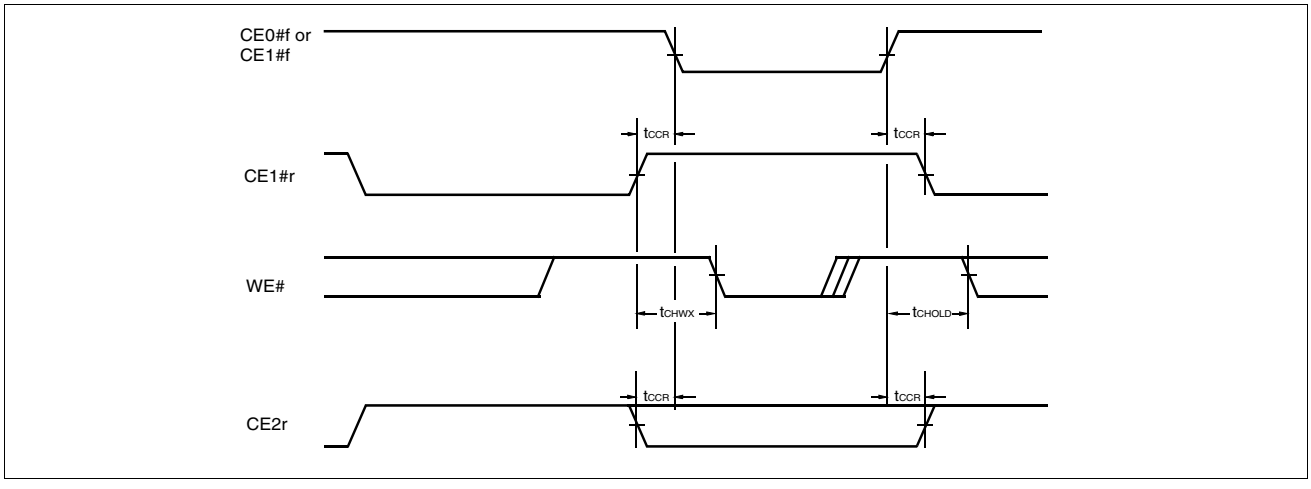
DC Characteristics

Electrical Characteristics (AC Characteristics)

CE# TIMING

Parameter	Symbol		Condition	Value		Unit
	JEDEC	Standard		Min.	Max.	
CE# Recover Time	—	t_{CCR}	—	0	—	ns
CE# Hold Time	—	t_{CHOLD}	—	3	—	ns
CE1#r High to WE Invalid time for Standby Entry	—	t_{CHWX}	—	10	—	ns

TIMING DIAGRAM FOR ALTERNATING RAM TO FLASH



- **Flash Characteristics**
  - Please refer to S29PL127J/S29PL129J specification on the S29PL032J/S29PL064J/S29PL127J/S29PL129J datasheet.
- **PSRAM Characteristics**
  - Please refer to "32Mb pSRAM (Supplier 1)" on page 14.

BGA Pin Capacitance

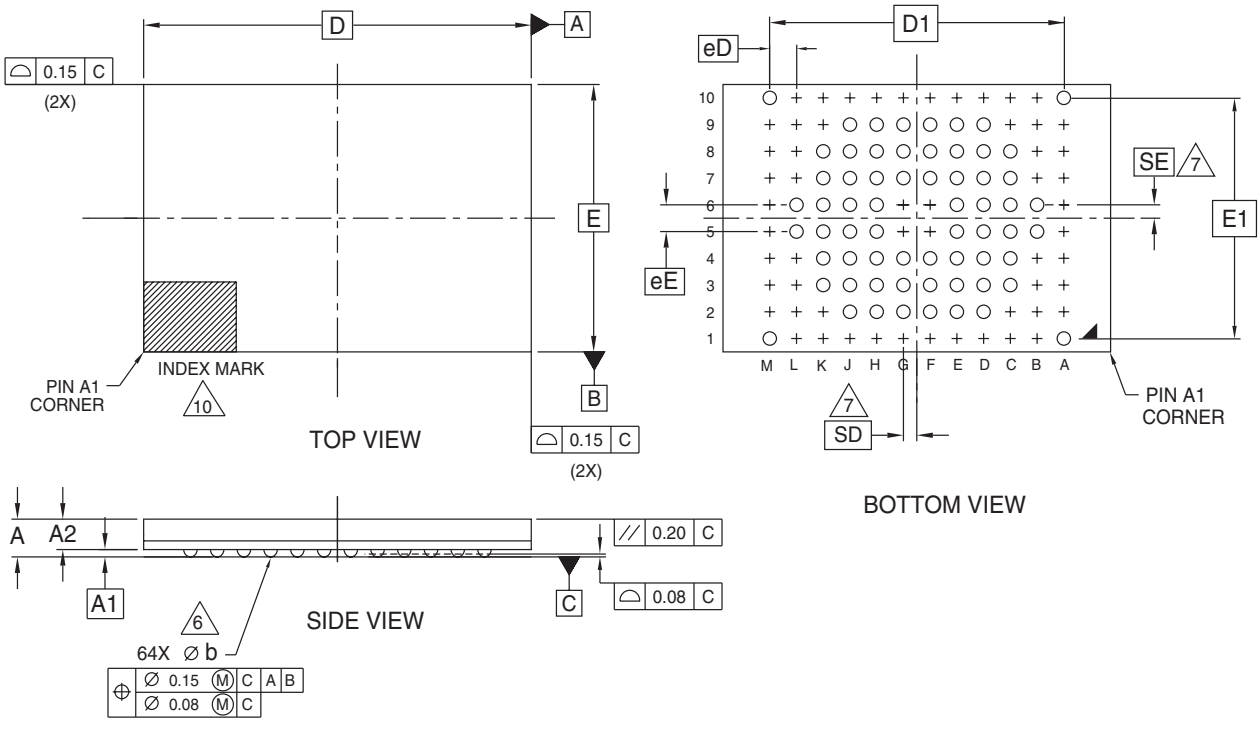
Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	tbd	tbd	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	tbd	tbd	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	tbd	tbd	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

Physical Dimensions

TLA064—64-ball Fine-Pitch Ball Grid Array (FBGA)
8 x 11.6 mm Package



PACKAGE	TLA 064			
JEDEC	N/A			
D x E	11.60 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		11.60 BSC.		BODY SIZE
E		8.00 BSC.		BODY SIZE
D1		8.80 BSC.		MATRIX FOOTPRINT
E1		7.20 BSC.		MATRIX FOOTPRINT
MD		12		MATRIX SIZE D DIRECTION
ME		10		MATRIX SIZE E DIRECTION
n		64		BALL COUNT
ϕb	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9 B1,B2,B3,B4,B7,B8,B9,B10 C1,C2,C9,C10,D1,D10,E1,E10, F1,F5,F6,F10,G1,G5,G6,G10 H1,H10,J1,J10,K1,K2,K9,K10 L1,L2,L3,L4,L7,L8,L9,L10 M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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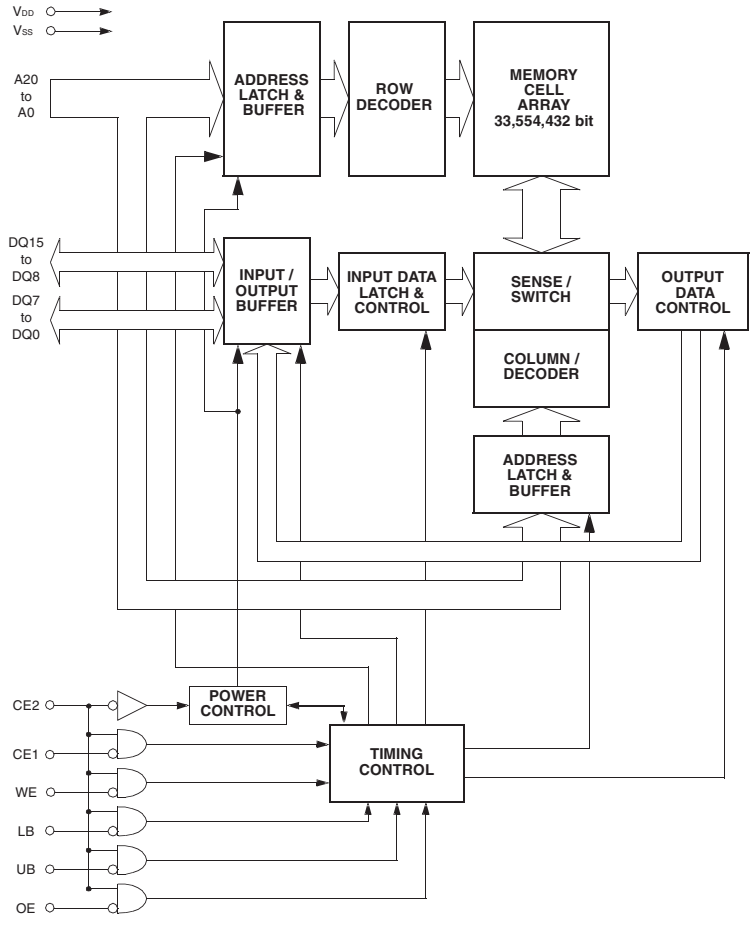
32Mb pSRAM (Supplier I)

32Mb (2 M word x 16 bit)
CMOS 2,097,152 x 16 BIT

pSRAM Block Diagram



Function Truth Table

Mode	CE2	CE1#	WE#	OE#	LB#	UB#	A20-0	DQ7-0	DQ15-8
Standby (Deselect)	H	H	X	X	X	X	X	High-Z	High-Z
Output Disable (Note 1)	H	L	H	H	H	X	(Note 3)	High-Z	High-Z
Output Disable (No Read)			H	L	H	H	Valid	High-Z	High-Z
Read (Upper Byte)					H	L	Valid	High-Z	Output Valid
Read (Lower Byte)					L	H	Valid	Output Valid	High-Z
Read (Word)					L	L	Valid	Output Valid	Output Valid
No Write			L	H (Note 4)	H	H	Valid	Invalid	Invalid
Write (Upper Byte)					H	L	Valid	Invalid	Input Valid
Write (Lower Byte)					L	H	Valid	Input Valid	Invalid
Write (Word)					L	L	Valid	Input Valid	Input Valid
Power Down (Note 2)	L	X	X		X	X	X	High-Z	High-Z

Note:

1. *Should not be kept this logic condition longer than 1 μs.*
2. *Power Down mode can be entered from Standby state and all DQ pins are in High-Z state. Data retention depends on the selection of Power Down Program. Refer to Power down for details.*
3. *Can be either V_{IL} or V_{IH} but must be valid for read or write.*
4. *OE# can be VIL during Write operation if the following conditions are satisfied; Write pulse is initiated by CE1# (refer to CE1# Controlled Write timing), or cycle time of the previous operation cycle is satisfied, OE stays during Write cycle.*

Power Down

Power Down

The Power Down is to enter low power idle state when CE2 stays Low. The pSRAM has two power down modes, Deep Sleep 4M Partial and 8M Partial. These can be programmed by series of read/write operation. See the following table for mode features.

Mode	Data Retention	Retention Address
Sleep (default)	No	N/A
4M Partial	4M bit	00000h to 3FFFFh
8M Partial	8M bit	00000h to 7FFFFh

The default state is Sleep and it is the lowest power consumption but all data will be lost once CE2 is brought to Low for Power Down. It is not required to program to Sleep mode after power-up.

Power Down Program Sequence

The program requires total 6 read/write operation with unique address and data. Between each read/write operation requires that device be in standby mode. The following table shows the detail sequence.

Cycle#	Operation	Address	Data
1st	Read	1FFFFFh (MSB)	Read Data (RDa)
2nd	Write	1FFFFFh	RDa
3rd	Write	1FFFFFh	RDa
4th	Write	1FFFFFh	Don't Care (X)
5th	Write	1FFFFFh	X
6th	Read	Address Key	Read Data (RDb)

The first cycle is to read from most significant address (MSB). The second and third cycle are to write back the data (RDa) read by first cycle. If the second or third cycle is written into the different address, the program is cancelled and the data written by the second or third cycle is valid as a normal write operation. The fourth and fifth cycle is to write to MSB. The data of fourth and fifth cycle is don't care. If the fourth or fifth cycle is written into different address, the program is also cancelled but write data may not be wrote as normal write operation. The last cycle is to read from specific address key for mode selection. Once this program sequence is performed from a Partial mode, the write data may be lost. So, it should perform this program prior to regular read/write operation if Partial mode is used.

Address Key

The address key has the following format.

Mode	Address			
	A20	A19	A18-A0	Binary
Sleep (default)	1	1	1	1FFFFFh
4M Partial	1	0	1	17FFFFh
8M Partial	0	1	1	07FFFFh

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{DD}	2.7	3.1	V
	V_{SS}	0	0	V
High Level Input Voltage	V_{IH}	0.8 V_{DD}	V_{DD} + 0.2 and ≤+3.6	V
	V_{IH}	0.8 V_{DD}	V_{DD} + 0.2	V
Low Level Input Voltage	V_{IL}	-0.3	0.2 V_{DD}	V
Ambient Temperature	T_A	–25	85	°C

Notes:

1. *Maximum DC voltage on input and I/O pins are V_{DD} + 0.2 V. During voltage transitions, inputs may positive overshoot to V_{DD} + 1.0 V for periods of up to 5 ns.*
2. *Minimum DC voltage on input or I/O pins are -0.3 V. During voltage transitions, inputs may negative overshoot V_{SS} to -1.0 V for periods of up to 5 ns.*

pSRAM DC Characteristics

Parameter	Symbol	Test Conditions		Min.	Max.	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{DD}		-1.0	+1.0	µA
Output Leakage Current	I_{LO}	$V_{OUT} = V_{SS}$ to V_{DD}, Output Disable		-1.0	+1.0	µA
Output High Voltage Level	V_{OH}	$V_{DD} = V_{DD}$(min), I_{OH} = –0.5mA		2.4	–	V
Output Low Voltage Level	V_{OL}	I_{OL} = 1 mA		–	0.4	V
V_{DD} Power Down Current	I_{DDPS}	$V_{DD} = V_{DD}$ max., $V_{IN} = V_{IH}$ or V_{IL}, CE2 ≤ 0.2V	SLEEP	–	10	µA
	I_{DDP8}		8M Partial	–	50	µA
V_{DD} Standby Current	I_{DDS}	$V_{DD} = V_{DD}$ max., $V_{IN} = V_{IH}$ or V_{IL}, CE1#		–	1.5	mA
	I_{DDS1}	$V_{DD} = V_{DD}$ max., $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{DD} - 0.2$ V, CE1# =CE2 ≥ VDD – 0.2V		–	80	µA
V_{DD} Active Current	I_{DDA1}	$V_{DD} = V_{DD}$ max., $V_{IN} = V_{IH}$ or V_{IL}, CE1# = V_{IL} and CE2 = V_{IH}, I_{OUT} = 0 mA	t_{RC}/t_{WC} = minimum	–	30	mA
	I_{DDA2}		t_{RC}/t_{WC} = 1 µs	–	3	mA
V_{DD} Page Read Current	I_{DDA3}	$V_{DD} = V_{DD}$ max., $V_{IN} = V_{IH}$ or V_{IL}, CE1# = V_{IL} and CE2 = V_{IH}, I_{OUT} = 0 mA, t_{PRC} = min.		–	10	mA

Notes:

1. *All voltages are referenced to V_{SS}.*
2. *DC Characteristics are measured after following POWER-UP timing.*
3. *I_{OUT} depends on the output load conditions.*

pSRAM AC Characteristics

Read Operation

Parameter	Symbol	Value		Unit
		Min.	Max.	
Read Cycle Time (Notes 1, 2)	t_{RC}	65	1000	ns
CE1# Access Time (Note 3)	t_{CE}	–	65	ns
OE# Access Time (Note 3)	t_{OE}	–	40	ns
Address Access Time (Notes 3,5)	t_{AA}	–	65	ns
LB#/UB# Access Time (Note 3)	t_{BA}	–	30	ns
Page Address Access Time (Notes 3,6)	t_{PAA}	–	20	ns
Page Read Cycle Time (Notes 1,6,7)	t_{PRC}	25	1000	ns
Output Data Hold Time (Note 3)	t_{OH}	5	–	ns
CE1# Low to Output Low-Z (Note 4)	t_{CLZ}	5	–	ns
OE# Low to Output Low-Z (Note 4)	t_{OLZ}	0	–	ns
LB#/UB# Low to Output High-Z (Note 4)	t_{BLZ}	0	–	ns
CE1# High to Output High-Z (Note 3)	t_{CHZ}	–	20	ns
OE# High to Output High-Z (Note 3)	t_{OHZ}	–	20	ns

Parameter	Symbol	Value		Unit
		Min.	Max.	
LB#/UB# High to Output High-Z (Note 3)	t_{BHZ}	–	20	ns
Address Setup Time to CE1# Low	t_{ASC}	-5	–	ns
Address Setup Time to OE# Low	t_{ASO}	10	–	ns
Address Invalid Time (Notes 5,8)	t_{AX}	–		ns
Address Hold Time from CE1# High (Note 9)	t_{CHAH}	-5	–	ns
Address Hold Time from OE# High	t_{OHAH}	-5	–	ns
CE1# High Pulse Width	t_{CP}	12	–	ns

Notes:

1. *Maximum value is applicable if CE1# is kept at Low without change of address input of A3 to A20.*
2. *Address should not be changed within minimum $t_{RC.}$*
3. *The output load 50pF.*
4. *The output load 5pF.*
5. *Applicable to A3 to A20 when CE1# is kept at Low.*
6. *Applicable only to A0, A1 and A2 when CE1# is kept at Low for the page address access.*
7. *In case Page Read Cycle is continued with keeping CE1# stays Low, CE1# must be brought to High within 4 μs. In other words, Page Read Cycle must be closed within 4 μs.*
8. *Applicable when at least two of address inputs among applicable are switched from previous state.*
9. *t_{RC} (min) and t_{PRC} (min) must be satisfied.*

PSRAM AC Characteristics

Write Operation

Parameter	Symbol	Value		Unit
		Min.	Max.	
Write Cycle Time (Notes 1, 2)	t_{WC}	65	1000	ns
Address Setup Time (Note 3)	t_{AS}	0	–	ns
CE1# Write Pulse Width (Note 3)	t_{CW}	40	–	ns
WE# Write Pulse Width (Note 3)	t_{WP}	40	–	ns
LB#/UB# Write Pulse Width (Note 3)	t_{BW}	40	–	ns
LB#/UB# Byte Mask Setup Time (Note 4)	t_{BS}	-5	–	ns
LB#/UB# Byte Mask Hold Time (Note 5)	t_{BH}	-5	–	ns
CE1# Write Recovery Time (Note 6)	t_{WRC}	12	–	ns
WE# Write Recovery Time (Note 6)	t_{WR}	7.5	1000	ns
LB#/UB# Write Recovery Time (Note 6)	t_{BR}	12	1000	ns
Data Setup Time	t_{DS}	12	–	ns
Data Hold Time	t_{DH}	0	–	ns
OE# High to CE1# Low Setup Time for Write (Note 7)	t_{OHCL}	-5	–	ns
OE# High to Address Setup Time for Write (Note 8)	t_{OES}	0	–	ns
WE#/UB#/LB# High to OE# Low Setup Time for Read (Note 10)	t_{WHOL}	12	–	10
LB# and UB# Write Pulse Overlap	t_{BWO}	30	–	ns
CE1# High Pulse Width	t_{CP}	12	–	ns
Address Hold Time for Write End (Note (Note 3)	t_{AH}	0	–	ns

Notes:

1. *Maximum value is applicable if CE1# is kept at Low without any address change.*
2. *Minimum value must be equal or greater than the sum of write pulse (t_{CW}, T_{WP}, T_{BW}) and write recovery time (t_{WCR}, T_{WR} or t_{BR}).*
3. *Write pulse is defined from High to Low transition of CE1#, WE#, or LB#/UB#, whichever occurs last.*
4. *Applicable for byte mask only. Byte mask setup time is defined to the High to Low transition of CE1# or WE# whichever occurs last.*
5. *Applicable for byte mask only. Byte mask hold time is defined from the Low to High transition of CE1# or WE# whichever occurs first.*
6. *Write recovery is defined from Low to High transition of CE1#, WE#, or LB#/UB#, whichever occurs first.*
7. *If OE# is Low after minimum t_{OHCL}, read cycle is initiated. In other words, OE# must be brought to High within 5 ns after CE1# is brought to Low. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met*
8. *If OE# is Low after new address input, read cycle is initiated. In other words, OE# must be brought to High at the same time or before new address valid. Once read cycle is initiated, new write pulse should be input*

after minimum t_{RC} is met and data bus is in High-Z

9. *Absolute minimum values and defined at minimum V_{IH} level.*
10. *If the actual value of t_{WHOL} is shorter than the specified minimum values, the actual t_{AA} of following Read may become longer by the amount of subtracting the actual value from the specified minimum value.*

AC Characteristics

Power Down Parameters

Parameter	Symbol	Value		Unit
		Min.	Max.	
CE2 Low Setup Time for Power Down Entry	t_{CSP}	10	–	ns
CE2 Low Hold Time after Power Down Entry	t_{C2LP}	65	–	ns
CE1# High Hold Time following CE2 High after Power Down Exit (SLEEP mode only) (Note 1)	t_{CHH}	300	–	µs
CE1# High Hold Time following CE2 High after Power Down Exit (not in SLEEP mode) (Note 2)	t_{CHHP}	1	–	µs
CE1# High Setup Time following CE2 High after Power Down Exit (Note 1)	t_{CHS}	0	–	ns

Notes:

1. *Applicable also to power up.*
2. *Applicable when 8M Partial mode is programmed.*

Other Timing Parameters

Parameter	Symbol	Value		Unit
		Min.	Max.	
CE#1 High to OE# Invalid Time for Standby Entry	t_{CHOX}	10	-	ns
CE#1 High to WE# Invalid Time for Standby Entry (Note 1)	t_{CHWX}	10	-	ns
CE2 Low Hold Time after Power up	t_{C2LH}	50	–	µs
CE1# High Hold Time following CE2 High after Power up	t_{CHH}	300	–	µs
Input Transition Time (Note 2)	t_T	1	25	ns

Notes:

1. *Some data might be written into any address location if t_{CHWX} (min) is not satisfied*
2. *The Input Transition Time (t_T) at AC testing is 5ns, as shown in AC Test Conditions below.. If actual t_T is longer than 5ns, it may violate AC specification of some timing parameters.*

AC Characteristics

AC Test Conditions

Symbol	Description	Test Setup	15, 11	Unit
V_{IH}	Input High Level		V_{DD} * 0.8	V
V_{IL}	Input Low Level		V_{DD} * 0.2	V
V_{REF}	Input Timing Measurement Level		V_{DD} * 0.5	V
t_T	Input Transition Time	Between V_{IL} and V_{IH}	5	ns

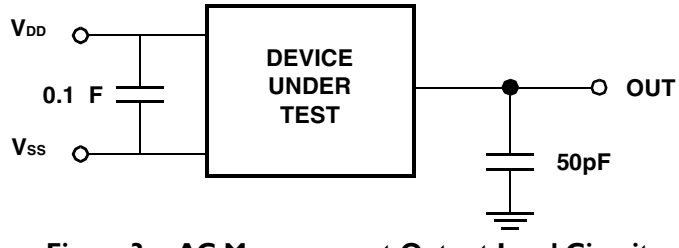
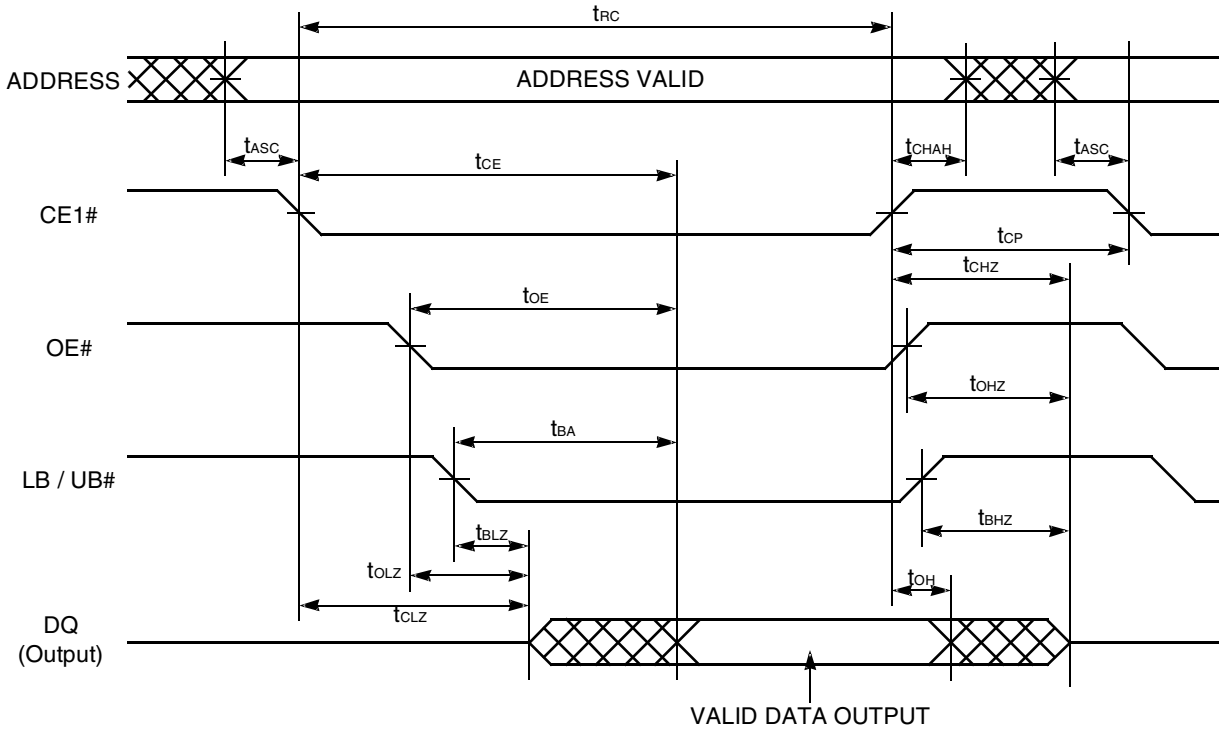


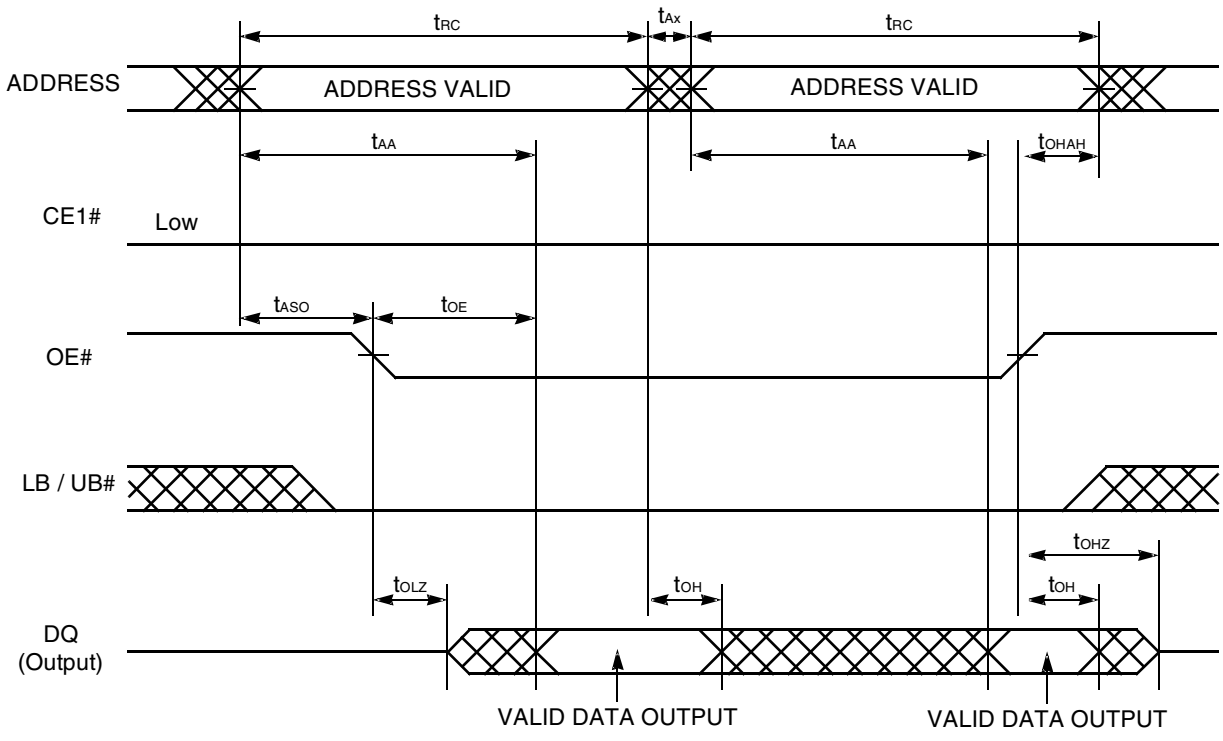
Figure 3. AC Measurement Output Load Circuit

Timing Diagrams



Note: *CE2 and WE# must be High for entire read cycle.*

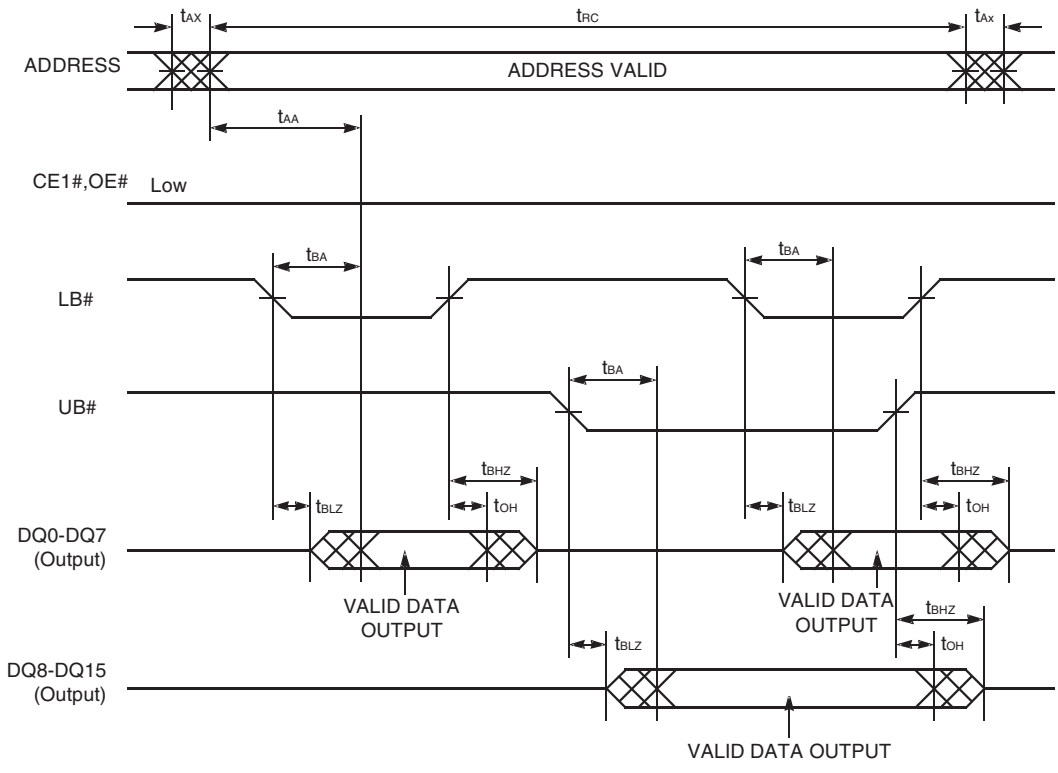
Figure 4. Read TIming #I (Basic Timing)



Note: *CE2 and WE# must be High for entire read cycle.*

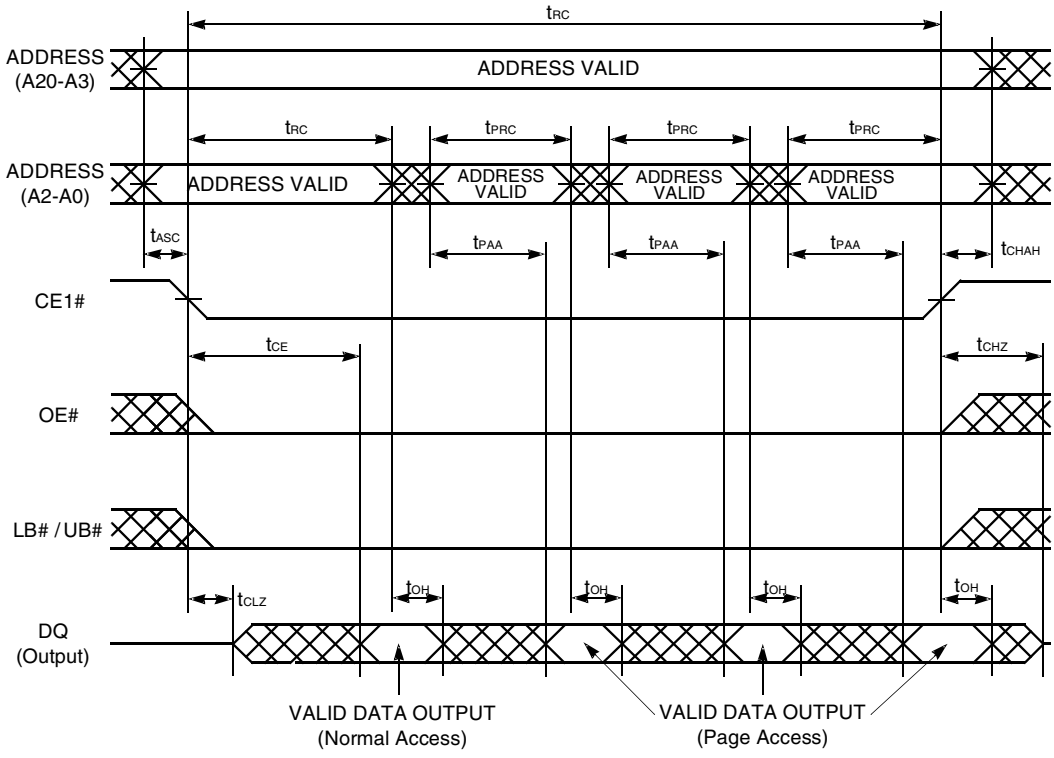
Figure 5. Read Timing #2 (OE# and Address Access)

Timing Diagrams



Note: *CE2 and WE# must be High for entire read cycle.*

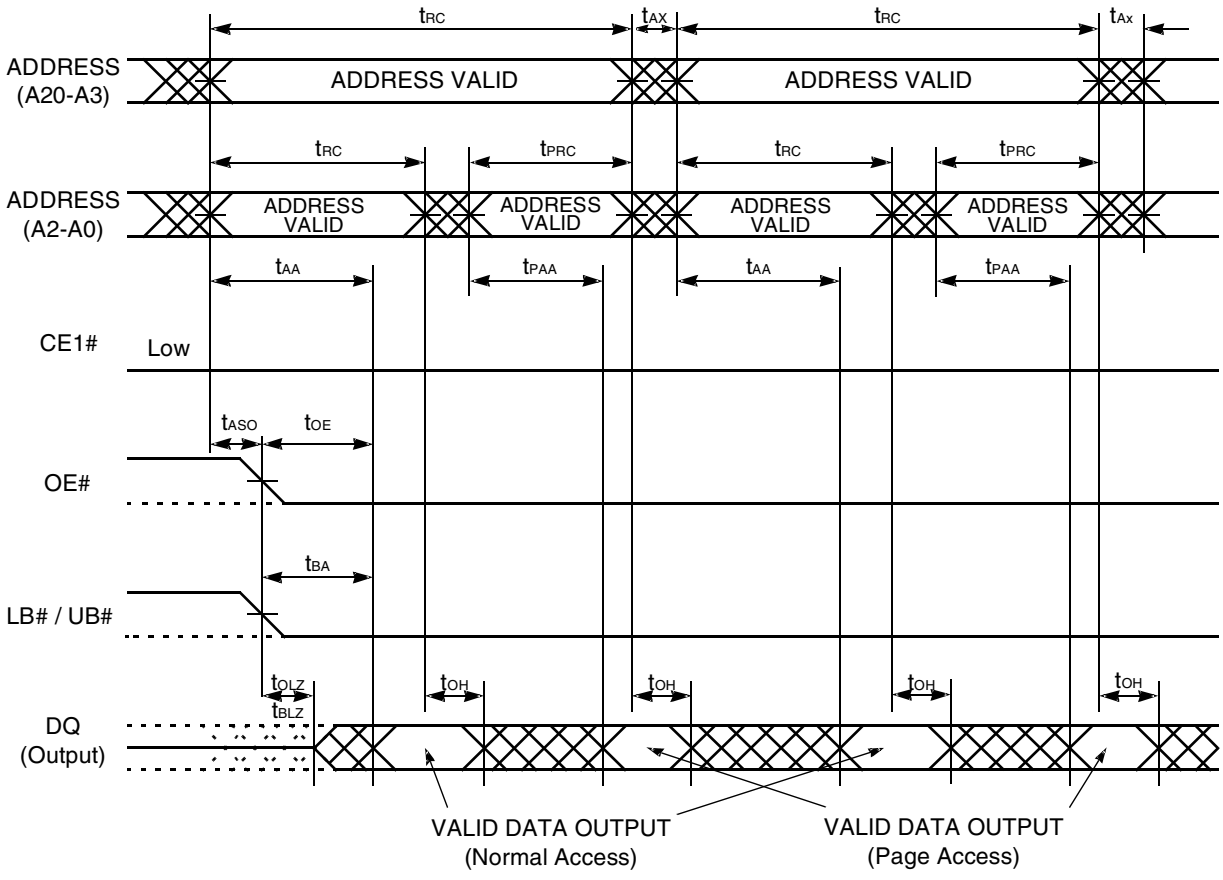
Figure 6. Read Timing #3 (LB#/UB# Byte Access)



Note: *CE2 and WE# must be High for entire read cycle.*

Figure 7. Read Timing #4 (Page Access after CEI# Control Access)

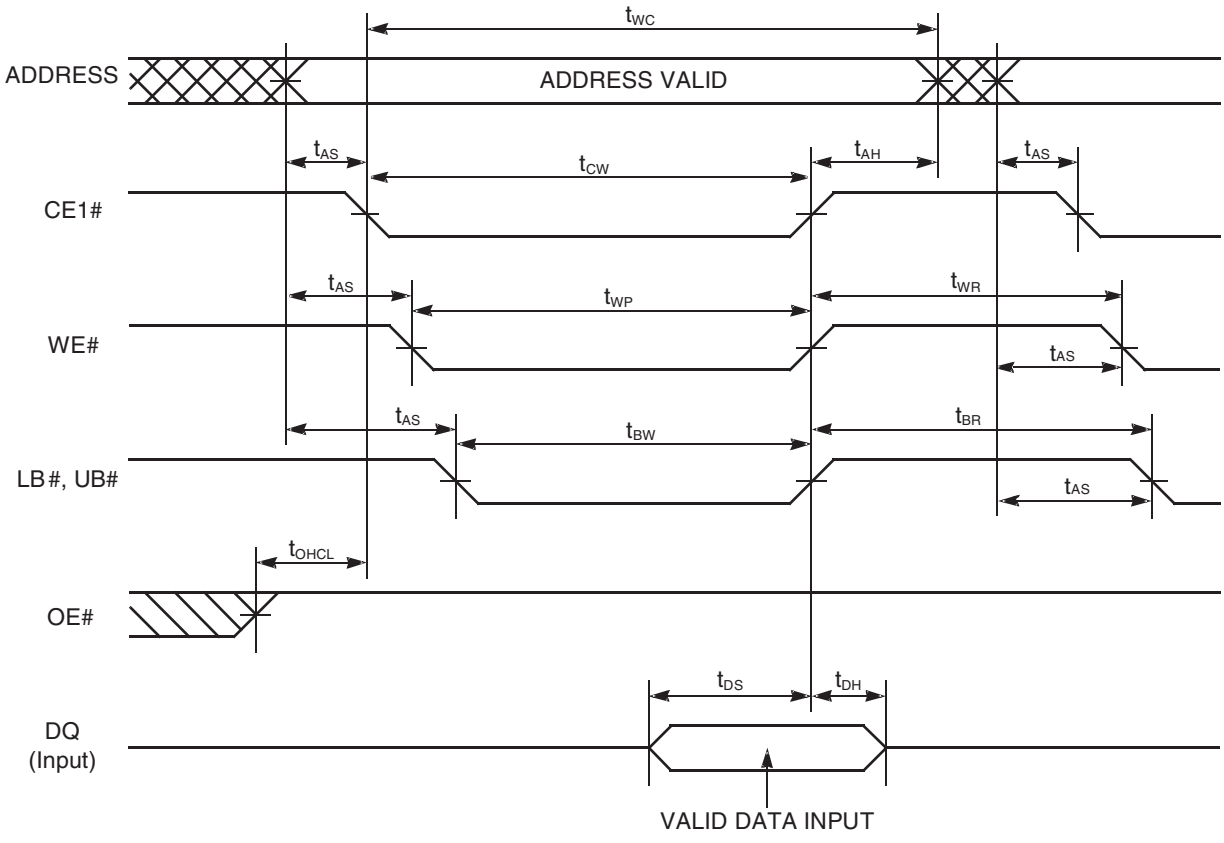
Timing Diagrams



Note: *CE2 and WE# must be High for entire read cycle. Either or both LB# and UB# must be Low when both CE1# and OE# are Low.*

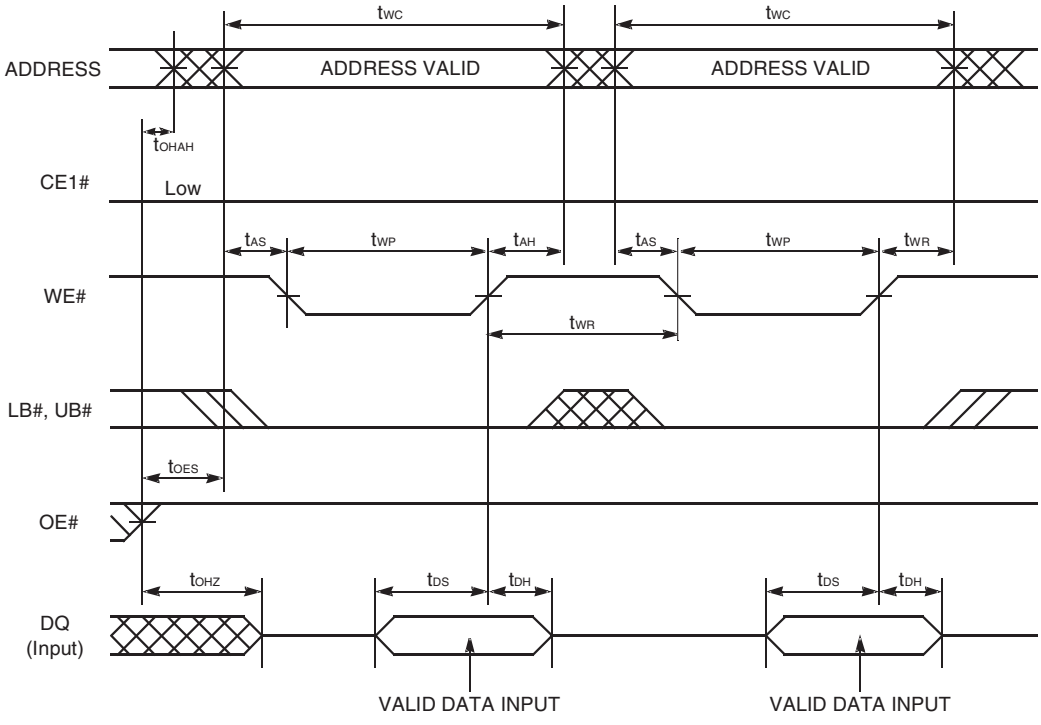
Figure 8. Read Timing #5 (Random and Page Address Access)

Timing Diagrams



Note: *CE2 must be High for Write Cycle.*

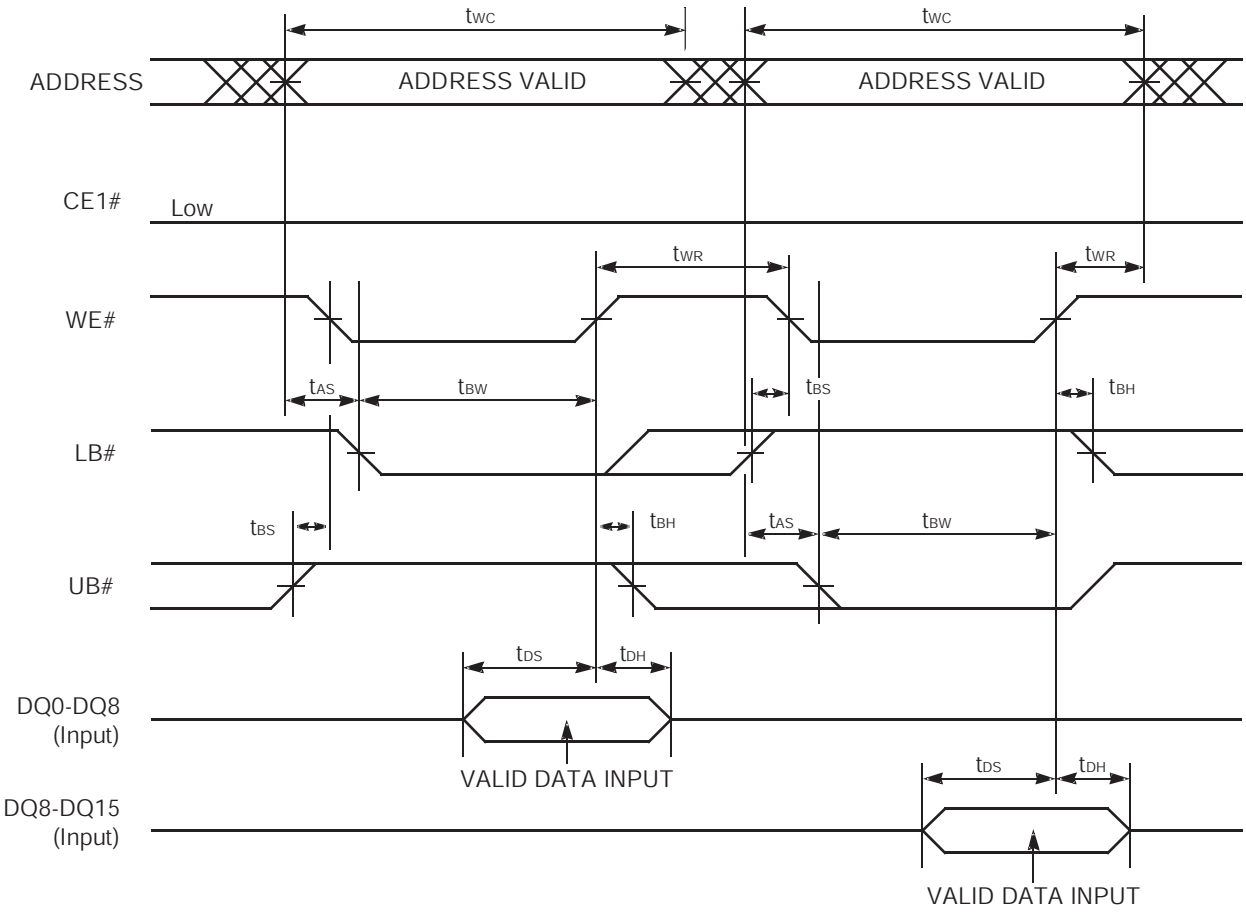
Figure 9. Write Timing #I (Basic Timing)



Note: *CE2 must be High for Write Cycle.*

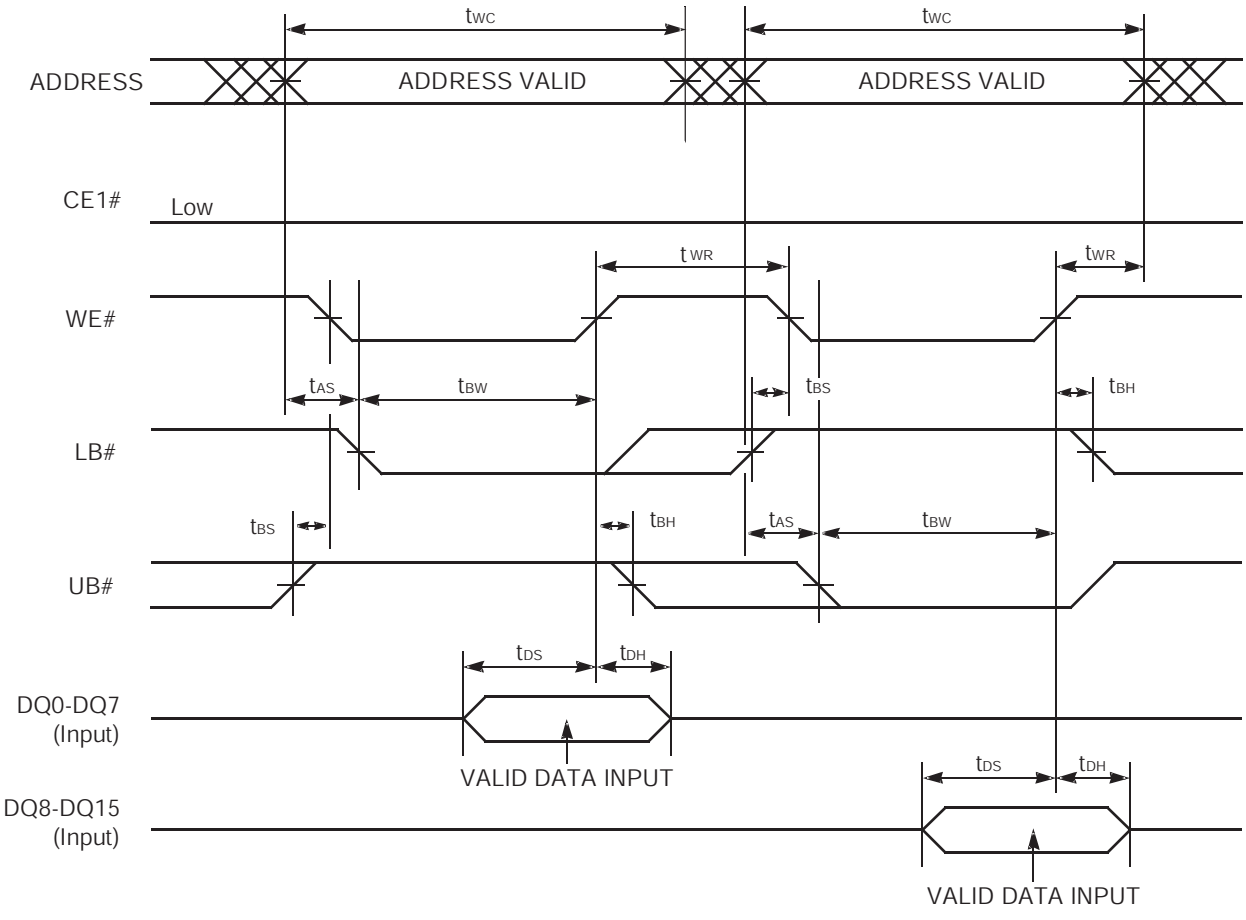
Figure 10. Write Timing #2 (WE# Control)

Timing Diagrams



Note: *CE2 must be High for Write Cycle.*

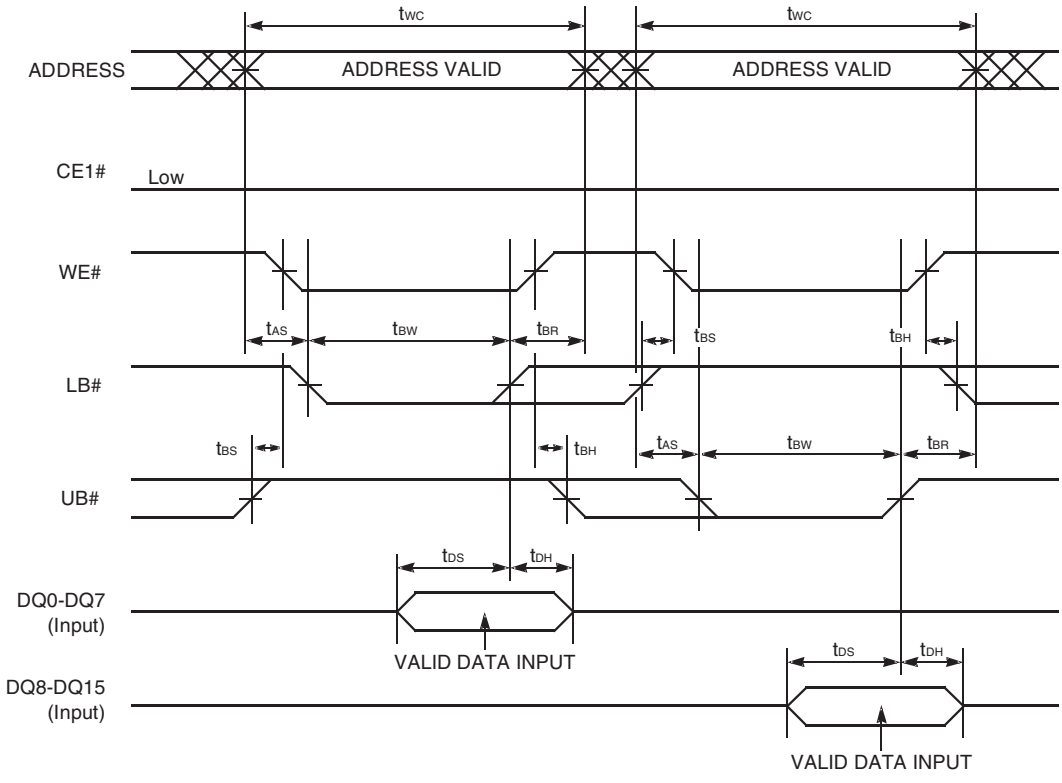
Figure 11. Write Timing #3-1 (WE#/LB#/UB# Byte Write Control)



Note: *CE2 must be High for Write Cycle.*

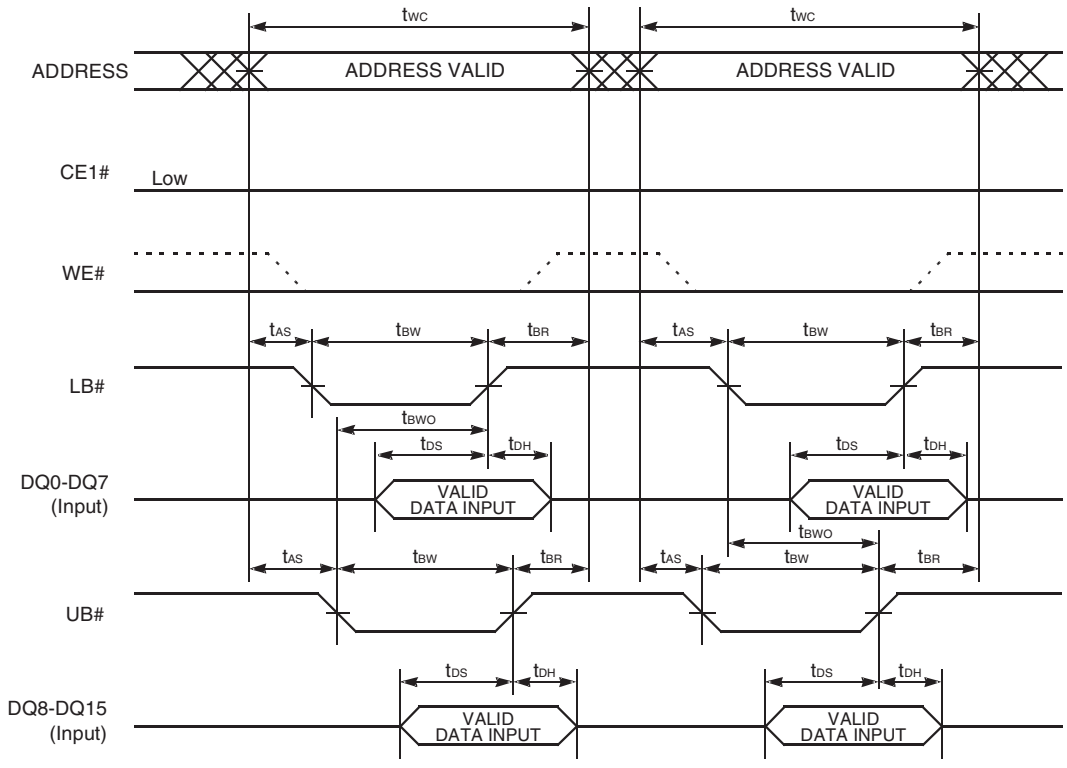
Figure 12. Write Timing #3-2 (WE#/LB#/UB# Byte Write Control)

Timing Diagrams



Note: *CE2 must be High for Write Cycle.*

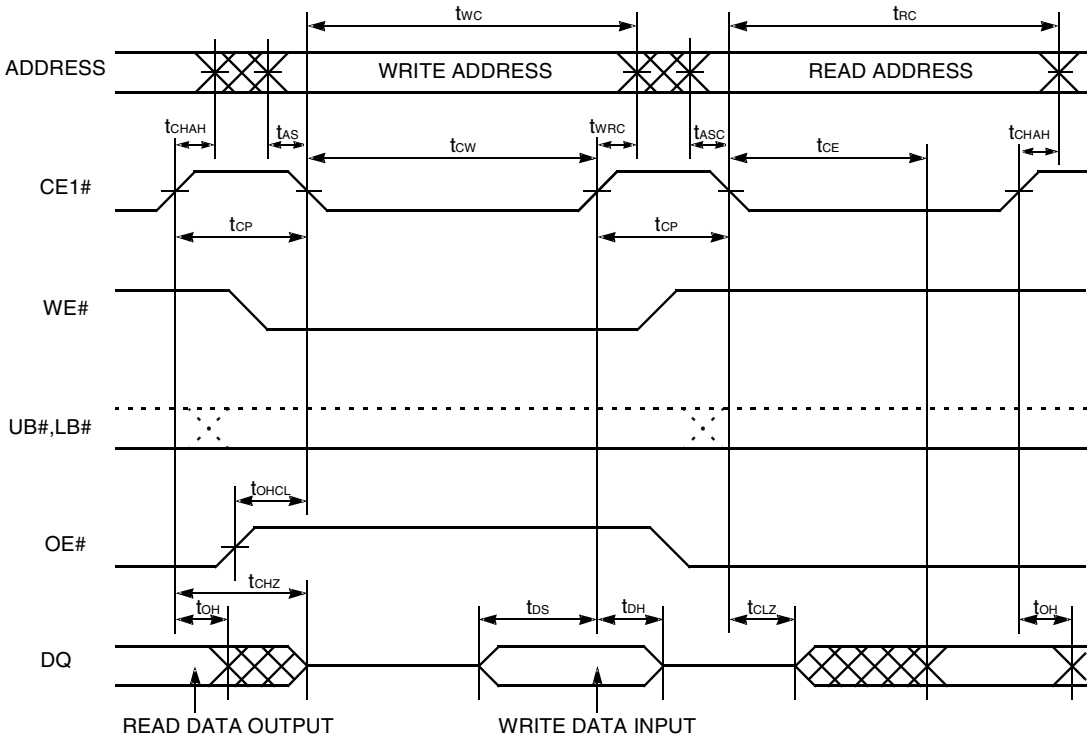
Figure 13. Write Timing #3-3 (WE#/LB#/UB# Byte Write Control)



Note: *CE2 must be High for Write Cycle.*

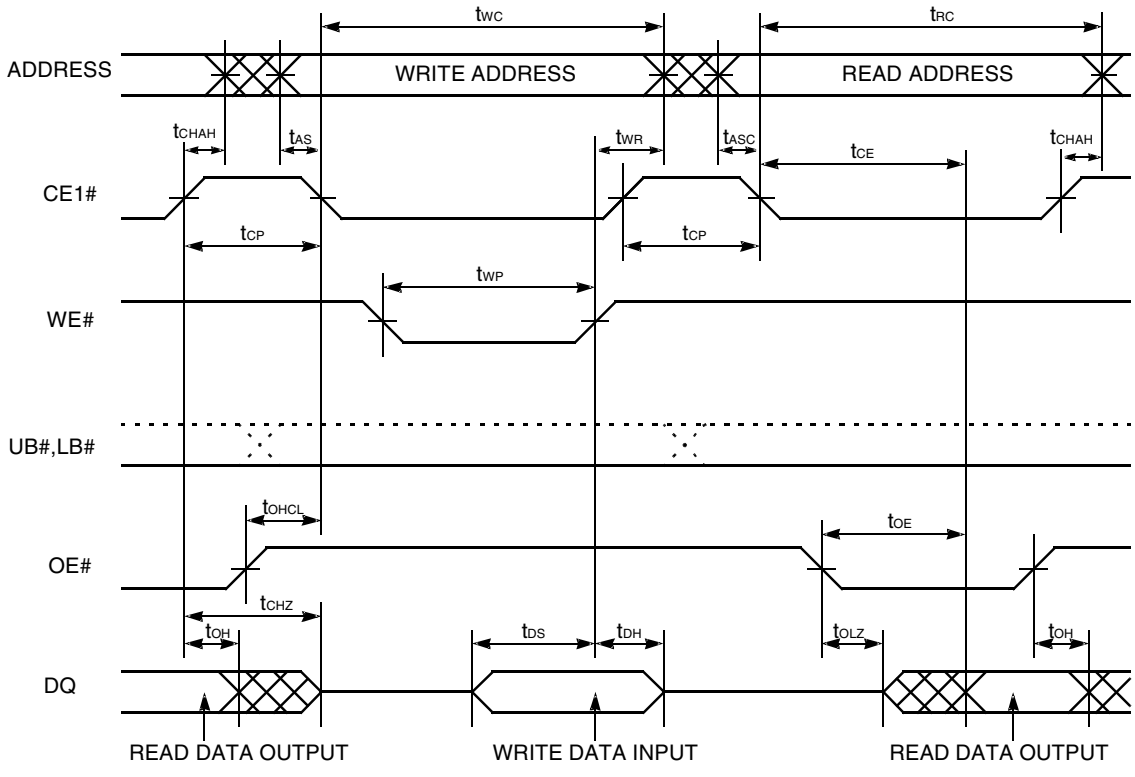
Figure 14. Write Timing #3-4 (WE#/LB#/UB# Byte Write Control)

Timing Diagrams



Note: *Write address is valid from either CE1# or WE# of last falling edge.*

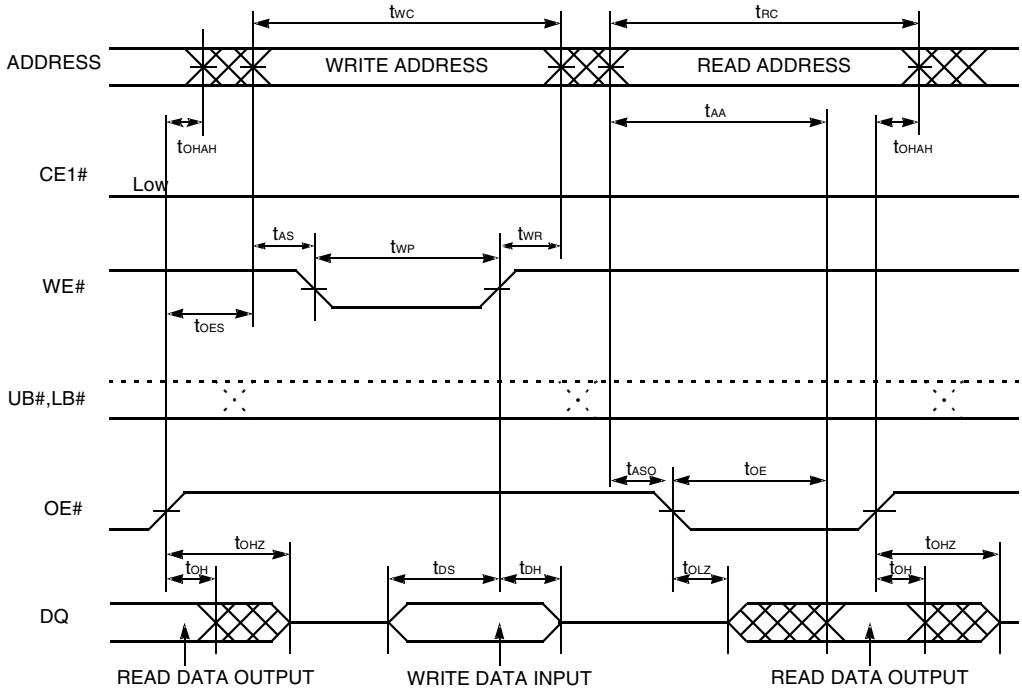
Figure 15. Read/Write Timing #1-1 (CE1# Control)



Note: *OE# can be fixed Low during write operation if it is CE1# controlled write at Read-Write-Read sequence.*

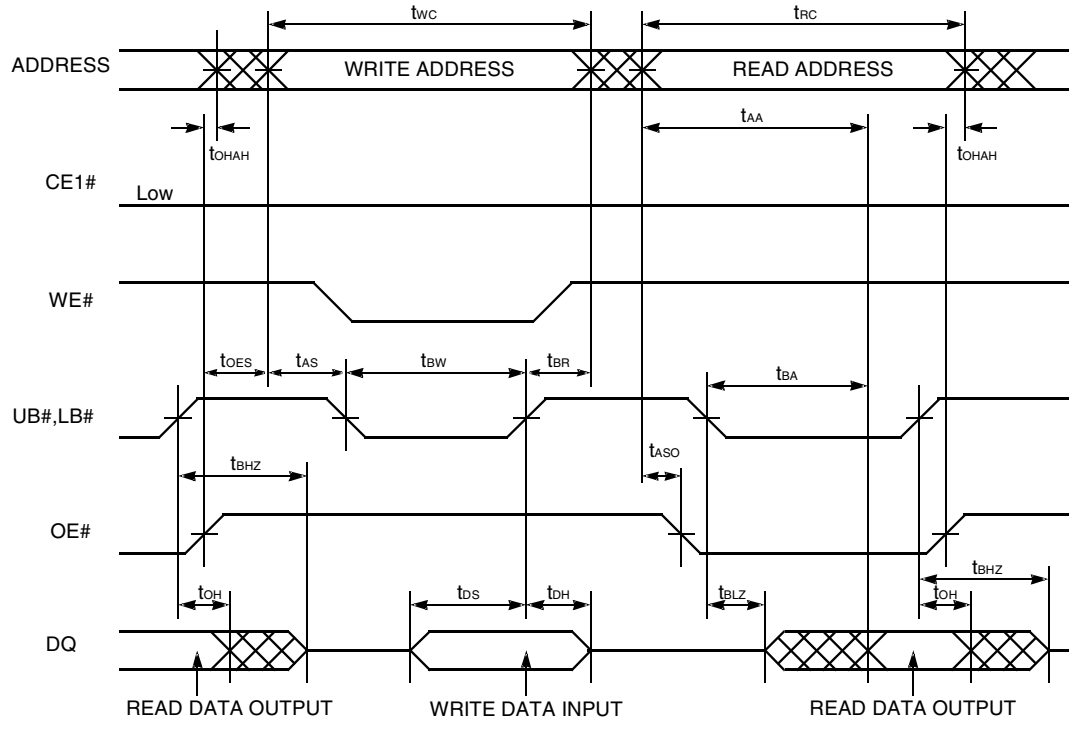
Figure 16. Read/Write Timing #I-2 (CEI#/WE#/OE# Control)

Timing Diagrams



Note: *CE1# can be tied to Low for WE# and OE# controlled operation.*

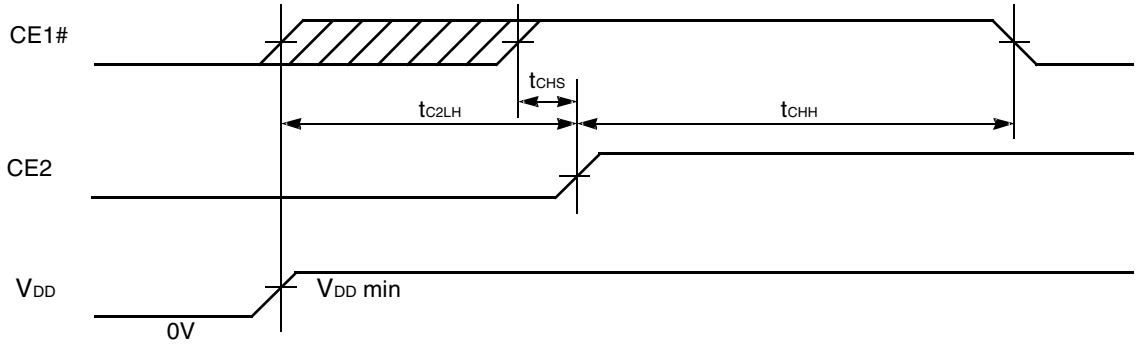
Figure 17. Read/Write Timing #2 (OE#, WE# Control)



Note: *CE#1 can be tied to Low for WE# and OE# controlled operation.*

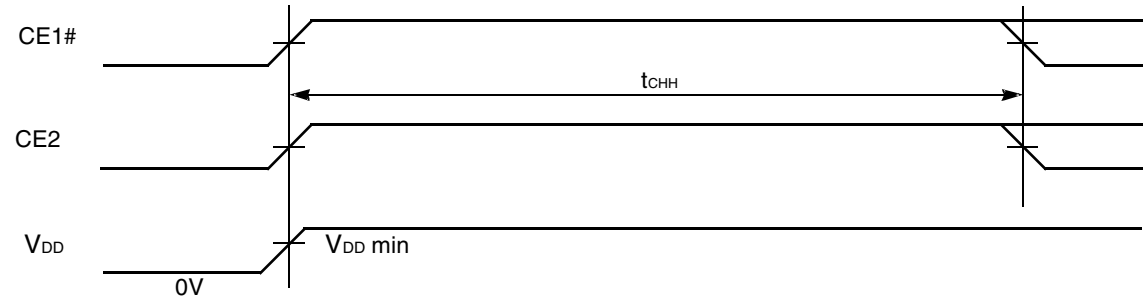
Figure 18. Read/Write Timing #3 (OE#, WE#, LB#, UB# Control)

Timing Diagrams



Note: *The t_{C2LH} specifies after V_{DD} reaches specified minimum level.*

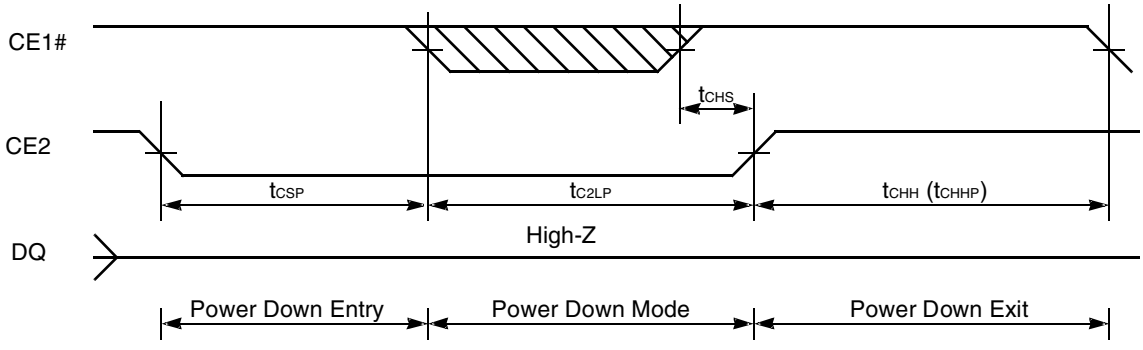
Figure 19. Power-up Timing #I



Note: *The t_{CHH} specifies after V_{DD} reaches specified minimum level and applicable to both CE1# and CE2.*

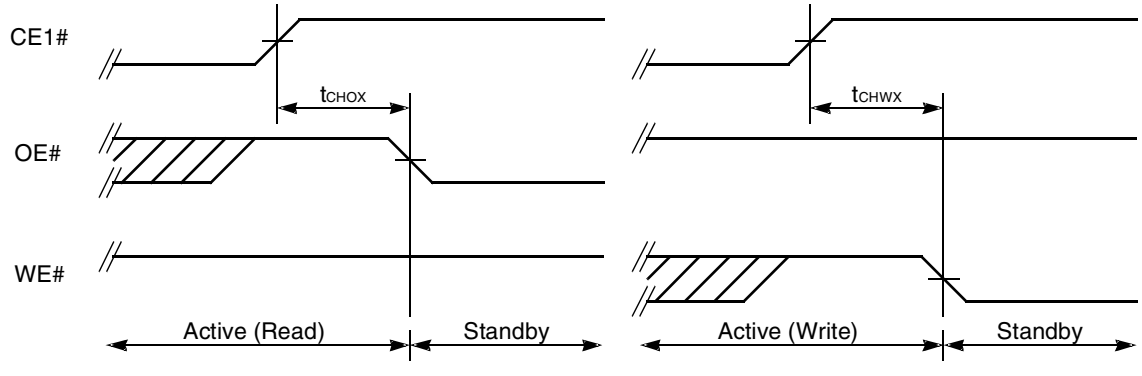
Figure 20. Power-up Timing #2

Timing Diagrams



Note: *This Power Down mode can be also used as a reset timing if Power-up timing above could not be satisfied and Power-Down program was not performed prior to this reset.*

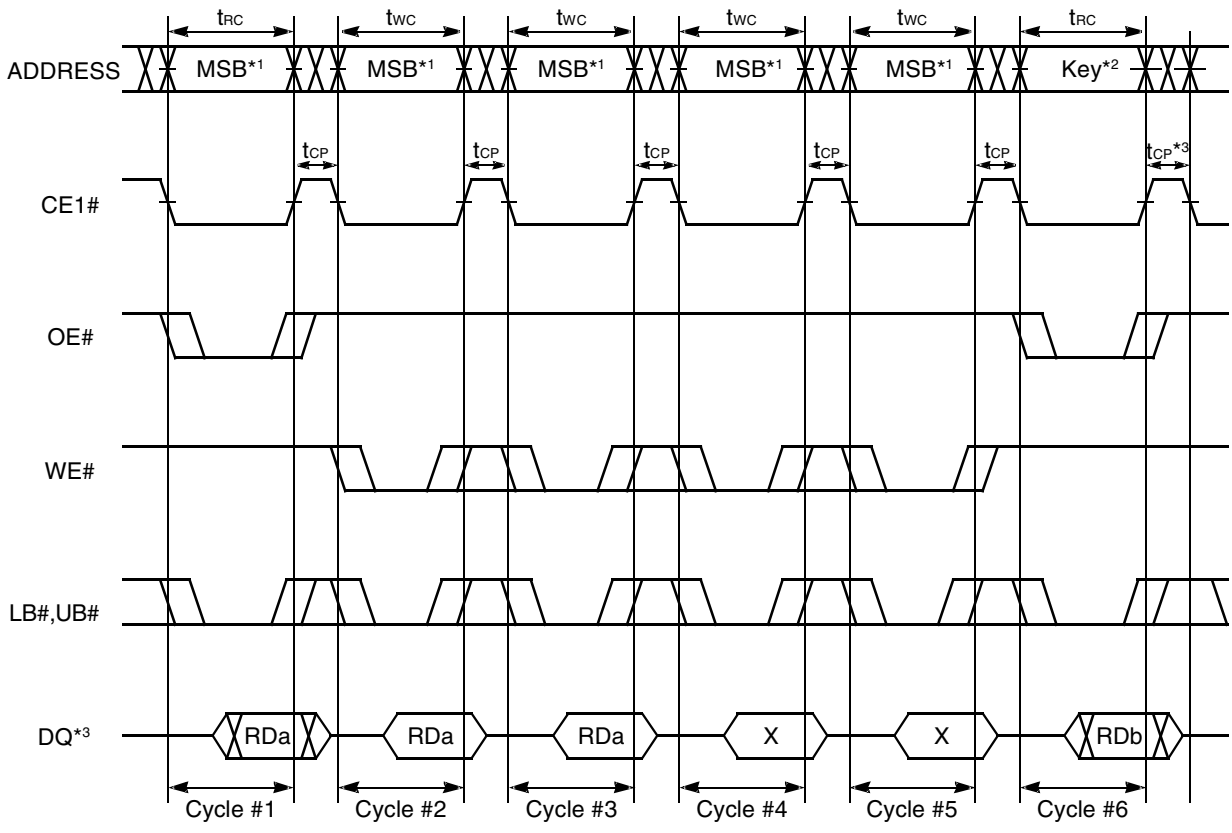
Figure 2I. Power-down Entry and Exit Timing



Note: *Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode. If either of timing is not satisfied, it takes t_{RC} (min) period for standby mode from CE1# Low to High transition.*

Figure 22. Standby Entry Timing after Read or Write

Timing Diagrams



Notes:

1. *The all address inputs must be High from Cycle #1 to #5.*
2. *After t_{CP} following Cycle #6, the Power Down Program is completed and returned to the normal operation.*

Revision Summary

Revision A (April 15, 2004)

Initial release.