FINAL

AmC0XXCFLKA

1, 2, 4, or 10 Megabyte 5.0 V-only Flash Memory PC Card

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - — 150 ns maximum access time
- **Single supply operation**
  - — Write and erase voltage, 5.0 V ±5%
  - — Read voltage, 5.0 V ±5%
- **CMOS low power consumption**
  - — 45 mA maximum active read current (x8 mode)
  - — 65 mA maximum active erase/write current (x8 mode)
- **High write endurance**
  - — Minimum 100,000 erase/write cycles
- **PCMCIA/JEIDA 68-pin standard**
  - — Selectable byte- or word-wide configuration
- **Write protect switch**
  - — Prevents accidental data loss
- **Zero data retention power**
  - — Batteries not required for data storage
- **Separate attribute memory**
  - — 512 byte EEPROM
- **Automated write and erase operations increase system write performance**
  - — 64K byte memory sectors for faster automated erase speed
  - — Typically 1.5 seconds per single memory sector erase
  - — Random address writes to previously erased bytes (16 µs typical per byte)
- **Total system integration solution**
  - — Support from independent software and hardware vendors
- **Low insertion and removal force**
  - — State-of-the-art connector allows for minimum card insertion and removal effort
- **Sector erase suspend/resume**
  - — Suspend the erase operation to allow a read operation in another sector within the same device

GENERAL DESCRIPTION

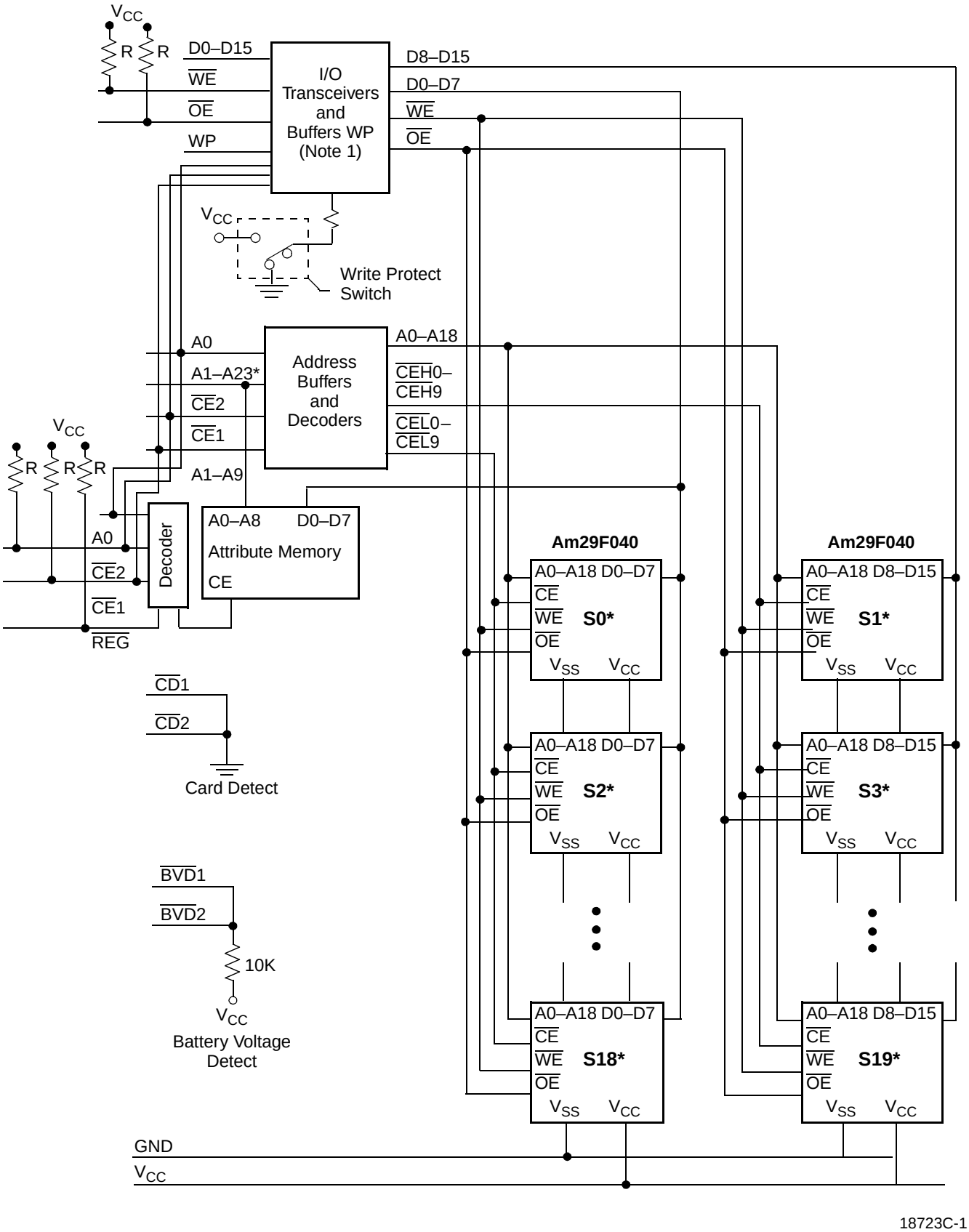
AMD's 5.0 V-only Flash Memory PC Card provides the highest system level performance for data and file storage solutions to the portable PC market segment. Manufactured with AMD's Negative Gate Erase, 5.0 V-only technology, the AMD 5.0 V-only Flash Memory Cards are the most cost-effective and reliable approach to single-supply Flash memory cards. Data files and application programs can be stored on the "C" series cards. This allows OEM manufacturers of portable systems to eliminate the weight, high power consumption and reliability issues associated with electromechanical disk-based systems. The "C" series cards also allow today's bulky and heavy battery packs to be reduced in weight and size. Typically only two "AA" alkaline batteries are required for total system operation. AMD's Flash Memory PC Cards provide the most efficient method to transfer useful work between different hardware platforms. The enabling technology of the "C" series cards enhances the productivity of mobile workers.

Widespread acceptance of the "C" series cards is assured due to their compatibility with the 68-pin PCMCIA/JEIDA international standard. AMD's Flash Memory Cards can be read in either a byte-wide or word-wide mode which allows for flexible integration into various system platforms. Compatibility is assured at the hardware interface and software interchange specification. The Card Information Structure (CIS) or Metaformat, can be written by the OEM at the memory card's attribute memory address space beginning at address 00000H by using a format utility. The CIS appears at the beginning of the Card's attribute memory space and defines the low-level organization of data on the PC Card. The "C" series cards contains a separate 512 byte EEPROM memory for the cards' attribute memory space. This allows all of the Flash memory to be used for the common memory space.

Third party software solutions such as Microsoft's Flash File System (FFS), M-System's True FFS, and SCM's SCM-FFS, enable AMD's Flash Memory PC Card to replicate the function of traditional disk-based memory systems.

Publication# **18723** Rev: **C** Amendment/**+1**
Issue Date: **May 1998**

BLOCK DIAGRAM



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Notes:

R = 20 K(min)/140 KΩ (max)

**1 Mbyte card = S0 + S1, *2 Mbyte card = S0…S3, *4 Mbyte card = S0…S7, *10 Mbyte card = S0…S19*

PC CARD PIN ASSIGNMENTS

Pin#	3	3	Function	Pin#	Signal	I/O	Function
1	GND		Ground	35	GND		Ground
2	D3	I/O	Data Bit 3	36	$\overline{CD}1$	O	Card Detect 1 (Note 3)
3	D4	I/O	Data Bit 4	37	D11	I/O	Data Bit 11
4	D5	I/O	Data Bit 5	38	D12	I/O	Data Bit 12
5	D6	I/O	Data Bit 6	39	D13	I/O	Data Bit 13
6	D7	I/O	Data Bit 7	40	D14	I/O	Data Bit 14
7	$\overline{CE}1$	I	Card Enable 1 (Note 3)	41	D15	I/O	Data Bit 15
8	A10	I	Address Bit 10	42	$\overline{CE}2$	I	Card Enable 2 (Note 3)
9	$\overline{OE}$	I	Output Enable	43	NC		No Connect
10	A11	I	Address Bit 11	44	NC		No Connect
11	A9	I	Address Bit 9	45	NC		No Connect
12	A8	I	Address Bit 8	46	A17	I	Address Bit 17
13	A13	I	Address Bit 13	47	A18	I	Address Bit 18
14	A14	I	Address Bit 14	48	A19	I	Address Bit 19 (Note 4)
15	$\overline{WE}$	I	Write Enable	49	A20	I	Address Bit 20 (Note 5)
16	NC		No Connect	50	A21	I	Address Bit 21 (Note 6)
17	V_{CC1}		Power Supply	51	V_{CC2}		Power Supply
18	NC		No Connect (Note 1)	52	NC		No Connect (Note 1)
19	A16	I	Address Bit 16	53	A22	I	Address Bit 22
20	A15	I	Address Bit 15	54	A23	I	Address Bit 23 (Note 7)
21	A12	I	Address Bit 12	55	NC		No Connect
22	A7	I	Address Bit 7	56	NC		No Connect
23	A6	I	Address Bit 6	57	NC		No Connect
24	A5	I	Address Bit 5	58	NC		No Connect
25	A4	I	Address Bit 4	59	NC		No Connect
26	A3	I	Address Bit 3	60	NC		No Connect
27	A2	I	Address Bit 2	61	$\overline{REG}$	I	Register Select
28	A1	I	Address Bit 1	62	$\overline{BVD}2$	O	Battery Voltage Detect 2 (Note 2)
29	A0	I	Address Bit 0	63	$\overline{BVD}1$	O	Battery Voltage Detect 1 (Note 2)
30	D0	I/O	Data Bit 0	64	D8	I/O	Data Bit 8
31	D1	I/O	Data Bit 1	65	D9	I/O	Data Bit 9
32	D2	I/O	Data Bit 2	66	D10	I/O	Data Bit 10
33	WP	O	Write Protect (Note 3)	67	$\overline{CD}2$	O	Card Detect 2 (Note 3)
34	GND		Ground	68	GND		Ground

Notes:

I = Input to card, O = Output from card

I/O = Bidirectional

NC = No connect

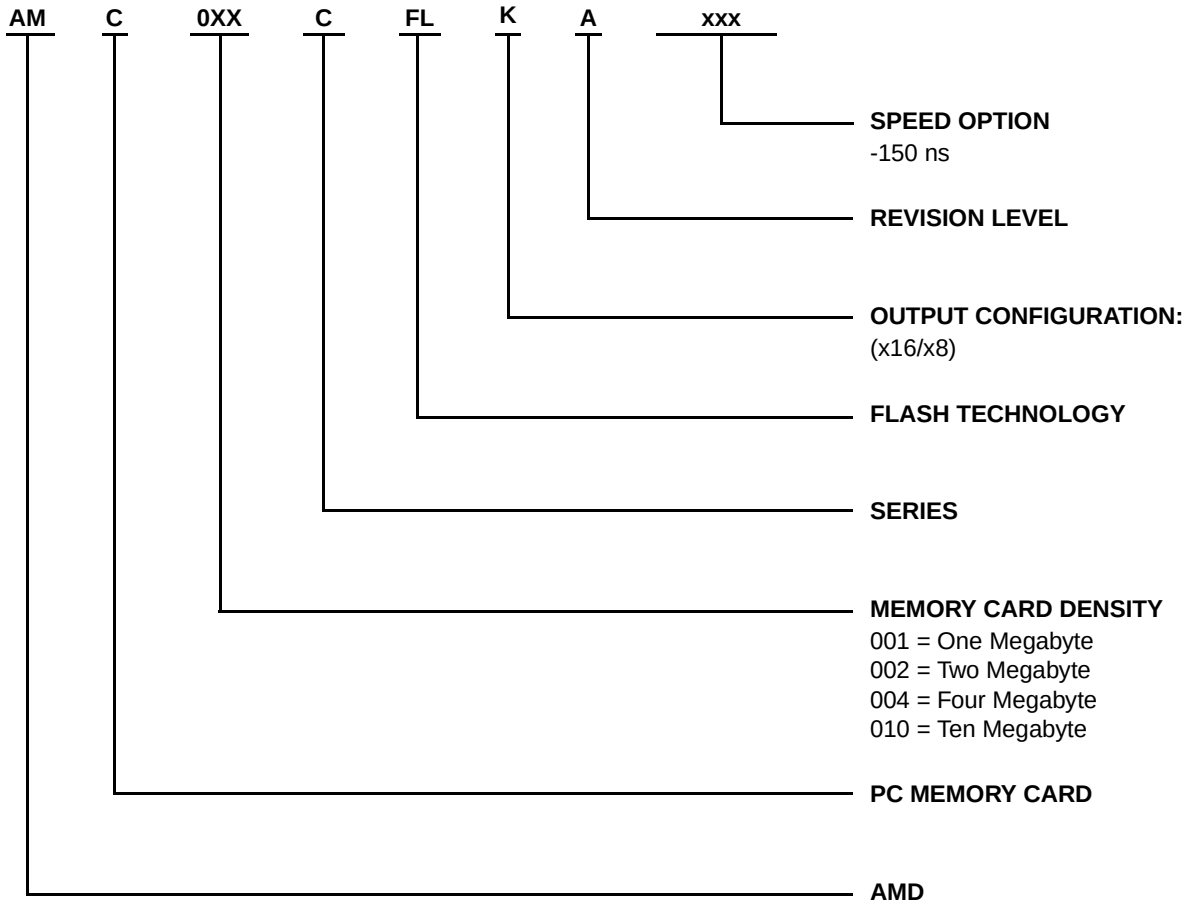
In systems which switch V_{CC} individually to cards, no signal should be directly connected between cards other than ground.

1. *V_{PP} not required for Programming or Reading operations.*
2. *$\overline{BVD}$ = Internally pulled-up.*
3. *Signal must not be connected between cards.*
4. *Highest address bit for 1 Mbyte card.*
5. *Highest address bit for 2 Mbyte card.*
6. *Highest address bit for 4 Mbyte card.*
7. *Highest address bit for 10 Mbyte card.*

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



PIN DESCRIPTION

A0–A23

Address Inputs

These inputs are internally latched during write cycles.

$\overline{BVD1}$, $\overline{BVD2}$

Battery Voltage Detect

Internally pulled-up.

$\overline{CD1}$, $\overline{CD2}$

Card Detect

When card detect 1 and 2 = ground the system detects the card.

$\overline{CE1}$, $\overline{CE2}$

Card Enable

This input is active low. The memory card is deselected and power consumption is reduced to standby levels when $\overline{CE}$ is high. $\overline{CE}$ activates the internal memory card circuitry that controls the high and low byte control logic of the card, input buffers segment decoders, and associated memory devices.

D0–D15

Data Input/Output

Data inputs are internally latched on write cycles. Data outputs during read cycles. Data pins are active high. When the memory card is deselected or the outputs are disabled the outputs float to tristate.

GND

Ground

NC

No Connect

Corresponding pin is not connected internally to the die.

$\overline{OE}$

Output Enable

This input is active low and enables the data buffers through the card outputs during read cycles.

$\overline{REG}$

Attribute Memory Select

This input is active low and enables reading the CIS from the EEPROM.

V_{CC}

PC Card Power Supply

For device operation (5.0 V ± 5%).

$\overline{WE}$

Write Enable

This input is active low and controls the write function of the command register to the memory array. The target address is latched on the falling edge of the $\overline{WE}$ pulse and the appropriate data is latched on the rising edge of the pulse.

WP

Write Protect

This output is active high and disables all card write operations.

MEMORY CARD OPERATIONS

The “C” series Flash Memory Card is organized as an array of individual devices. Each device is 512K bytes in size with eight 64K byte sectors. Although the address space is continuous each physical device defines a logical address segment size.

Byte-wide erase operations could be performed in four ways:

- In increments of the segment size
- In increments of the sectors in individual segments
- All eight sectors in parallel within individual segments
- Selected sectors of the eight sectors in parallel within individual segments

Multiple segments may be erased concurrently when additional I_{CC} current is supplied to the device. Once a memory sector or memory segment is erased any address location may be programmed. Flash technology allows any logical “1” data bit to be programmed to a logical “0”. The only way to reset bits to a logical “1” is to erase the entire memory sector of 64K bytes or memory segment of 512K bytes.

Erase operations are the only operations that work on entire memory sectors or memory segments. All other operations such as word-wide programming are not affected by the physical memory segments.

The common memory space data contents are altered in a similar manner as writing to individual Flash memory devices. On-card address and data buffers activate the appropriate Flash device in the memory array. Each device internally latches address and data during write cycles. Refer to Table 1.

Attribute memory is a separately accessed card memory space. The register memory space is active when the $\overline{REG}$ pin is driven low. The Card Information Structure (CIS) describes the capabilities and specification of a card. The CIS is stored in the attribute memory space beginning at address 00000H. The “C” series cards contain a separate 512 byte EEPROM memory for the Card Information Structure. D0–D7 are active during attribute memory accesses. D8–D15 should be ignored. Odd order bytes present invalid data. Refer to Table 2.

Word-Wide Operations

The “C” series cards provide the flexibility to operate on data in a byte-wide or word-wide format. In word-wide operations the Low-bytes are controlled with $\overline{CE}1$ when A0 = 0. The High-bytes are controlled with $\overline{CE}2$ with A0 = don’t care.

Table 1. Common Memory Bus Operations

Pins/Operation	$\overline{REG}$	$\overline{CE}2$	$\overline{CE}1$	$\overline{OE}$	$\overline{WE}$	A0	D8–D15	D0–D7
READ-ONLY								
Read (x8) (Note 6)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	High-Z	Data Out-Even
Read (x8) (Note 7)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	High-Z	Data Out-Odd
Read (x8) (Note 8)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	Data Out-Odd	High-Z
Read (x16) (Note 9)	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	Data Out-Odd	Data Out-Even
Output Disable	V_{IH}	X	X	V_{IH}	V_{IH}	X	High-Z	High-Z
Standby (Note 3)	X	V_{IH}	V_{IH}	X	X	X	High-Z	High-Z
READ/WRITE								
Read (x8) (Notes 2, 6)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	High-Z	Data Out-Even
Read (x8) (Notes 2, 7)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	High-Z	Data Out-Odd
Read (x8) (Notes 2, 8)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	Data Out-Odd	High-Z
Read (x16) (Notes 2, 9)	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	Data Out-Odd	Data Out-Even
Write (x8) (Notes 4, 6)	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	High-Z	Data In-Even
Write (x8) (Notes 4, 7)	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	High-Z	Data In-Odd
Write (x8) (Notes 4, 8)	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	Data In-Odd	High-Z
Write (x16) (Notes 5, 9)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	Data In-Odd	Data In-Even
Output Disable	V_{IH}	X	X	V_{IH}	V_{IL}	X	High-Z	High-Z
Standby (Note 3)	X	V_{IH}	V_{IH}	X	X	X	High-Z	High-Z

Legend:

X = Don’t Care, where Don’t Care is either at V_{IL} or V_{IH} level. See DC Characteristics for voltage levels of normal TTL or CMOS input levels.

Notes:

Volt-only?

1. *V_{PP} pins are not connected in the 5.0 V-Only Flash Memory Card.*
2. *Manufacturer and device codes may be accessed via a command register write sequence. (Refer to Autoselect Command in Tables 3 and 4.)*
3. *Standby current is I_{CCS}.*
4. *Refer to Tables 3 and 4 for valid D_{IN} during a byte write operation.*
5. *Refer to Table 5 for valid D_{IN} during a word write operation.*
6. *Byte access—Even. In this x8 mode, A0 = V_{IL} outputs or inputs the “even” byte (low byte) of the x16 word on D0–D7.*
7. *Byte access—Odd. In this x8 mode, A0 = V_{IH} outputs or inputs the “odd” byte (high byte) of the x16 word on D0–D7. This is accomplished internal to the card by transposing D8–D15 to D0–D7.*
8. *Odd byte only access. In this x8 mode, A0 = X outputs or inputs the “odd” byte (high byte) of the x16 word on D8–D15.*
9. *x16 word accesses present both “even” (low) and “odd” (high) bytes. A0 = X.*

Table 2. Attribute Memory Bus Operations

Pins/Operation	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	$\overline{OE}$	$\overline{WE}$	A0	D8–D15	D0–D7
READ-ONLY								
Read (x8) (Notes 2, 4)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	High-Z	Data Out-Even
Read (x8) (Notes 3, 4)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	High-Z	Not Valid
Read (x8) (Note 3)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	Not Valid	High-Z
Read (x16) (Notes 3, 4, 5)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	Not Valid	Data Out-Even
Output Disable	V_{IL}	X	X	V_{IH}	V_{IH}	X	High-Z	High-Z
Standby (Note 6)	X	V_{IH}	V_{IH}	X	X	X	High-Z	High-Z
READ/WRITE								
Read (x8) (Notes 2, 4)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	High-Z	Data Out-Even
Read (x8) (Notes 3, 4)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	High-Z	Not Valid
Read (x8) (Note 4)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	Not Valid	High-Z
Read (x16) (Note 4)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	Not Valid	Data Out-Even
Write (x8) (Notes 2, 5)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	High-Z	Data In-Even
Write (x8) (Note 5)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	High-Z	High-Z
Write (x8) (Notes 4, 5)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	High-Z	High-Z
Write (x16) (Note 5)	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	High-Z	Data In-Even
Output Disable	V_{IL}	X	X	V_{IH}	V_{IL}	X	High-Z	High-Z
Standby (Note 6)	X	V_{IH}	V_{IH}	X	X	X	High-Z	High-Z

Legend:

X = Don't Care, where Don't Care is either V_{IL} or V_{IH} levels. See DC Characteristics for voltage levels of normal TTL or CMOS input levels.

Notes:

Volt-only?

1. *V_{PP} pins are not connected in the 5.0 V-Only Flash Memory Card.*
2. *In this x8 mode, A0 = V_{IL} outputs or inputs the "even" byte (low byte) of the x16 word on D0–D7.*
3. *Only even-byte data is valid during Attribute Memory Read function.*
4. *During Attribute Memory Read function, $\overline{REG}$ and $\overline{OE}$ must be active for the entire cycle.*
5. *During Attribute Memory Write function, $\overline{REG}$ and $\overline{WE}$ must be active for the entire cycle, $\overline{OE}$ must be inactive for the entire cycle.*
6. *Standby current is I_{CCS}.*

Byte-Wide Operations

Byte-wide data is available on D0–D7 for read and write operations ($\overline{CE}1$ = low, $\overline{CE}2$ = high). Even and odd bytes are stored in separate memory segments (i.e., S0 and S1) and are accessed when A0 is low and high respectively. The even byte is the low order byte and the odd byte is the high order byte of a 16-bit word.

Erase operations in the byte-wide mode must account for data multiplexing on D0–D7 by changing the state of A0. Each memory sector or memory segment pair must be addressed separately for erase operations.

Card Detection

Each $\overline{CD}$ (output) pin should be read by the host system to determine if the memory card is adequately seated in the socket. $\overline{CD}1$ and $\overline{CD}2$ are internally tied to ground. If both bits are not detected, the system should indicate that the card must be reinserted.

Write Protection

The AMD Flash memory card has three types of write protection. The PCMCIA/JEIDA socket itself provides the first type of write protection. Power supply and control pins have specific pin lengths in order to protect the card with proper power supply sequencing in the case of hot insertion and removal.

A mechanical write protect switch provides a second type of write protection. When this switch is activated, $\overline{WE}$ is internally forced high. The Flash memory command register is disabled from accepting any write commands.

The third type of write protection is achieved with V_{CC1} and V_{CC2} below V_{LKO}. Each Flash memory device that comprises a Flash memory segment will reset the command register to the read-only mode when V_{CC} is below V_{LKO}. V_{LKO} is the voltage below which write operations to individual command registers are disabled.

MEMORY CARD BUS OPERATIONS

Read Enable

Two Card Enable ($\overline{CE}$) pins are available on the memory card. Both $\overline{CE}$ pins must be active low for word-wide read accesses. Only one $\overline{CE}$ is required for byte-wide accesses. The $\overline{CE}$ pins control the selection and gates power to the high and low memory segments. The Output Enable ($\overline{OE}$) controls gating accessed data from the memory segment outputs.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Output Disable

Data outputs from the card are disabled when $\overline{OE}$ is at a logic-high level. Under this condition, outputs are in the high-impedance state.

Standby Operations

Byte-wide read accesses only require half of the read/write output buffer (x16) to be active. In addition, only one memory segment is active within either the high order or low order bank. Activation of the appropriate half of the output buffer is controlled by the combination of both $\overline{CE}$ pins. The $\overline{CE}$ pins also control power to the high and low-order banks of memory. Outputs of the memory bank not selected are placed in the high impedance state. The individual memory segment is activated by the address decoders. The other memory segments operate in standby. An active memory segment continues to draw power until completion of a write or erase operation if the card is deselected in the process of one of these operations.

Auto Select Operation

A host system or external card reader/writer can determine the on-card manufacturer and device I.D. codes. Codes are available after writing the 90H command to the command register of a memory segment per Tables 3 and 4. Reading from address location 00000H in any segment provides the manufacturer I.D. while address location 00002H provides the device I.D.

To terminate the Auto Select operation, it is necessary to write the Read/Reset command sequence into the register.

Write Operations

Write and erase operations are valid only when V_{CC1} and V_{CC2} are above 4.75 V. This activates the state machine of an addressed memory segment. The command register is a latch which saves address, commands, and data information used by the state machine and memory array.

When Write Enable ($\overline{WE}$) and appropriate $\overline{CE}$(s) are at a logic-level low, and Output Enable ($\overline{OE}$) is at a logic-high, the command register is enabled for write operations. The falling edge of $\overline{WE}$ latches address information and the rising edge latches data/command information.

Write or erase operations are performed by writing appropriate data patterns to the command register of accessed Flash memory sectors or memory segments.

The byte-wide and word-wide commands are defined in Tables 3, 4, and 5, respectively.

Table 3. Even Byte Command Definitions (Note 5)

Embedded Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data
Reset/Read	4	AAAAH	AAH	5554H	55H	AAAAH	F0H	RA	RD				
Autoselect	4	AAAAH	AAH	5554H	55H	AAAAH	90H	00H/02H	01H/A4H				
Byte Write	4	AAAAH	AAH	5554H	55H	AAAAH	A0H	PA	PD				
Segment Erase	6	AAAAH	AAH	5554H	55H	AAAAH	80H	AAAAH	AAH	5554H	55H	AAAAH	10H
Sector Erase	6	AAAAH	AAH	5554H	55H	AAAAH	80H	AAAAH	AAH	5554H	55H	SA	30H
Sector Erase Suspend		Erase can be suspended during sector erase with Addr (don't care), Data (B0H)											
Sector Erase Resume		Erase can be resumed after suspend with Addr (don't care), Data (30H)											

** Address for Memory Segment 0 (S0) only. Address for the higher even memory segments (S2–S18) = (Addr) + (N/2)* 100000H where N = Memory Segment number (0) for 1 Mbyte, N = (0, 2) for 2 Mbyte, N = (0, 2, 4, 6) for 4 Mbyte, N = (0…18) for 10 Mbyte.*

Notes:

1. *Address bit A16 = X = Don't Care for all address commands except for Program Address (PA), Read Address (RA) and Sector Address (SA).*
2. *Bus operations are defined in Table 1.*
3. *RA = Address of the memory location to be read.*
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   SA = Address of the sector to be erased. The combination of A17, A18, A19 will uniquely select any sector of a segment.
   To select the memory segment:1 and 2 Mbyte: Use $\overline{CE}$1 and A20
   4 Mbyte: Use $\overline{CE}$1 and A20, A21
   10 Mbyte: Use $\overline{CE}$1 and A20–A23.
4. *RD = Data read from location RA during read operation.*
   PD = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$ pulse.
5. *A0 = 0 and $\overline{CE}$1 = 0*

Table 4. Odd Byte Command Definitions (Note 5)

Embedded Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data
Reset/Read	4	AAABH	AAH	5555H	55H	AAABH	F0H	RA	RD				
Autoselect	4	AAABH	AAH	5555H	55H	AAABH	90H	00H/02H	01H/A4H				
Byte Write	4	AAABH	AAH	5555H	55H	AAABH	A0H	PA	PD				
Segment Erase	6	AAABH	AAH	5555H	55H	AAABH	80H	AAABH	AAH	5555H	55H	AAABH	10H
Sector Erase	6	AAABH	AAH	5555H	55H	AAABH	80H	AAABH	AAH	5555H	55H	SA	30H
Sector Erase Suspend		Erase can be suspended during sector erase with Addr (don't care), Data (B0H)											
Sector Erase Resume		Erase can be resumed after suspend with Addr (don't care), Data (30H)											

**Address for Memory Segment 1 (S1) only. Address for the higher odd memory segments (S3–S19) = (Addr) + ((N–1)/2)* 100000H + 80000H where N = Memory Segment number (1) for 1 Mbyte, N = (1, 3) for 2 Mbyte, N = (1, 3, 5, 7) for 4 Mbyte, N = (1…19) for 10 Mbyte.*

Notes:

1. *Address bit A16 = X = Don't Care for all address commands except for Program Address (PA), Read Address (RA) and Sector Address (SA).*
2. *Bus operations are defined in Table 1.*
3. *RA = Address of the memory location to be read.*
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   SA = Address of the sector to be erased. The combination of A17, A18, A19 will uniquely select any sector of a segment.
   To select the memory segment:1 and 2 Mbyte: Use $\overline{CE}$2 and A20
   4 Mbyte: Use $\overline{CE}$2 and A20, A21
   10 Mbyte: Use $\overline{CE}$2 and A20–A23.
4. *RD = Data read from location RA during read operation.*
   PD = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$ pulse.
5. *A0 = 1 and $\overline{CE}$1 = 0 or A0 = X and $\overline{CE}$2 = 0.*

Table 5. Word Command Definitions (Note 7)

Embedded Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data
Reset/Read	4	AAAAH	AAAA	5554H	5555	AAAAH	F0F0	RA	RW				
Autoselect	4	AAAAH	AAAA	5554H	5555	AAAAH	9090	00H/02H	0101/ A4A4				
Byte Write	4	AAAAH	AAAA	5554H	5555	AAAAH	A0A0	PA	PW				
Segment Erase	6	AAAAH	AAAA	5554H	5555	AAAAH	8080	AAAAH	AAAA	5554H	5555	AAAAH	1010
Sector Erase	6	AAAAH	AAAA	5554H	5555	AAAAH	8080	AAAAH	AAAA	5554H	5555	SA	3030
Sector Erase Suspend		Erase can be suspended during sector erase with Addr (don't care), Data (B0H)											
Sector Erase Resume		Erase can be resumed after suspend with Addr (don't care), Data (30H)											

Notes:

1. *Address bit A16 = X = Don't Care for all address commands except for Program Address (PA) and Sector Address (SA).*
2. *Bus operations are defined in Table 1.*
3. *RA = Address of the memory location to be read.*
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   SA = Address of the sector to be erased. The combination of A17, A18, A19 will uniquely select any sector of a segment.
   To select the memory segment:1 and 2 Mbyte: Use $\overline{CE}1$, $\overline{CE}2$, A20
   4 Mbyte: Use $\overline{CE}1$, $\overline{CE}2$, A20, A21
   0 Mbyte: Use $\overline{CE}1$, $\overline{CE}2$, A20–A23.
4. *RW = Data read from location RA during read operation. (Word Mode).*
   PW = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$. (Word Mode).
5. *Address for Memory Segment Pair 0 (S0 and S1) only. Address for the higher Memory Segment Pairs (S2, S3 = Pair 1, S4, S5 = Pair 2, S6, S7 = Pair 3…) is equal to (Addr) + M* (80000H) where M = Memory Segment Pair number.*
6. *Word = 2 bytes = odd byte and even byte.*
7. *$\overline{CE}1$ = 0 and $\overline{CE}2$ = 0.*

Table 6. Memory Sector Address Table for Memory Segment S0

Sector	A19	A18	A17	Address Range
0	0	0	0	00000h-0FFFFh
1	0	0	1	10000h-1FFFFh
2	0	1	0	20000h-2FFFFh
3	0	1	1	30000h-3FFFFh
4	1	0	0	40000h-4FFFFh
5	1	0	1	50000h-5FFFFh
6	1	1	0	60000h-6FFFFh
7	1	1	1	70000h-7FFFFh

Note: *A0 is not mapped internally.*

FLASH MEMORY WRITE/ERASE OPERATIONS

Details of AMD's Embedded Write and Erase Operations

Embedded Erase™ Algorithm

The automatic memory sector or memory segment erase does not require the device to be entirely preprogramming prior to executing the Embedded Erase command. Upon executing the Embedded Erase command sequence, the addressed memory sector or memory segment will automatically write and verify the entire memory segment or memory sector for an all "zero" data pattern. The system is not required to provide any controls or timing during these operations.

When the memory sector or memory segment is automatically verified to contain an all "zero" pattern, a self-timed chip erase-and-verify begins. The erase and verify operations are complete when the data on D7 of the memory sector or memory segment is "1" (see "Write Operation Status" section) at which time the

device returns to the Read mode (D15 on the odd byte). The system is not required to provide any control or timing during these operations. A Reset command after the device has begun execution will stop the device but the data in the operated segment will be undefined. In that case, restart the erase on that sector and allow it to complete.

When using the Embedded Erase algorithm, the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard erase verify command is used.

The Embedded Erase command sequence is a command only operation that stages the memory sector or memory segment for automatic electrical erasure of all bytes in the array. The automatic erase begins on the rising edge of the $\overline{WE}$ and terminates when the data on D7 of the memory sector or memory segment is "1" (see "Write Operation Status" section) at which time the device returns to the Read mode. Please note that for the memory segment or memory sector erase operation, $\overline{Data}$ Polling may be performed at any address in that segment or sector.

Figure 1 and Table 7 illustrate the Embedded Erase Algorithm, a typical command string and bus operations.

Table 7. Embedded Erase Algorithm

Bus Operation	Command	Comments
Standby		Wait for V_{CC} ramp
Write	Embedded Erase command sequence	6 bus cycle operation
Read		$\overline{Data}$ Polling to verify erasure

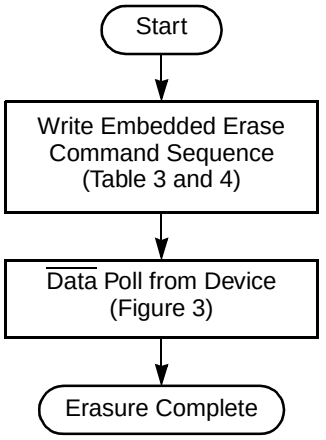


Figure 1. Embedded Erase Algorithm

As described earlier, once the memory sector in a device or memory segment completes the Embedded Erase operation it returns to the Read mode and addresses are no longer latched. Therefore, the device requires that a valid address input to the device is supplied by the system at this particular instant of time. Otherwise, the system will never read a "1" on D7. A system designer has two choices to implement the Embedded Erase algorithm:

1. The system (CPU) keeps the sector address (within any of the sectors being erased) valid during the entire Embedded Erase operation, or
2. Once the system executes the Embedded Erase command sequence, the CPU takes away the address from the device and becomes free to do other tasks. In this case, the CPU is required to keep track of the valid sector address by loading it into a temporary register. When the CPU comes back for performing $\overline{Data}$ Polling, it should reassert the same address.

Since the Embedded Erase operation takes a significant amount of time (1.5–30 s), option 2 makes more sense. However, the choice of these two options has been left to the system designer.

Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command (data) is latched on the rising edge of $\overline{WE}$. A time-out of 100 µs from the rising edge of the last sector erase command will initiate the sector erase command(s).

Multiple sectors may be erased concurrently by writing the six bus cycle operations as described above. This sequence is followed with writes of the sector erase command 30H to addresses in other sectors desired to be concurrently erased. A time-out of 100 µs from the rising edge of the $\overline{WE}$ pulse for the last sector erase command will initiate the sector erase. If another sector erase command is written within the 100 µs time-out window the timer is reset. Any command other than sector erase within the time-out window will reset the device to the read mode, ignoring the previous command string (refer to "Write Operation Status" section for Sector Erase Timer operation). Loading the sector erase buffer may be done in any sequence and with any sector number.

Sector erase does not require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector

or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations. A Reset command after the device has begun execution will stop the device but the data in the operated segment will be undefined. In that case, restart the erase on that sector and allow it to complete.

The automatic sector erase begins after the 100 µs time out from the rising edge of the $\overline{WE}$ pulse for the last sector erase command pulse and terminates when the data on D7 is "1" (see "Write Operation Status" section) at which time the device returns to read mode. $\overline{Data}$ Polling must be performed at an address within any of the sectors being erased.

Figure 1 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Embedded Program™ Algorithm

The Embedded Program Setup is a four bus cycle operation that stages the addressed memory sector or memory segment for automatic programming.

Once the Embedded Program Setup operation is performed, the next $\overline{WE}$ pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the $\overline{WE}$ pulse. Data is internally latched on the rising edge of the $\overline{WE}$ pulse. The rising edge of $\overline{WE}$ also begins the programming operation. The system is not required to provide further control or timing. The device will automatically provide an adequate internally generated write pulse and verify margin. The automatic programming operation is completed when the data on D7 of the addressed memory sector or memory segment is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to the Read mode (no write verify command is required).

Addresses are latched on the falling edge of $\overline{WE}$ during the Embedded Program command execution and hence the system is not required to keep the addresses stable during the entire Programming operation. However, once the device completes the Embedded Program operation, it returns to the Read mode and addresses are no longer latched. Therefore, the device requires that a valid address input to the device is supplied by the system at this particular instant of time. Otherwise, the system will never read a valid data on D7. A system designer has two choices to implement the Embedded Programming algorithm:

1. The system (CPU) keeps the address valid during the entire Embedded Programming operation, or
2. Once the system executes the Embedded Programming command sequence, the CPU takes away the address from the device and becomes free to do other tasks. In this case, the CPU is required to keep track of the valid address by loading it into a temporary register. When the CPU comes back for performing $\overline{Data}$ Polling, it should reassert the same address.

However, since the Embedded Programming operation takes only 16 µs typically, it may be easier for the CPU to keep the address stable during the entire Embedded Programming operation instead of reasserting the valid address during $\overline{Data}$ Polling. Anyway, this has been left to the system designer's choice to go for either operation. Any commands written to the segment during this period will be ignored.

Figure 2 and Table 8 illustrate the Embedded Program Algorithm, a typical command string, and bus operation.

Table 8. Embedded Program Algorithm

Bus Operation	Command	Comments
Standby		Wait for V_{CC} ramp
Write	Embedded Program command sequence	3 bus cycle operation
Write	Program Address/Data	1 bus cycle operation
Read		$\overline{Data}$ Polling to verify program

Reset Command

The Reset command initializes the sector or segment to the read mode. Please refer to Tables 3 and 4, "Byte Command Definitions," and Table 5, "Word Command Definitions" for the Reset command operation. The sector or segment remains enabled for reads until the command register contents are altered. There is a 6 µs Write Recovery Time before Read for the first read after a write.

The Reset command will safely reset the segment memory to the Read mode. Memory contents are not altered. Following any other command, write the Reset command once to the segment. This will safely abort any operation and reset the device to the Read mode.

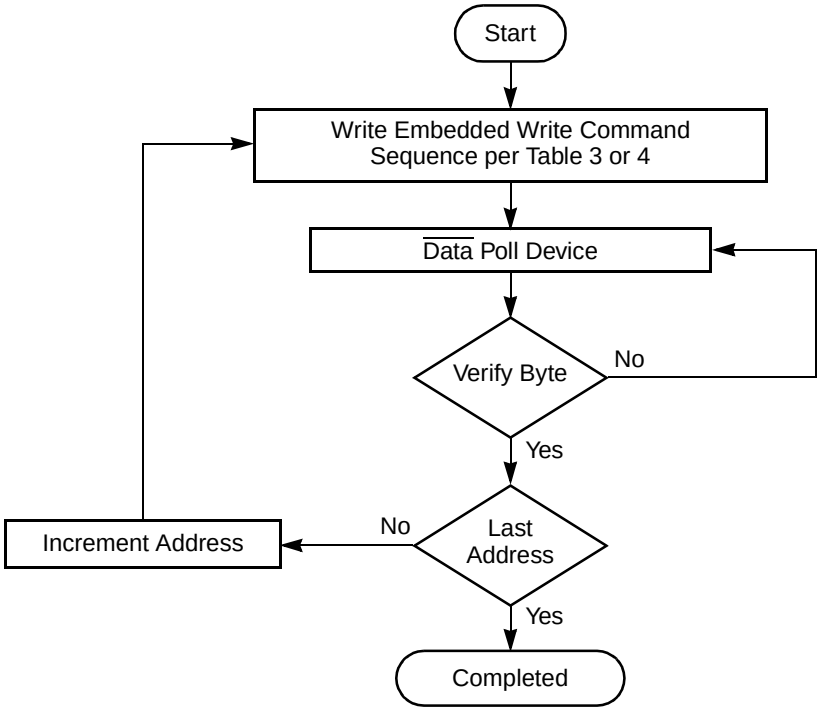
The Reset is needed to terminate the auto select operation. It can be used to terminate an Erase or Sector Erase operation, but the data in the sector or segment being erased would then be undefined.

Write Operation Status

$\overline{Data}$ Polling—D7 (D15 on Odd Byte)

The Flash Memory PC Card features $\overline{Data}$ Polling as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

While the Embedded Programming algorithm is in operation, an attempt to read the device will produce the complement of expected valid data on D7 of the addressed memory sector or memory segment. Upon



18723C-3

Figure 2. Embedded Programming Algorithm in Byte-Wide Mode

completion of the Embedded Program algorithm an attempt to read the device will produce valid data on D7. The Data Polling feature is valid after the rising edge of the fourth WE pulse of the four write pulse sequence.

While the Embedded Erase algorithm is in operation, D7 will read "0" until the erase operation is completed. Upon completion of the erase operation, the data on D7 will read "1".

The Data Polling feature is only active during the Embedded Programming or Erase algorithms. Please note that the AmC0XXCFLKA data pin (D7) may change asynchronously while Output Enable (OE) is asserted low. This means that the device is driving status information on D7 at one instant of time and then the byte's valid data at the next instant of time. Depending on when the system samples the D7 output, it may read either the status or valid data. Even if the device has completed the Embedded operation and D7 has a valid data, the data outputs on D0–D6 may be still invalid since the switching time for data bits (D0–D7) will not be the same. This happens since the internal delay paths for data bits (D0–D7) within the device are different. The valid data will be provided only after a certain time delay (<t_{OE}). Please refer to Figure 4a for detailed timing diagrams.

See Figures 3 and 5 for the Data Polling timing specifications and diagrams.

Toggle Bit—D6 (D14 on Odd Byte)

The Flash Memory PC Card also features a "Toggle Bit" as a method to indicate to the host system that the Embedded algorithms are either in progress or have been completed.

While the Embedded Program or Erase algorithm is in progress, successive attempts to read data from the device will result in D6 toggling between one and zero. Once the Embedded Program or Erase algorithm is completed, D6 will stop toggling and valid data on D0–D7 will be read on the next successive read attempt. The Toggle bit is also used for entering Erase Suspend mode. Please refer to the section entitled "Sector Erase Suspend."

Please note that even if the device completes the Embedded algorithm operation and D6 stops toggling, data bits D0–D7 (including D6) may not be valid during the current bus cycle. This may happen since the internal circuitry may be switching from status mode to the Read mode. There is a time delay associated with this mode switching. Since this time delay is always less than t_{OE} (OE access time), the next successive read attempt (OE going low) will provide the valid data on D0-D7. Also note that once the D6 bit has stopped toggling and the output enable OE is held low thereafter (without toggling) the data bits (D0–D7) will be valid after t_{OE}time delay.

See Figures 4 and 6 for the Data Polling diagram and timing specifications.

Sector Erase Suspend

Sector Erase Suspend command allows the user to interrupt the chip and then do data reads (not program) from a non-busy sector while it is in the middle of a Sector Erase operation (which may take up to several seconds). This command is applicable ONLY during the Sector Erase operation and will be ignored if written during the chip Erase or Programming operation. The Erase Suspend command (B0H) will be allowed only during the Sector Erase Operation that will include the sector erase time-out period after the Sector Erase commands (30H). Writing this command during the time-out will result in immediate termination of the time-out period. Any subsequent writes of the Sector Erase command will be ignored as such, but instead will be taken as the Erase Resume command. Note that any other commands during the time out will reset the device to read mode. The addresses are don't-cares in writing the Erase Suspend or Erase Resume commands.

When the Sector Erase Suspend command is written during a Sector Erase operation, the chip will take between 0.1 µs to 10 µs to suspend the erase operation and go into erase suspended read mode (pseudo-read mode), during which the user can read from a sector that is NOT being erased. A read from a sector being erased may result in invalid data. The user must monitor the toggle bit (D6) to determine if the chip has entered the pseudo-read mode, at which time the toggle bit stops toggling. Note that the user must keep track of what state the chip is in since there is no external indication of whether the chip is in pseudo-read mode or actual read mode. After the user writes the Sector Erase Suspend command and waits until the toggle bit stops toggling, data reads from the device may then be performed. Any further writes of the Sector Erase Suspend command at this time will be ignored.

Every time a Sector Erase Suspend command followed by an Erase Resume command is written, the internal (pulse) counters are reset. These counters are used to count the number of high voltage pulses the memory cell requires to program or erase. If the count exceeds a certain limit, then the D5 bit will be set (Exceeded Time Limit flag). This resetting of the counters is necessary since the Erase Suspend command can potentially interrupt or disrupt the high voltage pulses.

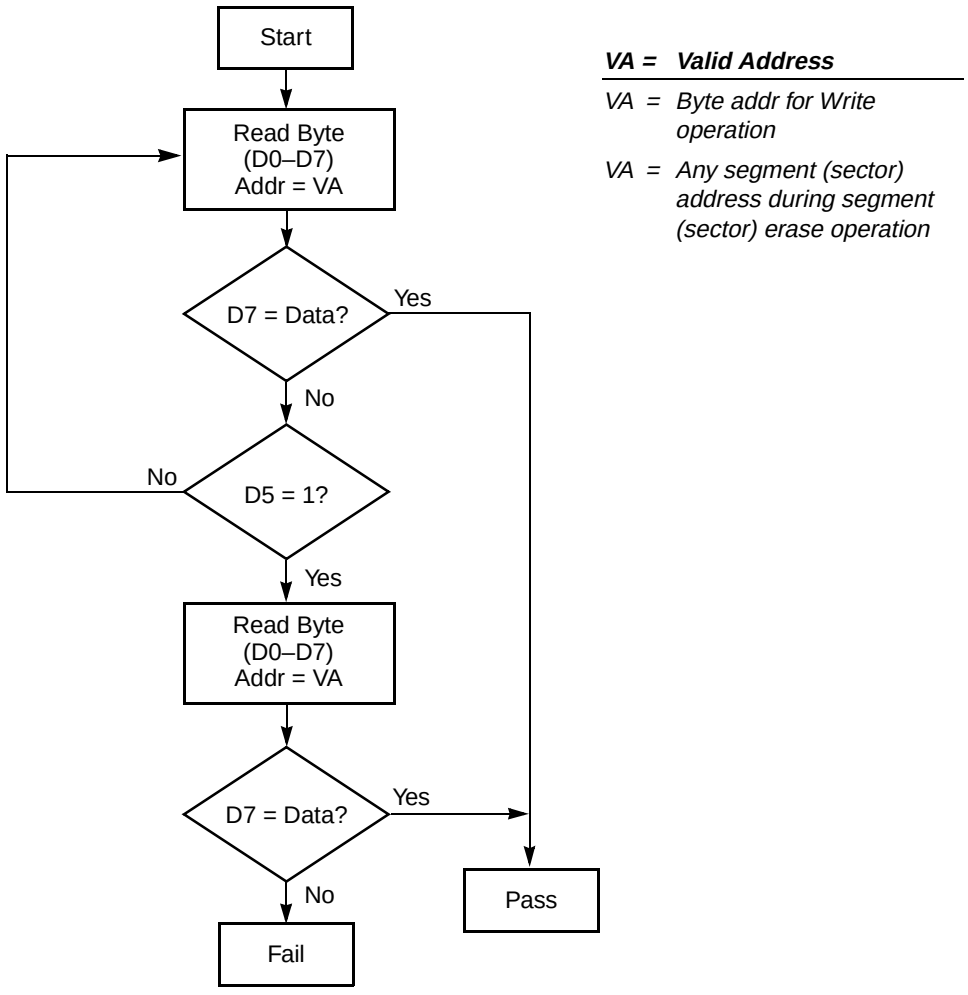
To resume the operation of Sector Erase, the Resume command (30H) should be written. Any further writes of the Resume command at this point will be ignore. Another Sector Erase Suspend command can be written after the chip has resumed.

Write Operation Status

Table 9. Hardware Sequence Flags

Status		D7	D6	D5	D3	D2–D0
In Progress	Auto-Programming	$\overline{D}$7	Toggle	0	0	
	Programming in Auto-Erase	0	Toggle	0	1	($\overline{D}$)
	Erasing in Auto-Erase	0	Toggle	0	1	
Exceeded Time Limits	Auto-Programming	$\overline{D}$7	Toggle	1	0	
	Programming in Auto-Erase	0	Toggle	1	1	($\overline{D}$)
	Erasing in Auto-Erase	0	Toggle	1	1	

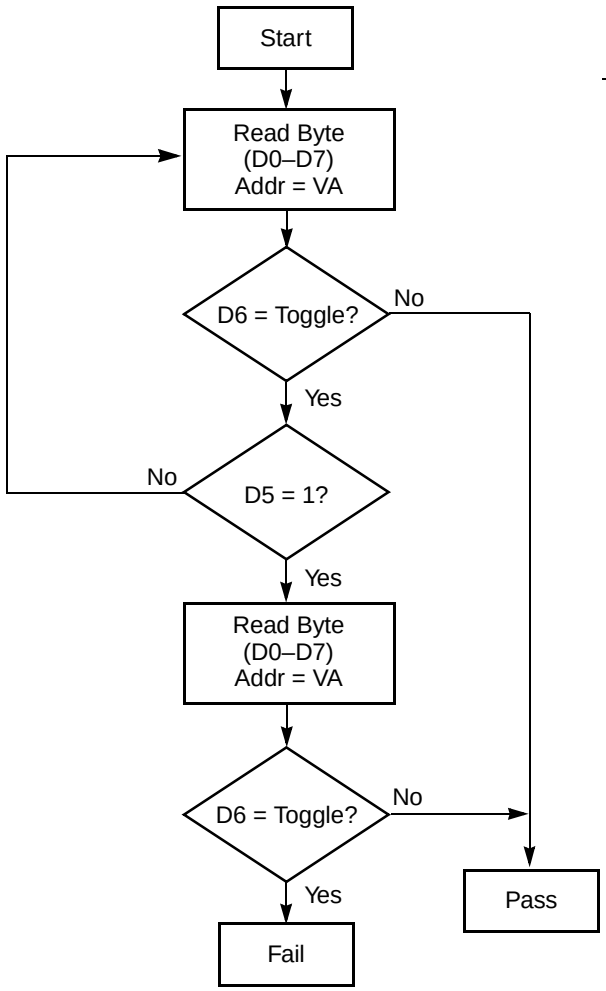
Note: *D0, D1, and D2 are reserve pins for future use. D4 is for AMD internal use only.*



18723C-4

Note: *D7 is rechecked even if D5 = 1 because D7 may change simultaneously with D5.*

Figure 3. $\overline{\text{Data}}$ Polling Algorithm



VA = Valid Address

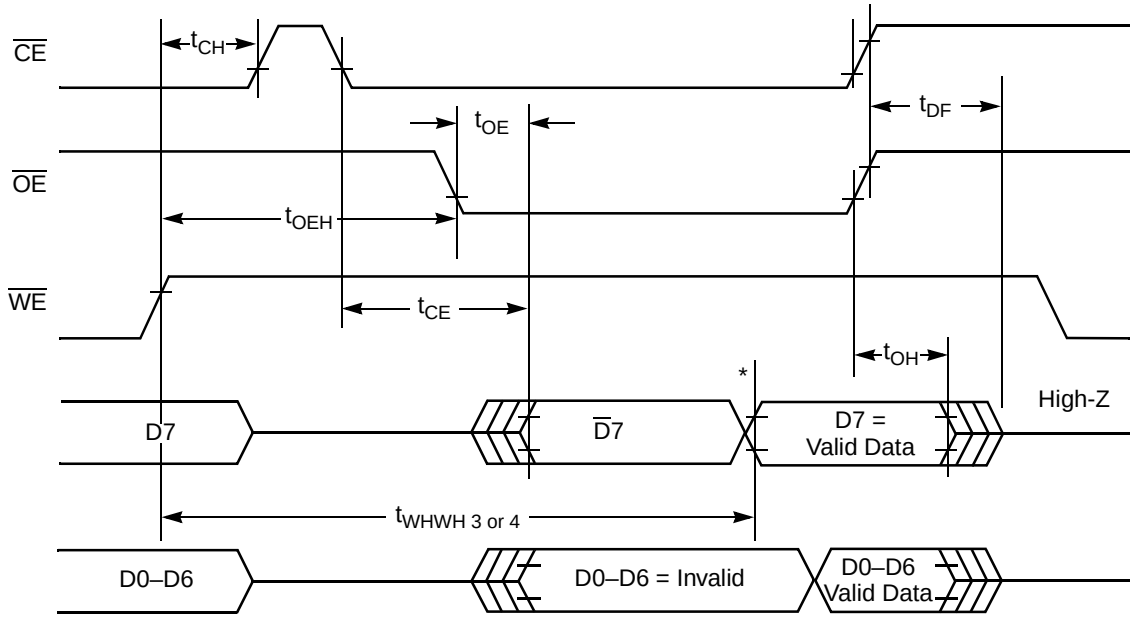
VA = Byte addr for Write operation

VA = Any segment (sector) address during segment (sector) erase operation

18723C-5

Note: *D6 is rechecked even if D5 = 1 because D6 may stop toggling at the same time as D5 changes to "1".*

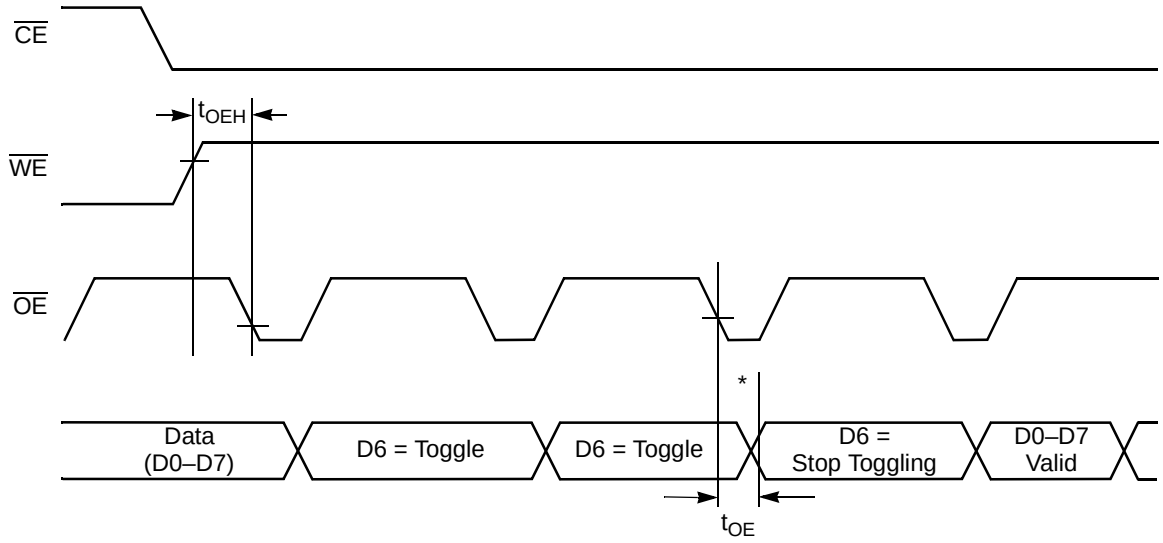
Figure 4. Toggle Bit Algorithm



18723C-6

** D7 = Valid Data (The device has completed the Embedded operation.)*

Figure 5. AC Waveforms for $\overline{\text{Data}}$ Polling During Embedded Algorithm Operations

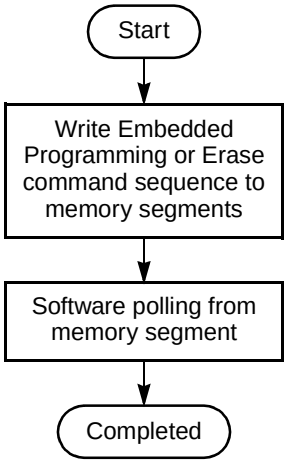


18723C-7

** D6 stops toggling (The device has completed the Embedded operation.)*

Figure 6. AC Waveforms for Toggle Bit During Embedded Algorithm Operations

EMBEDDED ALGORITHMS



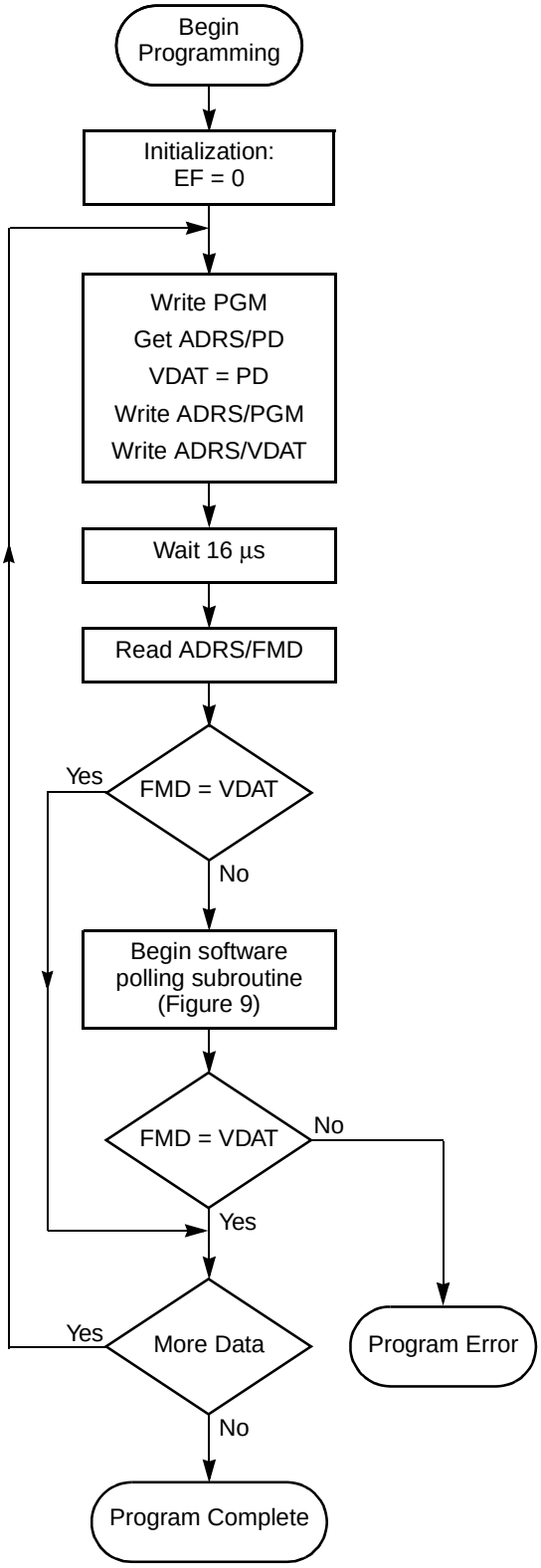
The Embedded Algorithm operations completely automate the programming and erase procedure by internally executing the algorithmic command sequence of original AMD devices. The devices automatically provide Write Operation Status information with standard read operations.

See Table 3 or 4 for Program Command Sequence.

18723C-8

Figure 7. Byte-Wide Programming and Erasure Overview

EMBEDDED ALGORITHMS



Activity

Initialize Programming Variables:
EF = Error Flag

PGM =Embedded Byte Write Command Sequence Cycle #1–3 (Table 3 or 4)

ADRS = Appropriate address for memory segment

PD = Program Data

VDAT = Valid Data

FMD = Flash Memory Data

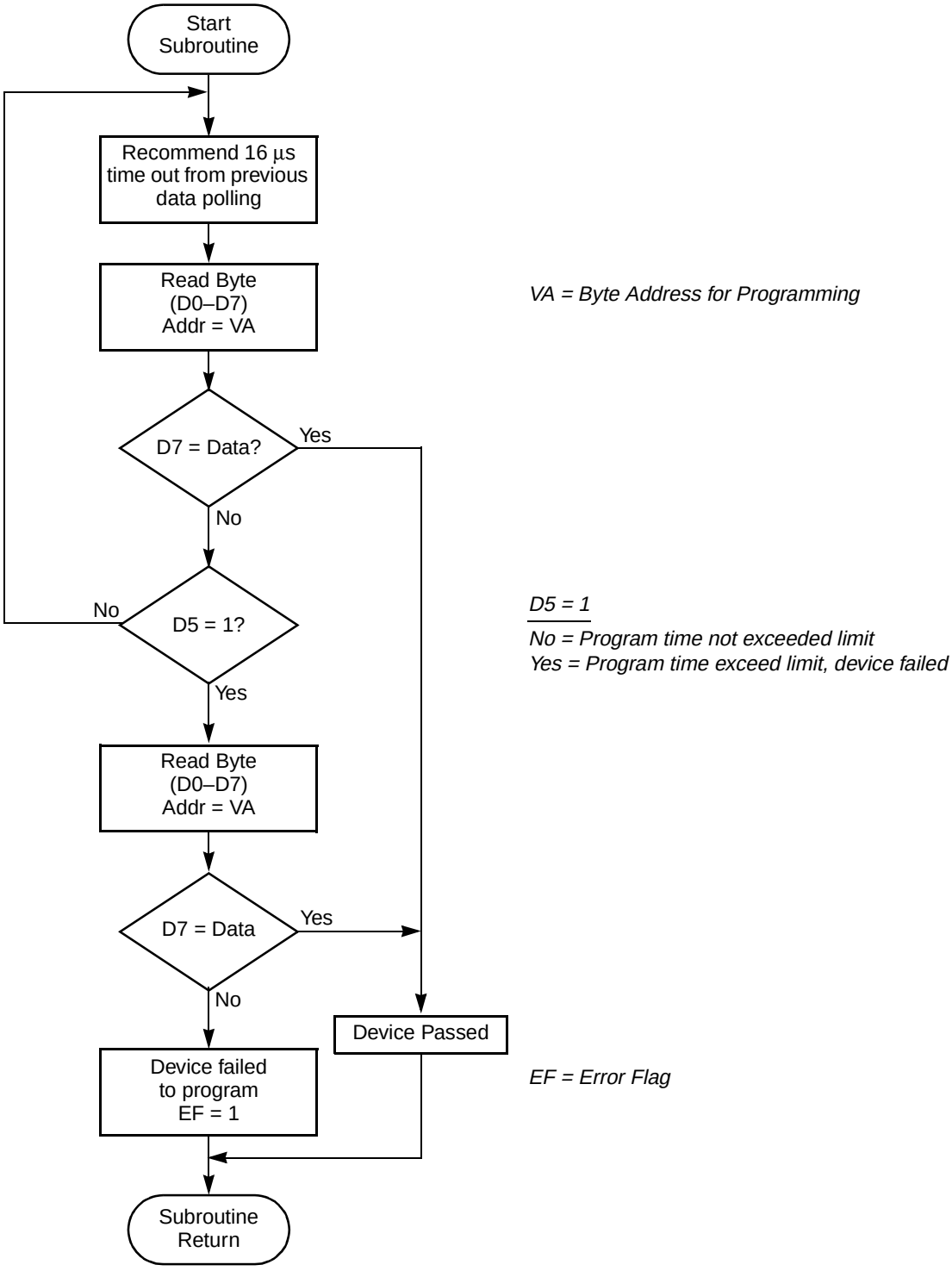
EF = 0 = No Programming error

EF = 1 = Programming error

18723C-9

Figure 8. Byte-Wide Programming Flow Chart

EMBEDDED ALGORITHMS

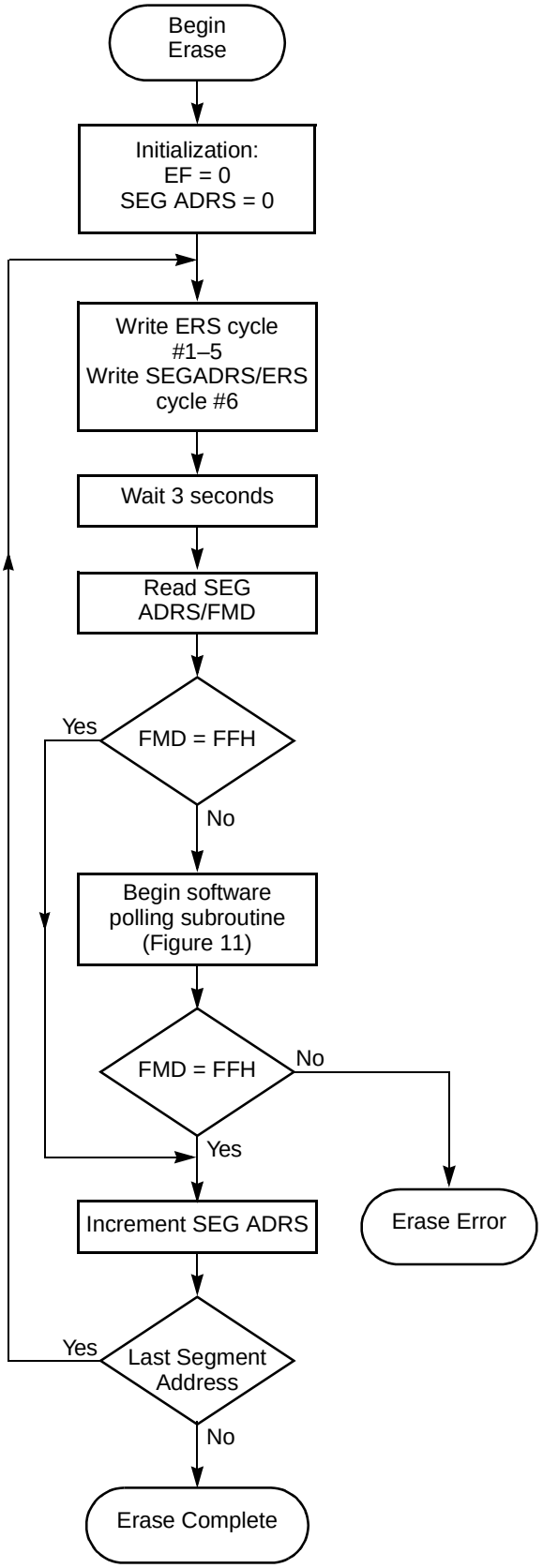


18723C-10

Note: *D7 is checked even if D5 = 1 because D7 may have changed simultaneously with D5 or immediately after D5.*

Figure 9. Byte-Wide Software Polling for Programming Subroutine

EMBEDDED ALGORITHMS



Activity

EF = Error Flag = 0

SEG ADRS = Segment Address = 0

ERS =Erase Command Sequence
(Even byte per Table 3, Odd byte per Table 4)

3 seconds wait = 2 seconds memory segment preprogram time +1 second memory segment erase time

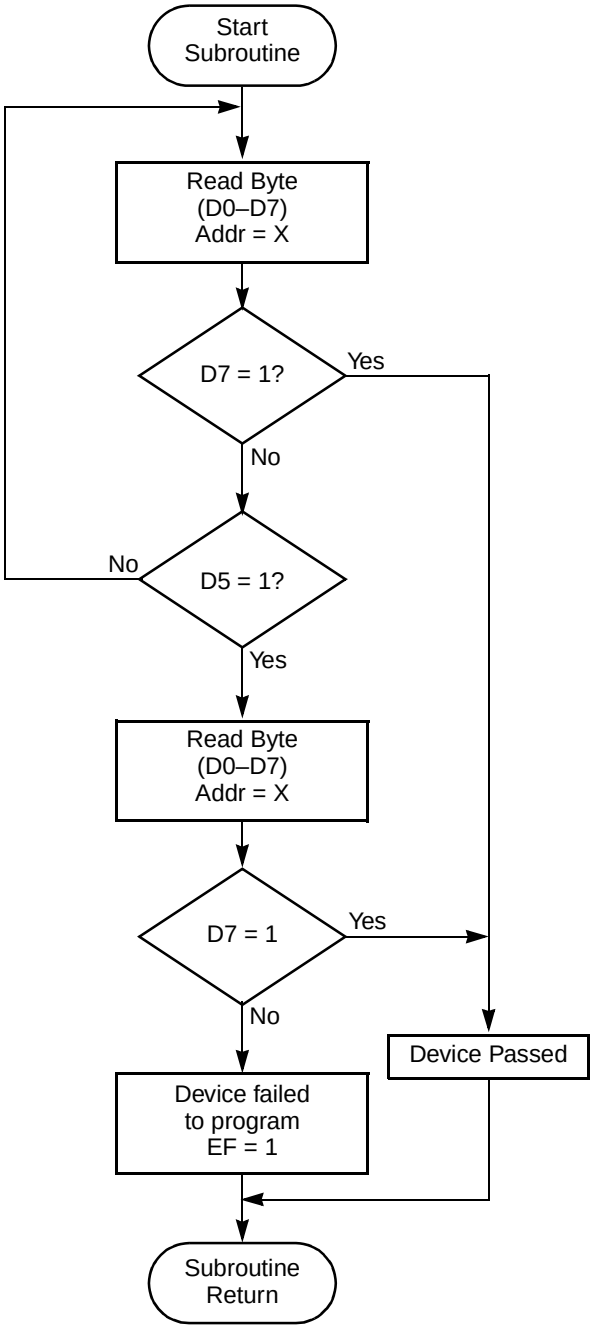
FMD = Flash Memory Data

FFH = Erased Flash Memory Data

18723C-11

Figure 10. Byte-Wide Erasure Flow Chart

EMBEDDED ALGORITHMS



X = Don't Care

D7 = 1

Yes = Erase Complete
No = Erase not Complete

D5 = 1

Yes = Erase time exceeded limit, device failed
No = Erase time has not exceeded limit

18723C-12

Figure 11. Byte-Wide Software Polling Erase Subroutine

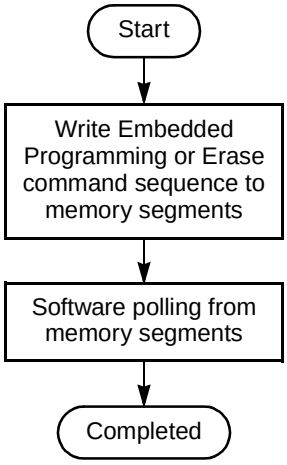
WORD-WIDE PROGRAMMING AND ERASING

Word-Wide Programming

The Word-Wide Programming sequence will be as usual per Table 5. The Program word command is A0A0H. Each byte is independently programmed. For example, if the high byte of the word indicates the successful completion of programming via one of its write status bits such as D15, software polling should continue to monitor the low byte for write completion and data verification, or vice versa. During the Embedded Programming operations the device executes programming pulses in 16 µs increments. Status reads provide information on the progress of the byte programming relative to the last complete write pulse. Status information is automatically updated upon completion of each internal write pulse. Status information does not change within the 16 µs write pulse width.

Word-Wide Erasing

The Word-Wide Erasing of a memory segment pair is similar to word-wide programming. The erase word command is a 6 bus cycle command sequence per Table 5. Each byte is independently erased and verified. Word-wide erasure reduces total erase time when compared to byte erasure. Each Flash memory device in the card may erase at different rates. Therefore each device (byte) must be verified separately.



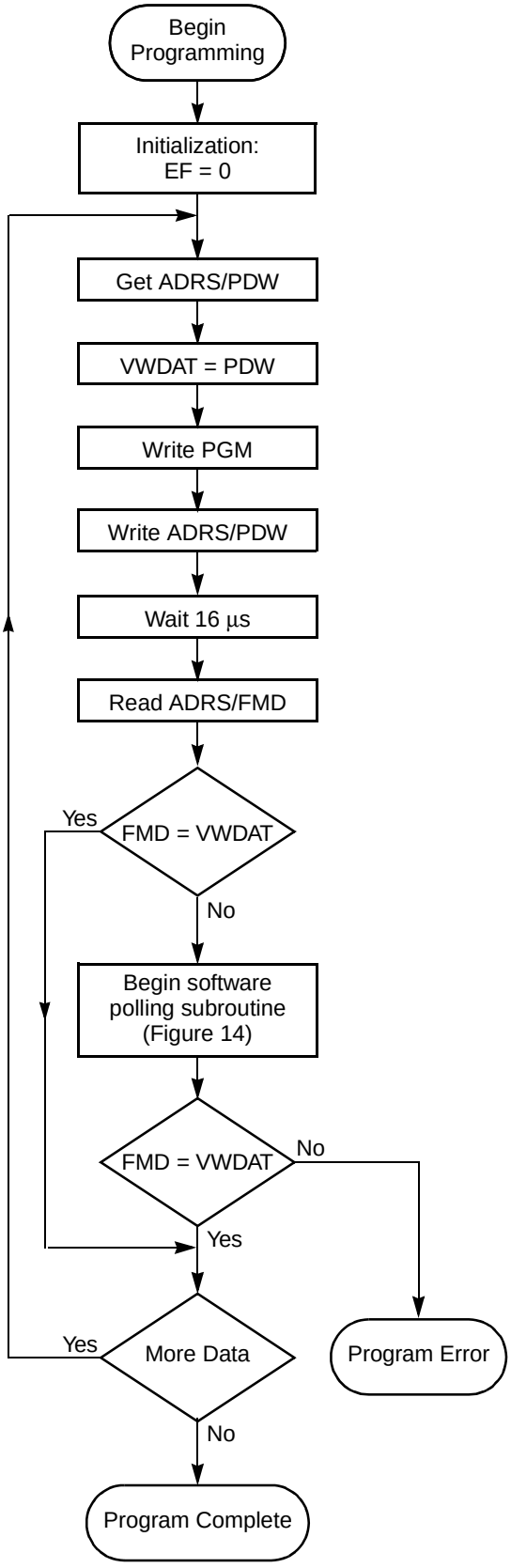
The Embedded Algorithm operations completely automate the parallel programming and erase procedures by internally executing the algorithmic command sequences of AMD's Flashrite and Flasherase algorithms. The devices automatically provide Write Operation Status information with standard read operations.

See Table 5 for Program Command Sequence.

18723C-13

Figure 12. Embedded Algorithm Word-Wide Programming and Erasure Overview

EMBEDDED ALGORITHMS



Activity

Initialize Programming Variables:
EF = Error Flag
EF = 0 = No failure
EF = 1 = Low byte program error
EF = 2 = High byte program error
EF = 3 = Word-wide program error

VWDAT = Valid Word Data

PGM =Embedded Word Write Command Sequence Cycle #1–3 (Table 5)

ADRS = Appropriate address for Memory Segment (Cycle #4)

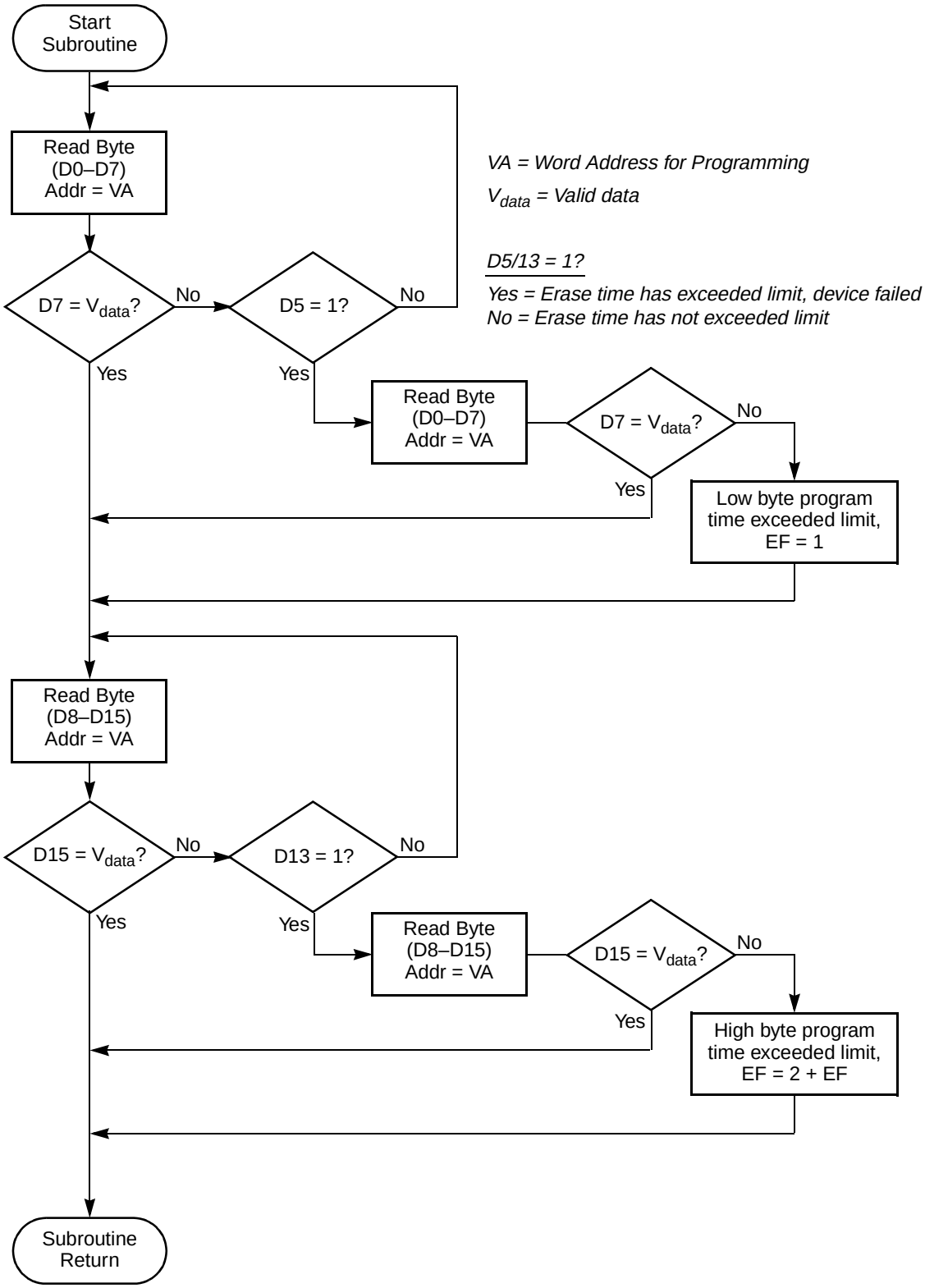
PDW = Program Data Word

FMD = Flash Memory Data

18723C-14

Figure 13. Word-Wide Programming Flow Chart

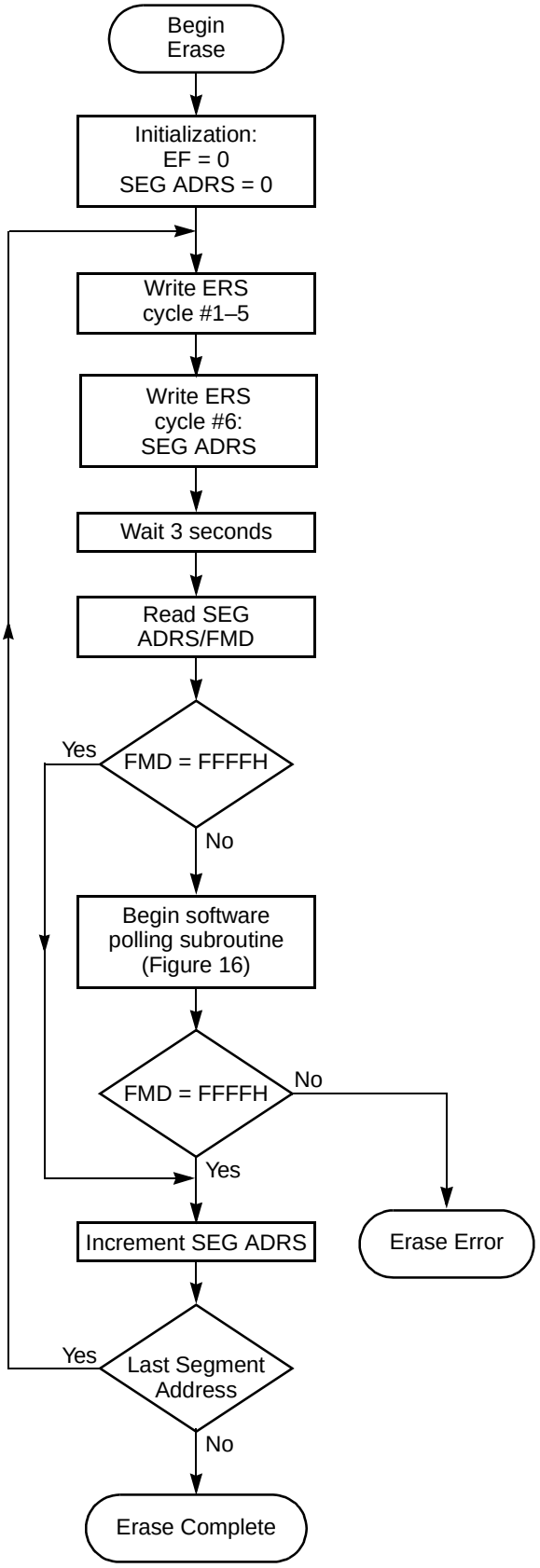
EMBEDDED ALGORITHMS



18723C-15

Figure 14. Word-Wide Software Polling Program Subroutine

EMBEDDED ALGORITHMS



Activity

EF = Error Flag

EF = 0 = No failure
EF = 1 = Low byte erase error
EF = 2 = High byte erase error
EF = 3 = Word-wide erase error

SEG ADRS = Segment Address

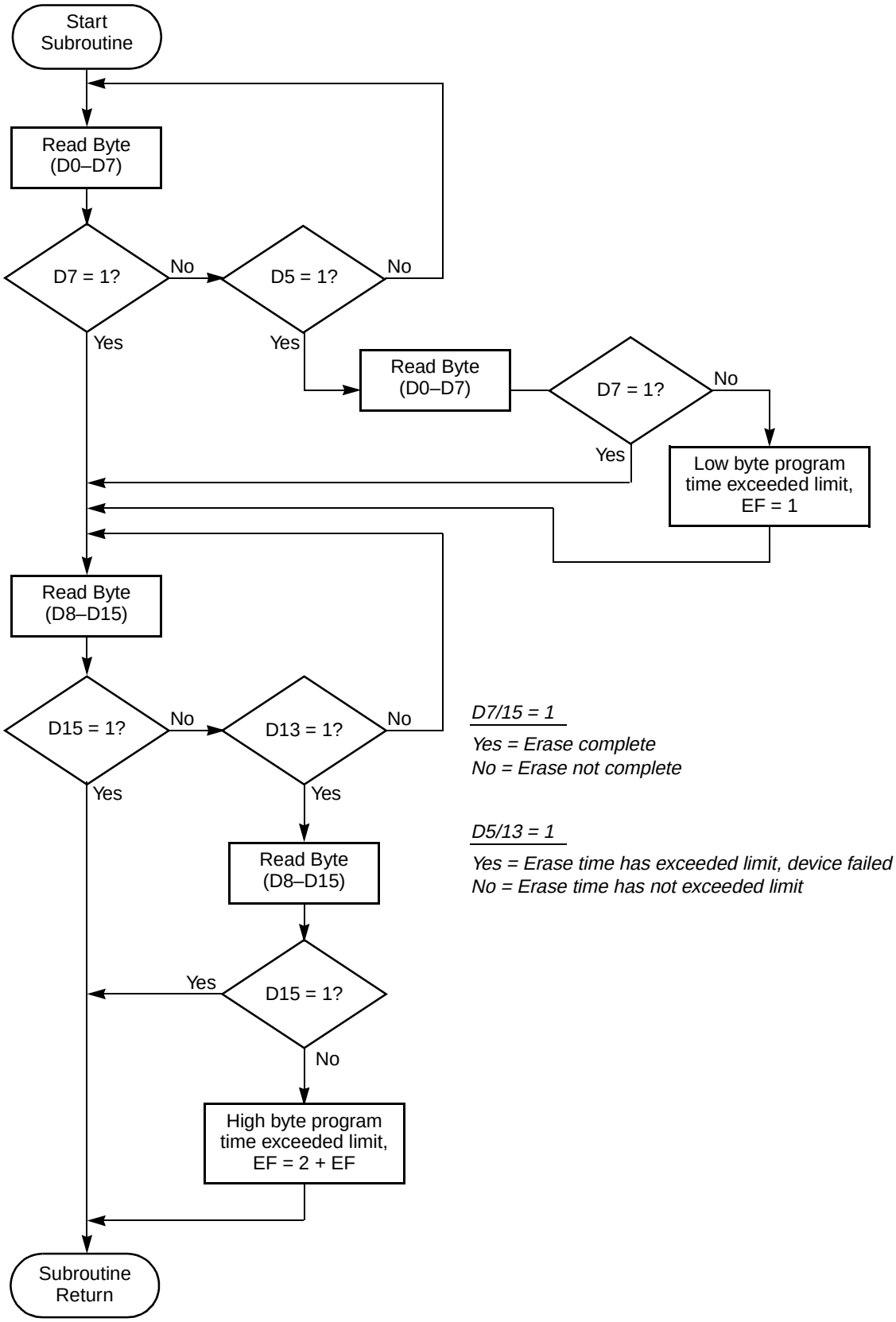
ERS = Segment Erase Command Sequence (Table 5)

FMD = Flash Memory Data

18723C-16

Figure 15. Word-Wide Erasure Flow Chart

EMBEDDED ALGORITHMS



18723C-17

Figure 16. Word-Wide Software Polling Erase Subroutine

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –30°C to +70°C

Ambient Temperature
with Power Applied. . . . . –10°C to +70°C

Voltage at All Pins (Note 1) . . . . . .–2.0 V to +7.0 V

V_{CC} (Note 1). . . . . .–0.5 V to 6.0 V

Output Short Circuit Current (Note 2) . . . . . 40 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20ns.*
2. *No more than one output shorted at a time. Durations of the short circuit should not be greater than one second. Conditions equal V_{OUT} = 0.5 V or 5.0 V, V_{CC} = V_{CC} max. These values are chosen to avoid test problems caused by tester ground degradation. This parameter is sampled and not 100% tested, but guaranteed by characterization.*
3. *V_{PP1} and V_{PP2} are not connected.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C). . . . . .0°C to +60°C

V_{CC} Supply Voltages. . . . . +4.75 V to 5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

Byte-Wide Operation

Parameter Symbol	Parameter Description	Test Description		Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or V_{SS} For all cards: ($\overline{CE}$, $\overline{REG}$, $\overline{WE}$, $\overline{OE}$ = –300 µA Min)	1 MB	–300	+ 20	µA
			2 MB	–300	+ 20	
			4 MB	–300	+ 20	
			10 MB	–300	+ 20	
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{CC}$ or V_{SS}	1 MB		± 20	µA
			2 MB		± 20	
			4 MB		± 20	
			10 MB		± 20	
I_{CCS}	V_{CC} Standby Current (Note 1)	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{CC} \pm 0.2$ V $V_{IN} = V_{CC}$ or GND	1 MB		0.7	mA
			2 MB		0.9	
			4 MB		1.3	
			10 MB		2.5	
I_{CC1}	V_{CC} Active Read Current (Notes 1, 2)	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, I_{OUT} = 0 mA, at 3.3 MHz			45	mA
I_{CC2}	V_{CC} Write/Erase Current (Notes 1, 2)	$\overline{CE} = V_{IL}$ Programming in Progress			65	mA
V_{IL}	Input Low Voltage			–0.5	0.8	V
V_{IH}	Input High Voltage			2.4	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA, $V_{CC} = V_{CC}$ Min			0.40	V
V_{OH}	Output High Voltage	I_{OH} = 2.0 mA, $V_{CC} = V_{CC}$ Min		3.8	V_{CC}	V
V_{LKO}	Low V_{CC} Lock-Out Voltage			3.2	4.2	V

Notes:

1. *For TTL input voltage levels (V_{IL} or V_{IH}), the minimum limit should be increased by: 1 mA for 1 Mbyte, 3 mA for 2 Mbyte, 7 mA for 4 Mbyte, 19 mA for 10 Mbyte.*
2. *One Flash device active, all the others in standby.*

Word-Wide Operation

Parameter Symbol	Parameter Description	Test Description		Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or V_{SS} ($\overline{CE}$, $\overline{REG}$, $\overline{WE}$, $\overline{OE}$ = –300 µA Min)	1 MB	–300	+ 20	µA
			2 MB	–300	+ 20	
			4 MB	–300	+ 20	
			10 MB	–300	+ 20	
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{CC}$ or V_{SS}	1 MB		± 20	µA
			2 MB		± 20	
			4 MB		± 20	
			10 MB		± 20	
I_{CCS}	V_{CC} Standby Current (Note 1)	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{CC} \pm 0.2$ V $V_{IN} = V_{CC}$ or GND	1 MB		0.7	mA
			2 MB		0.9	
			4 MB		1.3	
			10 MB		2.5	
I_{CC1}	V_{CC} Active Read Current (Notes 1, 2)	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, I_{OUT} = 0 mA, at 3.3 MHz			90	mA
I_{CC2}	V_{CC} Programming Current (Notes 1, 2)	$\overline{CE} = V_{IL}$ Programming in Progress			130	mA
V_{IL}	Input Low Voltage			–0.5	0.8	V
V_{IH}	Input High Voltage			2.4	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA, $V_{CC} = V_{CC}$ Min			0.40	V
V_{OH}	Output High Voltage	I_{OH} = 2.0 mA, $V_{CC} = V_{CC}$ Min		3.8	V_{CC}	V
V_{LKO}	Low V_{CC} Lock-Out Voltage			3.2	4.2	V

Notes:

1. *For TTL input voltage levels (V_{IL} or V_{IH}), the minimum limit should be increased by: 2 mA for 2 Mbyte, 6 mA for 4 Mbyte, 18 mA for 10 Mbyte.*
2. *Two Flash devices active, all the others in standby*

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Max	Unit
C_{IN1}	All except A1–A9	V_{IN} = 0 V	31	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	31	pF
C_{IN2}	A1–A9	V_{IN} = 0 V	45	pF
$C_{I/O}$	I/O Capacitance D0–D15	$V_{I/O}$ = 0 V	31	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

SWITCHING AC CHARACTERISTICS

Read Only Operation (Note 1)

Parameter Symbol		Parameter Description	Card Speed -150 ns		Unit
JEDEC	Standard		Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	150		ns
t_{ELQV}	t_{CE}	Chip Enable Access Time		150	ns
t_{AVQV}	t_{ACC}	Address Access Time		150	ns
t_{GLQV}	t_{OE}	Output Enable Access Time		75	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low-Z	5		ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High-Z		75	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low-Z	5		ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High-Z		75	ns
t_{AXQX}	t_{OH}	Output Hold from First of Address, $\overline{CE}$, or $\overline{OE}$ Change	5		ns
t_{WHGL}		Write Recovery Time Before Read	6		µs

Note:

1. *Input Rise and Fall Times (10% to 90%): ð 10 ns, Input Pulse levels: V_{OL} and V_{OH}, Timing Measurement Reference Level: Inputs—V_{IL} and V_{IH} Outputs—V_{IL} and V_{IH}*

AC CHARACTERISTICS

Write/Erase/Program Operations

Parameter Symbol		Parameter Description	Card Speed			Unit
			-150 ns			
JEDEC	Standard		Min	Typ	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	150			ns
t_{AVWL}	t_{AS}	Address Setup Time	20			ns
t_{WLAX}	t_{AH}	Address Hold Time	55			ns
t_{DVWH}	t_{DS}	Data Setup Time	50			ns
t_{WHDX}	t_{DH}	Data Hold Time	20			ns
t_{OEH}		Output Enable Hold Time for Embedded Algorithm	20			ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	6			µs
t_{GHWL}		Read Recovery Time before Write	0			µs
t_{WLOZ}		Output in High-Z from Write Enable	5			ns
t_{WHOZ}		Output in Low-Z from Write Enable			60	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time	0			ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time	20			ns
t_{WLWH}	t_{WP}	Write Pulse Width	45			ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	50			ns
t_{WHWH3}		Embedded Programming Operation (Notes 1, 2, 3)		16		µs
					48	ms
t_{WHWH4}		Embedded Erase Operation for each 64K Byte Memory Sector (Notes 1, 2)		1.5		s
t_{VCS}		V_{CC} Setup Time to $\overline{CE}$ LOW		50		µs

Notes:

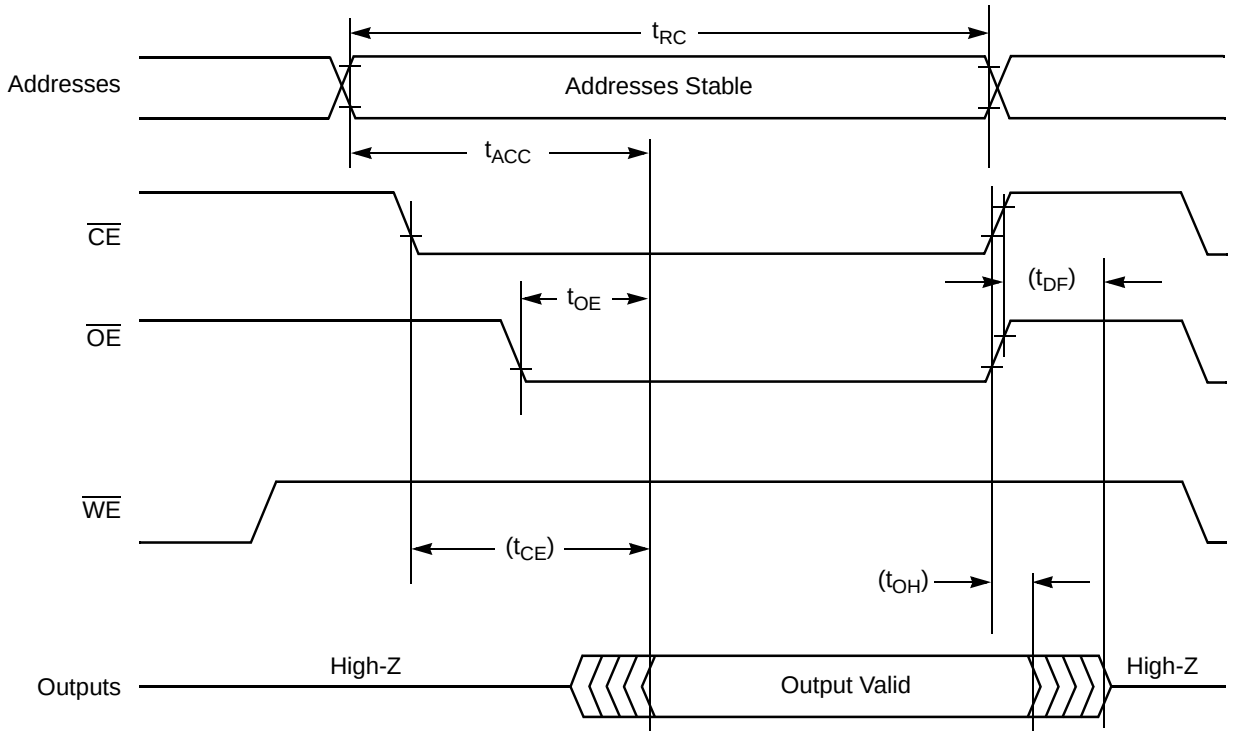
1. *Rise/Fall ð 10 ns.*
2. *Maximum specification not needed due to the devices internal stop timer that will stop any erase or write operation that exceed the device specification.*
3. *Embedded Program Operation of 16 µs consist of 10 µs program pulse and 6 µs write recovery before read. This is the minimum time for one pass through the programming algorithm. D5 = "1" only after a byte takes longer than 48 ms to Write.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING WAVEFORMS

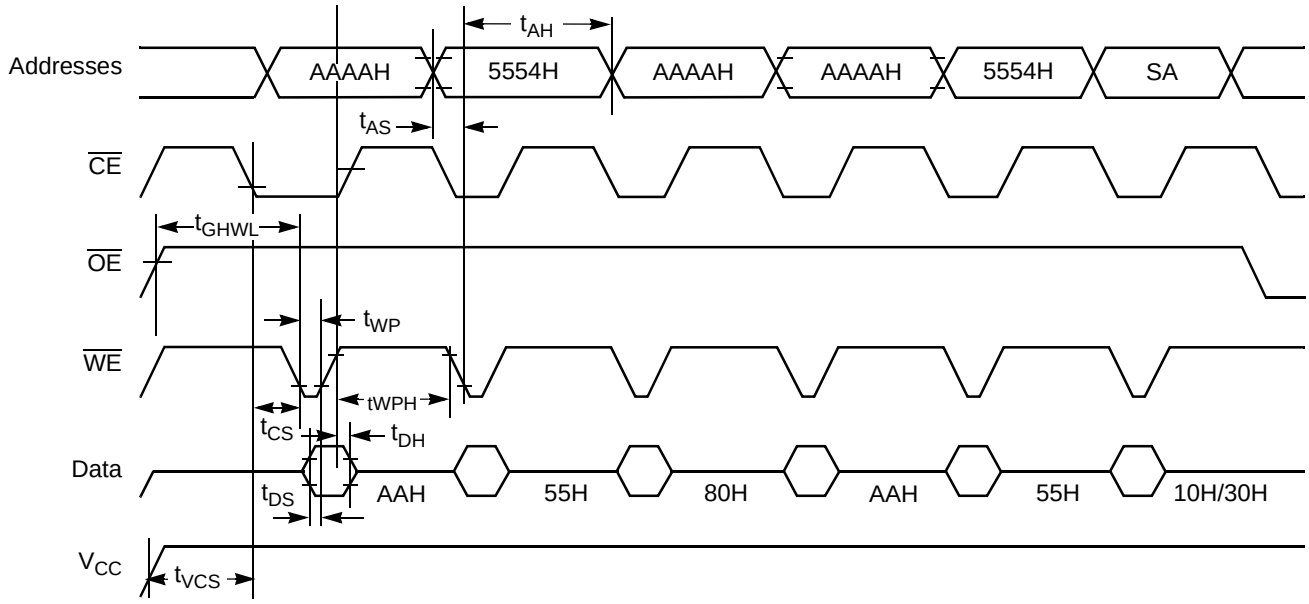


18723C-18

Note: *$\overline{CE}$ refers to $\overline{CE1}$ and $\overline{CE2}$.*

Figure 17. AC Waveforms for Read Operations

SWITCHING WAVEFORMS



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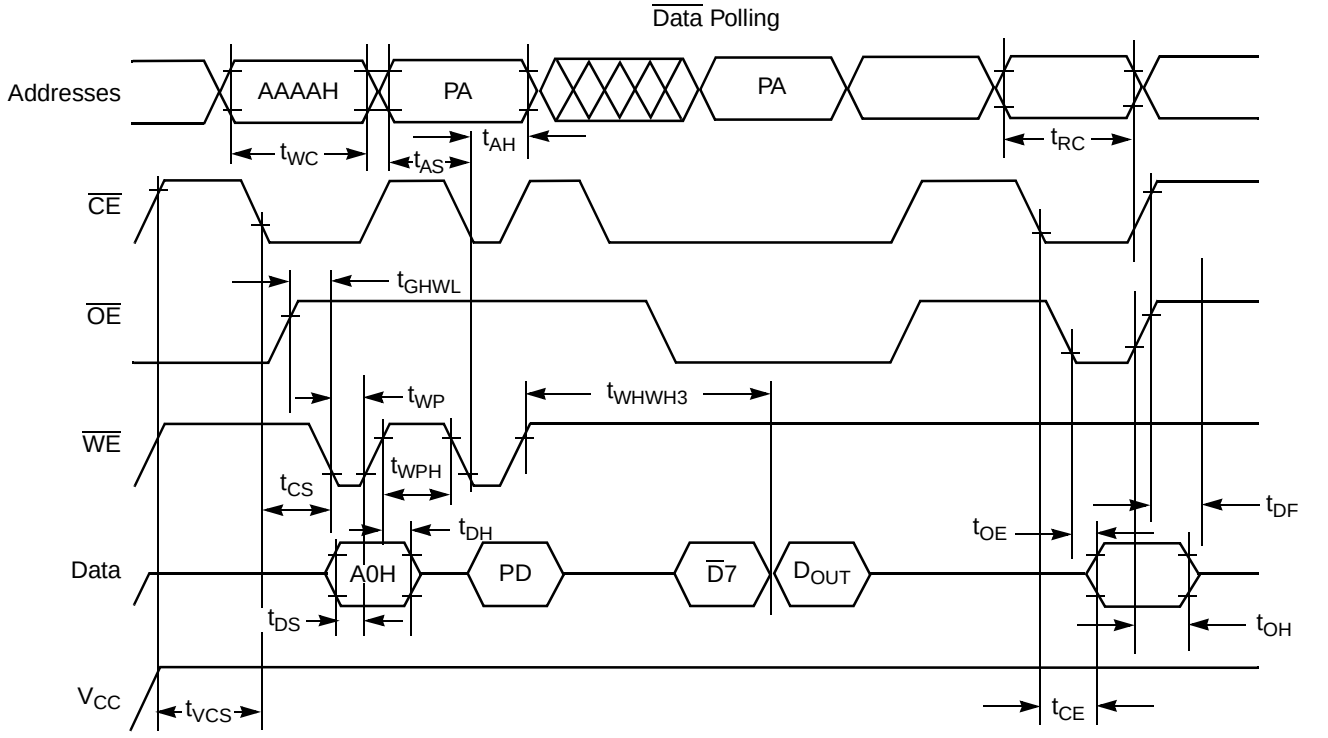
Note: *SA is the sector address for Sector Erase per Table 6.*

Figure 18. AC Waveforms Segment/Sector Byte Erase Operations

SWITCHING WAVEFORMS



Notes:

1. *Figure indicates last two bus cycles of four bus cycle sequence.*
2. *PA is address of the memory location to be programmed.*
3. *PD is data to be programmed at byte address.*
4. *$\overline{D}7$ is the output of the complement of the data written to the device.*
5. *D_{OUT} is the output of the data written to the device.*

Figure 19. AC Waveforms for Byte Write Operations

AC CHARACTERISTICS—ALTERNATE $\overline{CE}$ CONTROLLED WRITES

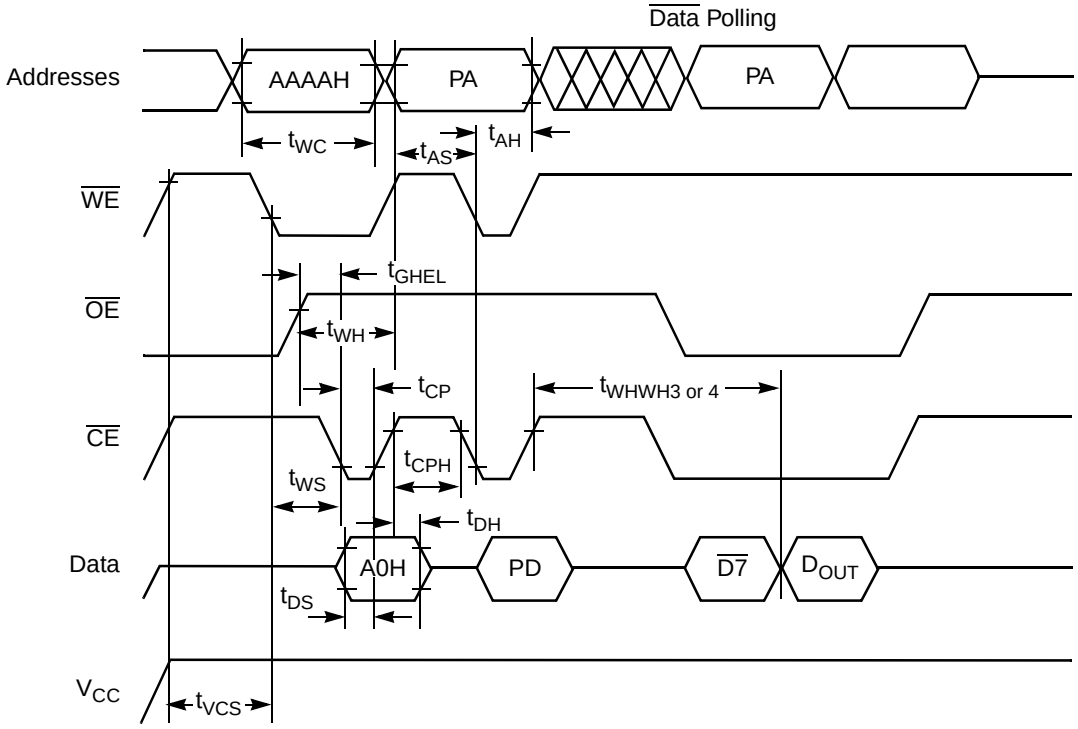
Write/Erase/Program Operations

Parameter Symbol		Parameter Description	Card Speed -150 ns		Unit
JEDEC	Standard		Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	150		ns
t_{AVEL}	t_{AS}	Address Setup Time	20		ns
t_{ELAX}	t_{AH}	Address Hold Time	55		ns
t_{DVEH}	t_{DS}	Data Setup Time	50		ns
t_{EHDX}	t_{DH}	Data Hold Time	20		ns
t_{GLDV}	t_{OE}	Output Enable Hold Time for Embedded Algorithm	20		ns
t_{GHEL}		Read Recovery Time before Write	0		µs
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time before $\overline{CE}$	0		ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time	0		ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width	65		ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ Pulse Width HIGH (Note 3)	50		ns
t_{EHEH3}		Embedded Programming Operation (Notes 3, 4)	16		µs
				48	ms
t_{EHEH4}		Embedded Erase Operation for each 64K byte Memory Sector (Notes 1, 2)	1.5		s
t_{VCS}		V_{CC} Setup Time to Write Enable LOW	50		ms

Notes:

1. *Rise/Fall ð10 ns.*
2. *Maximum specification not needed due to the internal stop timer that will stop any erase or write operation that exceed the device specification.*
3. *Card Enable Controlled Programming:*
   Flash Programming is controlled by the valid combination of the Card Enable ($\overline{CE}$1, $\overline{CE}$2) and Write Enable ($\overline{WE}$) signals. For systems that use the Card Enable signal(s) to define the write pulse width, all Setup, Hold, and inactive Write Enable timing should be measured relative to the Card Enable signal(s).
4. *Embedded Program Operation of 16 µs consist of 10 µs program pulse and 6 µs write recovery before read. This is the minimum time for one pass through the programming algorithm. D5 = "1" only after a byte takes longer than 48 ms to Write.*

SWITCHING WAVEFORMS



18723C-21

Notes:

1. *Figure indicates last two bus cycles of four bus cycle sequence.*
2. *PA is address of the memory location to be programmed.*
3. *PD is data to be programmed at byte address.*
4. *$\overline{D7}$ is the output of the complement of the data written to the device.*
5. *D_{OUT} is the output of the data written to the device.*

Figure 20. Alternate $\overline{CE}$ Controlled Byte Write Operation Timings

CARD INFORMATION STRUCTURE

The “C” series card contains a separate 512 byte EEPROM memory for the Card Information Structure (CIS).

All or part of the 512 byte could be used for the card’s attribute memory space. This allows all of the Flash memory to be used for the common memory space. Part of the common memory space could also be used to store the CIS if more than 512 bytes of CIS are needed.

The EEPROM used in the “C” series card is a NEC µPD28C05GX-20-EJA designed to operate from a 5 V single power supply. The µPD28C05 provides a Data Polling function that provides the End of Write Cycle and Auto Erase and Programming functions.

Table 10 shows the CIS information stored in the AMD Flash memory card.

SYSTEM DESIGN AND INTERFACE INFORMATION

Power Up and Power Down Protection

AMD’s Flash memory devices are designed to protect against accidental programming or erasure caused by spurious system signals that might exist during power transitions. The AMD PC Card will power-up into a READ mode when V_{CC} is greater than V_{LKO} of 3.2 V. Erasing of memory sectors or memory segments can be accomplished only by writing the proper Erase command to the card along with the proper Chip Enable, Output Enable and Write Enable control signals. Hot insertion of PC cards is not permitted by the PCMCIA standard.

Note: *Hot insertion is defined as the socket condition where the card is inserted or removed with any or all of the following conditions present: $V_{CC} = V_{CCH}$, $V_{PP} = V_{PPH}$, address and/or data lines are active).*

System Power Supply Decoupling

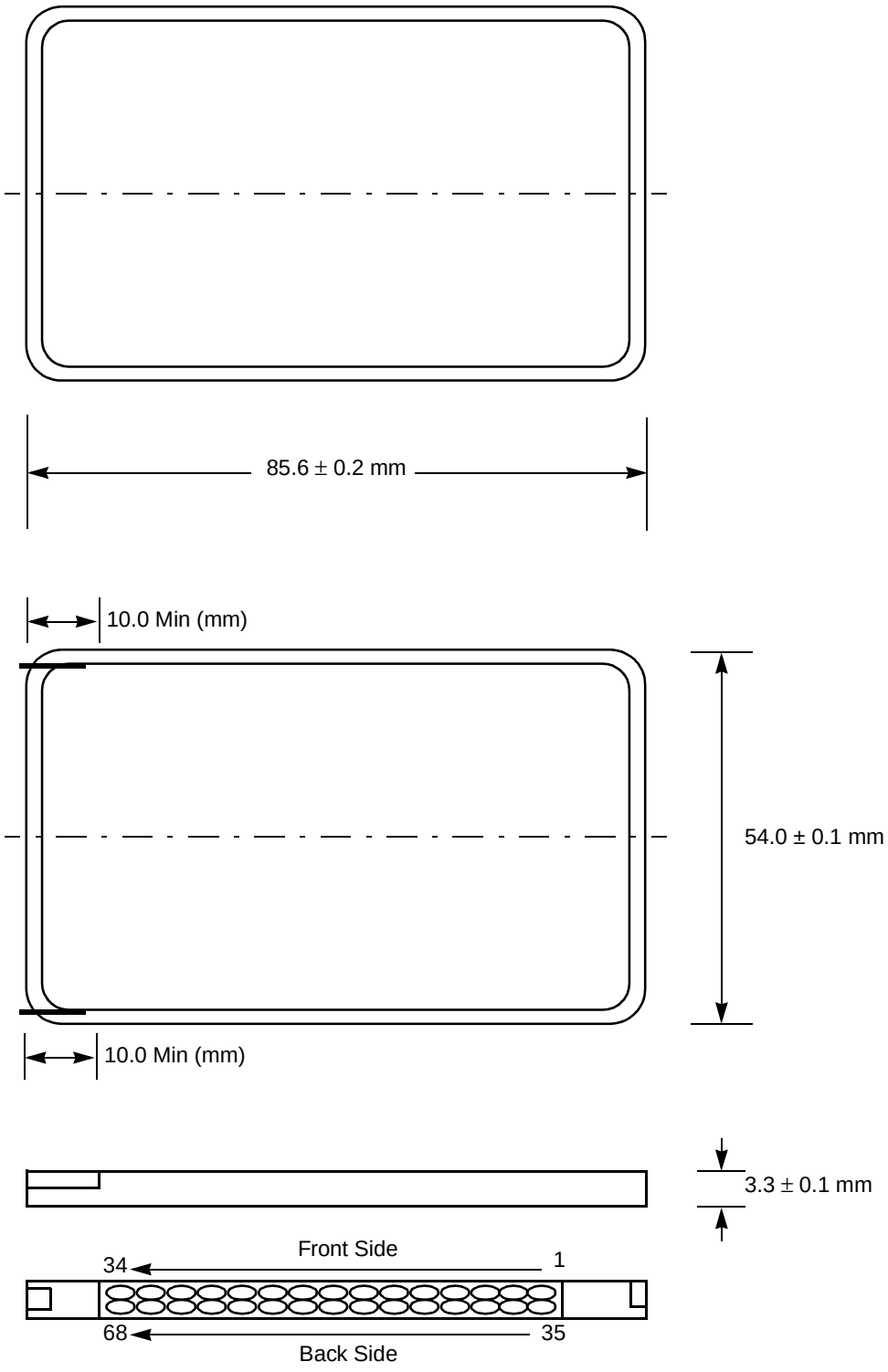
The AMD Flash memory card has a 0.1 µF decoupling capacitor between the V_{CC} and the GND pins. It is recommended the system side also have a 4.7 µF capacitor between the V_{CC} and the GND pins.

Table 10. AMD's CIS for "C" Series Card

Tuple Address	2 Mbyte Card Tuple Value	Tuples and Remarks
00h	01h	CISTPL_DEVICE [Common Memory]
02h	03h	TPL_LINK
04h	53h	Flash Device, Card Speed: 53h = 150 ns
06h	0Dh/06h/FCh/9Dh	Card Size: 0Dh = 1 MB, 06h = 2 MB, FCh = 4 MB, 9Dh = 10 MB
08h	FFh	End of Tuple
0Ah	18h	CISTPL_JEDEC [Common Memory]
0Ch	02h	TPL_LINK
0Eh	01h	AMD MFG ID Code
10h	A4h	Device ID Code: A4h = 4 Mbit Device
12h	1Eh	CISTPL_DEVICEGEO
14h	06h	TPL_LINK no FFh terminator
16h	02h	DGTPL_BUS: Bus Width
18h	11h	DGTPL_EBS: 11h = 64K Byte Erase Block size
1Ah	01h	DGTPL_RBS: Read Byte Size
1Ch	01h	DGTPL_WBS: Write Byte Size
1Eh	01h	DGTPL_PART: Number of partition
20h	01h	FL DEVICE INTERLEAVE: No interleave
22h	15h	CISTPL_VERS1
24h	03h	TPL_LINK
26h	04h	Major version number 1
28h	01h	Minor version for PCMCIA Std. 2.0
2Ah	FFh	End of Tuple
2Ch	17h	CISTPL_DEVICE_A [Attribute Memory]
2Eh	04h	TPL_LINK
30h	47h	EEPROM with extended speed
32h	3Ah	Extended speed = 250 ns
34h	00h	Device Size = 1 unit of 512 byte
36h	FFh	End of Tuple
38h	80h	Vendor-Specific Tuple
3Ah	0Ah	TPL_LINK
3Ch	41h	"A"
3Eh	4Dh	"M"
40h	44h	"D"
42h	26h	"&"
44h	42h	"B"
46h	45h	"E"
48h	52h	"R"
4Ah	47h	"G"
4Ch	00h	END TEXT
4Eh	FFh	End of Tuple
50h	81h	Vendor Specific Tuples: 81h
:	xxh	ASCII Characters
:	xxh	:
6Ah	xxh	ASCII Characters
6Ch	FFh	CISTPL_END

PHYSICAL DIMENSIONS*

Type 1 PC Card



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DATA SHEET SUMMARY FOR AMC0XXCFLKA

PIN DESCRIPTION

Added description for $\overline{REG}$ pin.

Table 3. Even Byte Command Definitions

Each density card now has a list of paired segment numbers. The address increment for Even bytes should be (N/2) * 100000H.

Added Note 5 for clarification. Note 3 requires use of $\overline{CE}$1, not $\overline{CE}$2, and A21. Note 2 was clarified.

Table 4. Odd Byte Command Definitions

Each density card now has a list of paired segment numbers. The address increment for Even bytes should be (N-1/2) * 100000H + 80000H.

Added Note 5 for clarification. Note 3 requires use of $\overline{CE}$2, not $\overline{CE}$1, and A21. Note 2 was clarified.

Autoselect operation data is A4h.

Table 5. Word Command Definitions

Added Note 7 for clarification. Note 3 requires use of $\overline{CE}$1 and $\overline{CE}$2 and A21. Note 5 was modified to reflect that the address should be (Addr) + M * (100000H). Note 2 was clarified.

Autoselect operation data is 0101/A4A4h.

Sector Erase

Clarified that any sector number can be loaded into the sector erase buffer.

Toggle Bit—D6

Added clarification that D6 is used for entering Sector Erase Suspend mode.

Sector Erase Suspend

Repeated sentence was deleted.

Write Operation Status Table

D3 in 'Exceeded Time Limit' mode is 0.

Figure 5. AC Waveforms for Data Polling During Embedded Algorithm Operations

Corrected $t_{WHWH3\ or\ 4}$. Removed erroneous t_{OE} reference.

Figure 6. AC Waveforms for Toggle Bit During Embedded Algorithm Operations

Clarified diagram.

Embedded Algorithm Flow Charts

Figures 6, 7, 11 references to 14 µs time outs were corrected to 16 µs.

DC Characteristics—Byte-Wide Operation

Note 1 has been modified to show standby current is increased by: 19 mA for 10 Mb, 7 mA for 4 Mb, 3 mA for 2Mb and 1 mA for 1 Mb card in TTL modes.

DC Characteristics—Word-Wide Operation

For $\overline{CE}$, $\overline{REG}$, $\overline{WE}$, $\overline{OE}$, I_{IL} minimum is –300 µA. Note 1 has been modified to show standby current is increased by: 18 mA for 10 Mb, 6 mA for 4 Mb, and 2 mA for 2 Mb card in TTL modes.

AC Characteristics—Write/Erase/Program Operations

t_{WHWH4} applies to 64K Byte sectors. Note 1 was modified to exclude the statement regarding preprogramming time.

Figure 19. AC Waveforms for Byte Write Operations

t_{WHWH1} is now t_{WHWH3}. The Unlock address was changed to AAAAh according to the Byte Write sequence. Added t.

AC Characteristics—Alternate CE Controlled Writes—Write/Erase/Program Operations

t_{WHWH4} applies to 64K Byte sectors. Note 1 was modified to exclude the statement regarding preprogramming time.

Figure 20. Alternate $\overline{CE}$ Controlled Byte Write Operation Timings

Added t_{VCS} and $t_{EHEH3\ or\ 4}$ to Figure 18.

Table 10. AMD's CIS for AmC0XXCFLKA

Removed bracketed reference for Tuple Address 04h. Tuple Address 32h now reflects CIS memory speed of 250 ns (3Ah).

Revision B+1

Sector Erase Suspend

Removed the statement requiring the address of a sector not being erased for valid D6 status.