FIBRE CHANNEL BIT STREAM MONITOR WITH REPEATER S2075

FEATURES

- Repeater with parallel monitor function
- Selectable parallel input provides local control of serial bit stream
- 1062MHz (Fibre Channel) line rates
- Half and full VCO output rates
- Functionally compliant ANSI X3T11 Fibre Channel Specification
- TTL Bypass Select
- Transmitter incorporating phase-locked loop (PLL) clock synthesis from low speed reference
- Repeater PLL provides clock and data recovery
- 10 bit parallel TTL compatible interface
- Low-jitter serial LVPECL compatible interface
- Local loopback
- Single +3.3V supply, 600 mW power dissipation
- 64 PQFP package
- Continuous downstream clocking from parallel output
- Drives 30m of Twinax cable directly

APPLICATIONS

- Storage area network
- Workstation
- Frame buffer
- Switched networks
- Data broadcast environments
- Proprietary extended backplanes

GENERAL DESCRIPTION

The S2075 bit stream monitor with repeater facilitates high speed serial transmission of data over fiber optic, coax, or twinax interfaces. The device conforms to the requirements of the ANSI X3T11 Fibre Channel specification, and runs at 1062 Mbps data rates with an associated 10-bit data word.

The chip provides a repeater function with serial-to-parallel conversion for monitoring the serial bit stream. An on-chip PLL performs clock recovery and data retiming of the serial bit stream. In transceiver mode, parallel data from the local controller is injected onto the serial bit stream. In this mode, the transmit PLL synthesizes the high-speed clock from a low speed reference.

The serial I/O support LVPECL compatible signals for copper or fiber optic component interfaces with excellent signal integrity. Local loopback mode allows for system diagnostics. The chip requires a +3.3V power supply and dissipates 600 mW under typical conditions.

The S2075 can be used for a variety of applications including Fibre Channel, serial backplanes, and proprietary point-to-point links. Figure 1 shows a typical configuration incorporating the chip.

Figure 1. System Block Diagram

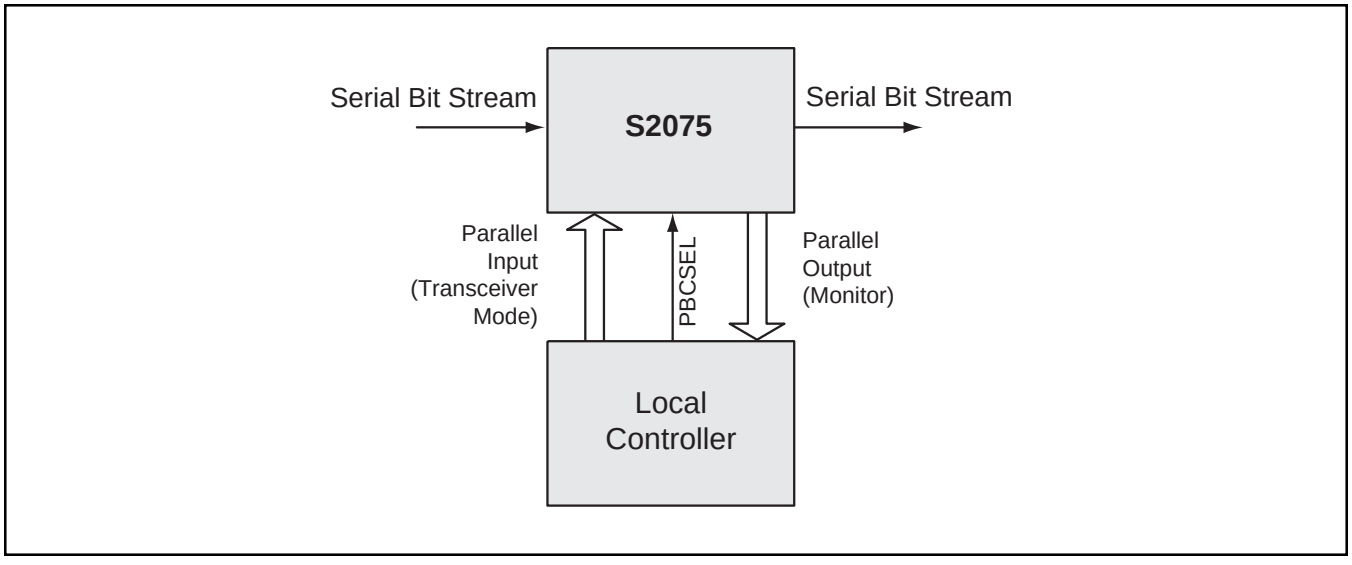
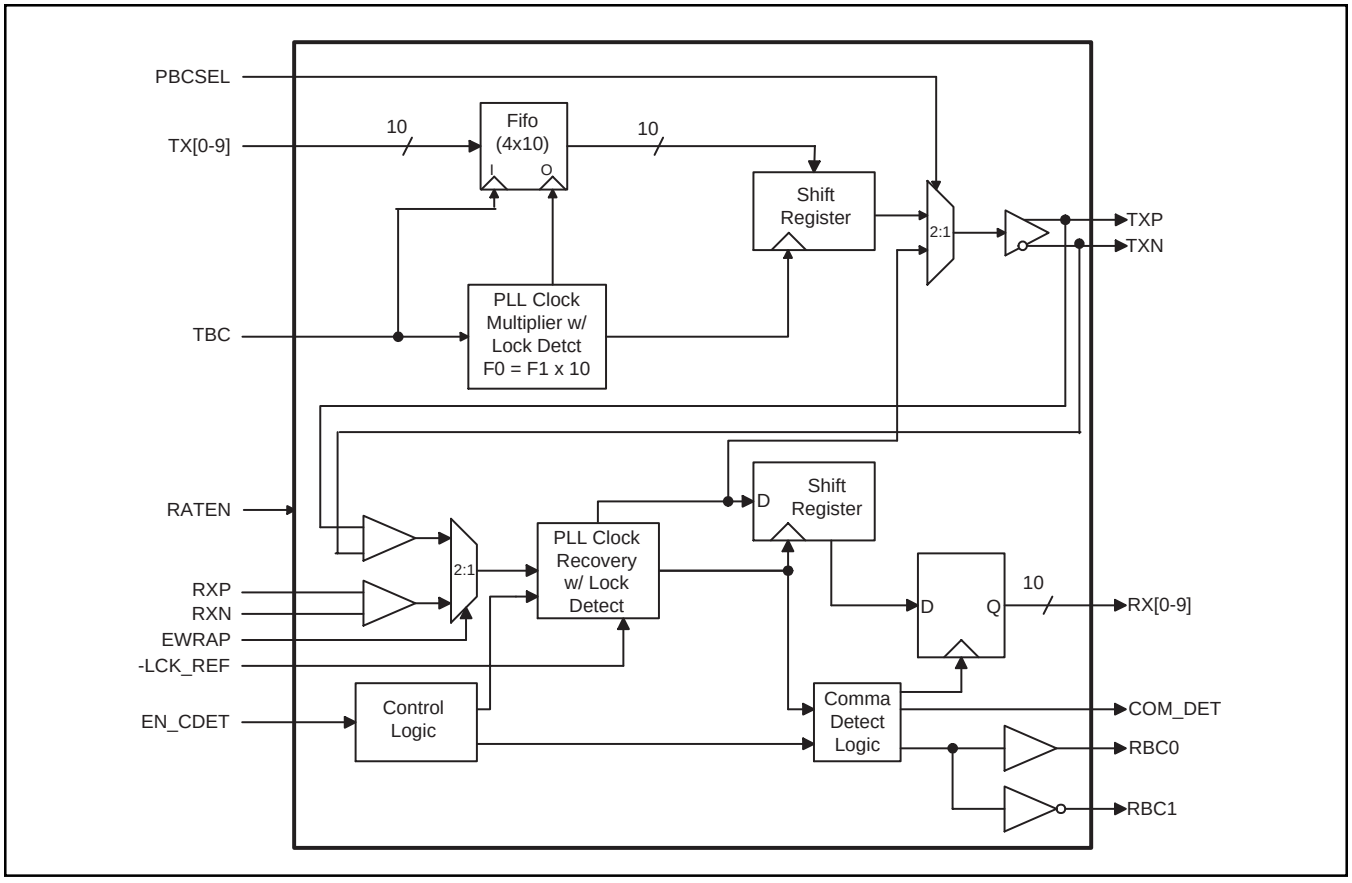


Figure 2. Functional Block Diagram



S2075 OVERVIEW

The S2075 provides repeater serialization and deserialization functions for block encoded data to implement a Fibre Channel interface. The S2075 functional block diagram is depicted in Figure 2.

The device operates in two basic modes, controlled by the PBCSEL input, as shown in Table 1. In monitor mode, the parallel input is unused, the device functions as a repeater with parallel output monitor capability. In transceiver mode, the device functions as a fibre channel transceiver. The sequence of operation for each mode is as follows:

Monitor Mode

1. Serial Input
2. Clock and data recovery

3a. Serial output

3b. Serial-to-parallel conversion, frame detection, and 10-bit parallel output.

Table 1. Operating Modes

PBCSEL	MODE
1	Transceiver
0	Monitor

Table 2. Data Mapping to 8B/10B Alphabetic Representation

	Data Byte									
TX[0:9] or RX[0:9]	0	1	2	3	4	5	6	7	8	9
8B/10B Alphabetic Representation	a	b	c	d	e	i	f	g	h	j

Transceiver Mode

Transmitter

1. 10-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver

1. Clock and data recoverery from serial input
2. Serial-to-parallel conversion
3. Frame detection
4. 10-bit parallel output

The 10-bit parallel data input to the S2075 should be from a DC-balanced encoding scheme, such as the 8B/10B transmission code, in which information to be transmitted is encoded 8 bits at a time into 10-bit transmission characters[1]. For reference, Table 2 shows the mapping of the parallel data to the 8B/10B codes.

Loop Back

Local loopback provides a capability for performing off-line testing. This is useful for ensuring the integrity of the serial channel before enabling the transmission medium. It also allows for system diagnostics.

Repeater

1. Fully differential for minimum deterministic jitter accumulation (10 ps nominal).
2. High speed LVPECL I/O.

[1]A.X. Widmer and P.A. Franaszek, "A Byte Oriented DC Balanced (0,4) 8B/10B Transmission Code," IBM Research Report RC 9391, May 1982.

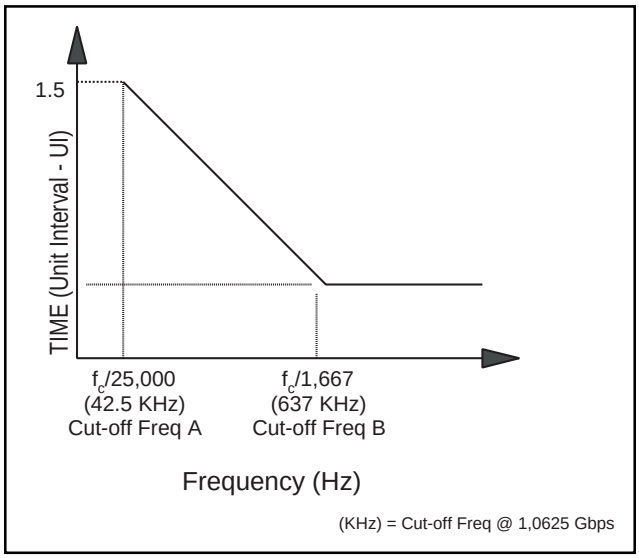
REPEATER DESCRIPTION

The S2075 provides serial input/output with a Clock Recovery Unit (CRU) and a parallel output for monitoring of the serial bit stream. The S2075 retimes incoming serial data, detects whether a valid character is present, and outputs both a low jitter serial data stream, and a 10-bit parallel data stream for monitoring of the serial data. The S2075 complies with the minimum jitter tolerance requirements proposed by the Fibre Channel Jitter Working Group.

Jitter Performance

Jitter tolerance is defined as the amplitude of jitter that causes the clock recovery PLL to violate the BER specifications. This is specified as Frequency Dependent, Random, and Deterministic jitter tolerance. Frequency Dependent jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter applied at the input. Figure 3 shows the Frequency Dependent Jitter tolerance mask. Random jitter tolerance is the amount of jitter with a Gaussian distribution (noise) that the clock recovery PLL must tolerate. Deterministic jitter tolerance is the amount of jitter that is due to non-Gaussian events that the clock recovery PLL must tolerate.

Figure 3. Frequency Dependent Jitter Tolerance Mask



TRANSMITTER DESCRIPTION

The S2075 accepts 10-bit parallel input data and serializes it for transmission over fiber optic or coaxial cable media. The chip is fully compatible with the ANSI X3T11 Fibre Channel standard, and supports the Fibre Channel data rate of 1062 Mbps. The S2075 uses a PLL to generate the serial rate transmit clock. The transmitter runs at 10 times the TBC input clock, and operates in either full rate or half rate mode. At the full VCO rate the transmitter runs at 1.062 GHz, while in half rate mode it operates at 531 MHz.

Parallel-to-Serial Conversion

The parallel-to-serial converter takes in 10-bit wide data from the input latch and converts it to a serial data stream. Parallel data is latched into the transmitter on the positive going edge of TBC. The data is then clocked into the serial output shift register. The shift register is clocked by the internally generated bit clock which is 10x the TBC input frequency. TX[0] is transmitted first.

Transmit Byte Clock (TBC)

The Transmit Byte Clock input (TBC) must be supplied from a clock source with 100 ppm tolerance to assure that the transmitted data meets the Fibre Channel frequency limits. The internal serial clock is frequency locked to TBC (106.2 MHz).

TBC may be 53.1 MHz or 106.2 MHz, determined by the state of the RATEN input. Operating rates are shown in Table 3.

Transmit Latency

The average transmit latency is 4 byte times.

Table 3. Operating Rates

RATEN	Parallel Input Rate (Mbps)	TBC Frequency (MHz)	Serial Output Rate (Gbps)
0	106.2	106.2	1.062
1	53.1	53.1	0.531

RECEIVER DESCRIPTION

Whenever a signal is present, the receiver attempts to recover the serial clock from the received data stream. The S2075 searches the serial bit stream for the occurrence of a positive polarity comma sync pattern (0011111xxx positive running disparity) to perform word synchronization. Once synchronization on both bit and word boundaries is achieved, the receiver provides the decoded data on its parallel outputs.

Clock Recovery Function

Clock recovery is performed on the input data stream. A simple state machine in the clock recovery macro decides whether to acquire lock from the serial data input or from the reference clock. The decision is based upon the frequency and run length of the input serial data.

The lock to reference frequency criteria ensure that the S2075 will respond to variations in the serial data input frequency (as compared to the reference frequency). The new lock state is dependent upon the current lock state, as shown in Table 4. The run-length criteria ensure that the S2075 will respond appropriately and quickly to a loss of signal. The run-length checker flags a condition of consecutive ones or zeros across 12 parallel words. Thus, 119 or less consecutive ones or zeros does not cause signal loss, 129 or more causes signal loss, and 120 – 128 may or may not, depending on how the data aligns across byte boundaries. If both the off-frequency detect test and the run-length test is satisfied, the CRU will attempt to lock to the incoming data.

Table 4. Lock to Reference Frequency Criteria

Current Lock State	PLL Frequency (vs. TBC)	New Lock State
Locked	< 488 ppm	Locked
	488 to 732 ppm	Undetermined
	> 732 ppm	Unlocked
Unlocked	< 244 ppm	Locked
	244 to 366 ppm	Undetermined
	> 366 ppm	Unlocked

In any transfer of PLL control between the serial data and the reference clock, the RBC0 and RBC1 remain phase continuous and glitch free, assuring the integrity of downstream clocking.

Reference Clock Input

The reference clock must be provided from a low jitter clock source. The frequency of the received data stream must be within 400 ppm of the reference clock to ensure reliable locking of the receiver PLL. A single reference clock is provided to both the transmit and receive PLLs.

Data Output

The S2075 provides either framed or unframed parallel output data, determined by the state of EN_CDET. With EN_CDET held ACTIVE, the S2075 will detect and align to the 8B/10B comma codeword anywhere in the data stream. When EN_CDET is INACTIVE, no attempt is made to synchronize on any particular incoming character. The S2075 will achieve bit synchronization within 250 bit times and begin to deliver unframed parallel output data words whenever it has received full transmission words. Upon change of state of the EN_CDET input, the COM_DET output response will be delayed by a maximum of 3 byte times.

The COM_DET output signal is ACTIVE whenever EN_CDET is active and the comma control character is present on the RX[0-9] parallel data outputs. The COM_DET output signal will be INACTIVE at all other times.

Parallel Output Clock Rate and Data Stretching

The S2075 supports both full rate and half rate outputs, selected via the RATEN input. Table 5 shows the operating rate scenarios. When RATEN is INACTIVE, a data clock is provided on RBC1 at the data rate. Data should be clocked on the rising edge of RBC1. When RATEN is ACTIVE the device is in full rate mode, and complementary TTL clocks are provided on the RBC0 and RBC1 outputs at 1/2 the data rate as required by the Fibre Channel standard. Data is clocked on the rising edges of both RBC0 and RBC1. See Figures 8 and 9.

Fibre Channel and Gigabit Ethernet standards require that the comma sync character appears on the rising edge of the RBC1 signal. In full rate mode the phase of the data is adjusted such that this requirement is met. No alignment is necessary when the S2075 is operating in half rate mode since the output clock frequency is equal to the parallel word rate (RATEN INACTIVE).

In ethernet applications it is illegal for multiple consecutive comma characters to be generated. However, multiple consecutive comma characters can occur in serial backplane applications. The S2075 is able to operate properly when multiple consecutive comma characters are received: after the first comma is detected and aligned, the RBC0/RBC1 clock operates without glitches or loss of cycles. Additionally, COM_DET stays high while multiple commas are being output.

Receive Latency

The average receive latency is 8 byte times.

Table 5. Operating Rates

RATEN	Serial Input Rate (Gbps)	RBC0 (MHz)	RCB1 (MHz)	Parallel Output Rate (Mbps)
0	1.062	53.1	53.1	106.2
1	0.531	N/A	53.1	53.1

Table 6. Pin Description and Assignment

Pin Name	Level	I/O	Pin #	Description
TX[9] TX[8] TX[7] TX[6] TX[5] TX[4] TX[3] TX[2] TX[1] TX[0]	TTL	I	13 12 11 9 8 7 6 4 3 2	Transmit Data. Parallel data on this bus is clocked in on the rising edge of TBC. TX[0] is transmitted first.
TBC	LVTTL	I	22	Transmit Byte Clock. Reference clock input to the PLL clock multiplier. The frequency of TBC is the bit rate divided by 10. When TESTEN is active, TBC replaces the VCO clock to facilitate factory test. TBC should be supplied by a crystal controlled reference since jitter on this line directly translates to jitter on the output data.
RATEN	TTL	I	14	Rate Select. Active Low. This signal configures the PLL's for the appropriate TBC frequency. When High, the operating range is 531 MHz. When Low, the operating range is 1.062 GHz. See Tables 3 and 5.
EN_CDET	TTL	I	24	Enable Comma Detect. When High, enables detection of the comma sync pattern to set the word frame boundary for the data to follow. When Low, data is treated as unframed.
EWRAP	TTL	I	19	Enable Wrap. When High, the transmitter serial data outputs are internally routed to the receiver serial data inputs. TXP/N are static (logic 1) in this state. When Low, the RXP/N serial inputs are selected (normal operation).
RXP RXN	Diff. LVPECL	I	54 52	(Externally capacitively coupled.) LVPECL Receive Serial Data Inputs. RXP is the positive differential input, RXN is negative. Internally biased to VCC -1.3 V.
-LCK_REF	TTL	I	27	Active Low. Lock to Reference Input. When High or open, the receive PLL will lock to the incoming data (normal operation). When Low, the receive PLL is forced to lock to the TBC input.

Table 6. Pin Description and Assignment (Continued)

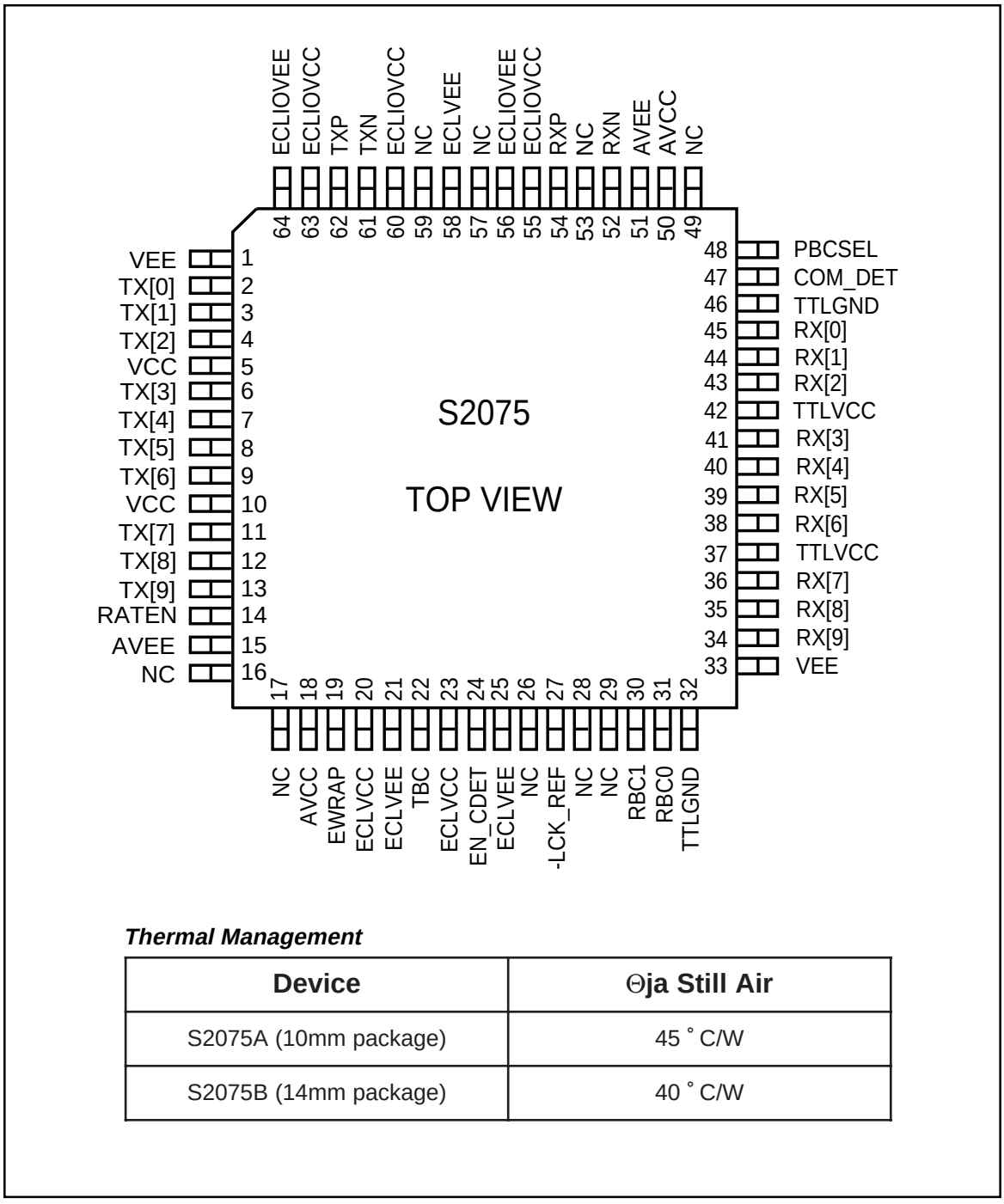
Pin Name	Level	I/O	Pin #	Description
RX[9] RX[8] RX[7] RX[6] RX[5] RX[4] RX[3] RX[2] RX[1] RX[0]	TTL	O	34 35 36 38 39 40 41 43 44 45	Receive Data Outputs. For full rate output, parallel data on this bus is valid on the rising edges of RBC0 and RBC1. RX[0] is the first bit received.
RBC1 RBC0	TTL	O	30 31	Complementary Receive Byte Clocks. In full rate mode, parallel receive data is valid on the rising edges of RBC0 and RBC1 (see Figure 9, timing diagram). For half rate, output data is valid on the rising edge of RBC1.
COM_DET	TTL	O	47	Comma Detect. When EN_CDET is active, COM_DET indicates that the sync character is present on the parallel bus bits RX[0-9]. Upon detection of the comma sync character (0011111xxx positive polarity) this output data is valid on the rising edge of RBC1 and remains High for one RBC1 clock period. When EN_CDET is inactive, COM_DET is held Low (logic 0). Upon change of state of the EN_CDET input, the COM_DET output response will be delayed by a maximum of 3 byte times.
TXP TXN	Diff. LVPECL	O	62 61	Transmit Serial Data. These lines are static (TXN HIGH, TXP HIGH) when EWRAP is active. These lines are static (TXN HIGH, TXP LOW) when TXRST is active. Upon startup, these outputs are held static (TXN HIGH, TXP LOW) until the TXPLL has locked to the reference clock. Each output can drive 150 Ohms to ground.
PBCSEL	TTL		48	Port Bypass Control Select. When High or open, data input on TX[0-9] is passed out on serial output TXP/N. When Low, receiver serial data input is internally routed to the transmitter serial data output. See Table 1.

Note: All TTL inputs have internal 15KΩ pull-up networks.

Table 7. Power and Ground Signals

Pin Name	Level	Pin #	Description
ECLVCC	+3.3V	20, 23	Core +3.3V
ECLVEE	GND	21, 25, 58	Core Ground
ECLIOVCC	+3.3V	55, 60, 63	LVPECL I/O Power Supply (+3.3V)
ECLIOVEE	GND	56, 64	LVPECL I/O Ground
TTLVCC	+3.3V	37, 42	TTL Power Supply (+3.3V)
TTLGND	GND	32, 46	TTL Ground
AVCC	+3.3V	18, 50	Analog Power Supply (+3.3V)
AVEE	GND	15, 51	Analog Ground
VCC	+3.3V	5, 10	Power
VEE	GND	1, 33	Ground
NC	—	16, 17, 26, 28, 29, 49, 53, 57, 59	Not connected

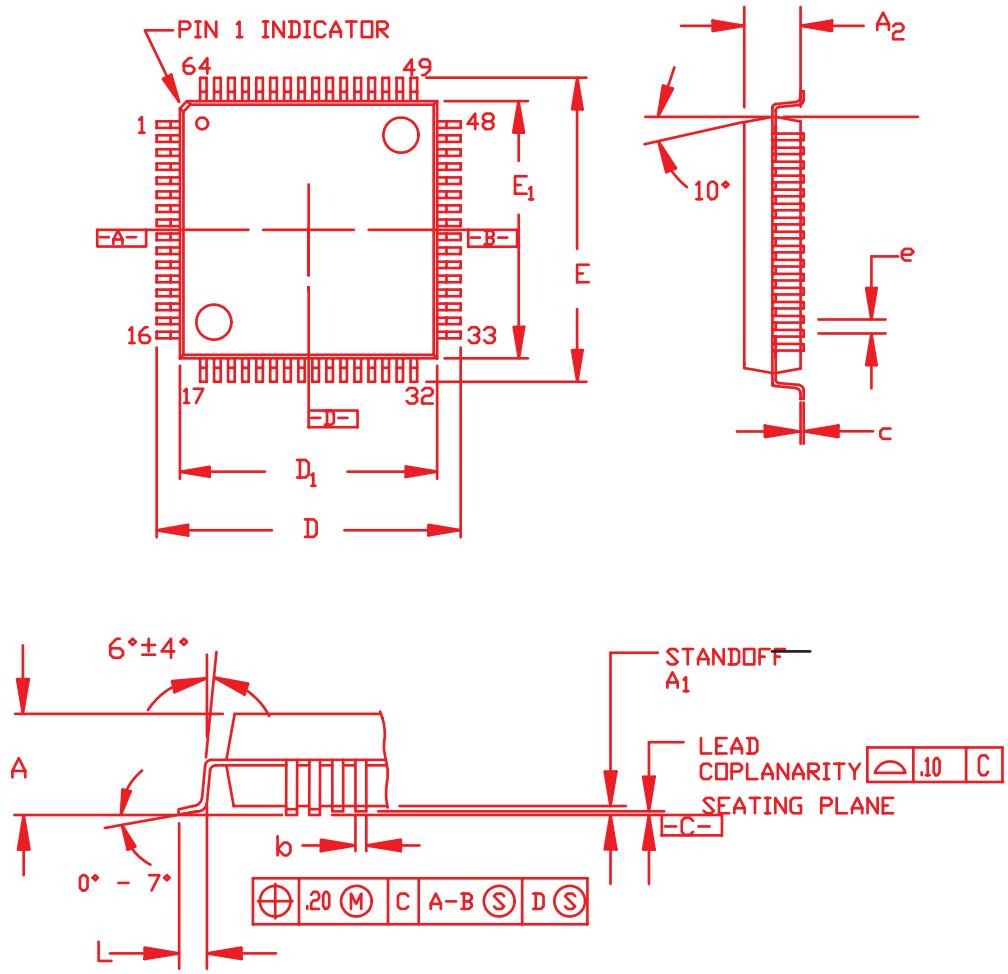
Figure 4. S2075 Pinout



Thermal Management

Device	Θja Still Air
S2075A (10mm package)	45 ˚ C/W
S2075B (14mm package)	40 ˚ C/W

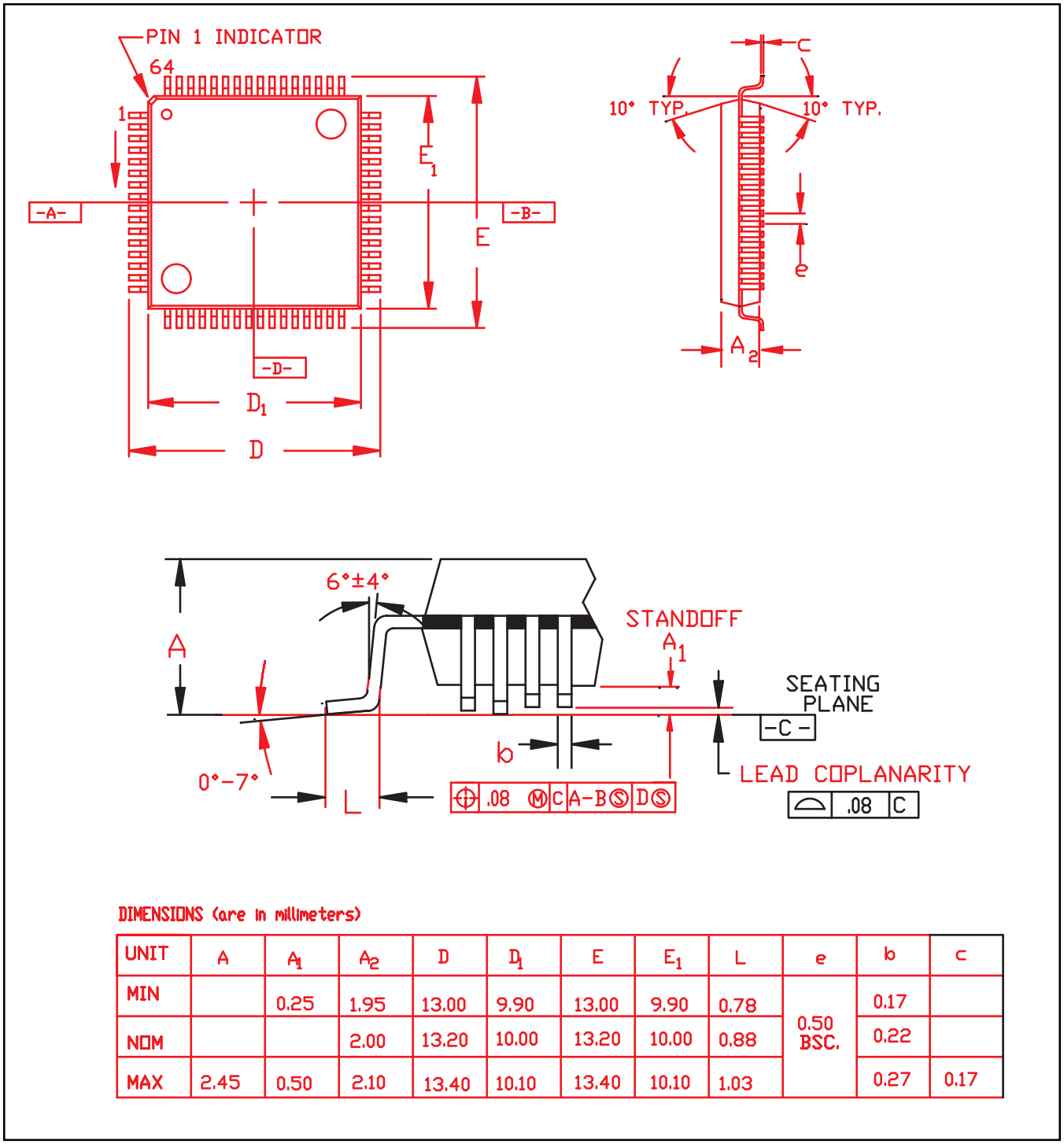
Figure 5. 14mm x 14mm 64 PQFP Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	b	e	c
MIN			1.90	16.95	13.90	16.95	13.90	0.78	0.30	0.80 BSC.	
NOM			2.00	17.20	14.00	17.20	14.00	0.88	0.35		
MAX	2.35	0.25	0.95	17.45	14.10	17.45	14.10	1.03	0.40		0.17

Figure 6. 10mm x 10mm 64 PQFP Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c
MIN		0.25	1.95	13.00	9.90	13.00	9.90	0.78	0.50 BSC.	0.17	
NOM			2.00	13.20	10.00	13.20	10.00	0.88		0.22	
MAX	2.45	0.50	2.10	13.40	10.10	13.40	10.10	1.03		0.27	0.17

Table 8. Power and Ground Application Information

Function	Pin Names	Instructions
ANALOG	AVCC	Connect to low noise or filtered +3.3V supply through a ferrite bead (600Ω at 100 MHz: Murrata BLM31B601S or equivalent). Provide dual local HF bypassing to AVEE (0.1 µf, 100 pf) for low inductance and resistance. A single low inductance 0.1 µf capacitor can be substituted for the pair (Vishay VJ0612 or equivalent, <0.5 nH max inductance).
	AVEE	Connect to ground plane.
LVPECL I/O	ECLIOVCC	Provide low impedance connection to +3.3V. Provide dual local bypassing to GND plane (0.1 µf and 100 pf in parallel, or a single low inductance Vishay VJ0612 or equivalent 0.1 µf capacitor).
	ECLIOVEE	Connect to ground plane.
CORE	ECLVCC	Provide low impedance connection to +3.3V. Provide dual local bypassing to GND plane (0.1 µf and 100 pf in parallel, or a single low inductance Vishay VJ0612 or equivalent 0.1 µf capacitor).
	ECLVEE	Connect to ground plane.
LVTTL I/O	LVTTLVCC	Provide low impedance connection to +3.3V. Provide dual local bypassing to GND plane (0.1 µf and 100 pf in parallel, or a single low inductance Vishay VJ0612 or equivalent 0.1 µf capacitor).
	LVTTLVEE	Connect to ground plane.

Figure 7. Power and Ground Connection Diagram

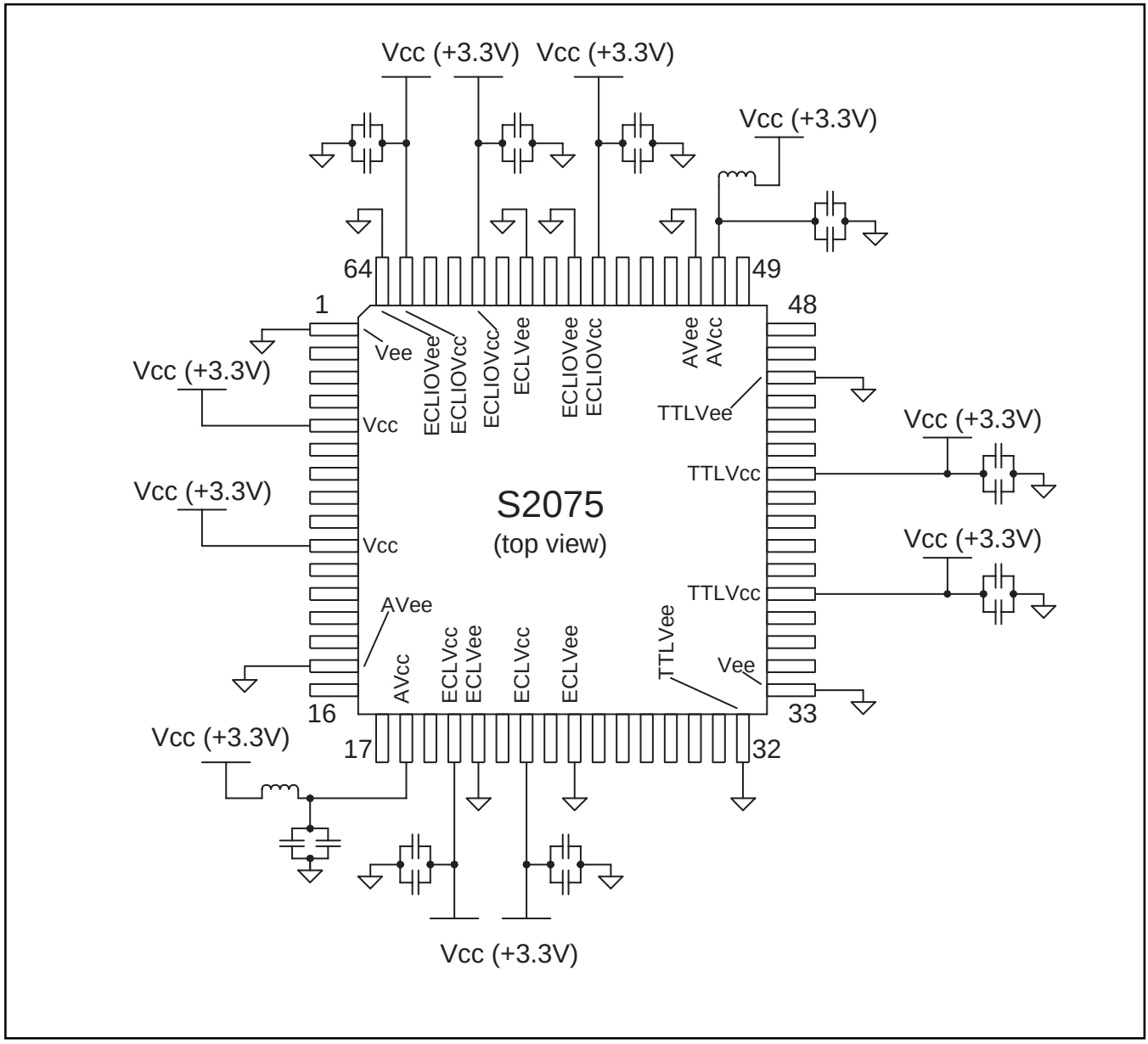


Figure 8. Transmitter Timing

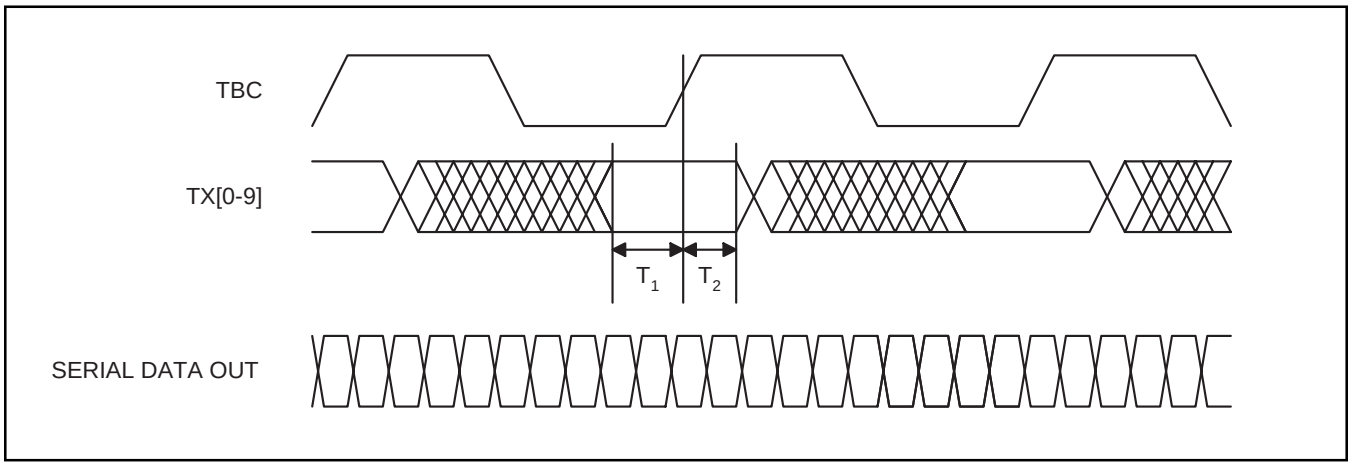


Table 9. S2075 Transmitter Timing

Parameters	Description	Min	Max	Units	Conditions
T_1	Data Setup w.r.t. ↑ TBC	2.0	-	ns	See Note 1.
T_2	Data Hold w.r.t. ↑ TBC	1.0	-	ns	
T_{SDR}, T_{SDF}	Serial Data Rise and Fall	-	300	ps	20% - 80%, tested on sample basis.
T_J	Serial Data Output total jitter (p-p)	-	0.23	UI	Peak-to-peak, measured on sample basis. Measured with ±K28.5 or 2^7-1 pattern at 1.062 GHz.
T_{DJ}	Serial Data Output deterministic jitter (p-p)	-	0.08	UI	Peak-to-peak, tested on a sample basis. Measured with ±K28.5 pattern at 1.062 GHz.

1. All AC measurements are made from the reference voltage level of the clock (+1.4V) to the valid input or output data levels (+.8V or +2.0V).

Figure 9. Receiver Timing Full Rate Mode (RATEN Active)

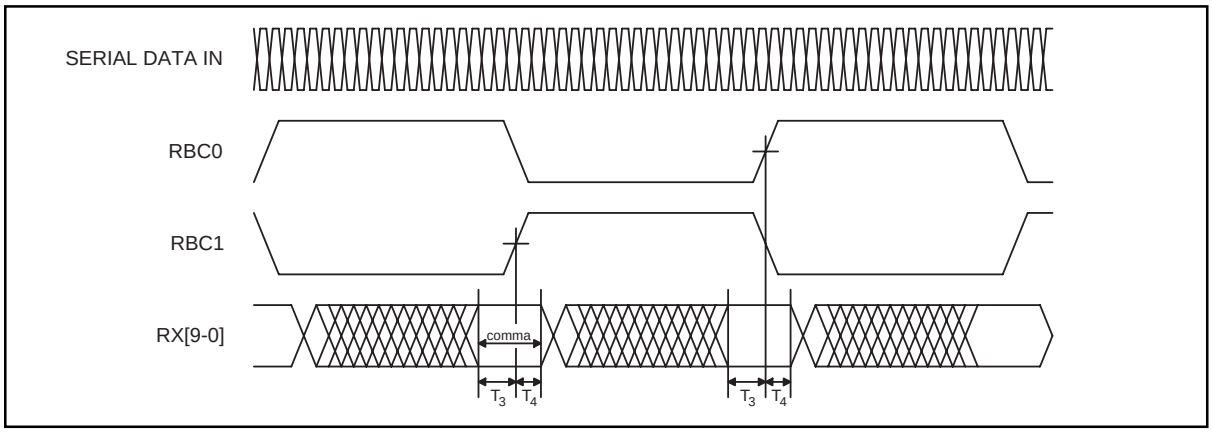


Figure 10. Receiver Timing Half Rate Mode (RATEN Inactive)

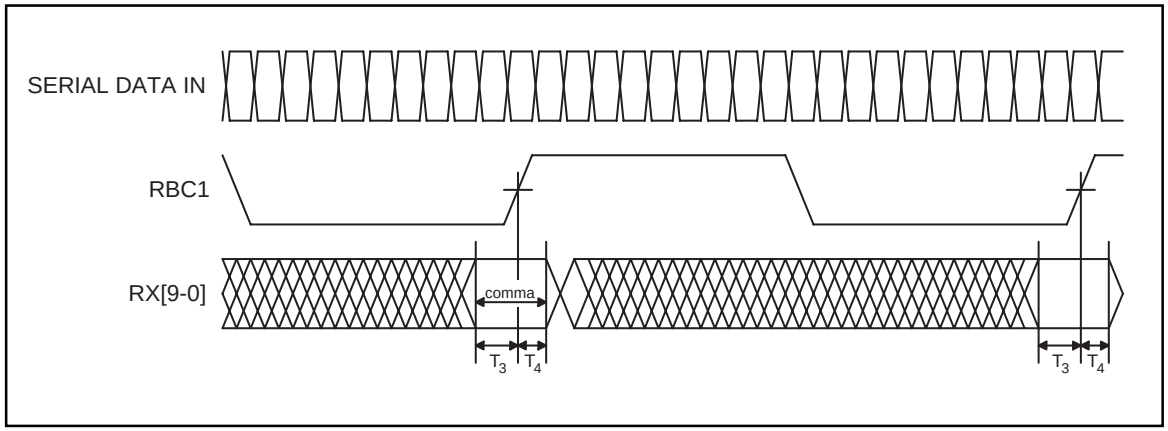


Table 10. S2075 Receiver Timing

Parameters	Description	Min	Max	Units	Conditions
T_3	Data Setup w.r.t. ↑ RBC1/0 (full rate)	3.0	-	ns	
T_4	Data Hold w.r.t. ↑ RBC1/0 (full rate)	1.5	-	ns	
T_5	Data Setup w.r.t. ↑ RBC1/0 (half rate)	6.0	-	ns	
T_6	Data Hold w.r.t. ↑ RBC1/0 (half rate)	5.0	-	ns	
T_{RCR}, T_{RCF}	RBC1, RBC0 Rise and Fall Time	-	2.4	ns	Measured +.8V to +2.0V.
T_{DR}, T_{DF}	Data Output Rise and Fall Time	-	3.0	ns	Measured +.8V to +2.0V.
T_{LOCK} (startup)	Startup acquision lock time (1.062G)	-	2.5	µs	
T_{LOCK} (reacquire)	Data Acquisition Lock Time (1.062G)	-	100	ns	90% input data eye (see Figure 17).
		-	250	ns	24% input data eye.
Duty Cycle	RBC1 (RBC0)	35	65	%	
T_J	Total Input Jitter Tolerance	0.7	-	UI	As specified in ANSI 3XT11 Fibre Channel.
T_{DJ}	Deterministic Input Jitter Tolerance	0.38	-	UI	As specified in ANSI 3XT11 Fibre Channel.
T_{RJ}	Random Input Jitter Tolerance	0.22	-	UI	As specified in ANSI 3XT11 Fibre Channel.
T_{FJ}	Frequency Dependent Input Jitter Tolerance	0.1	-	UI	As specified in ANSI 3XT11 Fibre Channel.
R_{Jout}	Random Jitter Out (RMS)	-	20	ps	Tested on a sample basis.
D_{Jout}	Deterministic Jitter Out (p-p)		100	ps	Tested on a sample basis.

1. All AC measurements are made from the reference voltage level of the clock (+1.4V) to the valid input or output data levels (+.8V or +2.0V).

OTHER OPERATING MODES

Test and Reset Functions

S2075 receive and transmit reset functionality are summarized in Table 11 and Table 12. Test functionality is summarized in Table 13.

Loopback Mode

The S2075 supports internal loopback mode in which the serial data from the transmitter replaces external serial data. The loopback function is enabled when the loopback enable signal, EWRAP, is set ACTIVE.

The loopback mode provides the ability to perform system diagnostics and to perform off-line testing of the interface to guarantee the integrity of the serial channel before enabling the transmission medium. Figure 11 shows the basic loopback operation.

Figure 11. Loopback Operation

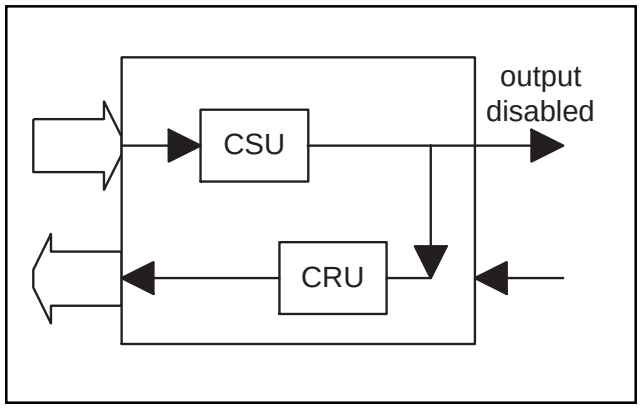


Table 11. Receive Reset Summary

RXRSTN	RX PLL	RX[0-9]	RBC0	RBC1	COM_DET
H	Normal	Normal	Normal	Normal	Normal
L	Reset	Low	Fixed	Fixed	Low

Table 12. Transmit Reset Summary

TXRST	TX PLL	TXP	TXN
H	Reset	Low	High
L	Normal	Normal	Normal

Table 13. Test

TESTN	Internal TX Bitclock	RX PLL Input
H	PLL Output (TBCx10)	Serial Data Stream
L	TBC	TBC

Table 14. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Case Temperature Under Bias	-55		125	˚C
Junction Temperature Under Bias	-55		150	˚C
Storage Temperature	-65		150	˚C
Voltage on VCC with Respect to GND	-0.5		+4.0	V
Voltage on any TTL Input Pin except TBC	-0.5		5.0	V
Voltage on TBC	0		VCC	V
Voltage on any LVPECL Input Pin	0		VCC	V
TTL Output Sink Current			8	mA
TTL Output Source Current			8	mA
Static Discharge Voltage	2000			V

Table 15. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	0		70	˚C
Junction Temperature Under Bias			130	˚C
Voltage on TTLVCC, ECLVCC, ECLIOVCC, and AVCC with respect to GND/VEE	3.13	3.3	3.47	V
Voltage on any TTL Input Pin except TBC	0	VCC	5.0	V
Voltage on any LVPECL Input Pin	VCC -2.0		VCC	V
Voltage on TBC	0		VCC	V

Table 16. Reference Clock Requirements

Parameters	Description	Min	Max	Units	Conditions
FT	Frequency Tolerance	-100	+100	ppm	
TD_{1-2}	Symmetry	40	60	%	Duty Cycle at 50% pt.
T_{RCR}, T_{RCF}	REFCLK Rise and Fall Time		2	ns	20% - 80%.
J_R	Random Jitter		100	ps	Peak-to-Peak.

Table 17. DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Comments
V_{OH}	Output High Voltage (TTL)	2.4	2.8	V_{CC}	V	V_{CC} = min, I_{OH} = 4 mA
V_{OL}	Output Low Voltage (TTL)	GND	0.1	0.4	V	V_{CC} = min, I_{OL} = 1 mA
V_{IH}	Input High Voltage (TTL)	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage (TTL)	GND		0.8	V	
I_{IH}	Input High Current (TTL)			40	µA	V_{IN} = 2.4V, V_{CC} = Max
I_{IL}	Input High Current (TTL)			600	µA	V_{IN} = 0V, V_{CC} = Max
I_{CC}	Supply Current		182	260	mA	Outputs open.
P_D	Power Dissipation		600	900	mW	Outputs open.
V_{DIFF}	Min. differential input voltage swing for differential LVPECL inputs	100		1100	mV	
ΔV_{OUT}	Serial Output Differential Voltage Swing	1200	2000	2200	mV	150Ω to ground.
C_{IN}	Input Capacitance			3	pf	

OUTPUT LOAD

The S2075 serial outputs require a resistive load to set the output current. The recommended resistor value is 150 ohms to ground. This value can be varied to adjust drive current, signal voltage swing, and power usage on the board.

ACQUISITION TIME

With the input eye diagram shown in Figure 17, the S2075 will recover data within the time specified by T_{LOCK} in Table 10 after an instantaneous phase shift of the incoming data.

Figure 12. Serial Input Rise and Fall Time

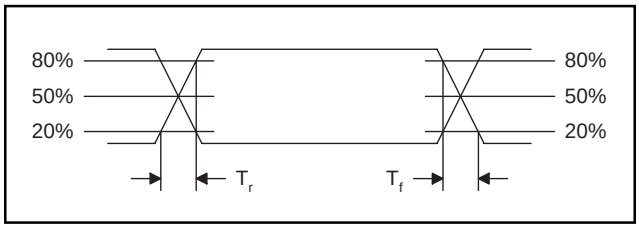


Figure 13. TTL Input/Output Rise and Fall Time

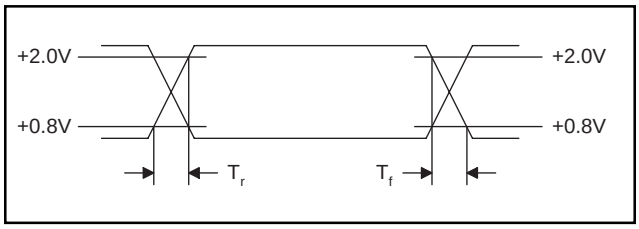


Figure 14. Serial Output Load

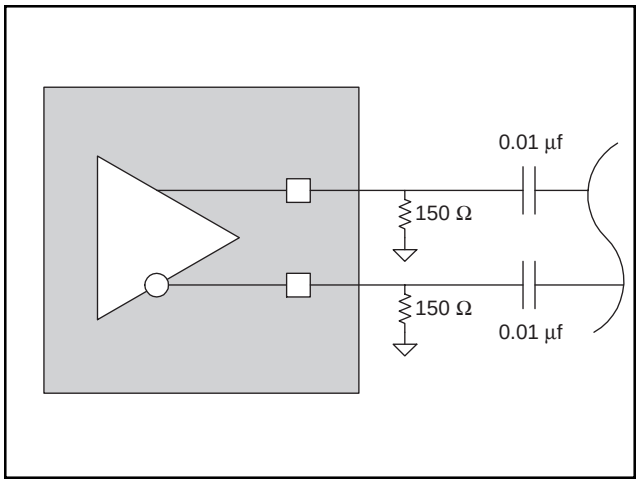


Figure 15. High Speed Differential Inputs

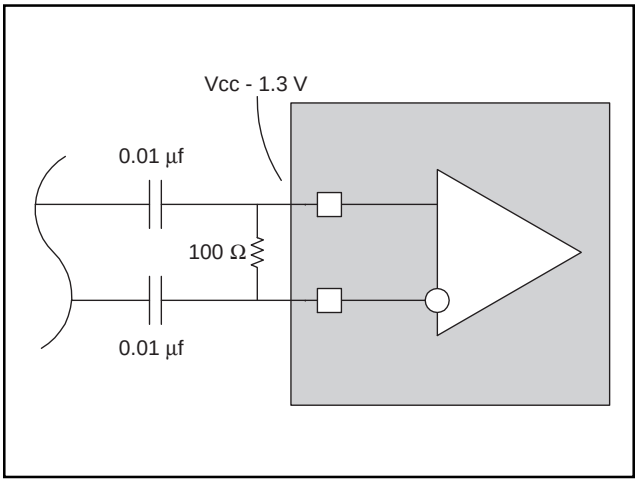


Figure 16. Receiver Input Eye Diagram Jitter Mask

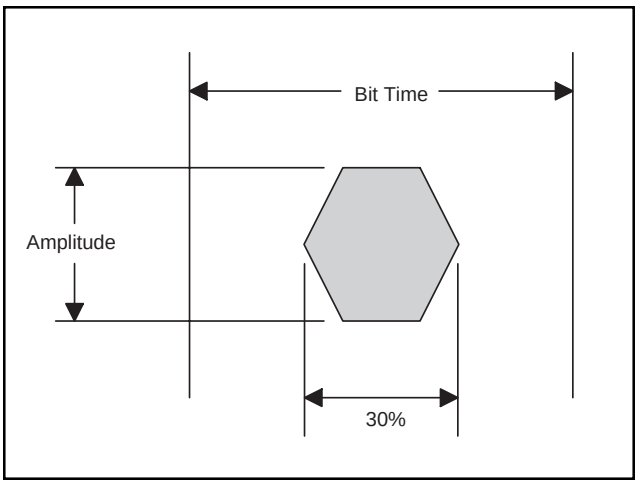
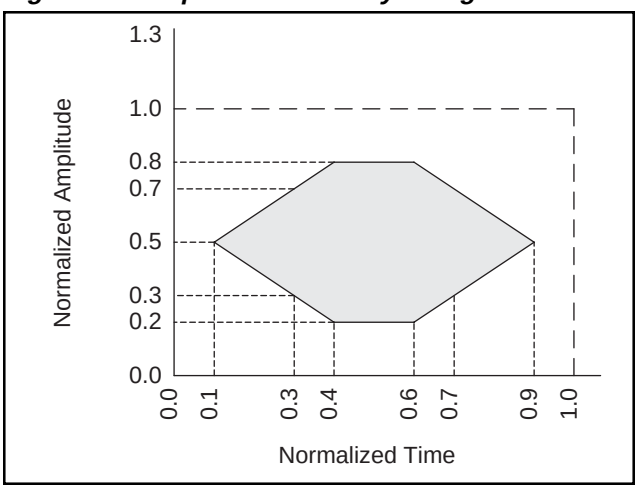
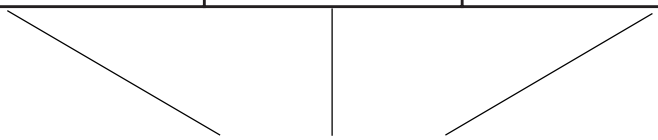


Figure 17. Acquisition Time Eye Diagram



Ordering Information

GRADE	PART NO.	PACKAGE
S- Commercial	2075	A–(64 PQFP 10mm) B–(64 PQFP 14mm)



X Grade XXXX Part No. X Package

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