DDR 13-Bit to 26-Bit Registered Buffer

Features

- Differential clock signals.
- Meets SSTL_2 class II specifications on outputs.
- Low voltage operation: V_{DD} = 2.3V to 2.7V.
- Available in 64-pin TSSOP, 64-pin TVSOP, and 56-pin VFQFN packages.

Product Description

The ASM4SSTVF16859 is a universal 13/26 bit register (D F/F based), designed for 2.3V to 2.7V V_{DD} operation. The device supports SSTL_2 I/O levels, and is fully compliant with the JEDEC JC40, JC42.5 DDR I specifications covering PC1600, PC 2100, PC2700, and PC3200 operational ranges (DDR 400 – 200 MHz). 13/26 bits refers to 2Q outputs for each D input - designed for use in Stacked Registered (stacked Memory Devices), Buffered DIMM applications.

Data flow from D to Q is controlled by the differential clock (CLK/CLKB) and a control signal (RESETB). The positive edge of CLK is used to trigger the data transfer, and CLKB is used to maintain sufficient noise margins, whereas RESETB input is designed and intended for use at power-up.

The ASM4SSTVF16859 supports a low power standby mode of operation. A logic level low at RESETB, assures that all internal registers and outputs (Q) are reset to a logic low state, and that all input receivers, data (D) buffers, and clock (CLK/CLKB) are switched off. Note that RESETB should be supported with a LVCMOS level at a valid state since VREF may not be stable during power-up.

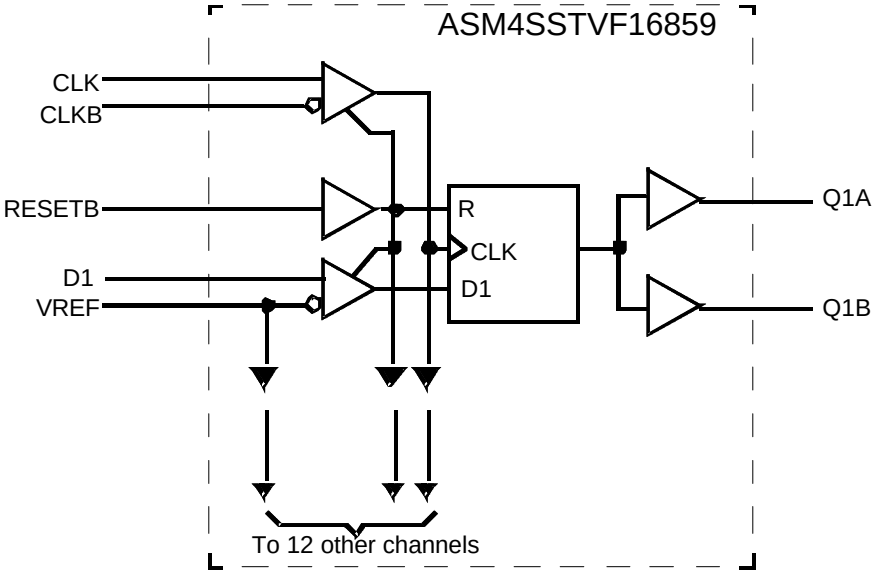
To ensure that outputs are at a defined logic state before a stable clock has been supplied, RESETB must be held at a logic low level during power-up.

In the JEDEC defined Registered DDR DIMM application, RESETB is specified to be asynchronous with respect to CLK/CLKB; therefore, no timing relationship can be guaranteed between the two signals. When entering a low-power standby state, the register will be cleared and the outputs will be driven to a logic low level quickly relative to the time to disable the differential input receivers. This ensures there are no “glitches” on any output. However, when coming out of low power standby mode, the register will become active quickly relative to the time taken to enable the differential input receivers. When the data inputs are at a logic level low and the clock is stable during the low-to-high transition of RESETB until the input receivers are fully enabled, the design ensures that the outputs will remain at a logic low level.

Applications

- JEDEC and Non-JEDEC DDR Memory Modules
  - Stacked or Planar configurations.
  - Supports PC1600 - PC2100 - PC2700 - PC3200
    - DDR 400 compliant (200MHz+).
- SSTL_2 I/O.
- Provides a complete support solution for JEDEC JC42.5 DIMMs’ when used with the ASM5CVF857 Zero Delay Buffer.

Block Diagram



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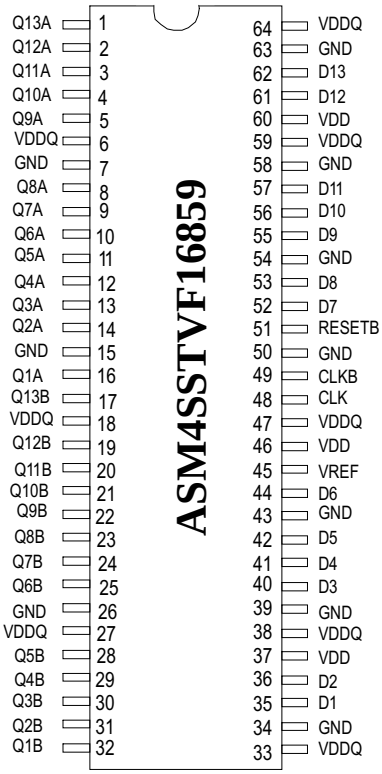
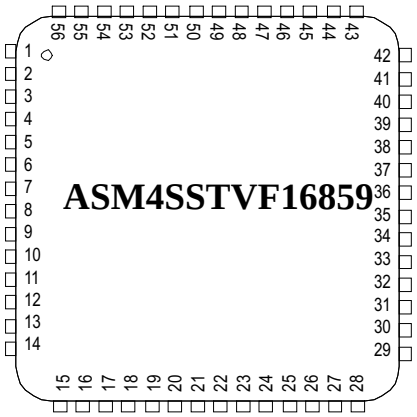
Pin Configurations



64-pin TSSOP
6.10 mm body, 0.50 mm pitch



56-pin VFQFN (MLF2)

Pin Descriptions

64-pin TSSOP

Pin #	Pin Name	Type	Description
1, 2, 3, 4, 5, 8, 9, 10, 11, 12, 13, 14, 16, 17, 19, 20, 21, 22, 23, 24, 25, 28, 29, 30, 31, 32	Q (13:1)	O	Data output.
7, 15, 26, 34, 39, 43, 50, 54, 58, 63	GND	P	Ground to entire chip.
6, 18, 27, 33, 38, 47, 59, 64	VDDQ	P	Output supply voltage, 2.5V nominal.
35, 36, 40, 41, 42, 44, 52, 53, 55, 56, 57, 61, 62	D(13:1)	I	Data input.
48	CLK	I	Positive master clock input.
49	CLKB	I	Negative master clock input.
37, 46, 60	VDD	P	Core supply voltage, 2.5V nominal.
51	RESETB	I	Rest Active low.
45	VREF	I	Input reference voltage, 1.25V nominal.

56-pin MLF2

Pin #	Pin Name	Type	Description
1, 2, 3, 4, 5, 6, 7, 8, 10, 11, 12, 13, 14, 15, 16, 18, 19, 20, 21, 22, 50, 51, 52, 53, 54, 56	Q (13:1)	O	Data output.
37, 48	GND	P	Ground to entire chip.
9, 17, 23, 27, 34, 44, 49, 55	VDDQ	P	Output supply voltage, 2.5V nominal.
24, 25, 28, 29, 30, 31, 39, 40, 41, 42, 43, 46, 47	D(13:1)	I	Data input.
35	CLK	I	Positive master clock input.
36	CLKB	I	Negative master clock input.
26, 33, 45	VDD	P	Core supply voltage, 2.5V nominal.
38	RESETB	I	Rest Active low.
32	VREF	I	Input reference voltage, 1.25V nominal.
-	Center Pad	P	Ground (VFQFN package only)

Truth Table

Inputs				Q Outputs
RESETB	CLK	CLKB	D	Q
L	X or floating	X or floating	X or floating	L
H			H	H
H			L	L
H	L or H	L or H	X	Q_0[2]

Note:
1. H=High signal level, L=Low signal level, = transition from low to high, = transition from high to low, X = don't care
2. Output level before the indicated steady state input conditions were established.

1

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	+150	°C
Supply Voltage	-0.5	3.6	V
Input Voltage[1]	-0.5	V_{DD} + 0.5	V
Output Voltage[1,2]	-0.5	V_{DD} + 0.5	V
Input Clamp Current	± 50		mA
Output Clamp Current	±50		mA
Continuous Output Current	±50		mA
VDD, VDDQ or GND current/pin	100		mA
Package Thermal Impedance[3]	55		°C/W

Note:
1. The input and output negative voltage ratings may be excluded if the input and output clamp ratings are observed.
2. This current will flow only when the output is in the high state level $V_0 > V_{DDQ}$.
3. The package thermal impedance is calculated in accordance with JESD 51.
These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged periods can affect device reliability.

Recomended Operating Conditions - DDRI / DDR333 (PC1600, PC2100, PC2700)*

Parameter	Description		Min	Typ	Max	Unit
V_{DD}	Supply voltage		2.3	2.5	2.7	V
V_{DDQ}	I/O supply voltage		2.3	2.5	2.7	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{TT}	Termination voltage		V_{REF} - 0.04	V_{REF}	V_{REF} + 0.004	V
V_I	Input voltage		0		VDD	V
$V_{IH(DC)}$	DC input high voltage	Data Inputs	V_{REF} + 0.15			V
$V_{IH(AC)}$	AC input high voltage		V_{REF} + 0.31			V
$V_{IL(DC)}$	DC input low voltage				V_{REF} - 0.15	V
$V_{IL(AC)}$	AC input low voltage				V_{REF} - 0.31	V
V_{IH}	Input high voltage level	RESETB	1.7			V
V_{IL}	Input low voltage level				0.7	V
V_{ICR}	Common mode input range	CLK	0.97		1.53	V
V_{ID}	Differential input voltage	CLKB	0.36			V
V_{IX}	Cross-point voltage of differential clock pair		(V_{DDQ}/2) - 0.2		(V_{DDQ}/2) +0.2	V
I_{OH}	High-level output current				-20	mA
I_{OI}	Low-level output current				20	mA
T_A	Operating free-air temperature		0		70	°C

Recomended Operating Conditions - DDRI-400 (PC3200)*

Parameter	Description		Min	Typ	Max	Units
V_{DD}	Supply Voltage		2.5	2.6	2.7	V
V_{DDQ}	I/O supply voltage		2.5	2.6	2.7	V
V_{REF}	Reference voltage		1.25	1.3	1.35	V
V_{TT}	Termination voltage		V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V
V_I	Input voltage		0		V_{DDQ}	V
$V_{IH(DC)}$	DC input high voltage	Data Inputs	V_{REF} + 0.15			V
$V_{IH(AC)}$	AC input high voltage		V_{REF} + 0.31			V
$V_{IL(DC)}$	DC input low voltage				V_{REF} - 0.15	V
$V_{IL(AC)}$	AC input low voltage				V_{REF} - 0.31	V
V_{IH}	Input high voltage level	RESETB	1.7			V
V_{IL}	Input low voltage level				0.7	V
V_{ICR}	Common mode input range	CLK, CLKB	0.97		1.53	V
V_{ID}	Differential input voltage		0.36			V
V_{IX}	Cross-point voltage of differential clock pair		(V_{DDQ}/2) - 0.2		(V_{DDQ}/2) + 0.2	V
I_{OH}	High-level output current				-16	mA
I_{OL}	Low-level output current				16	mA
T_A	Operating free-air temperature		0		70	° C

* Guaranteed by design. Not 100% production tested.

DC Electrical Characteristics - DDRI / DDR333 (PC1600, PC2100, PC2700)

T_A = 0°C to 70°C, V_{DD} = 2.5 ± 0.2V, and V_{DDQ} = 2.5 ± 0.2V (unless otherwise stated)

Guaranteed by design. Not 100% production tested.

Symbol	Parameters	Test conditions		V_{DD}	Min	Typ	Max	Units
V_{IK}		I_I = -18 mA		2.3 V			-1.2	V
V_{OH}		I_{OH} = -100 µA		2.3 V to 2.7 V	V_{DD} - 0.2			V
		I_{OH} = -16 mA		2.3 V	1.95			V
V_{OL}		I_{OL} = 100 µA		2.3 V to 2.7 V			0.2	V
		I_{OL} = 16 mA		2.3 V			0.35	V
I_I	All inputs	$V_I = V_{DD}$ or GND		2.7 V			± 5	µA
I_{DD}	Standby (static)	RESETB = GND	I_O = 0	2.7 V			0.01	µA
	Operating (static)	$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, RESETB = V_{DD}		2.7 V			25	mA
I_{DDD}	Dynamic operating (clock only)	RESETB = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLKB switching 50% duty cycle		2.7 V		30		µA/clock MHz
	Dynamic operating (per each data input)	RESETB = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLKB = switching 50% duty cycle One data input switching at half clock frequency, 50% duty cycle		2.7 V		10		µA/clock MHz/data input
r_{OH}	Output high	I_{OH} = -20 mA		2.3 V to 2.7 V	7		20	W
r_{OL}	Output low	I_{OL} = 20 mA		2.3 V to 2.7 V	7		20	W
$r_{O(D)}$	$\lvert r_{OH} - r_{OL} \rvert$ each separate bit	I_O = 20 mA, T_A = 25° C		2.5 V			4	W
C_i	Data inputs	$V_I = V_{REF}$ ± 310 mV, V_{ICR} = 1.25 V, $V_{I(PP)}$ = 360 mV		2.5 V	2.5		3.5	pF
	CLK and CLKB			2.5 V	2.5		3.5	pF
	RESETB	$V_I = V_{DD}$ or GND		2.5V	2.5		3.5	pF

DC Electrical Characteristics - DDRI - 400 (PC3200)

T_A = 0°C to 70°C, V_{DD} = 2.6 ± 0.2V, and V_{DDQ} = 2.6 ± 0.2V (unless otherwise stated)
Guaranteed by design. Not 100% production tested.

Symbol	Parameters	Test conditions		V_{DD}	Min	Typ	Max	Units
V_{IK}		I_I = -18 mA		2.5 V			-1.2	V
V_{OH}		I_{OH} = -100 µA		2.5 V to 2.7 V	V_{DD} - 0.2			V
		I_{OH} = -8 mA		2.5 V	1.95			V
V_{OL}		I_{OL} = 100 µA		2.5 V to 2.7 V			0.2	V
		I_{OL} = 8 mA		2.5 V			0.35	V
I_I	All inputs	$V_I = V_{DD}$ or GND		2.7 V			± 5	µA
I_{DD}	Standby (static)	RESETB = GND	I_O = 0	2.7 V			0.01	µA
	Operating (static)	$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, RESETB = V_{DD}		2.7 V			25	mA
I_{DDD}	Dynamic operating (clock only)	RESETB = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLKB switching 50% duty cycle		2.7 V		30		µA/clock MHz
	Dynamic operating (per each data input)	RESETB = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLKB = switching 50% duty cycle; One data input switching at half clock frequency, 50% duty cycle		2.7 V		10		µA/clock MHz/data input
r_{OH}	Output high	I_{OH} = -16 mA		2.5 V to 2.7 V	7		20	W
r_{OL}	Output low	I_{OL} = 16 mA		2.5 V to 2.7 V	7		20	W
$r_{O(D)}$	$\lvert r_{OH} - r_{OL} \rvert$ each separate bit	I_O = 20 mA, T_A = 25° C		2.6 V			4	W
C_i	Data inputs	$V_I = V_{REF}$ ± 310 mV, V_{ICR} = 1.25 V,		2.6 V	2.5		3.5	pF
	CLK and CLKB	$V_{I(PP)}$ = 360 mV		2.6 V	2.5		3.5	pF
	RESETB	$V_I = V_{DD}$ or GND		2.6V	2.5		3.5	pF

Timing Requirements**

Guaranteed by design. Not 100% production tested.

Symbol	Parameters		V_{DDQ} = 2.5V±0.2V		V_{DDQ} = 2.6V±0.1V		Units
			Min	Max	Min	Max	
f_{CLOCK}	Clock frequency			200		270	MHz
t_W	Pulse duration, CK, CKLB high or low		2.5		2.5		ns
t_{ACT}*	Differential inputs active time			22		22	ns
t_{INACT}*	Differential inputs inactive time			22		22	ns
t_S	Setup time, fast slew rate	Data before CLK↑, CLKB↓	0.75		0.4		ns
	Setup time, slow slew rate		0.9		0.6		
t_h	Hold time, fast slew rate	Data after CLK↑, CLKB↓	0.75		0.4		ns
	Hold time, slow slew rate		0.9		0.6		

Note:
1. Data inputs must be low for a minimum time of t_{ACT} max, after which RESETB is taken high.
2. Data and clock inputs must be held at valid levels (not floating) for a minimum time of t_{INACT}max after which RESETB is taken low.
3. For data signal input slew rate >=V/ns
4. For data signal input slew rate >=0.5 V/ns and < 1V/ns
5. CLK,CLKB signals input slew rates are >=1V/ns

Switching Characteristics - DDRI / DDR333 (PC1600, PC2100, PC2700)**

Symbol	From (input)	To (output)	VDD = 2.5 V ± 0.2 V			Units
			Min	Typ	Max	
f_{max}			200	–	–	MHz
t_{PD}	CLK, CLKB (TSSOP)	Q	1.1		2.8	ns
	CLK, CLKB (VFQFN[MLF2])	Q	1.1		2.8	ns
t_{phl}	RESETB	Q	–	–	5.0	ns

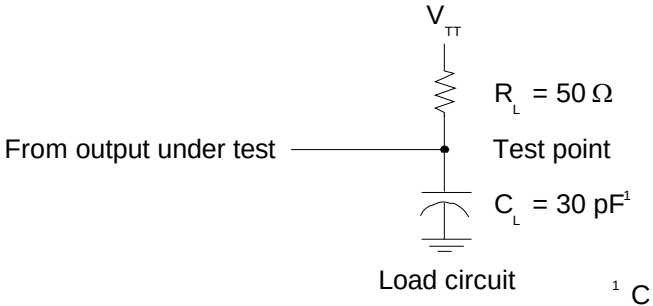
Switching Characteristics - DDRI-400 (PC3200)**

Symbol	From (input)	To (output)	VDD = 2.6 V ± 0.1 V			Units
			Min	Typ	Max	
f_{max}			210			MHz
t_{PD}	CLK, CLKB (VFQFN[MLF2]) Simultaneous switching	Q	1.1		2.2	ns
t_{PDSS}		Q			2.48	ns
t_{phl}	RESETB	Q			3.5	ns

*this parameter is not necessarily production tested.

**Over recommended operating free-air temperature range unless otherwise noted.

Parameter Measurement Information (V_{DD} = 2.5 V ± 0.2 V)



[1] C_L includes probe and jig capacitance.

Voltage and Current Waveforms

In the following waveforms, note that all input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z_o = 50 Ω, input slew rate = 1 V/ns ± 20% (unless otherwise specified).

The outputs are measured one at a time with one transition per measurement.

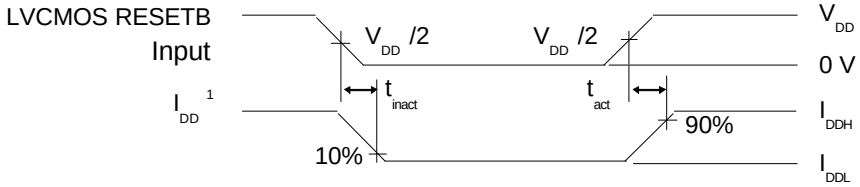
$V_{TT} = V_{REF} = V_{DDQ}/2$.

$V_{IH} = V_{REF}$ + 310 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS input.

$V_{IL} = V_{REF}$ - 310 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.

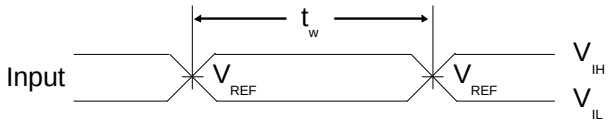
t_{PLH} and t_{PHL} are the same as t_{pd}.

Input active and inactive times

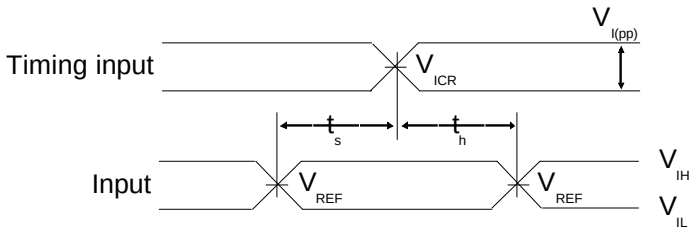


[1] I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0 mA.

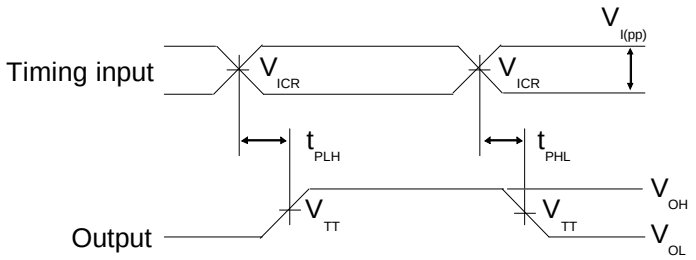
Pulse duration

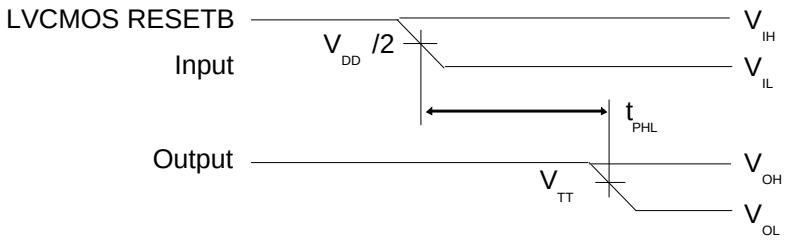


Setup and hold times



Propagation delay times





Output slew rates over recommended operating free-air temperature range (unless otherwise noted)

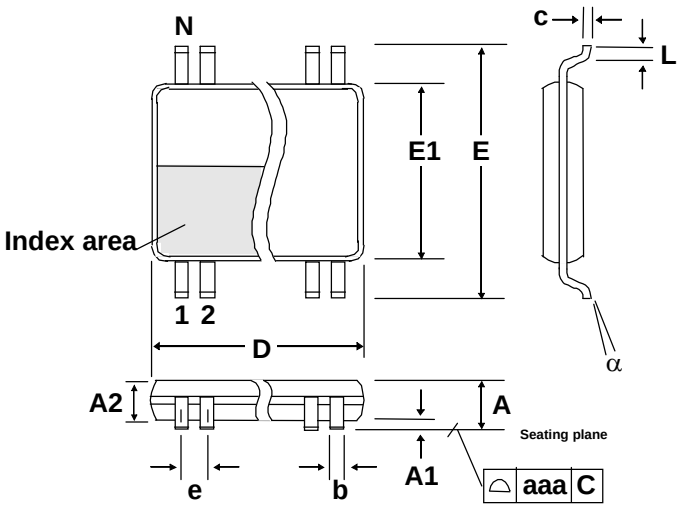
Parameter	From	To	V_{CC}= 2.5 V ± 0.2V *		V_{CC} = 2.6 V ± 0.1 V *		Unit
			Min	Max	Min	Max	
dV/dt_r	20%	80%	1	4	1	4	V/ns
dV/dt_f	80%	20%	1	4	1	4	V/ns
dV/dt_Δ**	20% or 80%	80% or 20%		1		1	V/ns

*For this test condition, V_{DDQ} is always equal to V_{DD}

**Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate)

rev 2.0

Package Dimensions (64- Pin TSSOP)



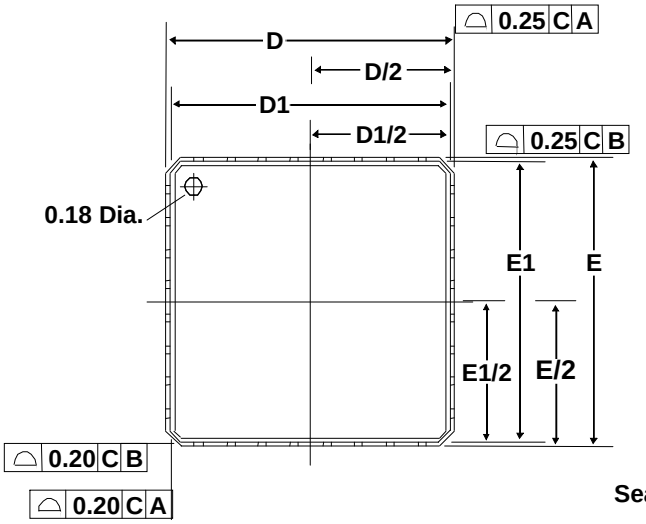
6.10 mm (240 mil) body,
0.50 mm (0.020 mil) pitch TSSOP

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	–	1.20	–	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.32	0.041
b	0.17	0.27	0,007	0.011
c	0.09	0.20	0.0035	0.008
D	See variations below			
E	8.10 basic		0.319 basic	
E1	6.00	6.20	0.236	0.244
e	0.50 basic		0.020 basic	
L	0.45	0.75	0.018	0.030
N	See variations below			
a	0°	8°	0°	8°
aaa	–	0.10	–	0.004

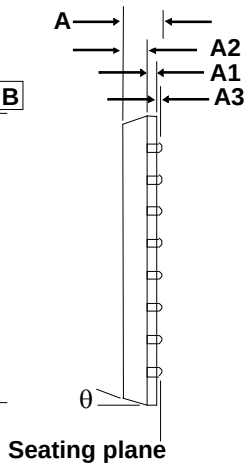
Variations:

N	D (mm)		D (inch)	
	Min	Max	Min	Max
64	16.90	17.10	0.665	0.673

Package Dimensions (56-Pin MLF2)

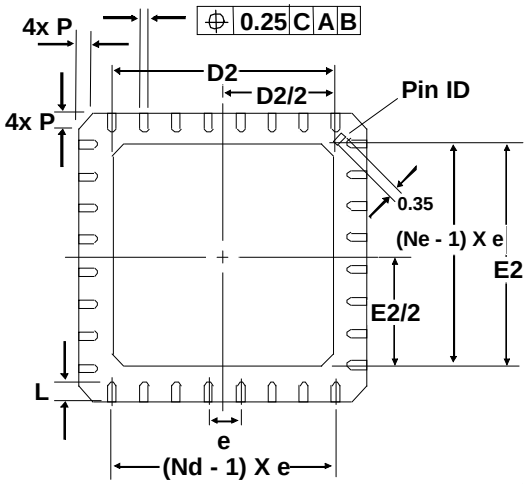


Top view

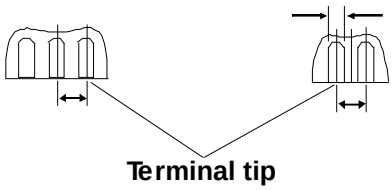


Side view

Symbol	Common dimensions		
	Min	Typ	Max
A		0.85	1.00
A1	0.00	0.01	0.05
A2		0.65	0.80
A3		0.20 BSC	
D		8.00 BSC	
D1		7.75 BSC	
E		8.00 BSC	
E1		7.75 BSC	
q			12
P	0.24	0.42	0.60
R	0.13	0.17	0.23
Pitch variation D			
e		0.50 BSC	
N		56	
Nd		14	
Ne		14	
L	0.30	0.40	0.50
b	0.18	0.23	0.30
Q	0.00	0.20	0.45
D2	4.35	4.50	4.65
E2	5.05	5.20	5.35

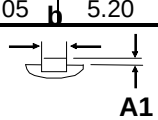


Bottom view



Terminal tip

For odd terminal/side For even terminal/side



Cross section

Ordering Information

Ordering Number	Marking	Package	Qty per Reel	Temperature
ASM4SSTVF16859-64TT	AS4SSTVF16859T	64-Pin TSSOP, Tube		0°C to 70°C
ASM4SSTVF16859-64TR	AS4SSTVF16859T	64-Pin TSSOP, Tape & Reel	2500	0°C to 70°C
ASM4SSTVF16859-56QT	AS4SSTVF16859Q	56-pin MLF2 - VQFN, Tube		0°C to 70°C
ASM4SSTVF16859-56QR	AS4SSTVF16859Q	56-pin MLF2 - VQFN, Tape & Reel	2500	0°C to 70°C

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Advance Information
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