Agilent ADCC-3960 Landscape 1.3 Megapixel CMOS Image Sensor with JPEG

Data Sheet

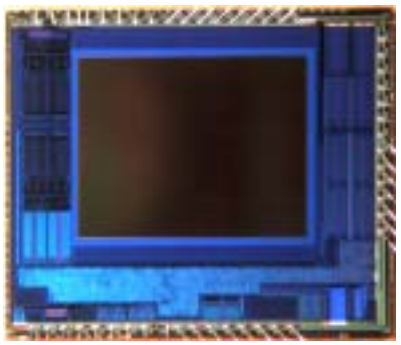
Overview

The Agilent ADCC-3960 is a SXGA image sensor with an integrated image processor. The ADCC-3960 is an advanced, low-power 1.3 megapixel image sensor and processor for embedded applications. The CMOS image sensor and image processing pipeline delivers images in JPEG and other data formats, ready for storage or transmission.

The CMOS image sensor incorporates Agilent's cutting-edge, 3.3 µm pixel design with virtually zero image lag and high sensitivity. Combined with our proprietary low noise 0.18 µm process results in the smallest high quality CMOS image sensor available.

The CMOS active-pixel digital array incorporates 1,280H x 1,024V active pixels in a 1/3-inch format, along with a on-chip ADC which provides up to 10-bit resolution per pixel.

A wide range of auto-camera functions allows standalone operation with minimal overhead. Extensive hardware and firmware interfacing options simplifies system integration. Also included is a line-up of features normally associated with high quality digital still cameras for excellent imaging capability and image quality.



Features

- 1/3-inch optical format
- 3.3µm x 3.3µm active-pixel EP photodiode-type
- 1,304H x 1,034V (1,348,336 pixels) total pixels (including dark pixels)
- 1,280H x 1,024V array format at (5:4) (1,310,720 active pixels)
- Subsampling and scaling (N by M resize) – any size less than the array
- Horizontal/vertical (X, Y) mirroring
- Panning – window can be placed anywhere in the 1280 x 1024 array
- 10-bit A/D converter and image pipe
- High sensitivity sensor, 5 lux minimum illumination
- Electronic rolling shutter
- Efficient JPEG compression to 15 fps SXGA
- Smooth digital zoom
- 24-bit color depth (16 million colors)
- True 1.3 megapixel Bayer pattern landscape sensor
- 15 fps SXGA, 30 fps VGA
- 50 MHz maximum data rate
- Output for video streaming
- Frame statistics gathering, including histograms for each color channel
- Lens shaping correction
- Bad pixel correction
- Sharpening
- Adaptive tone mapping
- Locally adaptive color noise suppression
- Auto exposure with auto flicker correction
- Advanced auto white balance for true color accuracy
- Direct RGB or YCbCr 8-bit parallel output (CCIR 656-compatible)
- RGB preview modes with halftoning
- Embedded sync capability – CCIR
- Programmable LED and Xenon flash strobe synchronization support and estimation
- Control using 2-wire SCI interface
- On-board PLL
- Low power: ~145 mW typical QVGA preview with PLL enabled
- Less than 10 µA sleep mode
- Dual 1.8V/2.8V supply voltage or on-board dual voltage regulators
- Die size = 7060 x 6030 µm

Applications

- Mobile phones
- Video phones
- Personal Digital Assistants
- Image-enabled appliances
- Digital still mini cameras
- Security cameras

General Specifications

Feature	Description
Output format	8-bit parallel YCbCr CCIR 656-compliant 8-bit parallel YCbCr or RGB 4:4:4 YCbCr 4:2:2 $Y_1Cb_{12}Y_2Cr_{12}$ 4:2:2 $Cb_{12}Y_1Cr_{12}Y_2$ 4:2:2 $Y_1Cr_{12}Y_2Cb_{12}$ 4:2:2 $Cr_{12}Y_1Cb_{12}Y_2$ JPEG
Maximum frame rate	15 fps at 1280 x 1024 (landscape SXGA)
Image modes	Grayscale and full color
Gamma correction	33 value programmable interpolated table
Serial data synchronization	End_of_Line, End_of_Frame, Data_Clock
Parallel data synchronization	HSYNC, VSYNC, VCLK
Serial control identification	0x56
Supply voltage requirements	2.8V (2.65 to 3.1) nominal supply 1.8V (1.65 to 1.95) nominal supply • May be generated on chip from 2.8V (not preferred)
External clock frequency	12 to 50 MHz
Power consumption	145 mW typical at QVGA (15 fps, PLL on)
Scene illumination (minimum)	5 lux at 5 fps or user can define minimum fps (low light mode)

Pixel Specifications – Preliminary

Function	Description
Pixel count	1280 x 1024 active pixels, (landscape SXGA) 1288 x 1032 with sacrificial Bayer pixels 1304 x 1034 with sacrificial Bayer pixels and dark pixels
Pixel type	3.3 µm square EP low noise
Effective fill factor	~55%
Lens chief ray angle design value	27 degrees
Recommended IR blocking filter	Thin film, cut frequency = 650 nm $\pm$ 10 nm
Responsitivity (green pixels)	0.87 V/lux-sec with source illumination at 550 nm
Maximum SNR	> 40dB
Dynamic range	64 dB
Quantum efficiency	Red: 48%, Green: 49%, Blue: 43%
Temporal noise	0.243 mV (6 electrons)
Saturation voltage	390 mV
Dark signal @ 25 °C	0.9 mV/s
Dark current @ 25 °C	26.4 pA/cm^2

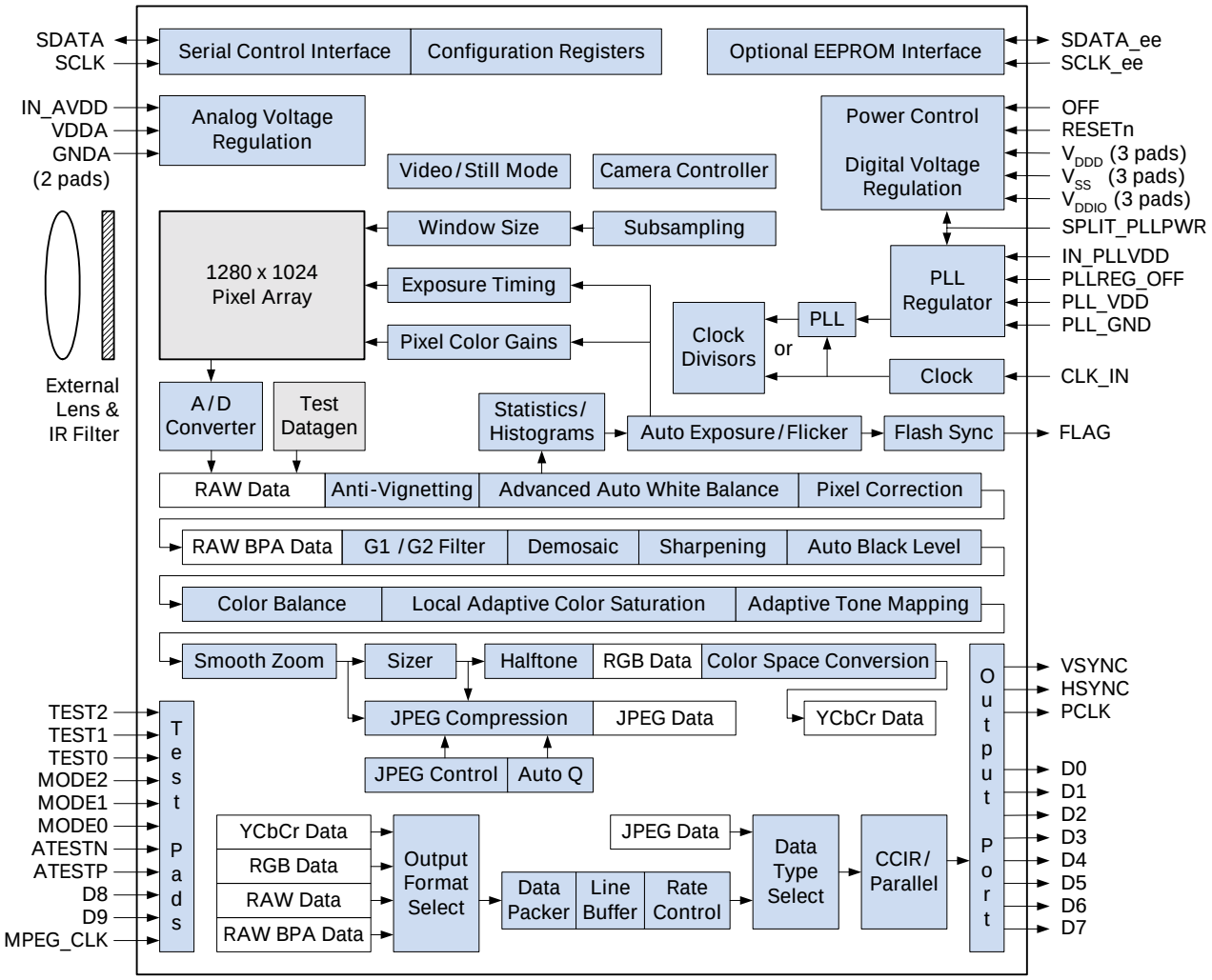
Design Assumptions

The ADCC-3960 sensor was designed to be used with specific types of external lenses and IR blocking filters.

The lens chief ray angle should be ~ 27 degrees. If the chief ray angle is different, the anti-vignetting tables will have to be revised to correct for the different light falloff.

The IR blocking filter should be a thin film design, with a nominal cut frequency of 650 nm, ± 10 nm. If a cut frequency or an absorptive filter is used, then the color correction matrices will have to be adjusted for proper color rendition.

Block Diagram



NOTE: Unshaded boxes represent data formats at different points of the image pipeline.

ADCC-3960 block diagram descriptions

Feature	Description
A/D converter	Converts the analog pixel voltages to 10-bit digital values
Advanced auto white balance	Accommodates the slight color shifts that affect white in different kinds of light (daylight, fluorescent, incandescent). The image sensor performs white balancing by digitally changing the gain-ratio of the red, green and blue channels and by adjusting the color-balancing matrix. White objects in the scene always look white in the final image.
Analog voltage regulator	Controls the separate voltage regulator used
Anti-vignetting	Corrects the illumination ratio of corner darkness to normalize the level of the image center
Auto black level	Subtracts the same value from each pixel making the darkest pixel appear black
Auto exposure	Adjusts the sensor to the amount of light present in the window using both exposure time and pixel gain
Auto flicker	Adjusts exposure time to eliminate flicker
Auto Q	Automatic Q Table function, changes the JPEG compression to have the same file sizes with different scenes
Camera controller	Centrally controls the overall functions of the image sensor and processor
CCIR data	Parallel port using CCIR 656 formatted data. Data is sent using an 8-bit parallel, CCIR 656 interface, with either external horizontal and vertical synchronization signals, or using embedded synchronization codes.
Clock divisors	User controllable divisors to control the clock
Color correction	Uses programmable color correction registers to adjust for color filter response of the image sensors, to correct for flare or scattered light, to bring black values back to wanted levels and to correct the color saturation level.
Color space conversion	Programmable color space conversion function to convert RGB values to a different color space. RGB values are multiplied by a 3 x 3 transform coefficient matrix and then offset. RGB to YCbCr is the default color space conversion.
Configuration registers	Controls all of the features of the image sensor and processor
Data packer	Data can be output in a variety of formats that use between 8 and 24 bits/pixel
Demosaic	Sensor produces a single red, green or blue pixel value for each location—demosaic performs color interpolation to produce all three color components for each pixel location. The data is reduced to 8 bits per color per pixel at this stage.
Digital voltage regulator	Regulator for the digital logic, busses the I/O voltage to the pads
Flash Sync	Supports either LED or Xenon external flash for still pictures in dark situations; flash is not supported in video mode
G1/G2 filter	Balances the responsivity of the two green channels
Gamma correction (tone mapping)	Pixel values acquired from the sensor are a linear function of the light present in the original window. In computer monitors, the intensity produced by the display is a non-linear function of the pixel value. This non-linear relationship is characterized by a “gamma” curve. The gamma corrects the image data for display on a computer monitor. It can also make corrections to the contrast of the image. Conceptually, gamma correction is a 33-entry lookup table translating the linear response of the sensor into the non-linear characteristics of the display.
Halftoning	Adds pseudo random noise to bit reduced outputs to eliminate banding that may be caused by low color depth in the display
Image statistics/ histograms	Registers contain data for each color plane, and also contains data for auto exposure and auto white balance functions (readable). When auto flicker is enabled, the histogram section of RAM is used to determine if the current image has flicker present.
JPEG compression	JPEG compression block uses 64 fixed quantization tables—with auto quantization enabled, the Q-tables are picked to match the currently requested compression ratio (default ratio = 16:1)

ADCC-3960 block diagram descriptions (continued)

Feature	Description
JPEG control	Controls the details of the JPEG compression block
Line buffer	Balances row output
Local desaturation	Desaturates colors in the dark areas, when the scene has low illumination
Optional EEPROM	Optional non-volatile memory to store a subset of register values
Parallel output	Outputs data using a parallel port with a video clock
Pixel array	Image sensor consists of a 1280 x 1024 pixel-array, which can be windowed to any size between 1280 x 1024 and 24 x 24. The array can be mirrored in both the horizontal and vertical directions.
Pixel color gains	Controlled by the auto white balance function, these ratios set the differential gains of the color channels
Pixel correction	Circuit reduces the effects of pixel mismatch
PLL	Optional PLL to change input clock frequencies (maximum output = 81 MHz)
PLL regulator	Controls the separate voltage regulator for the PLL. May be connected to the main digital power (but not recommended)
Power control	Allows the part to be reset or turned off via logic signals
Serial control interface	Image sensor is controlled using a 2-wire serial interface, which is used to read and write to the image sensor registers and image processor
Sharpening	Applies a variable sharpening filter to the image which enhances the image edges
Sizer	Allows the output image to be scaled from the sensor input. The scaling occurs after the demosaic operation and before the color balance.
Smooth digital zoom (window size control)	Reduces the image field of view; allows the sensor output to be windowed to any location on the sensor. Beginning and ending rows and columns can be specified, allowing the window to be any size, in any location.
Subsampling	Subsamples the image array to reduce the size without changing the field of view
Test pads	Pads used in the manufacture and test of the imager. Do not bond to these pads
Test pattern generator	Image sensor has the ability to generate test patterns for normal, white, random, sum or coordinates, eight pixel wide border, checkerboard and color bars modes
Timing control	Exposure control for the image sensor; exposure is in row times
Video / still mode	Video mode is nominally QVGA; still mode is SXGA
Window size	Controls what area of the sensor is used for imaging. Zoom and pan are possible using the window size controls

Electrical Specifications –

Absolute maximum ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Storage temperature [2]	T_S	-30		85	°C	
Operating temperature (reduced) [2]	T_{AR}	-25		65	°C	
Humidity [1]	RH	5		95	%	Non-condensing
Analog power supply [2]	$AV_{DD2.8}$	-0.3		3.6		
I/O power supply [2]	V_{DDIO}	-0.3		3.6	V	
Low voltage power supply [2]	V_{DDD}	-0.3		2.0	V	
ESD [2]				2	kV	All pads, human body model MIL 883 Method 3015
Input voltage [2]	V_{IN}	-0.3		V_{DDIO} + 0.3	V	All input pads

Recommended operating conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Operating temperature [1]	T_A	-25		40	°C	
Analog power supply [2]	IN_AVDD	2.65	2.8	3.1	V	
I/O power supply [2]	V_{DDIO}	2.65	2.8	3.1	V	
Low voltage power supply [1]	V_{DDD}	1.65	1.8	1.95	V	May be generated on-chip (not recommended)
Analog quiscent current [2]	I_A			25	mA	Runs off regulator driven by high voltage supply
2.8V V_{DDIO} dynamic current	$I_{2.8IOD}$			15	mA	Valid for high voltage I/O mode
1.8V V_{DDIO} dynamic current	$I_{1.8IOD}$			10	mA	Valid for low voltage I/O mode
$V_{DD1.8}$ digital core dynamic current	I_C			10	mA	Runs off low voltage supply
All supplies, rise time [2]	V_{DDIO_RT}			50	ms	
All supplies, supply noise [2]	V_{DDIO_N}			50	mV	Vp-p within 0 - 1 MHz
External clock frequency [2] Duty cycle [2]	MCLK	12 45	13 50	50 55	MHz %	Sensor clock is limited to 27 MHz, image pipeline to 40.5 MHz, the clock divisors must be properly set to observe these limits.
Serial control clock frequency	SCLK			400	kHz	

1. Guaranteed by design.
2. Guaranteed by characterization.
3. Guaranteed by production test.

Electrical Specifications (continued)

DC electrical specifications (typical values at 25°C, V_{DDIO} = 2.8V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes	
Total supply current [2]						See Power Consumption vs. Modes below	
Supply current (low power) [2]	I_{DDIO}		100		µA	Power on, MCLK stopped	
Supply current (power off) [2]	I_{DDIO}			10	µA	OFF = high, MCLK stopped	
All pads except SCLK and SDATA							
Input low voltage [1]	V_{IL}			0.30 V_{IO}	V	V_{IO} can be either 1.8V or 2.8V nominal	
Input high voltage [1]	V_{IH}	0.7 V_{IO}			V		
Output low voltage [1]	V_{OL}	0	0.1 V_{IO}				
Output high voltage [1]	V_{OH}		0.9 V_{IO}		V		
Input low current [2]	I_{IL}	< - 10		< 10	µA	At 0.4V	
Input high current [2]	I_{IH}	< - 10		< 10	µA	At 2.4V	
Slew Rate [2] (programmed via the OUT_CTRL register)						V_{DDIO}	Load
	SR_O	0.4	0.8		V/ns	1.8V	5 pF
	SR_O	0.4	0.8		V/ns	1.8V	50 pF
	SR_O	0.9	1.3		V/ns	2.8V	5 pF
	SR_O	0.9	1.3		V/ns	2.8V	50 pF
SCLK and SDATA							
Input low voltage [1]	V_{IL_S}		0.25 V_{DDIO}	0.5	V		
Input high voltage [1]	V_{IH_S}	0.7 V_{DDIO}	0.75 V_{DDIO}		V		
Output low voltage [1]	V_{OL_S}	0		0.4	V	At 3 mA sink current	
Output high voltage [1]	V_{OH_S}			3.6	V	Output voltage depends on external pull-up resistor and V_{DDIO} value	

1. Guaranteed by design.
2. Guaranteed by characterization.
3. Guaranteed by production test.

Electrical Specifications (continued)

AC electrical specifications (typical values at 25°C, V_{DDIO}= 2.8V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Power up from V_{DDIO} [2]	t_{PU}		10		ms	From V_{DDIO} valid
Video clock frequency [2]	V_{CLK}	12	13	50	MHz	User programmable
Frame rate (SXGA) [1]				15	frame/s	User programmable
Frame rate (VGA) [1]				30	frame/s	User programmable
SCLK, SDATA						
Rise time [2]	t_{DCR}	20		250	ns	Depends on external pull-up resistor, V_{DDIO} value, and line capacitance. Default values are 5 kW and 5 pF.
Fall time [2]	t_{DCF}	20		250	ns	
Input pad capacitance [1]	C_{IN}		1.6		pF	

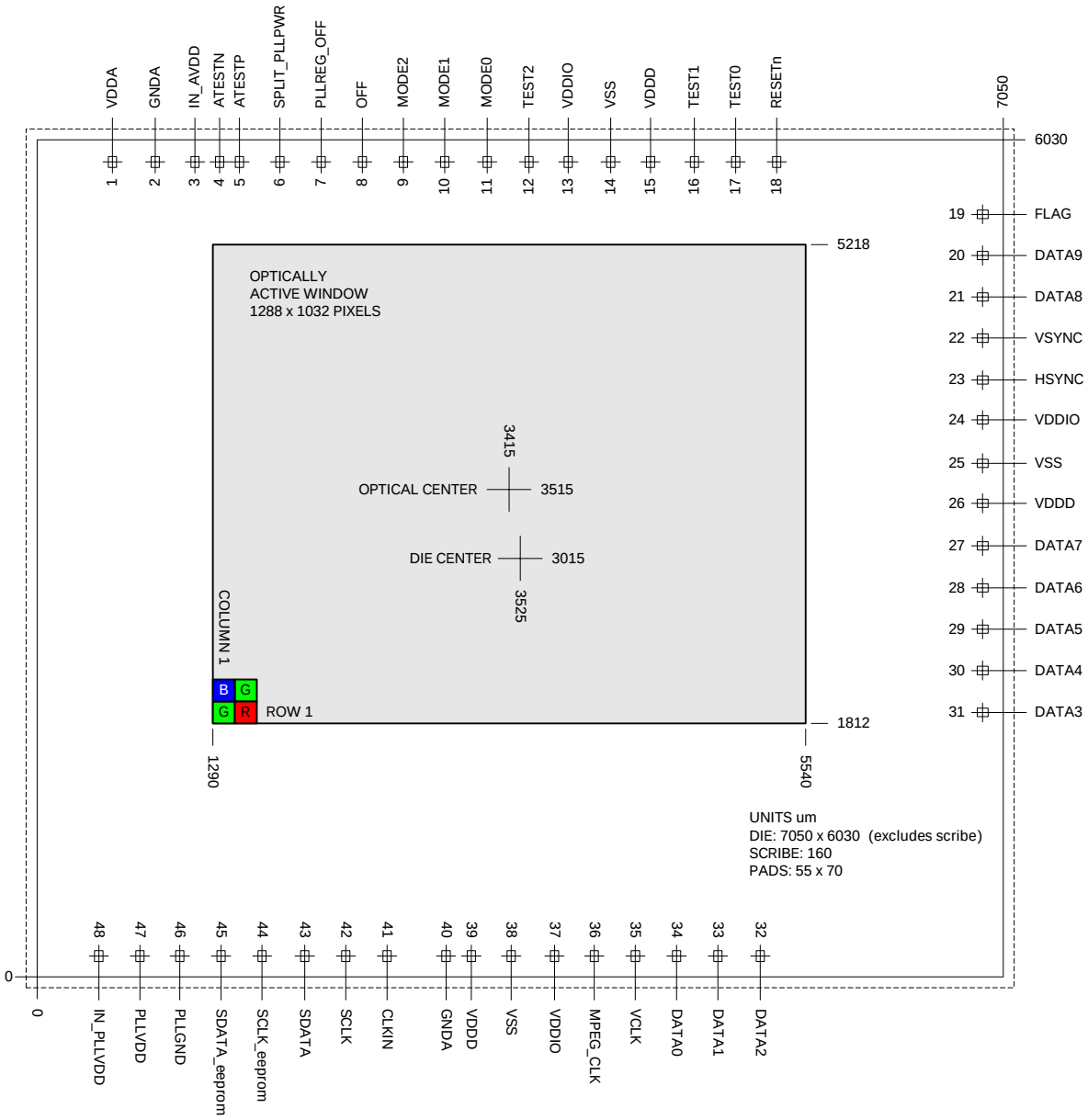
1. Guaranteed by design.
2. Guaranteed by characterization.
3. Guaranteed by production test.

Power consumption vs. modes – typical, at 25°C, V_{DDIO}= 2.8V, AV_{DD} = 2.8V, V_{DDD}= 1.8V

Mode	frames/second	Subsampled	Sizered	PLL enabled	I_{DD}	I_{DDIO}	I_{DDA}	Units
QQVGA (160 x 120)	15	Yes	Yes	No	12.3	0.3	9.4	mA
	15	No	Yes	Yes	35.5	0.3	31.9	mA
QVGA (320 x 240)	15	Yes	Yes	No	12.7	0.8	9.4	mA
	15	No	Yes	Yes	36.0	0.9	31.9	mA
VGA (640 x 480)	15	Yes	Yes	No	13.8	2.7	9.4	mA
	15	No	Yes	Yes	37.2	3.0	31.9	mA
	30	Yes	No	Yes	25.2	6.2	16.8	mA
4XVGA (1280 x 960)	15	No	No	Yes	40.3	11.4	31.8	mA
SXGA (1280 x 1024)	15	No	No	Yes	41.3	11.4	31.9	mA

NOTE: Enabling subsampling and disabling the PLL result in the lowest power consumption; data is from a limited sample.

Die Drawing



Orientation

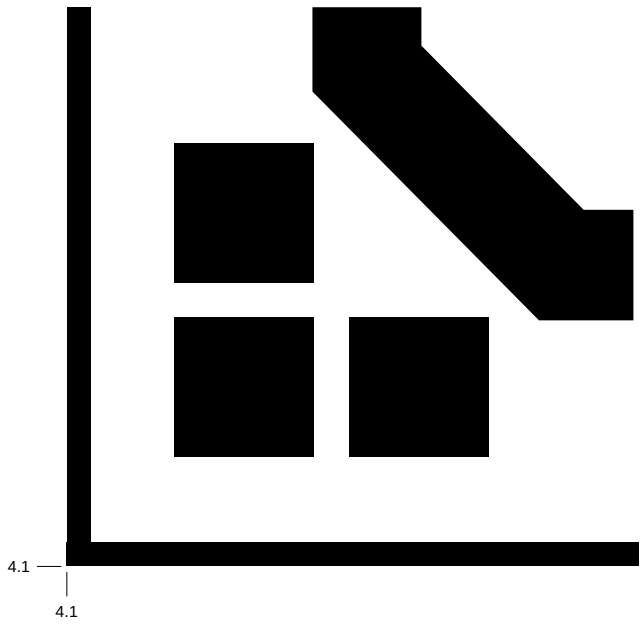
To take pictures “right side up”, orient the IC as shown above. This assumes a lens in front of the sensor. The image can be electronically flipped either horizontally or vertically

Bond Pad Center Positions (dimensions are in μm)

Pad	Name	X	Y	Pad	Name	X	Y	Pad	Name	X	Y
1	VDDA	544	5880	17	TEST0	5058	5880	33	DATA1	4934	150
2	GNDA	857	5880	18	RESETn	5358	5880	34	DATA0	4634	150
3	IN_AVDD	1144	5880	19	FLAG	6900	5518	35	VCLK	4334	150
4	ATESTN	1324	5880	20	DATA9	6900	5218	36	MPEG_CLK	4034	150
5	ATESTP	1466	5880	21	DATA8	6900	4918	37	VDDIO	3746	150
6	SPLIT_PLLPWR	1758	5880	22	VSYNC	6900	4618	38	VSS	3434	150
7	PLLREG_OFF	2058	5880	23	HSYNC	6900	4318	39	VDDD	3146	150
8	OFF	2358	5880	24	VDDIO	6900	4030	40	GNDA	2965	150
9	MODE2	2659	5880	25	VSS	6900	3718	41	CLKIN	2534	150
10	MODE1	2959	5880	26	VDDD	6900	3430	42	SCLK	2234	150
11	MODE0	3259	5880	27	DATA7	6900	3118	43	SDATA	1934	150
12	TEST2	3558	5880	28	DATA6	6900	2818	44	SCLK_eeprom	1634	150
13	VDDIO	3846	5880	29	DATA5	6900	2518	45	SDATA_eeprom	1334	150
14	VSS	4158	5880	30	DATA4	6900	2218	46	PLLGND	1034	150
15	VDDD	4446	5880	31	DATA3	6900	1918	47	PLLVDD	746	150
16	TEST1	4758	5880	32	DATA2	5234	150	48	IN_PLLVDD	446	150

Die Fiducial Mark

The 0, 0 datum point is just off of the thin metal lines at the lower left of the die. The outer edges of the lines are at location 4.1, 4.1



Pad Descriptions (NOTE: Blue pads should be left unconnected)

Pad #	Name	Pad Type	Description
1	VDDA	VDDA_SHUNT	Analog V_{DD}, 2.5V nominal – output of the analog regulator. Must have 2.2 µF cap to GNDA
2	GNDA	ANALOG_GND	Analog ground – tied to the substrate
3	IN_AVDD	VDDA_SHUNT	2.8V nominal input to the analog voltage regulator
4	ATESTN	ANALOG	Analog I/O – tri-stated during normal operation (NO CONNECT)
5	ATESTP	ANALOG	Analog I/O – tri-stated during normal operation (NO CONNECT)
6	SPLIT_PLLPWR	WR_CTRL	Disconnects the PLLVDD and V_{DD} power nets; may be connected to GND to supply 1.8V to the core, but not recommended due to noise
7	PLLREG_OFF	WR_CTRL	Enables the PLL voltage regulator; required for stable PLL operation
8	OFF	WR_CTRL	Global power switch (1 = power off); must be bonded low if not externally controlled
9	MODE2	BIDIR_IO	Test mode pad – pull-up to IN_AVDD in ALL modes (only turned off when OFF is high)
10	MODE1	BIDIR_IO	Test mode pad – pull-up to IN_AVDD in ALL modes (only turned off when OFF is high)
11	MODE0	BIDIR_IO	Test mode pad – pull-up to IN_AVDD in ALL modes (only turned off when OFF is high)
12	TEST2	BIDIR_IO	Scan test pad – pull-up to VDDIO in normal mode
13	VDDIO	VDDIO_SHUNT	Input for variable 1.8V to 2.8V I/O voltage; needs a 1.0 µF cap to GND
14	VSS	GND_VDD	Digital ground – isolated from on chip substrate and GNDA
15	VDDD	VDDD_SHUNT	Input for 1.8V digital core; needs 1.0 µF cap to GND
16	TEST1	BIDIR_IO	Scan test pad – pull-up to VDDIO in normal mode
17	TEST0	BIDIR_IO	Scan test pad – pull-up to VDDIO in normal mode
18	RESETn	BIDIR_IO	Chip reset pad – pull-up on in normal mode
19	FLAG	BIDIR_IO	General purpose I/O pad (default low) – can be configured as a flash sync output
20	DATA9	BIDIR_IO	Engineering characterization; not used in normal modes (NO CONNECT)
21	DATA8	BIDIR_IO	Engineering characterization; not used in normal modes (NO CONNECT)
22	VSYNC	BIDIR_IO	Vertical sync output
23	HSYNC	BIDIR_IO	Horizontal sync output
24	VDDIO	VDDIO_SHUNT	Input for variable 1.8V to 2.8V I/O voltage; needs a 1.0 µF cap to GND
25	VSS	GND_VDD	Digital ground – isolated from on chip substrate and GNDA
26	VDDD	VDDD_SHUNT	Input for 1.8V digital core; needs 1.0 µF cap to GND
27	DATA7	BIDIR_IO	Data output (MSB)
28	DATA6	BIDIR_IO	Data output
29	DATA5	BIDIR_IO	Data output
30	DATA4	BIDIR_IO	Data output
31	DATA3	BIDIR_IO	Data output
32	DATA2	BIDIR_IO	Data output
33	DATA1	BIDIR_IO	Data output
34	DATA0	BIDIR_IO	Data output (LSB)

Pad Descriptions (NOTE: Blue pads should be left unconnected) (continued)

Pad #	Name	Pad Type	Description
35	VCLK	BIDIR_IO	Pixel data clock
36	MPEG_CLK	BIDIR_IO	MPEG clock (not enabled; NO CONNECT)
37	VDDIO	VDDIO_SHUNT	Input for variable 1.8V to 2.8V I/O voltage; needs a 1.0 µF cap to GND
38	VSS	GND_VDD	Digital ground – isolated from on chip substrate and GNDA
39	VDDD	VDDD_SHUNT	Input for 1.8V digital core; needs 1.0 µF cap to GND
40	GNDA	ANALOG_GND	Analog ground – tied to the substrate
41	CLKIN	CLK_INPUT	Input clock – 50 MHz maximum frequency; may be driven when the power is off
42	SCLK	SERIAL_IO	Serial control clock – requires external pull-up; may be driven with the power off
43	SDATA	SERIAL_IO	Serial control data– requires external pull-up; may be driven with the power off
44	SCLK_eeprom	18_BIDIR_IO	Controls optional 1.8V EEPROM; must NOT be driven with the power off
45	SDATA_eeprom	18_BIDIR_IO	Controls optional 1.8V EEPROM– internal pull-up on in normal mode; must NOT be driven with the power off
46	PLLGND	PLL_GND	Digital ground
47	PLLVDD	VDD_PLL_SHUNT	V_{DD} for the PLL– output of the PLL regulator; needs a 2.2 µF cap to PLLGND
48	IN_PLLVDD	PLL_VDD_SHUNT	2.8V nominal input to the PLL regulator

ADCC-3960 schematic option #1: Variable, externally driven VDDIO

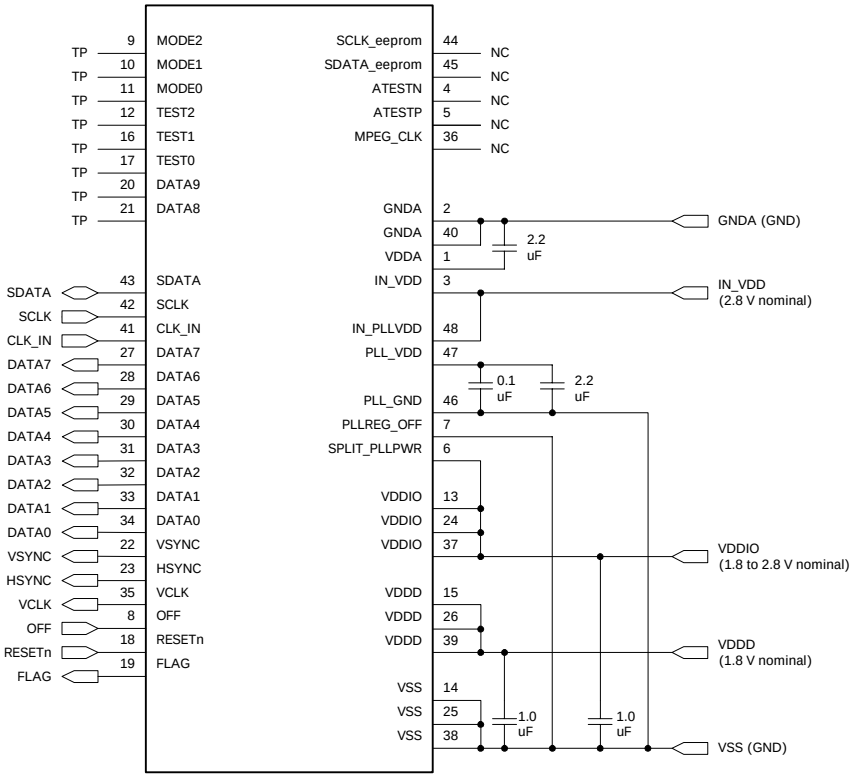
VDDIO can be varied from 1.8V to 2.8V.

The PLL 1.8V regulator is enabled (PLLREG_OFF = GND) for reliable PLL performance.

All regulators are turned off when the OFF pad is high. Valid high level is determined by the V_{DDIO} value.

NC = No Connect

TP = Test Point



ADCC-3960 schematic option #2: VDDIO = 2.8V

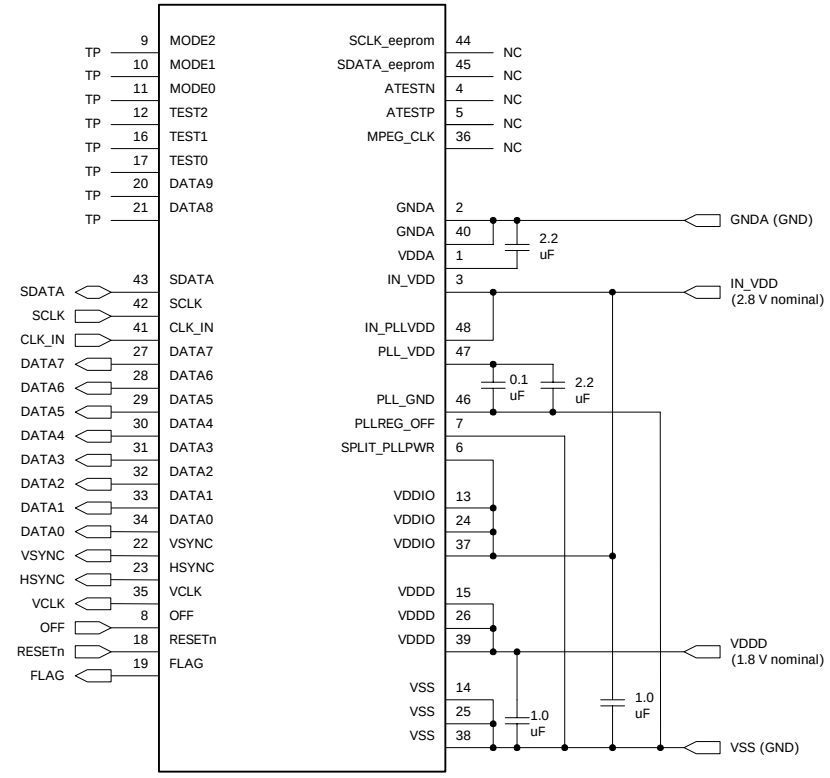
VDDIO in this case is connected to IN_VDD, which is 2.8V.

The PLL 1.8V regulator is enabled (PLLREG_OFF = GND) for reliable PLL performance.

All regulators are turned off when the OFF pad is high. Valid high level is determined by the V_{DDIO} value.

NC = No Connect

TP = Test Point



ADCC-3960 schematic option #3: V_{DDIO} = 1.8V

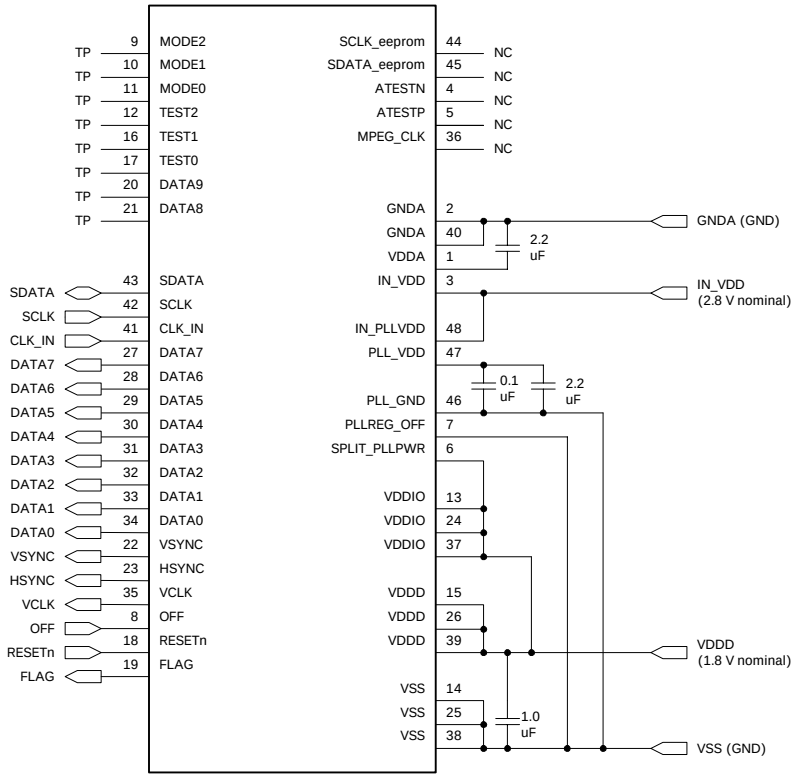
V_{DDIO} in this case is connected to V_{DDD}, which is 1.8V.

The PLL 1.8V regulator is enabled (PLLREG_OFF = GND) for reliable PLL performance.

All regulators are turned off when the OFF pad is high. Valid high level is determined by the V_{DDIO} value.

NC = No Connect

TP = Test Point

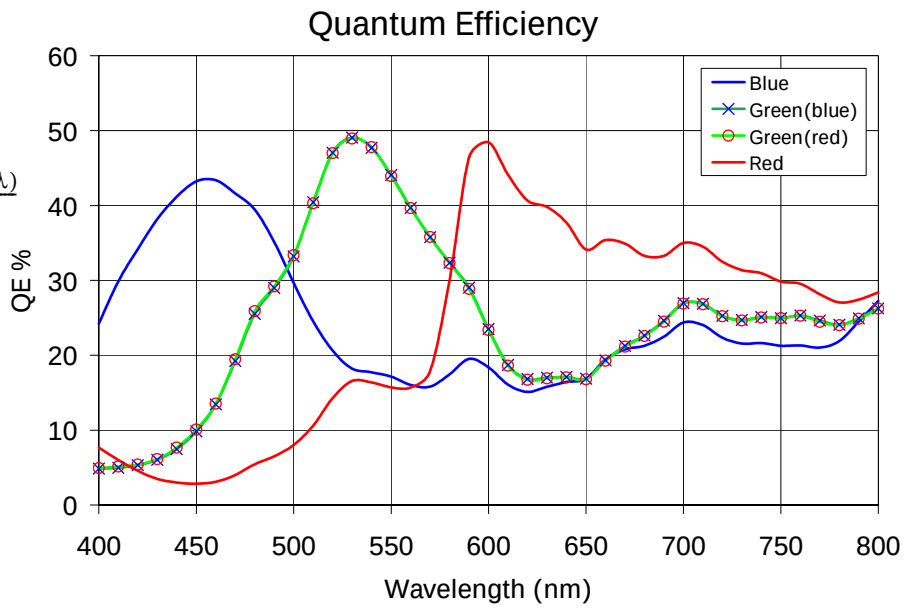


Quantum Efficiency

The quantum efficiency of the ADCC-3960 is shown to the right. As can be seen, an IR blocking filter is needed for proper color images.

$$QE(\lambda) = \frac{Sensitivity(\lambda) \cdot h \cdot c \cdot m(\lambda)}{CG \cdot A \cdot \lambda}$$

h is Plank's constant
c is the speed of light
A is the pixel area
l is the wavelength
m is the factor to convert photometric units to radiometric units.
CG is conversion gain
A is the area of the pixel



Quantum Efficiency

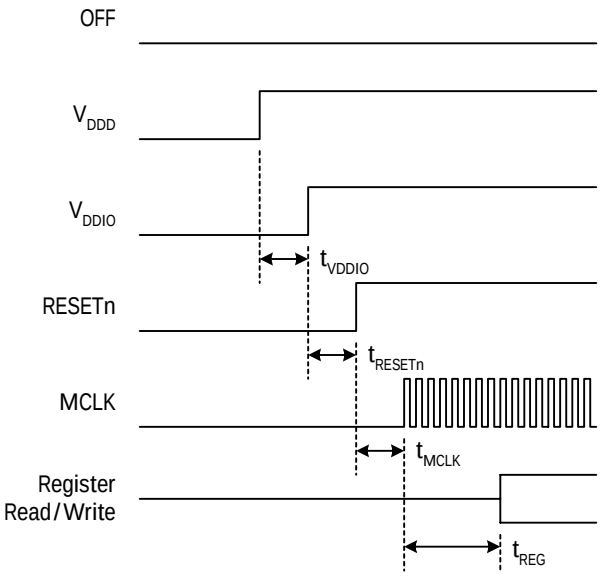
Wavelength	Blue	Green (blue)	Green (red)	Red	Wavelength	Blue	Green (blue)	Green (red)	Red
400	24.22	4.86	4.93	7.68	610	16.09	18.71	18.60	44.11
410	29.86	4.97	5.16	6.01	620	15.12	16.85	16.73	40.65
420	34.16	5.33	5.40	4.56	630	15.80	17.02	16.93	39.82
430	38.17	6.04	6.13	3.50	640	16.44	17.11	17.03	37.73
440	41.18	7.48	7.66	3.01	650	16.87	16.88	16.78	34.13
450	43.23	9.87	10.09	2.86	660	19.45	19.31	19.28	35.39
460	43.38	13.44	13.55	3.10	670	20.79	21.25	21.14	34.91
470	41.62	19.24	19.47	4.02	680	21.27	22.65	22.56	33.29
480	39.46	25.54	25.89	5.45	690	22.47	24.62	24.49	33.28
490	35.13	28.99	29.20	6.51	700	24.38	26.97	26.89	35.00
500	29.67	33.21	33.36	8.03	710	24.05	26.87	26.82	34.50
510	24.53	40.43	40.32	10.59	720	22.35	25.27	25.21	32.50
520	20.62	47.03	47.00	14.27	730	21.57	24.72	24.65	31.38
530	18.23	49.08	48.97	16.57	740	21.63	25.12	25.04	30.95
540	17.72	47.71	47.80	16.37	750	21.28	24.96	24.97	29.84
550	17.15	44.07	43.92	15.73	760	21.32	25.31	25.28	29.56
560	16.03	39.70	39.67	15.71	770	21.04	24.65	24.46	28.15
570	15.82	35.78	35.81	17.92	780	21.90	24.09	24.02	27.07
580	17.46	32.37	32.29	30.08	790	24.51	24.93	24.86	27.43
590	19.51	29.05	28.86	46.41	800	27.26	26.24	26.23	28.42
600	18.38	23.50	23.37	48.44					

Power Up Timing

Initial power up

Parameter	Minimum	Typical	Maximum	Units
t_{DDIO}	50	-	-	ms
t_{RESETn}	250	-	-	ns
t_{MCLK}	50	-	-	ms
t_{REG}	10	-	-	MCLK periods

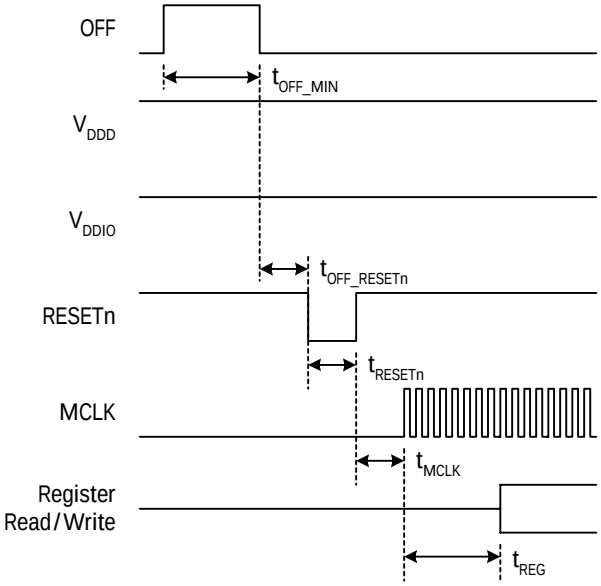
The OFF pad must be low when the V_{DDD} and V_{DDIO} lines are low.



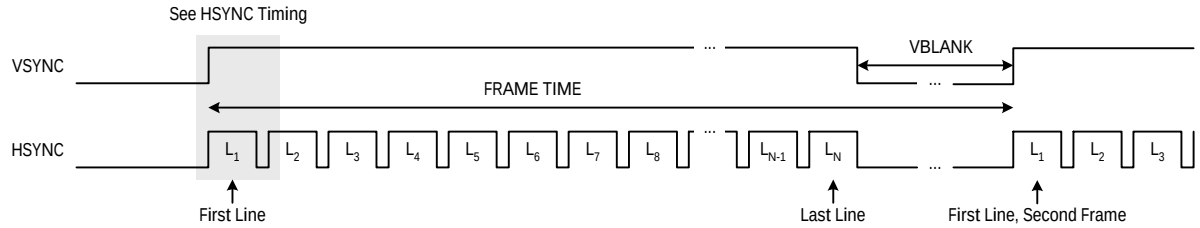
Using the OFF pad

Parameter	Minimum	Typical	Maximum	Units
t_{OFF_MIN}	200	-	-	µs
t_{OFF_RESETn}	0	-	-	ns
t_{MCLK}	50	-	-	ms
t_{REG}	10	-	-	MCLK periods

The toggling of the RESETn line is optional.

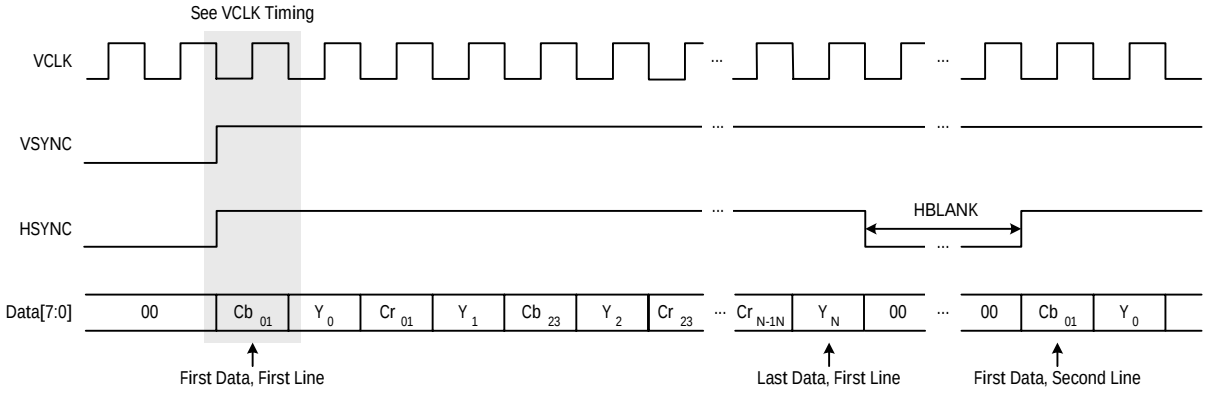


VSYNC Timing – One Frame



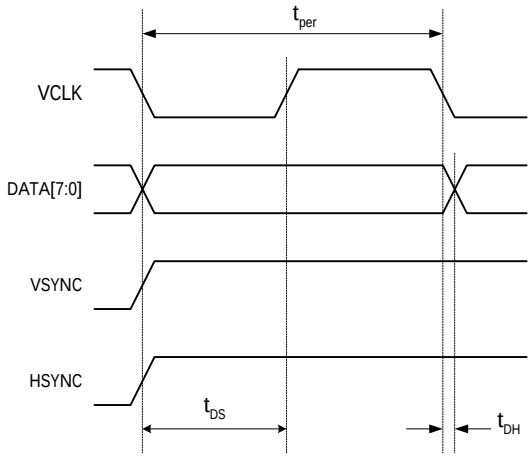
$$\text{Frame rate} = \frac{1}{\text{FRAME TIME}}$$

HSYNC Timing – One Line, YCbCr Output



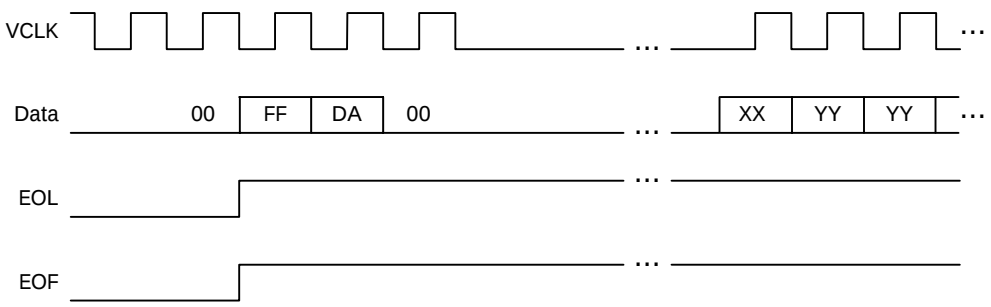
VCLK Timing

Parameter	Typical	Units
Data Setup, before ! VCLK	0.5	VCLK period (t_{per})
Data Hold, after # VCLK	0	ns



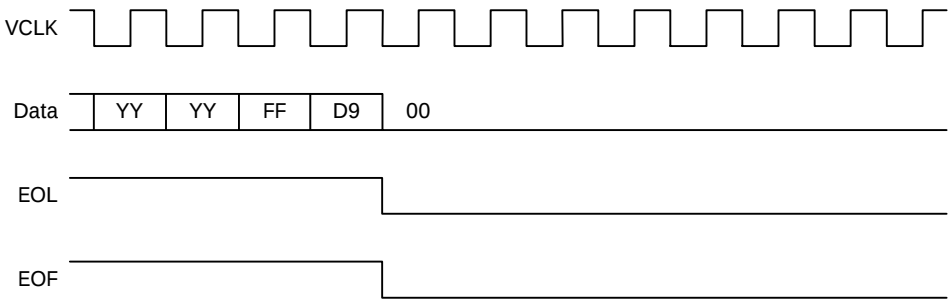
JPEG Timing

Normal JPEG start of frame



The ADCC-3960 does not generate a full JFIF header for JPEG data. The FF DA 00 XX four byte header specifies which Q table was used to compress the data. See the *ADCC-3960 SXGA CMOS Imager Register Reference* for details on how to use this information to create the JFIF header.

Normal JPEG end of frame

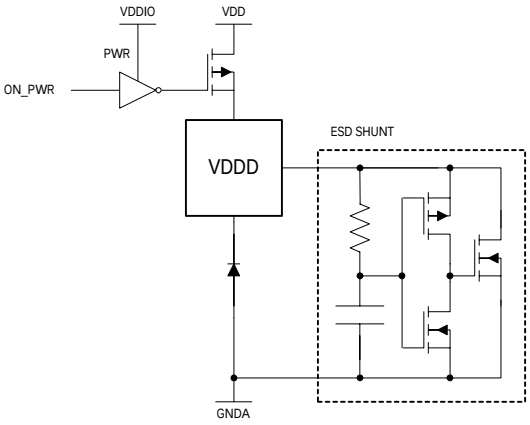


The FF D9 is the valid end of image indicator. There are many other options for the JPEG output (see *ADCC-3960 SXGA CMOS Imager Register Reference* for additional information).

Pad Schematics

VDDD_SHUNT

Pad	Pad #
VDDD	15, 26, 39



The V_{DDD} pad has an ESD shunt to GNDA, analog ground. The shunt provides a strike path to ground, but conducts no current in DC mode. During positive ESD strikes, the node between the resistor and the capacitor stays low during the fast voltage rise time. This makes the output of the inverter go high and turns on the large NFET to short the energy to ground. Negative ESD protection is via the diode to GNDA.

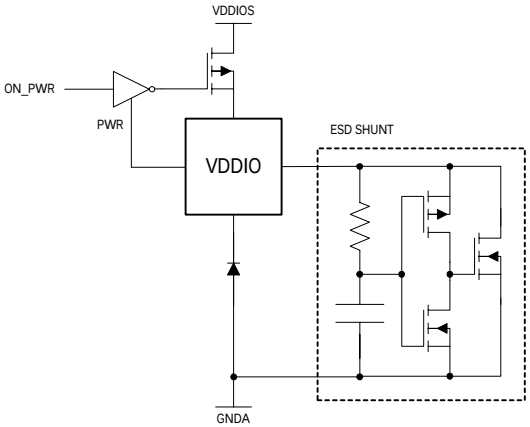
V_{DDD} comes in from the pad and through a large PFET switch which is controlled by the ON_PWR line, which is an inverted buffered version of the OFF pad. The switched output is called V_{DD}.

V_{DD} is bussed to the digital core and I/O pads to power their level shifters.

During normal operation V_{DD} is the same value as V_{DDD}, but when the OFF pad is raised high (i.e., ON_PWR is low) the PFET switches turn off and power to the core and pad receivers is turned off, and the pad outputs are tri-stated.

VDDIO_SHUNT

Pad	Pad #
VDDIO	13, 24, 37



The V_{DDIO} pad has an ESD shunt to GNDA, analog ground. The shunt provides a strike path to ground, but conducts no current in DC mode. During positive ESD strikes, the node between the resistor and the capacitor stays low during the fast voltage rise time. This makes the output of the inverter go high and turns on the large NFET to short the energy to ground. Negative ESD protection is via the diode to GNDA.

V_{DDIO} comes in from the pad and through a large PFET switch which is controlled by the ON_PWR line, which is an inverted buffered version of the OFF pad. The switched output is called V_{DDIOS}.

V_{DDIO} is bussed to the I/O pads to power their outputs and stageup logic, V_{DDIOS} is bussed to the I/O pads to power their input receivers.

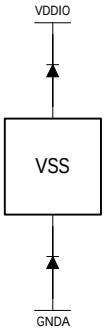
During normal operation V_{DDIOS} is the same value as V_{DDIO}, but when the OFF pad is raised high (i.e., ON_PWR is low) the PFET switches turn off and power to the core and pad receivers is turned off, and the pad outputs are tri-stated.

GND_VDD

Pad	Pad #
VSS	14, 25, 38

V_{SS} is bussed to the I/O pads and into the digital core.

For positive ESD strikes the V_{DDIO} shunt is used via the diode. For negative ESD, the diode to GNDA is used.



ANALOG_GND

Pad	Pad #
GNDA	2, 40

GNDA is the main “quiet” ground. It is the reference for the ESD shunts, the ESD diode stack, and the pixel ground reference.

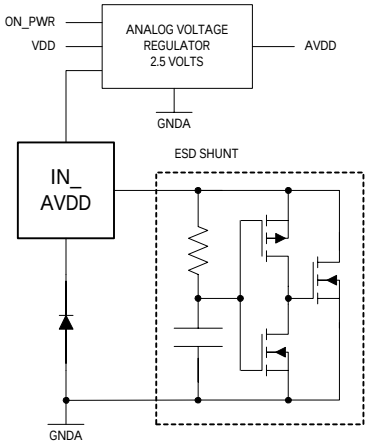
VDDA_SHUNT

Pad	Pad #
IN_AVDD	3
VDDA	1

The IN_AVDD pad has an ESD shunt before it goes into the 2.5V analog voltage regulator. The output of the regulator goes to the VDDA pad.

For positive ESD strikes, the shunt is used. For negative ESD is handled via the diode to GNDA.

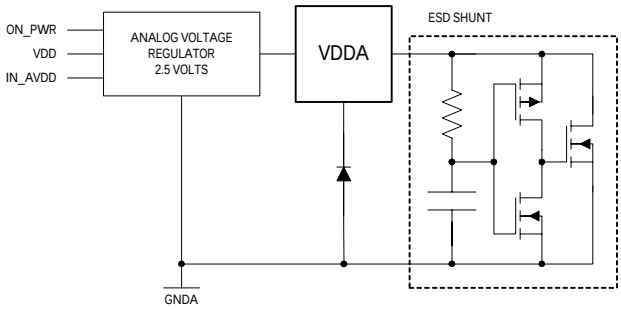
ON_PWR is an inverted buffered version of the OFF pad.



The VDDA pad has an ESD shunt and is used in the sensor as the analog power supply. *The VDDA pad must be connected to a 2.2 µF cap to GNDA*.

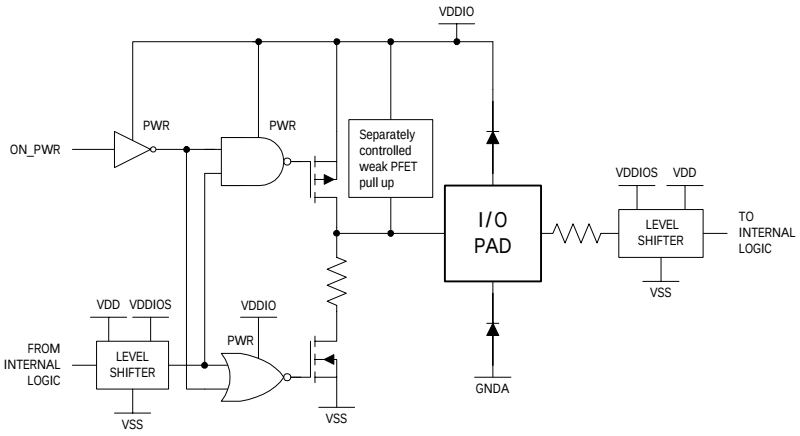
For positive ESD strikes, the shunt is used. For negative ESD is handled via the diode to GNDA.

ON_PWR is an inverted buffered version of the OFF pad.



BIDIR_IO

Pad	Pad #
DATA[7:0]	27, 28, 29, 30, 31, 32, 33, 34
HYSNC	23
VSYNC	22
VCLK	35
RESETn	18
FLAG	19
MODE[2:0]	9, 10, 11
TEST[2:0]	12, 16, 17
DATA[9:8]	20, 21
MPEG_CLK	36



Note: Blue pads must be left unconected.

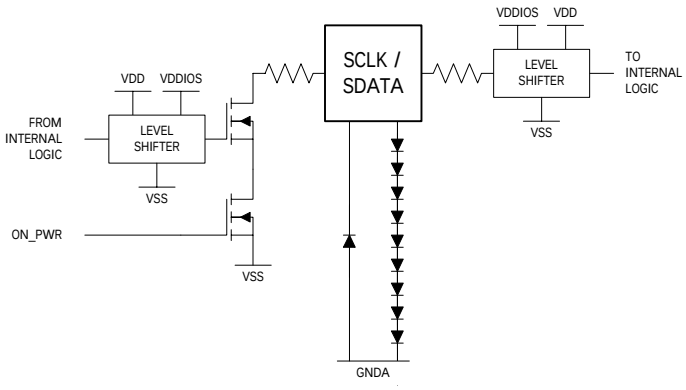
- The general purpose I/O pad output drivers and stageup logic are powered by V_{DDIO}, and the inputs and level shifters are powered by V_{DD} and V_{DDIOS}
- Note that when the OFF pad is raised high (ON_PWR is low) the pad outputs are tri-stated (also V_{DD} and V_{DDIOS} go to zero volts)
- All the instances of the general purpose IO pad have an internal weak PFET pull-up which may or may not be enabled depending on the pad function (it is also turned off when ON_PWR is low)
- Positive ESD events are handled via the diode to the V_{DDIO} shunt. Negative ESD is controlled by the diode to GNDA

SERIAL_IO

Pad	Pad #
SCLK	42
SDATA	43

The SCLK and SDATA pads do not require V_{DDIO} for their output power since they do not drive out high. ESD high (positive) protection is done via a stack of 9 diodes connected in series to GNDA. Negative protection is via the diode to GNDA.

These pads CAN be driven when the power is off.

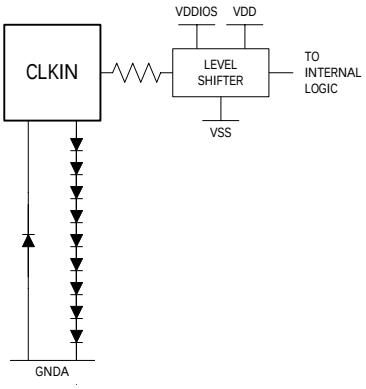


CLK_INPUT

Pad	Pad #
CLKIN	41

The CLKIN pad is similar to the SERIAL_IO pads, except that it does not have the output circuitry since CLKIN is only an input. ESD high (positive) protection is also done with the 9 diode stack to GNDA. Negative protection is via the diode to GNDA.

This pad CAN be driven when the power is off.

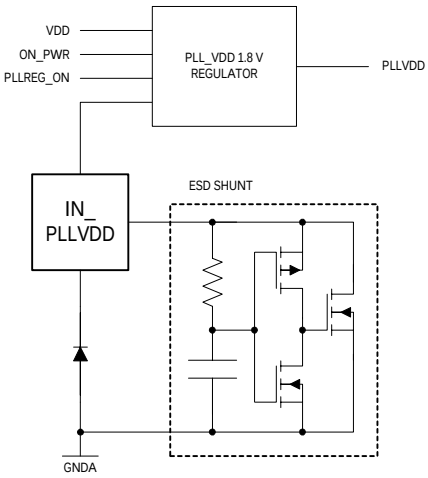


PLL_VDD_SHUNT

Pad	Pad #
IN_PLLVDD	48

The IN_PLLVDD pad has an ESD shunt before it goes into the 1.8V PLL regulator.

The regulator is controlled by ON_PWR which is a buffered, inverted version of the OFF pad, and PLLREG_ON, which is a buffered, inverted version of the PLLREG_OFF pad.

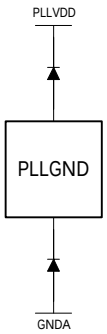


PLL_GND

Pad	Pad #
PLLGND	46

The PLLGND pad is connected only to the PLL DCO.

Positive ESD events are handled via the diode to the PLLVDD shunt. Negative ESD is controlled by the diode to GNDA.



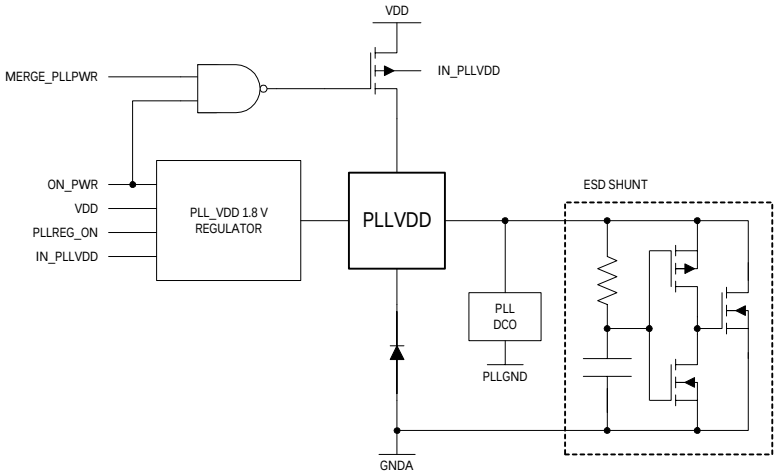
VDD_PLL_SHUNT

Pad	Pad #
PLLVDD	47

The PLLVDD pad is connected to the output of the 1.8V PLL regulator.

It is connected to an ESD shunt, the PLL digital controlled oscillator, and a PFET that is controlled by MERGE_PWR, which is a buffered, inverted version of SPLIT_PWR. This allows the PLL regulator to supply the 1.8 volt core voltage. *This is NOT recommended.*

A 2.2 µF cap from PLLVDD to GNDA is required for proper operation.

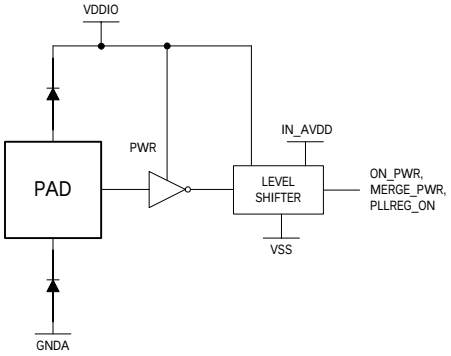


VWR_CTRL

Pad	Pad #
SPLIT_PWR	6
PLLREG_OFF	7
OFF	8

The SPLIT_PWR and PLLREG_OFF and OFF pads are input only pads that run from the VDDIO and IN_AVDD power supplies. These signals are inverted and level shifted to become the MERGE_PWR, PLLREG_ON and ON_PWR signals.

Positive ESD events are handled via the diode to the VDDIO shunt. Negative ESD is controlled by the diode to GNDA.



18_BIDIR_IO

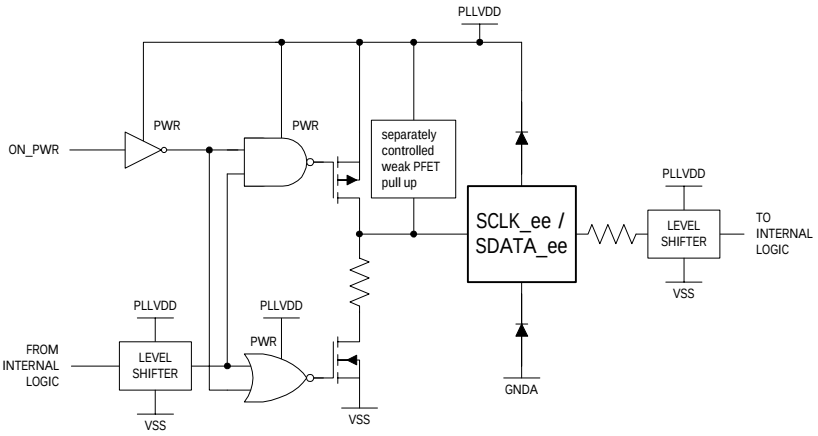
Pad	Pad #
SCLK_eeprom	44
SDATA_eeprom	45

The optional EEPROM is controlled via 1.8 volt IO pads. The weak PFET is enabled for the SDATA_eeprom pad, and disabled for the SCLK_eeprom pad.

Positive ESD events are handled via the diode to the PLLVDD shunt. Negative ESD is controlled by the diode to GNDA.

ON_PWR is an inverted buffered version of the OFF pad.

These pads must not be driven when the power is off.

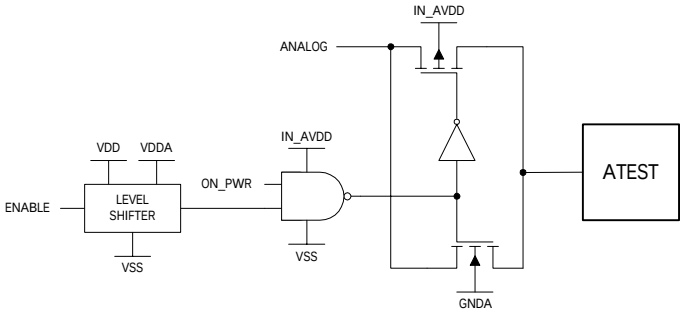


ANALOG

Pad	Pad #
ATESTN	4
ATESTP	5

Note: These pads must be left unconected.

The ATESTN and ATESTP pads are not used under normal operation. They are analog IO pads, transmission gates controlled by IN_AVDD, with control logic powered by VDD and VDDA.



Programmable Registers

The ADCC-3960 imager has programmable registers in the image processor and the image sensor, which are listed below. For additional information on the usage of the programmable registers, see the *ADCC-3960 SXGA CMOS Imager Register Reference*.

Registers and RAM by Mnemonic

Mnemonic	Description	Mnemonic	Description
A_FRAME_RATE	Achievable frame rate	AV_OF_GRN	Anti-vignetting oval factor, green channel
ABL_MAX_BLACK	Auto black level maximum black	AV_OF_RED	Anti-vignetting oval factor, red channel
ABL_MIN_BLACK	Auto black level maximum black	AV_OS_BLUE	Anti-vignetting blue offset
ABL_SUBTRACT	Auto black level subtraction	AV_OS_GREEN1	Anti-vignetting green 1 offset
ABL_TARGET	Auto black level target	AV_OS_GREEN2	Anti-vignetting green 2 offset
ADC_CTRL	ADC control	AV_OS_RED	Anti-vignetting red offset
AE_DOE_FACTOR	Auto exposure deliberate overexposure factor	AV_RED_xx	Red anti-vignetting table, entries 0 to 31
AE_DOE_MARGIN	Auto exposure deliberate overexposure margin	AV_RIGHT	Anti-vignetting right (LWROW)
AE_ETIME_DFLT	Auto exposure time default	AV_TOP	Anti-vignetting top (FWCOL)
AE_ETIME_MAX	Auto exposure time maximum	AV_WIN_BOT_S	Anti-vignetting window bottom, still mode
AE_ETIME_MIN	Auto exposure time minimum	AV_WIN_BOT_V	Anti-vignetting window bottom, video mode
AE_GAIN_DFLT	Auto exposure gain default	AV_WIN_LEFT_S	Anti-vignetting window left, still mode
AE_GAIN_MAX	Auto exposure gain maximum	AV_WIN_LEFT_V	Anti-vignetting window left, video mode
AE_GAIN_MIN	Auto exposure gain minimum	AV_WIN_RIGHT_S	Anti-vignetting window right, still mode
AE_GAIN_MIN_P	Auto exposure gain minimum, preferred	AV_WIN_RIGHT_V	Anti-vignetting window right, video mode
AE_MARGIN	Auto exposure margin	AV_WIN_TOP_S	Anti-vignetting window top, still mode
AE_TARGET	Auto exposure target	AV_WIN_TOP_V	Anti-vignetting window top, video mode
AE_TOL_ACQ	Auto exposure tolerance acquire	AWB_BLUE_DFLT	AWB default blue/green ratio
AE_TOL_MON	Auto exposure tolerance monitor	AWB_BLUE_MAX	AWB maximum blue/green ratio
AF_CTRL1	Auto functions control 1	AWB_BLUE_MIN	AWB minimum blue/green ratio
AF_CTRL2	Auto functions control 2	AWB_CONTROL	AWB manual control of plausible illuminant
AF_STATUS	Auto functions status	AWB_DD_T	AWB lux threshold, Direct daylight
AFSTAT_SUM	Auto focus stats sums – READ ONLY	AWB_ID_T	AWB lux threshold, Indirect daylight
APS_COEF_BLUE	Blue auto white balance gain	AWB_M_V_POS	AWB min variance positive hysteresis
APS_COEF_GRN1	Green 1 auto white balance gain	AWB_M_VAR	AWB min variance
APS_COEF_GRN2	Green 2 auto white balance gain	AWB_PREV_T	AWB previous threshold
APS_COEF_RED	Red auto white balance gain	AWB_RED_DFLT	AWB default red/green ratio
ATM_CTRL	Adaptive tone map control	AWB_RED_MAX	AWB maximum red/green ratio
AV_BLUE_xx	Blue anti-vignetting table, entries 0 to 31	AWB_RED_MIN	AWB minimum red/green ratio
AV_BOT	Anti-vignetting bottom (LWCOL)	AWB_SENS_C	AWB sensitivity constant
AV_C_COL_BLUE	Anti-vignetting center column, blue channel	AWB_TOL_ACQ	Auto white balance tolerance acquire
AV_C_COL_GRN	Anti-vignetting center column, green channel	AWB_TOL_MON	Auto white balance tolerance monitor
AV_C_COL_RED	Anti-vignetting center column, red channel	B_CR_MAX_MIN	Chrominance, Cr (or blue) max/min
AV_C_ROW_BLUE	Anti-vignetting center row, blue channel	BFRAC	Baud rate fraction
AV_C_ROW_GRN	Anti-vignetting center row, green channel	BLUE_DIFF_SUM	Blue channel difference sum
AV_C_ROW_RED	Anti-vignetting center row, red channel	BLUE_GAIN	Blue analog gain
AV_GRN_xx	Green anti-vignetting table, entries 0 to 31	BLUE_HISTO_BIN_xx	Blue histogram, bins 0 to 20 (enabled)
AV_LEFT	Anti-vignetting left (FWROW)	BLUE_SUM	Blue pixel sum
AV_OF_BLUE	Anti-vignetting oval factor, blue channel	BLUE_SUM_SH	Blue sums, shadowed

Registers and RAM by Mnemonic (continued)

Mnemonic	Description	Mnemonic	Description
BPA_BADPIX_CNT	BPA bad pixel count (read only)	CROP_LEFT	Optional data crop before JPEG
BPA_D2_T	BPA second derivative threshold	CROP_PIX_CNT_HI	Number of cropped pixels (upper 5 bits)
BPA_OUTL_PED	BPA outlier, pedestal	CROP_PIX_CNT_LO	Number of cropped pixels (lower 16 bits)
BPA_SF_GTHRESH	BPA scale factor, green filter threshold	CROP_TOP	Optional data crop before JPEG
BPR_5LINE_T	BPA 5 line threshold	CSC_COEF_xx	Color space conversion coefficients (9 reg)
BRATE	Baud rate register	CSC_OS_x	Color space conversion offsets (3 reg)
C_BG_RATIO	Current blue/green ration (read only)	CSC_OSx_S	Still color space conversion offsets (3 reg)
C_BNF_TIME	Current base no flicker time (read only)	CSC_OSx_V	Video color space conversion offsets (3 reg)
C_ETIME	Current exposure time (read only)	CSC_xx_S	Still color space conversion coefficients (9 reg)
C_FRAME_RATE	Current frame rate	CSC_xx_V	Video color space conversion coefficients (9 reg)
C_GAIN	Current gain (read only)	CTL_CLK_DIV	Clock dividers for control and serial interfaces
C_OFF_THRESH	Channel offset threshold	CTL_CLK_DIV_PLL	PLL clock divider, control and serial interface
C_RG_RATIO	Current red/green ratio (read only)	CURRENT_ILLUM	Current PI illuminant
CC_COEF_xx	Color correction coefficients (9 reg)	DATA_GEN	Test data generator
CC_OS_x	Color correction offsets (3 reg)	EOF_CODES	End of frame codes
CCIR_CTRL	CCIR control	EOF_CODES_W	End of frame codes working copy
CCIR_D2HS_HOLD	CCIR data to HSYNC hold time	ERROR	Error control
CCIR_HS2D_SU	CCIR HSYNC to data setup time	EXP_ADJ	Exposure adjustment
CCIR_HS2VS_HOLD	CCIR HSYNC to VSYNC hold time	EXP_END	Exposure sequence pattern end
CCIR_HSYNC_PASS	CCIR HSYNC passive time	EXP_STRT	Exposure sequence pattern start
CCIR_VS2HS_SU	CCIR VSYNC to HSYNC setup time	EXPOSURE	Exposure
CHN_0_OFF	Channel 0 offset	EXT_DIV	External clock divider
CHN_1_OFF	Channel 1 offset	FIRMWARE_REV	Current firmware revision
CHN_2_OFF	Channel 2 offset	FLASH_BLUE	Flash blue/green ratio
CHN_3_OFF	Channel 3 offset	FLASH_EGP_T	Flash exposure gain product threshold
CHN_x_CPP_STL	Number of channels times CPP, still mode	FLASH_GAIN	Flash gain, green 1 and green 2 channels
CHN_x_CPP_VID	Number of channels times CPP, video mode	FLASH_RED	Flash red/green ratio
CLK_DIV_S	Clock divisors, still mode	FLASH_TIME	Flash time
CLK_DIV_V	Clock divisors, video mode	FLICK_CFG_1	Flicker configuration 1
CLK_FREQ	Input clock frequency	FLICK_CFG_2	Flicker configuration 2
CLK_GATE_1	Clock gating 1	FLICKER_STATS	Flicker statistics (programmable) (enabled)
CLK_GATE_2	Clock gating 2	FRAME_TIME	Flash frame time
CLK_PIXEL	Clocks per pixel	FWCOL	Window first column address
CMD_1	Main command 1	FWROW	Window first row address
CMD_2	Main command 2 (write 1s only)	G_CB_MAX_MIN	Chrominance, Cb (or green) maximum/minimum
COMP_BUF	Number of bytes in COMPBUF FIFO	G1G2_DIAG_T	Green 1/green 2 diagonal threshold
CONFIG_1	Image sensor configuration 1	GREEN_1_HISTO_BIN_xx	Green 1 histogram, bins 0 to 20 (enabled)
CONFIG_2	Image sensor configuration 2	GREEN_1_SUM	Green 1 pixel sum
CONTROL	Camera control	GREEN_2_HISTO_BIN_xx	Green 2 histogram, bins 0 to 20 (enabled)
CONTROL_1	Image sensor control 1	GREEN_2_SUM	Green 2 pixel sum
CPP_S	Clocks per pixel, still mode	GREEN_DIFF_SUM	Green 1 channel difference sum
CPP_V	Clocks per pixel, video mode	GRN_1_SUM_SH	Green 1 sums, shadowed
CROP_GREEN_SUM	Sum of green pixels in cropped image	GRN1_GAIN	Green 1 analog gain

Registers and RAM by Mnemonic (continued)

Mnemonic	Description	Mnemonic	Description
GRN2_GAIN	Green 2 analog gain	OUTPUT_CTRL_S	Output control, still mode
GRN_2_SUM_SH	Green 2 sums, shadowed	OUTPUT_CTRL_V	Output control, video mode
H_DLY_L	Half clock delay lower	OUTPUT_FORMAT	Output format
H_DLY_U	Half clock delay upper	OUTPUT_HGT_S	Output window height, still mode
HBLANK	Horizontal blank	OUTPUT_HGT_V	Output window height, video mode
HBLANK_S	Horizontal blanking period, still mode	OUTPUT_WID_S	Output window width, still mode
HBLANK_V	Horizontal blanking period, video mode	OUTPUT_WID_V	Output window width, video mode
HSYNC_PER	Horizontal synchronization period	PARALLEL_CTRL	Parallel output control working copy
HYSNC_PER_S	HSYNC period, still mode	PARALLEL_CTRL_S	Parallel output control, still mode
HYSNC_PER_V	HSYNC period, video mode	PARALLEL_CTRL_V	Parallel output control, video mode
I_CLK_DIV	Initial clock divider	PC_RAM_xxx	Pixel control RAM locations: 0 to 255
I_HEIGHT	Current image height	PIXEL_CLK	Pixel RAM clock divisor
I_MASK	Interrupt mask	PIXEL_CLK_S	Pixel clock, still mode
I_WIDTH	Current image width	PIXEL_CLK_V	Pixel clock, video mode
ICTRL	Interface control	PIXEL_MSK_L_ADDR	Pixel mask lower address
ID	Chip ID	PIXEL_MSK_U_ADDR	Pixel mask upper address
IDENT	Image sensor identification	PLL_CTRL	PLL control
ILLUM	Illumination	PLL_DITHER_CNT	PLL dither counter
INTP_CTRL_1	Interpolation control 1 (demosaic)	PLL_DIV_L	PLL divisors, large values
INTP_CTRL_2	Interpolation control 2 (demosaic)	PLL_DIV_S	PLL divisors, small values
IP_CLK_DIV	Clock dividers for image pipeline	PROC_CTRL_S	Processing control, still mode
IS_STATUS	Image sensor status	PROC_CTRL_V	Processing control, video mode
JPEG_CbCr_xx	JPEG Chrominance “CbCr” Q Table (64 entries)	PROCESS_CTRL	Processing control working copy
JPEG_CLKGATE	Clock gating for JPEG block	PROCESS_CTRL_2	Processing control 2
JPEG_CONFIG	JPEG configuration	PROCESS_CTRL_2_S	Process control 2, still mode
JPEG_CONFIG_S	JPEG configuration, still mode	PROCESS_CTRL_2_V	Process control 2, video mode
JPEG_CONFIG_V	JPEG configuration, video mode	QTABLE_CTRL	JPEG Q-table control
JPEG_EOF_CODE	JPEF end of frame code	QTABLE_MAX_MIN	JPEG Q-table maximum and minimum values
JPEG_SOF_CODE	JPEG start of frame code	R_FRAME_RATE	Requested frame rate
JPEG_STATUS	JPEG status	R_Y_MAX_MIN	Luminance, Y (or red) maximum/minimum
JPEG_Y_xx	JPEG luminance “Y” Q-table (64 entries)	RED_DIFF_SUM	Red channel difference sum
LOCAL_DESAT	Local color desaturation	RED_GAIN	Red analog gain
LWCOL	Window last column address	RED_HISTO_BIN_xx	Red histogram, bins 0 to 20 (histograms enabled)
LWROW	Window last row address	RED_SUM	Red pixel sum
MAX_SCLK	Maximum sensor clock	RED_SUM_SH	Red sums, shadowed
MIN_MAX_F_S	Frame convergence rates, still mode	ROWEXP_H	Row exposure high
MIN_MAX_F_V	Frame convergence rates, video mode	ROWEXP_L	Row exposure low
NACC_BC_xx	NACC bright coefficients (9 reg)	RPT_S	Row processing time, still mode
NACC_DC_xx	NACC dark coefficients (9 reg)	RPT_V	Row processing time, video mode
NACC_EGP_x	NACC, exposure gain product (8 reg)	RS_STL	Row sample time, still mode
NACC_SAT_x	Noise adaptive color correction, saturation values (8 reg)	RS_VID	Row sample time, video mode
OUT_CTRL	Output control	SAMP_END	Sample sequence pattern end
OUTPUT_CTRL	Output control, working		

Registers and RAM by Mnemonic (continued)

Mnemonic	Description	Mnemonic	Description
SCENE_LUX	Current scene illumination	SZR_OUT_H	Sizer output height
SCL_CLK_FREQ	SCL clock frequency	SZR_OUT_HGT_S	Sizer output height, still mode
SEN_CFG_S	Sensor configuration, still mode	SZR_OUT_WID_V	Sizer output width, video mode
SEN_CFG_V	Sensor configuration, video mode	TEMP	Temporary register
SEN_CLK_DIV	Sensor clock dividers	TEST_1	Test control 1
SEN_CTRL_S	Sensor control, still mode	TEST_2	Test control 2
SEN_CTRL_V	Sensor control, video mode	TEST_ACT_RST	Test, array active reset
SENSOR_HGT_S	Sensor window height, still mode	TEST_ADC	Test, ADC control
SENSOR_HGT_V	Sensor window height, video mode	TEST_AID	Test, array identification
SENSOR_WID_S	Sensor window width, still mode	TEST_AMUX_1	Test, analog MUX 1
SENSOR_WID_V	Sensor window width, video mode	TEST_AMUX_2	Test, analog MUX 2
SER_ADDR	Serial interface device address	TEST_ANLP	Test, analog low power
SER_PARM	Serial Interface parameters	TEST_APD_1	Test, analog power down 1
SERIAL_CTRL	Serial control	TEST_APD_2	Test, analog power down 2
SIZE	Image size and orientation	TEST_ARR_CA	Test, array column amplifier
SIZEPAD_HGT	Image height to pad to before compression	TEST_ARR_CTL	Test, array control
SIZEPAD_IN_H	Measured height of image into JPEG	TEST_ARR_TST	Test, array test
SIZEPAD_IN_W	Measured width of image into JPEG	TEST_DAC_H	Test, DAC high
SIZEPAD_WID	Image width to pad to before compression	TEST_DAC_L	Test, DAC low
SOF_CODE_W	Start of frame code working copy	TEST_REF	Test, reference
SOF_CODES	Start of frame codes	TEST_VRC_1	Test, voltage regulator control 1
SROWEXP	Sub row exposure	TEST_VRC_2	Test, voltage regulator control 2
STAT_CAP_CTRL	Image statistics capture control	TM_ALL_xx	All colors tonemap (33 reg)
STAT_MODE_CTRL	Image statistics mode control	TM_COEF_xx_S	Still tonemap coefficients (33 reg)
STATUS	Camera status	TM_COEF_xx_V	Video tonemap coefficients (33 reg)
STATUS_FLAGS	Status flags (read only)	VBLANK	Vertical blank
SZR_IN_H	Sizer input height	VBLANK_S	Vertical blanking period, still mode
SZR_IN_HGT_S	Sizer input height, still mode	VBLANK_V	Vertical blanking period, video mode
SZR_IN_HGT_V	Sizer input height, video mode	WIN_MSB	Window most significant bits
SZR_IN_W	Sizer input width	Y_QTABLE_SELECT	JPEG luminance Q-table selection
SZR_IN_WID_S	Sizer input width, still mode	ZOOM_CTRL	Zoom control
SZR_IN_WID_V	Sizer input width, video mode		

Additional Available Documentation

- *ADCC-3960 SXGA CMOS Imager Design Guide* – schematics, flex circuit design guidelines
- *ADCC-3960 SXGA CMOS Imager User Manual* – operation, data output formats, communications details
- *ADCC-3960 SXGA CMOS Imager Register Reference* – bit-level detail of all programmable registers

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