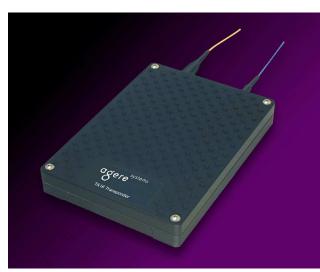
# ageressystems

Data Sheet March 2001

# TA16-Type 2.5 Gbits/s Transponder with 16-Channel 155 Mbits/s Multiplexer/Demultiplexer



The TA16-Type transponders integrate up to 15 discrete ICs and optical components, including a 2.5 Gbits/s optical transmitter and receiver pair, all in a single, compact package.

# Features

- 2.5 Gbits/s optical transmitter and receiver with 16-channel 155 Mbits/s multiplexer/demultiplexer
- Available with 1.31 µm Fabry-Perot laser transmitter and PIN receiver for intraoffice applications, and 1.31 µm or 1.55 µm DFB laser transmitters and PIN or APD receiver for short-haul to long-haul applications
- Pigtailed low-profile package
- Differential LVPECL data interface
- Operating case temperature range: 0 °C to 65 °C
- Automatic transmitter optical power control
- Laser bias monitor output
- Optical transmitter disable input
- SONET frame-detect enable
- Loss of signal, loss of sync, loss of framing alarms
- Diagnostic loopback capability
- Line loopback operation

### **Applications**

- Telecommunications:
  - Inter- and intraoffice SONET/SDH
  - Subscriber loop
  - Metropolitan area networks
- High-speed data communications

# Description

The TA16 transponder performs the parallel-to-serialto-optical transport and optical transport-to-serial-toparallel function of the SONET/SDH protocol. The TA16 transmitter performs the bit serialization and optical transmission of SONET/SDH OC-48/STM-16 data that has been formatted into standard SONET/ SDH compliant, 16-bit parallel format. The TA16 receiver performs the optical-to-electrical conversion function and is then able to detect frame and byte boundaries and demultiplex the serial data into 16-bit parallel OC-48/STM-16 format.

**Note**: The TA16 transponder does not perform bytelevel multiplexing or interleaving.

Figure 1 shows a simplified block diagram of the TA16-type transponder. This device is a bidirectional module designed to provide a SONET or SDH compliant electro-optical interface between the SONET/SDH photonic physical layer and the electrical section layer. The module contains a 2.5 Gbits/s optical transmitter and a 2.5 Gbits/s optical receiver in the same physical package along with the electronics necessary to multiplex and demultiplex sixteen 155 Mbits/s electrical channels. Clock synthesis and clock recovery circuits are also included within the module.

In the transmit direction, the transponder module multiplexes sixteen 155 Mbits/s LVPECL electrical data signals into an optical signal at 2488.32 Mbits/s for launching into optical fiber. An internal 2.488 GHz reference oscillator is phase-locked to an external 155 MHz data timing reference.

Page

# **Table of Contents**

#### Contents

#### Page Tables

Features	1
Applications	1
Description	1
Absolute Maximum Ratings	3
Pin Information	
Pin Descriptions	6
Functional Description	12
Receiver	
Transmitter	12
Loopback Modes	. 13
Transponder Interfacing	13
Optical Characteristics	
Electrical Characteristics	15
Timing Characteristics	. 17
Transmitter Data Input Timing	17
Input Timing Mode 1	18
Input Timing Mode 2	19
Forward Clocking	20
PCLK-to-PICLK Timing	21
PHERR/PHINIT	22
Receiver Framing	24
Qualification and Reliability	26
Laser Safety Information	
Class 1 Laser Product	26
Electromagnetic Emissions and Immunity	26
Outline Diagram	27
Ordering Information	
Related Product Information	28

Table 1. TA16-Type Transponder Pinout         Table 2. TA16-Type Transponder Input	6
Pin Descriptions	10
Table 3. TA16-Type Transponder Output	
Pin Descriptions	11
Table 4. OC48/STM-16 Transmitter Optical	
Characteristics	14
Table 5. OC48/STM-16 Receiver Optical	
Characteristics	14
Table 6. Transmitter Electrical I/O Characteristics	15
Table 7. Receiver Electrical I/O Characteristics	16
Table 8. Power Supply Characteristics	16
Table 9. Transmitter ac Timing Characteristics	23
Table 10. Receiver ac Timing Characteristics	23
Table 11. Ordering Information	28
Table 12. Related Product Information	28

# Figures

#### Page

Figure 1. TA16-Type Transponder Block Diagram	4
Figure 2. TA16-Type Transponder Pinout	5
Figure 3. Transponder Interfacing	13
Figure 4. Block Diagram Timing Mode 1	18
Figure 5. Block Diagram Timing Mode 2	19
Figure 6. Forward Clocking of TA16 Transmitter	20
Figure 7. PCLK-to-PICLK Timing	21
Figure 8. PHERR/PHINIT Timing	22
Figure 9. ac Input Timing	22
Figure 10. Receiver Output Timing Diagram	23
Figure 11. Frame and Byte Detection	24
Figure 12. OOF Timing (FRAMEN = High)	24
Figure 13. FRAMEN Timing	25
Figure 14. Interfacing to TxREFCLK Input	25

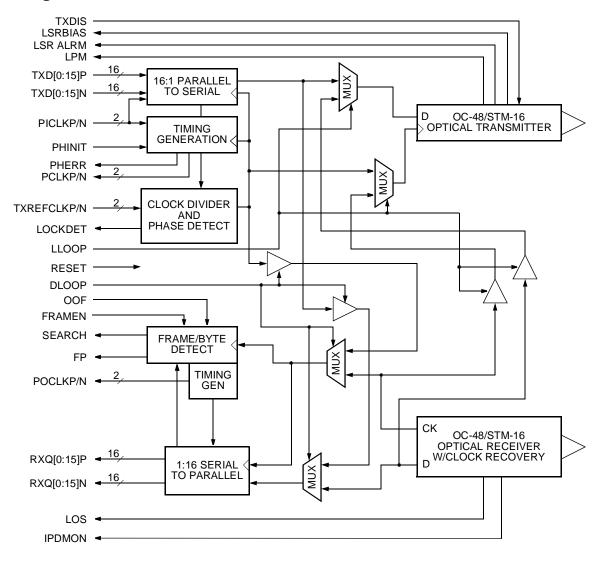
The optical transmitter is available with either a 1.31  $\mu$ m Fabry-Perot laser for short-reach applications or 1.31  $\mu$ m and 1.55  $\mu$ m DFB lasers for intermediate- to long-reach applications. The optical output signal is SONET and ITU compliant for OC-48/STM-16 applications as shown in Table 4, Optical Characteristics. In the receive direction, the transponder module receives a 2488.32 Mbits/s optical signal and converts it to an electrical signal, extracts a clock signal, and then demultiplexes the data into sixteen 155 Mbits/s differential LVPECL data signals. The optical receiver is available with either a PIN photodetector or with an APD photodetector. The receiver operates over the wavelength range of 1.1  $\mu$ m to 1.6  $\mu$ m and is fully compliant to SONET/SDH OC-48/STM-16 physical layer specifications as shown in Table 5, Optical Characteristics.

# **Absolute Maximum Ratings**

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect reliability.

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature Range	Тс	0	75	°C
Storage Case Temperature Range	Ts	-40	85	°C
Supply Voltage	—	-0.5	5.5	V
Voltage on Any LVPECL Pin	—	0	Vcc	—
High-speed LVPECL Output Source Current	—	—	50	mA
Static Discharge Voltage <sup>1</sup>	ESD	—	500	V
Relative Humidity (noncondensing)	RH	—	85	%
Receiver Optical Input Power—Biased: APD PIN	Pin Pin		0 8	dBm dBm
Minimum Fiber Bend Radius	_	1.25 (31.8)		in. (mm)

1. Human body model.



#### **Block Diagram**

1-1011(F).e

Figure 1. TA16-Type Transponder Block Diagram

# **Pin Information**

80         FCND         0         FCND         160           NC         0         NC         0         NC           NC         0         NC         0         NC           RXDGND         0         RXDGND         RXDGND           RXDGND							1
NC         0         NC           R         0         NC           PROCND         0         NCC           PROCND         0 <tn< td=""><td>80</td><td>FGND</td><td>0 0</td><td>FGND</td><td>160</td><td></td><td></td></tn<>	80	FGND	0 0	FGND	160		
NC         0         NC           RX0000         0         RX0010         RX0010           RX0000         0         RX0010         RX0010           RX0000         0         RX0010         RX0010           RX0000         0         RX0010         RX0010           RX0000         0         RX0000         RX0000           RX0000         0         RX0000         RX00000           RX0000         0         RX00000         RX00000           RX0000         0         RX00000         RX00000           RX00000         0 <td< td=""><td></td><td>NC</td><td></td><td>NC</td><td></td><td></td><td></td></td<>		NC		NC			
NSG         0         0         NC           PR X0000         0         RX0000         0         RX0000           PR X0000         0         RX0000         RX0000         RX0000           PR X0000         0         RX0000         RX0000         RX0000           RX0000         0         RX0000         RX00000         RX           RX0100         0         RX0110         0         RX0100           G0         RX0100         0         RX0110         0         RX0100           RX0100         0         RX0100         0         RX0100         0         RX0100           G0         RX0100         0         RX0100         0         RX0100         0         RX0100           RX0100         0         RX0100         0         RX0100         0         RX0100           RX0100         0         RX01000         0         RX01000         0         RX01000           RX01000 </td <td></td> <td></td> <td></td> <td>NC</td> <td></td> <td></td> <td></td>				NC			
RX0000       0       0       RX0010         RX0020       0       0       RX0010         RX0020       0       0       RX0010         RX0020       0       0       RX0010         RX0020       0       RX0020       0         RX0040       0       RX0050       0         RX0040       0       RX0050       0         RX0050       0       RX0070       RX0070         RX0050       0       RX0070       RX0070         RX0050       0       RX0070       RX0110         RX0100       0       RX0110       RX0110         RX0100       0       RX0110       RX0110         RX0100       0       RX0110       RX0110         RX0100       0       RX0110       RX0110         RX0100       0       RX0150       RX0100         RX0100       0       RX0110       RX0110         RX0100       0       RX0110       RX0110         RX01100       RX0110       RX0110       RX0110         RX01100       RX0110       RX0110       RX0110         RX01100       RX0110       RX0110       RX0110		NC	0 0	NC			
RX0000         0         0         RX0000           70         RX0000         0         RX0000           70         RX0000         0         RX0000           RX00000         0         RX0000		RXDGND		RXDGND			
RX0230       0       0       RX0330         70       RX0340       0       RX0340       150         RX0440       0       RX0350       RX0357         RX0440       0       RX0357       RX0357         RX0440       0       RX0357       RX0357         RX04580       0       RX0357       RX0357         RX04580       0       RX0357       RX0357         RX04581       0       RX0357       RX0457         RX04581       0       RX0458       RX0458         RX04581       0       RX0458							
70       RXDGND       0       RXDGND       150         RXDGND       0       RXDGND       RXDGND         RXDGND       0       RXDGND       RX         RXDGND       0       RXGND       RX         RXDGND       0       RXGND       RX         RXDGND       0       RXGND       RX         RXDGND       0       RXGND       IA         RXDGND       0       RXGND       IA         RXDGND       0       RXGND       IA         RXDGND       0       RXGND       IA         RXDGND       0       NC       IA         RXGND       0       RXAGND       IX         RXAGND       0       RXAGND       IX         RXAGND       0       RX330       IX       IX         RXAGND       0       RX330       IX       IX         RXAGND <td></td> <td>RXQ02N</td> <td></td> <td>RXQ03N</td> <td></td> <td></td> <td></td>		RXQ02N		RXQ03N			
R XQ04P       0       R XQ05P         R XQ04P       0       R XQ05P         R XQ05P       0       R XQ05P	70	RXQ02P		RXQ03P RXDGND	150		
RX0080         •         RX0070         RX           RX0080         •         RX0070         RX           RX0080         •         RX0070         RX           RX0100         •         RX0100         RX           RX0100         •         RX0110         RX           RX0100         •         RX0110         •           RX0100         •         RX0100         •           RX0100         •         RX320         •         RX320           RX0100         •         RX320         •         RX320           RX0000         •         RX320         • <td< td=""><td>10</td><td>RXQ04N</td><td>0 0</td><td>RXQ05N</td><td>150</td><td></td><td></td></td<>	10	RXQ04N	0 0	RXQ05N	150		
RX00P0         0         RX00FP         RX           RX00R0         0         RX00R0         0           RX00R0         0         RX00R0         0           RX00R0         0         RX00R0         0           RX00R0         0         RX011P           RX01F0         0         RX01P           RX01F0         0         RX01F0           RX01F0         0         RX00F0							
RXDCMD         0         RXDORND         KX           RXDQRD         0         RXDQRD         0         RXDQRD           RXDQRD         0         RXDQRD         0         RXDQRD           8000P         0         RXDQRD         0         RXDQRD           60         RXDCMD         0         RXDTP         0           8000P         0         RXDTP         0         RXDTP           8000P         0         RXDTP         RXDTP           8000P         RXDTP         RXDTP         RXDTP           8000P         RXDTP         RXDTP         RXDTP           8000P         RXDTP		RXQ06N RXQ06P		RXQ07N RXQ07P			
RX00P         0         RX01P         0         RX01P           00         RX01P         0         RX01P         0         RX01P           01         RX01P         0         RX01P         0         RX01P           01         RX01P         0         RX01P         0         RX01P           02         RX01P         0         RX01P         0         RX01P           03         RX01P         0         RX01P         0         RX01P           04         RX01P         0         RX01P         0         RX01P           05         RX02P         0         RX03P         0         NC           0         0         NC         0         NC         0           0         RX3AN         0         NC         0         NC           0         RX3AN         0         RX3AN         NC         0         NC           0         RX3AN         0         RX3AN         NC         0         RX3AN           0         RX3AN         0         RX3AN         0         RX3AN         NC           0         RXAGND         0         RX3AN         NC         0		RXDGND	0 0	RXDGND		RX	
RX0100         0         RX0110           00         RX0100         0         RX0110           01         RX0120         0         RX0110           01         RX0120         0         RX0130           01         RX0140         0         RX0150           02         RX0140         0         RX0150           03         RX0140         0         RX0150           04         RX0140         0         RX0150           05         RX0100         0         RX0140           05         RX0100         0         RX0150           050         RX0100         0         RX0100           0         0         RX0100         0           10         RX0100         0         RX0100           10         RX0000							
60         RX00RN         0         RX013         RX013           RX0128         0         RX0139         RX0139           RX0129         0         RX0139         RX0139           RX0129         0         RX0139         RX0139           RX0129         0         RX0139         RX0139           RX0120         0         RX0139         RX0139           RX0120         0         RX0110         RX0110           NC         0         NC         NC           NC         0         NC         NC           NC         0         NC         NC           NC         0         NC         NC           RX330         0         RX330         RX330           RX330         0         RX00ND         RX00ND           RX330         0         RX00ND         120           NC         0         OCF         RX00ND           RX330         0         RX00ND         120           NC         0         NC         NC           LSRMA         0         NC         NC           LSRMA         0         NC           LSRMA         0		RXQ10N		RXQ11N			
RX0129         0         RX013N           RX0124         0         RX013P           RX0140         0         RX013P           RX0140         0         RX013P           RX0140         0         RX013P           RX0140         0         RX014P           RX0140         0         RX014P           RX0140         0         RX014P           RX0140         0         RX014P           RX0140         0         NC           RX0140         0         NC           RX0140         0         NC           RX0140         0         RX014N           RX0140         0         RX46ND           RX0140         0         RX46ND           RX330         0         RX33D           RX330         0         RX40ND		RXQ10P					
RX0129         0         RX0139           RX0144         0         RX0159           RX0147         0         RX0159           RX0148         0         RX0159           RX0149         0         RX0159           RX0149         0         RX0050           NC         0         NC           NC         0         NC           NC         0         NC           NC         0         NC           RX0200         0         NC           RX0300         0         POCLKN           RX330         0         RX330           RX0RND	60				140		
RX014P         0         0         RX05ND           NC         0         NC           RX05ND         0         NC           RX05ND         0         POCLKN           RX3AR         0         PCCLKN           RX3AB         0         RX3AB           RXDGND         0         RXDGND           LPM         0         RXDGND           LPM         0         TXA3A           TX3AB         0         TXAGND           10         TXAGND         0         TXAGND <td< td=""><td></td><td>RXQ12P</td><td>0 0</td><td>RXQ13P</td><td></td><td></td><td></td></td<>		RXQ12P	0 0	RXQ13P			
RXDGND         0         0         NC           NC         0         NC           S0         RXAGND         0           RX3A30         0         PCCLKN           RX3A30         0         RX3A30           NC         0         SEARCH           RX3A30         0         RX3A30           NC         0         SEARCH           RX3A30         0         RX3A30           NC         0         NX3A30           NC         0         NX3A3A           NC         0         NX3A3		RXQ14N RXQ14P		RXQ15N RXQ15P			/
NC         0         0         NC           NC         0         NC         NC           RX4610         0         NC         NC           50         RX4610         0         POCLKN         130           RX333         0         0         RX333         0         POCLKN           RX333         0         0         RX330         RX333         0         RX330           NC         0         SEARCH         RX330         RX330         RX330         RX330           NC         0         SEARCH         RX330         RX330         RX330         RX330           RX330         0         RX330         RX330         RX330         RX330         RX330           NC         0         RXGRMD         RX330         RX330         RX330         RX330           10         RX331         0         RX330         RX330         RX330         RX330           10         TX330         0         RX330         RX330         RX330         RX330           10         TX330         0         RX330         RX330         RX330         RX330           10         TX0040         RX330         R		RXDGND	0 0	RXDGND			
NC         0         NC           50         RXAGND         0         POCLKN           50         RXAGND         0         PCCLKN           RXAGND         0         RXAGND         RXAGND           RXAGND         0         PCCLKN         130           RXAGND         0         RXAGND         RXAGND           RXAGND         0         RXAGND         0           RXAGND         0         RXAGND         0           RXAGND         0         RXAGND         0           RXAGND         0         TXAGND         0           RXAGND         0         TXAGND           RXAGND				NC			
RXAGND       0       NC         50       RXAGND       0       POCLKN         RXAGND       0       0       ROCLKP         RXAGND       0       0       RXAGND         RX330       0       0       RXAGND         RXDGND       0       RXAGND       0         RXDGND       0       COC       RXAGND         RXAGND       0       RXAGND       0         RXAGND       0       RXAGND       0         RXDGND       0       TXAGND       0       RXAGND				NC			
RXAGND       0       0       RXAGND         RXAGND       0       RXAGND       0       RXAGND         RX3330       0       RX330       0       RX330         RXBOND       0       RX00ND       120         RXBND       0       RXGND       0         FRAMEN       0       0       RXGND         DLOOP       0       DLOOP       0         DLOOP       0       DLOOP       0         NC       0       RXGND       0         XAGND       0       NC       TX330         JUNC       0       NC       TX330         JUNC       0       NC       TX330         JUNC       0       NC       TX330         JUNC       0       TXAGND       0         TXAGND       0       TXAGND       0         TXAGND       0       TXAGND       TXAGND         TXDGND       0       TXDORN       TXDORN     <				NC			
RX33A       0       0       RX3A         RXAGND       0       0       RXAGND         RXAGND       0       0       SEARCH         RX33D       0       RX33D       0       RX33D         RX33D       0       RX0GND       120         H0       FF       0       O       O         RX6ND       0       D       D       D         LSRALM       0       NC       ISA       ISA         LSRALM       0       TX03P       NC       ISA         TX33A       0       TX3A       TX3A       ISA         TX33A       0       TX3A       ISA       ISA         TX33A       0       TX0GND       ISA       ISA         TXAGND       0       TX0GND       ISA       ISA         TX00ND       0	50	RXAGND		POCLKN	130		
RXACND       0       0       RXACND         NC       0       0       RX3.3D         RX3.3D       0       0       RX3.3D         RX0DND       0       0       RXDGND         RX0END       0       0       OC         NC       0       0       OC         DLOOP       0       LCOP       OC         NC       0       NC       OC         LSRALM       0       NCC       TX3.3D         TXAGND       0       TX3.3D       O         TXAGND       0       TX3.3D       O         TXAGND       0       TXAGND       O         TX3.3D       O       TXAGND       O         TXAGND       O       TXOND       O       TXOND         PICLKN       O       TXOCND       TXOCND         TXORND       O       TXOCND       TXOCND         TXORND       O       TXOCND       TXOCND		RX3.3A	0 0	RX3.3A			
NC         0         0         SEARCH           RX3.3D         0         0         RX3.3D           RXDGND         0         RX3.3D           FRAMEN         0         0         COF           40         FP         0         0         COP           NC         0         0         LOOP         0           LOOP         0         LLOOP         0         LOOP           NC         0         0         PHERR         0           LSRALM         0         0         PHINIT         TX3.3A           TX3.3A         0         0         TX3.3A         0           TXAGND         0         TXAGND         0         TXAGND           TXAGND         0         TXAGND         0         TXAGND           TXAGND         0         TXDOND         0         PCLKN           TXDOND         0         TXDOND         0         TXDOND           PCLKP         0         TXDOND         0         TXDOND           TXDOND         0         TXDOND         0         TXDOND           TXDOND         0         TXDOND         0         TXDOND		RXAGND		RXAGND			
RX330       0       RXX330       0       RXX330       0       RXX330       0       RXX330       0<		NC	0 0	SEARCH			
RXDGND       0       0 CF         40       FP       0       RXDGND         10       C       0       0.05         DLOOP       0       LLOOP         NC       0       0.05         DLOOP       0       LLOOP         NC       0       PHERR         LSRALM       0       TXDIS         LPM       0       PHINIT         TXAGND       0       TX3.30         30       TXAGND       0         TX3.30       0       TXOGND         TX3.30       0       TXOGND         PCLKP       ICKP         LOCKDET       0       TXDOGND         TXDGND       0       TXDOGND         PICLKP       0       TXDOGND         LOCKDET       0       TXDOGND         TXDOGND		RX3.3D					
40 FP 0 0 1 RXDGND 120 NC 0 1 LLOOP NC 0 0 1 LLOOP NC 0 0 PHERR LSRBIAS 0 0 NC TX333 0 0 TXDIS LPM 0 0 PHINIT TX33A 0 0 TX33D 30 TXAGND 0 0 TXAGND 110 T333 D 0 0 TXAGND 110 T333 D 0 0 PCLN TX33D 0 0 PCLP LOCKDET 0 0 TXDGND PICLKP 0 0 TXDGND PICLKP 0 0 TXDGND PICLKP 0 0 TXDGND TXD01N 0 0 TXD02P TXD01N 0 0 TXD02P TXD01N 0 0 TXD02P TXD03N 0 0 TXD04N TXD03N 0 0 TXD04N TXD03N 0 0 TXD04N TXD03N 0 0 TXD04N TXD05N 0 0 TXD14N TXD05N 0 0 TXD14N TXD15N 0 0 TXD4P TXD5N 0 0 0 TXD4P TXD5N 0 0 TXD4P		RXDGND	0 0	RXDGND			
NC         0 $IOS$ NC           DLOOP         NC         0         PHERR           LSRBIAS         0         NC           LSRBIAS         0         TXJIS           LPM         0         PHINIT           TXA3A         0         TX3.3A           TX3.3A         0         TX3.3D           30         TXAGND         0           TX3.3D         0         TXAGND           TX3.3D         0         TXAGND           J         TX3.3D         10           TX3.3D         0         TXAGND           J         TX3.3D         10           TX3.3D         0         TXAGND           J         TX3.3D         10           TXDGND         0         TXDGND           TXDONN         0         TXDONN           PICLKN         0         TXDONN           TXDONN         0	40	FRAMEN		OOF	120		
DLOOP         0         0         LUCOP           NC         0         NC           LSRALM         0         TXDIS           LPM         0         PHINIT           TX33A         0         TX3A           TX33A         0         TX3A           TX33A         0         TX3A           TX33A         0         TXAGND           TX33D         0         TXAGND           TX33D         0         TXAGND           TX33D         0         TXAGND           TX33D         0         PCLKN           TX33D         0         PCLKN           TXDOND         0         PCLKN           PICLKN         0         TXDOOP           TXDOND         0         TXDOND           PICLKN         0         TXDOOP           TXDOND         0         TXDOND	40	NC		LOS	120		
LSRBIAS 0 0 NC LSRALM 0 0 PHINIT TXAGND 0 0 PHINIT TXAGND 0 0 TX3.3A TX3.3A 0 0 TX3.3A TX3.3A 0 0 TX3.3A TX3.3B 0 0 TXAGND 110 TX3.3D 0 0 PCLNN TXDGND 0 0 TXDGND PCLN 0 0 TXDGND PCLN 0 0 TXDGND PCLN 0 0 TXDGND PCLN 0 0 TXDGND TXDOIP 0 0 TXDOP TXDOIP 0 0 TXDOP TXDOIP 0 0 TXDOAN TXDOIP 0 0 TXDOAN TXDOSP 0 0 TXDOAN TXDOAN TXDOSP 0 0 TXDOAN TXDOAN TXDOSP 0 0 TXDOAN		DLOOP		LLOOP			
LSRALM 0 0 TXDIS LPM 0 0 PHINT TXAGND 0 0 TX33A TX33A 0 0 TX33D 30 TXAGND 0 0 TX33D 30 TXAGND 0 0 TXAGND 110 TX33D 0 0 TXAGND 110 TX33D 0 0 PCLKP TXDGND 0 0 PCLKP LOCKDET 0 0 TXDGND PICLKN 0 TXD00N PICLKP 0 0 TXD00N PICLKP 0 0 TXD00P TXD01N 0 0 TXD02N TXD01N 0 0 TXD02P 20 TXD03P 0 0 TXD04M 100 TXD03P 0 0 TXD04P TXD05N 0 0 TXD06N TXD05P 0 0 TXD06N TXD05P 0 0 TXD06N TXD05P 0 0 TXD08N TX TXD05N 0 0 TXD04P TXD05N 0 0							
TXAGND       0       0       NC         TX33A       0       TX33A       TX33D         30       TXAGND       0       TXAGND         TX33D       0       TXAGND       110         TX33D       0       PCLKN         TX0GND       0       PCLKP         LOCKDET       0       TXDOND         PICLKN       0       TXDOND         PICLKP       0       TXDOND         TXDOND       0		LSRALM		TXDIS			
TX3.3A       0       0       TX3.3A         30       TXAGND       0       0       TXAGND       110         TX3.3D       0       0       TXDGND       110         TX3.3D       0       0       PCLKN       TXDGND       110         TX3.3D       0       0       PCLKN       TXDGND       110         TX3.3D       0       0       PCLKN       110       TX3.3D       110         TX3.3D       0       0       PCLKN       0       TXDGND       110       TX3.3D       110       TX3.3D       110       TX3.3D       0       0       PCLKN       0       TXDGND       0       TXDGND       0       TXDGND       0       TXDON       TXDON       TXDON       TXDON       0 <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>							
30 TXAGND 0 0 TXAGND 110 TX33D 0 0 PCLKN TXDGND 0 PCLKN TXDGND 0 PCLKP PCLKN 0 PCLKP PCLKN 0 TXDGND PCLKN 0 TXDGND PCLKN 0 0 TXDGND TXDGND 0 0 TXDGND TXDGND 0 0 TXD02P TXD01P 0 TXD02P 20 TXD3N 0 TXD02P TXD03N 0 TXD04N 100 TXD05P 0 TXD04P TXD05N 0 0 TXD04P TXD05N 0 0 TXD06P TXD05P 0 0 TXD06P TXD07N 0 0 TXD06P TXD07N 0 0 TXD08N TX TXD07N 0 0 TXD08N TX TXD07N 0 0 TXD08P TXD05N 0 0 TXD08P TXD05N 0 0 TXD04P TXD05N 0 0 TXD10P 10 TXD1N 0 0 TXD12P TXD1N 0 0 TXD14P TXD1N 0 0 TXD14P TXD1SP 0 0 TXD14P TXD1SP 0 0 TXD14P TXD1SP 0 0 TXD14P TXD1SP 0 0 TXBFCLKN TXD1SP 0 0 TXBFCLKN TXD1SP 0 0 TXREFCLKN TXD1SP 0 0 TXREFCLKN TXD1SP 0 0 TXREFCLKN TXD1SP 0 0 TXD14P		TX3.3A	0 0	TX3.3A			
TX3.3D       0       0       TXDGND         TX3.3D       0       0       PCLKP         TXDGND       0       PCLKP         LOCKDET       0       TXDGND         PICLKP       0       TXDONP         PICLKP       0       TXDONP         TXD1P       0       TXD0P         TXD01N       0       TXD02P         20       TXD3N       0         TXD0N       0       TXD04P         TXD0NP       0       TXD04P         TXD0NP       0       TXD1N         TXD0NP       0       TXD1N         TXD1NP       0       TXD1N         TXD1	30			TX3.3D	110		
TXDGND         0         PCLKP           LOCKDET         0         TXDGND           PICLKN         0         TXD00N           PICLKP         0         TXD0N           0         TXD02N         0           TXD01N         0         TXD02N           TXD01N         0         TXD02N           TXD01N         0         TXD02N           TXD03N         0         TXD04N           TXD05N         0         TXD1N           TXD05N         0         TXD1N           TXD11N         0         TXD12N <td>50</td> <td></td> <td>0 0</td> <td>TXDGND</td> <td>110</td> <td></td> <td></td>	50		0 0	TXDGND	110		
LOCKDET 0 0 TXDGND PICLKP 0 0 TXD00P TXDGND 0 0 TXD00P TXDGND 0 0 TXD02P TXD01P 0 0 TXD02P 20 TXD03P 0 0 TXD04P TXD03P 0 0 TXD04P TXD05P 0 0 TXD04P TXD05P 0 0 TXD04P TXD05P 0 0 TXD06P TXD05P 0 0 TXD06P TXD05P 0 0 TXD08P TXD05P 0 0 TXD08P TXD05P 0 0 TXD08P TXD07P 0 0 TXD08P TXD07P 0 0 TXD08P TXD09P 0 0 TXD08P TXD09P 0 0 TXD10P TXD09P 0 0 TXD10P TXD11P 0 0 TXD12P TXD09P 0 0 TXD12P TXD11P 0 TXD12P TXD11P 0 TXD12P TXD11P 0 TXD12P TXD11P 0 TXD12P TXD15P 0 0 TXD12P TXD15P 0 0 TXD14P TXD15P 0 0 TXREFCLKN TXD15P 0 0 TXREFCLKN		TX3.3D					
PICLKN 0 0 TXD00N PICLKP 0 0 TXD00P TXDGND 0 0 TXD00P TXD01P 0 TXD02N TXD01P 0 0 TXD02P 20 TXD03N 0 0 TXD04N 100 TXD05N 0 0 TXD04N TXD05D 0 0 TXD06P TXD05P 0 0 TXD06P TXD05P 0 0 TXD06P TXD07N 0 0 TXD08N TX TXD07N 0 0 TXD08N TX TXD07N 0 0 TXD08N TXD09P 0 0 TXD08N TXD09P 0 0 TXD08P TXD0N 0 0 TXD10P TXD09N 0 0 TXD12N TXD09N 0 0 TXD12N TXD09N 0 0 TXD12N TXD1N 0 0 TXD1N TXD1N 0 0 TXD1N 0 0 TXD1N TXD1N 0 0 TXD1N 0 0 TXD1N TXD1N 0 0 TXD1N 0 0 TXD1N 0 0 TXD1N 0 0 0		LOCKDET	0 0	TXDGND			
TXDGND       0       TXDGND         TXD01N       0       TXD02N         TXD01P       0       TXD02P         20       TXD03N       0       TXD04N         TXD05ND       0       TXD04N       100         TXD05ND       0       TXD04P       TXD04P         TXD05ND       0       TXD04P       TXD04P         TXD05ND       0       TXD06N       TXD04P         TXD05ND       0       TXD06N       TXD04P         TXD05ND       0       TXD06N       TXD04P         TXD05ND       0       TXD06N       TXD04P         TXD05ND       0       TXD08N       TX         TXD07P       0       TXD08N       TX         TXD09N       0       TXD10N       TXD1NN         TXD09N       0       TXD1NN       TXD1NN         TXD1N       0       TXD12N       90         TXD1N       0       TXD12N       90         TXD1N       0       TXD12N       10         TXD13P       0       TXD14N       TXD13N         TXD13N       0       TXD14N       TXD14N         TXD13P       0       TXD14N       TX		PICLKN					/
TXD01P         0         TXD02P           20         TXD03N         0         TXD04N         100           TXD03P         0         0         TXD04P         100           TXD03N         0         0         TXD04P         100           TXD05N         0         TXD05N         0         TXD05N           TXD05N         0         TXD05N         0         TXD05N           TXD05N         0         TXD05N         0         TXD05N           TXD07N         0         TXD08N         TX           TXD09N         0         TXD01P         10           TXD11N         0         TXD12N         90           TXD11P         0         TXD12P         10           TXD11P         0         TXD12P         10           TXD11P         0         TXD12P         10           TXD13N         0         TXD14P           TXD15P         0		TXDGND	0 0	TXDGND			
20 TXD03N 0 0 TXD04N 100 TXD03P 0 0 TXD04P TXD05N 0 0 TXD04P TXD05N 0 0 TXD06P TXD07N 0 0 TXD08P TXD07N 0 0 TXD08P TXD07N 0 0 TXD08P TXD07N 0 0 TXD08P TXD09P 0 0 TXD10P TXD09P 0 0 TXD10P TXD1N 0 0 TXD12P TXD1N 0 0 TXD14P TXD13P 0 0 TXD14P TXD14P TXD14P 0 0 TXD14P TXD14P 0 0 TXD14P TXD14P							
TXD03P       0       0       TXD04P         TXD05D       0       TXD06N         TXD05P       0       TXD06N         TXD07N       0       TXD08N         TXD07N       0       TXD08N         TXD07N       0       TXD08N         TXD07N       0       TXD08N         TXD07N       0       TXD08P         TXD07N       0       TXD08N         TXD07N       0       TXD08P         TXD07P       0       TXD08P         TXD09N       0       TXD08D         TXD11N       0       TXD12N         TXD11P       0       TXD12P         TXD11P       0       TXD12P         TXD11P       0       TXD14N         TXD13N       0       TXD14P         TXD13N       0       TXREFCLKN         TXD15P       0       TXREFCLKN         TXD15P       0       TXREFCLKN         TXD08ND       0       TXD6ND         TXD0ND       0       TXD6ND         TXD10N       0       TXREFCLKN         TXD10N       0       TXD6ND         IPDMON       0       RESET <td>20</td> <td></td> <td></td> <td></td> <td>100</td> <td></td> <td></td>	20				100		
TXD05N       0       0       TXD06P         TXD07N       0       TXD08P       TX         TXD07D       0       TXD08P       TX         TXD07D       0       TXD08P       TX         TXD07D       0       TXD08P       TX         TXD07D       0       TXD08P       TXD08P         TXD07D       0       TXD08P       TXD08P         TXD07D       0       TXD10N       TXD10N         TXD09P       0       TXD10N       TXD12N         TXD09D       0       TXD12P       TXD12P         TXD11P       0       TXD14N       TXD14N         TXD13N       0       TXD14P       TXD14P         TXD13N       0       TXREFCLKN       TOP VIEW         TXD15P       0       TXREFCLKN       TOP VIEW         TXD15P       0       TXREFCLKN       TOP VIEW         TXD08ND       0       RESET       TOP VIEW		TXD03P		TXD04P			
TXD05P         0         0         TXD06P           TXD07N         0         0         TXD08N         TX           TXD07N         0         0         TXD08P         TX           TXD09N         0         TXD08N         TX           TXD09N         0         TXD09N         TXD10N           TXD09P         0         TXD10N         TXD1N           TXD11N         0         TXD12N         90           TXD11P         0         TXD12P         TXD13N           TXD13N         0         TXD14N         TXD13P           TXD13P         0         TXD14P         TXD14P           TXD13N         0         TXD14N         TXD13N           TXD15P         0         TXREFCLKN         TOP VIEW           TXD6ND         0         TXREFCLKN         TOP VIEW           TXD6ND         0         TXREFCLKN         TOP VIEW							
TXDGYP         0         0         TXD08P           TXDGND         0         0         TXDGND           TXD09N         0         TXD10N           TXD09P         0         TXD10P           10         TXD11         0         TXD12N           TXD11P         0         TXD12P           TXD11P         0         TXD12P           TXD13N         0         TXD14N           TXD13P         0         TXD14P           TXD13P         0         TXD14P           TXD13P         0         TXBEFCLKN           TXD5P         0         TXREFCLKN           TXD6ND         0         TXD6ND           TXD5P         0         TXREFCLKN           TXD6ND         0         TXB6ND           IPDMON         0         RESET		TXD05P	0 0	TXD06P			
TXDGND       0       0       TXDGND         TXD09N       0       TXD10N         TXD09P       0       TXD10P         10       TXD11N       0       TXD12N         TXD1N       0       TXD12P         TXD1N       0       TXD12P         TXD1N       0       TXD12P         TXD1N       0       TXD14N         TXD13P       0       TXD14N         TXD13P       0       TXD14P         TXD15P       0       TXREFCLKN         TXD5P       0       TXREFCLKN         TXD6ND       0       TXD6ND         IPDMON       0       RESET				TXD08N		IX	
TXD09P       0       TXD10P         10       TXD11N       0       TXD12N         10       TXD11P       0       TXD12N         TXDGND       0       TXD12P         TXD3N       0       TXD14N         TXD13N       0       TXD14N         TXD13P       0       TXD14P         TXD13P       0       TXD14P         TXD13P       0       TXD14N         TXD15N       0       TXREFCLKN         TXD15P       0       TXREFCLKP         TXDGND       0       TXD6ND         IPDMON       0       RESET		TXDGND	0 0	TXDGND			
10 TXD11N 0 0 TXD12N 90 TXD1P 0 0 TXD12P TXDGND 0 0 TXD12P TXD13N 0 0 TXD14N TXD13P 0 0 TXD14P TXD15N 0 0 TXREFCLKN TXD15P 0 0 TXREFCLKP TXD15P 0 0 TXREFCLKP TXDGND 0 0 TXREFCLKP TXDGND 0 0 TXREFCLKP TXDGND 0 0 TXREFCLKP							
TXD11P       0       1 XD12P         TXD60D       0       1 XD6ND         TXD13N       0       1 XD14N         TXD13P       0       1 XD14P         TXD15N       0       1 XREFCLKN         TXD15P       0       1 XREFCLKP         TXD6ND       0       1 XD6ND         IPDMON       0       RESET	10	TXD11N	0 0	TXD12N	90		
TXD13N       0       0       TXD14N         TXD13P       0       0       TXD14P         TXD15N       0       0       TXREFCLKN         TXD15P       0       0       TXREFCLKP         TXDGND       0       0       TXDGND         IPDMON       0       RESET		TXD11P		TXD12P			
TXD13P         0         0         TXD14P           TXD15N         0         0         TXREFCLKN         TOP VIEW           TXD15P         0         TXREFCLKP         TOP VIEW           TXDGND         0         TXDGND         0           IPDMON         0         RESET         TOP VIEW		TXD13N	0 0	TXD14N			
TXD15P 0 0 TXREFCLKP TXDGND 0 0 TXRGND TXDGND 0 0 RESET		TXD13P		TXD14P			
TXDGND O TXDGND IPDMON O RESET							TOP VIEW
		TXDGND		TXDGND			
	1			FGND	81		
			-		- 1		

1-1014(F).r2

Figure 2. TA16-Type Transponder Pinout

# **Pin Descriptions**

#### Table 1. TA16-Type Transponder Pinout

01         FGND         I         Supply         Frame Ground           02         IPDMON         O         Analog         Receiver Photon	nd <sup>1</sup>		
02 IPDMON O Analog Receiver Pho			
	Receiver Photodiode Current Monitor		
03 TxDGND I Supply Transmitter D	Digital Ground		
04 TxD15P I LVPECL Transmitter 1	Transmitter 155 Mbits/s MSB Data Input		
05 TxD15N I LVPECL Transmitter 1	Transmitter 155 Mbits/s MSB Data Input		
06 TxD13P I LVPECL Transmitter 1	155 Mbits/s Data Input		
07 TxD13N I LVPECL Transmitter 1	Transmitter 155 Mbits/s Data Input		
08 TxDGND I Supply Transmitter D	Transmitter Digital Ground		
09 TxD11P I LVPECL Transmitter 1	155 Mbits/s Data Input		
10 TxD11N I LVPECL Transmitter 1	155 Mbits/s Data Input		
11 TxD09P I LVPECL Transmitter 1	155 Mbits/s Data Input		
12 TxD09N I LVPECL Transmitter 1	155 Mbits/s Data Input		
13 TxDGND I Supply Transmitter D	Digital Ground		
14 TxD07P I LVPECL Transmitter 1	155 Mbits/s Data Input		
15 TxD07N I LVPECL Transmitter 1	155 Mbits/s Data Input		
16 TxD05P I LVPECL Transmitter 1	155 Mbits/s Data Input		
17 TxD05N I LVPECL Transmitter 1	155 Mbits/s Data Input		
18 TxDGND I Supply Transmitter D	Digital Ground		
19 TxD03P I LVPECL Transmitter 1	Transmitter 155 Mbits/s Data Input		
20 TxD03N I LVPECL Transmitter 1	Transmitter 155 Mbits/s Data Input		
21 TxD01P I LVPECL Transmitter 1	Transmitter 155 Mbits/s Data Input		
22 TxD01N I LVPECL Transmitter 1	Transmitter 155 Mbits/s Data Input		
23 TxDGND I Supply Transmitter D	Transmitter Digital Ground		
24 PICLKP I LVPECL Byte-Aligned	Byte-Aligned Parallel Input Clock at 155 MHz		
25 PICLKN I LVPECL Byte-Aligned	Byte-Aligned Parallel Input Clock ar 155 MHz		
26 LOCKDET O LVTTL Lock Detect			
27 TxDGND I Supply Transmitter D	Digital Ground		
28 Tx3.3D I Supply Transmitter 3	3.3 V Digital Supply		
29 Tx3.3D I Supply Transmitter 3	3.3 V Digital Supply		
30 TxAGND I Supply Transmitter A	Analog Ground		
31 Tx3.3A I Supply Transmitter 3	3.3 V Analog Supply		
32 Tx3.3A I Supply Transmitter 3	3.3 V Analog Supply		
33 TxAGND I Supply Transmitter A	Analog Ground		
34 LPM O Analog Laser Power	<sup>r</sup> Monitor		
35 LSRALRM O Analog Laser Degrad	de Alarm		
36 LSRBIAS O Analog Transmitter L	_aser Bias Output		
37 NC — — No User Con	nnection Permitted		
38 DLOOP I LVTTL Diagnostic Lo	oopback		
39 NC — — No User Con	nnection Permitted		
40 FP O LVPECL Frame Pulse	)		
41 FRAMEN I LVTTL Frame Enabl	le		
42 RxDGND I Supply Receiver Digital Ground			

1. Frame ground is connected to the housing and is isolated from all circuit grounds (TxDGND, TxAGND, RxDGND, RxAGND).

Pin #	Pin Name	I/O	Logic	Description	
43	Rx3.3D	Ι	Supply	Receiver 3.3 V Digital Supply	
44	Rx3.3D	Ι	Supply	Receiver 3.3 V Digital Supply	
45	NC		_	No User Connection Permitted	
46	RxAGND	Ι	Supply	Receiver Analog Ground	
47	RxAGND	Ι	Supply	Receiver Analog Ground	
48	Rx3.3A	Ι	Supply	Receiver 3.3 V Analog Supply	
49	RxAGND	Ι	Supply	Receiver Analog Ground	
50	RxAGND	Ι	Supply	Receiver Analog Ground	
51	RxDGND	Ι	Supply	Receiver Digital Ground	
52	NC	_		No User Connection Permitted	
53	NC	_		No User Connection Permitted	
54	NC			No User Connection Permitted	
55	RxDGND	I	Supply	Receiver Digital Ground	
56	RxQ14P	0	LVPECL	Receiver 155 Mbits/s Data Output	
57	RxQ14N	0	LVPECL	Receiver 155 Mbits/s Data Output	
58	RxQ12P	0	LVPECL	Receiver 155 Mbits/s Data Output	
59	RxQ12N	0	LVPECL	Receiver 155 Mbits/s Data Output	
60	RxDGND	I	Supply	Receiver Digital Ground	
61	RxQ10P	0	LVPECL	Receiver 155 Mbits/s Data Output	
62	RxQ10N	0	LVPECL	Receiver 155 Mbits/s Data Output	
63	RxQ08P	0	LVPECL	Receiver 155 Mbits/s Data Output	
64	RxQ08N	0	LVPECL	Receiver 155 Mbits/s Data Output	
65	RxDGND	Ι	Supply	Receiver Digital Ground	
66	RxQ06P	0	LVPECL	Receiver 155 Mbits/s Data Output	
67	RxQ06N	0	LVPECL	Receiver 155 Mbits/s Data Output	
68	RxQ04P	0	LVPECL	Receiver 155 Mbits/s Data Output	
69	RxQ04N	0	LVPECL	Receiver 155 Mbits/s Data Output	
70	RxDGND	Ι	Supply	Receiver Digital Ground	
71	RxQ02P	0	LVPECL	Receiver 155 Mbits/s Data Output	
72	RxQ02N	0	LVPECL	Receiver 155 Mbits/s Data Output	
73	RxQ00P	0	LVPECL	Receiver 155 Mbits/s LSB Data Output	
74	RxQ00N	0	LVPECL	Receiver 155 Mbits/s LSB Data Output	
75	RxDGND	I	Supply	Receiver Digital Ground	
76	NC	—		No User Connection Permitted	
77	NC	—		No User Connection Permitted	
78	NC	—	—	No User Connection Permitted	
79	NC	—	—	No User Connection Permitted	
80	FGND	I	Supply	Frame Ground <sup>1</sup>	
81	FGND	Ι	Supply	Frame Ground <sup>1</sup>	
82	RESET	Ι	LVTTL	Master Reset	
83	TxDGND	Ι	Supply	Transmitter Digital Ground	
84	TxRefClkP	Ι	LVPECL		
85	TxRefClkN	I	LVPECL	Transmitter 155 Mbits/s Reference Clock Input	

#### Table 1. TA16-Type Transponder Pinout (continued)

1. Frame ground is connected to the housing and is isolated from all circuit grounds (TxDGND, TxAGND, RxDGND, RxAGND). Agere Systems Inc.

#### Table 1. TA16-Type Transponder Pinout (continued)

Pin #	Pin Name	I/O	Logic	Description	
86	TxD14P	I	LVPECL	Transmitter 155 Mbits/s Data Input	
87	TxD14N	I	LVPECL	Transmitter 155 Mbits/s Data Input	
88	TxDGND	I	SUPPLY	Transmitter Digital Ground	
89	TxD12P	I	LVPECL	Transmitter 155 Mbits/s Data Input	
90	TxD12N	I	LVPECL	Transmitter 155 Mbits/s Data Input	
91	TxD10P	I	LVPECL	Transmitter 155 Mbits/s Data Input	
92	TxD10N	I	LVPECL	Transmitter 155 Mbits/s Data Input	
93	TxDGND	I	Supply	Transmitter Digital Ground	
94	TxD08P	I	LVPECL	Transmitter 155 Mbits/s Data Input	
95	TxD08N	I	LVPECL	Transmitter 155 Mbits/s Data Input	
96	TxD06P	I	LVPECL	Transmitter 155 Mbits/s Data Input	
97	TxD06N	I	LVPECL	Transmitter 155 Mbits/s Data Input	
98	TxDGND	I	Supply	Transmitter Digital Ground	
99	TxD04P	I	LVPECL	Transmitter 155 Mbits/s Data Input	
100	TxD04N	I	LVPECL	Transmitter 155 Mbits/s Data Input	
101	TxD02P	I	LVPECL	Transmitter 155 Mbits/s Data Input	
102	TxD02N	I	LVPECL	Transmitter 155 Mbits/s Data Input	
103	TxDGND	I	Supply	Transmitter Digital Ground	
104	TxD00P	I	LVPECL	Transmitter 155 Mbits/s LSB Data Input	
105	TxD00N	I	LVPECL	Transmitter 155 Mbits/s LSB Data Input	
106	TxDGND	Ι	Supply	Transmitter Digital Ground	
107	PCLKP	0	LVPECL	Transmitter Parallel Reference Clock Output	
108	PCLKN	0	LVPECL	Transmitter Parallel Reference Clock Output	
109	TxDGND	Ι	Supply	Transmitter Digital Ground	
110	TxAGND	I	Supply	Transmitter Analog Ground	
111	Tx3.3D	I	Supply	Transmitter Digital 3.3 V Supply	
112	Tx3.3A	I	Supply	Transmitter Analog 3.3 V Supply	
113	NC	—		No User Connection Permitted	
114	PHINIT	I	LVPECL	Phase Initialization	
115	TxDIS	I	TTL	Transmitter Disable	
116	NC	—		No User Connection Permitted	
117	PHERR	0	LVPECL	Phase Error	
118	LLOOP	I	LVTTL	Line Loopback (active-low)	
119	LOS	0	LVTTL	Loss of Signal	
120	RxDGND	I	Supply	Receiver Digital Ground	
121	OOF	I	LVTTL	Out of Frame (enable frame detection)	
122	RxDGND	I	Supply	Receiver Digital Ground	
123	Rx3.3D	I	Supply	Receiver Digital 3.3 V Supply	
124	Rx3.3D	I	Supply	Receiver Digital 3.3 V Supply	
125	SEARCH	0	LVTTL	Frame Search Output	
126	RxAGND	I	Supply	Receiver Analog Ground	
127	RxAGND		Supply	-	
128	Rx3.3A	I	Supply	Receiver Analog 3.3 V Supply	

1. Frame ground is connected to the housing and is isolated from all circuit grounds (TxDGND, TxAGND, RxDGND, RxAGND).

Pin #	Pin Name	I/O	Logic	Description
129	POCLKP	0	LVPECL	Byte-Aligned Parallel Output Clock at 155 MHz
130	POCLKN	0	LVPECL	Byte-Aligned Parallel Output Clock at 155 MHz
131	NC			No User Connection Permitted
132	NC		_	No User Connection Permitted
133	NC	_	_	No User Connection Permitted
134	NC	_		No User Connection Permitted
135	RxDGND	I	Supply	Receiver Digital Ground
136	RxQ15P	0	LVPECL	Receiver MSB 155 Mbits/s Data Output
137	RxQ15N	0	LVPECL	Receiver MSB 155 Mbits/s Data Output
138	RxQ13P	0	LVPECL	Receiver 155 Mbits/s Data Output
139	RxQ13N	0	LVPECL	Receiver 155 Mbits/s Data Output
140	RxDGND	I	Supply	Receiver Digital Ground
141	RxQ11P	0	LVPECL	Receiver 155 Mbits/s Data Output
142	RxQ11N	0	LVPECL	Receiver 155 Mbits/s Data Output
143	RxQ09P	0	LVPECL	Receiver 155 Mbits/s Data Output
144	RxQ09N	0	LVPECL Receiver 155 Mbits/s Data Output	
145	RxDGND	I	Supply Receiver Digital Ground	
146	RxQ07P	0	LVPECL Receiver 155 Mbits/s Data Output	
147	RxQ07N	0	LVPECL Receiver 155 Mbits/s Data Output	
148	RxQ05P	0	LVPECL	Receiver 155 Mbits/s Data Output
149	RxQ05N	0	LVPECL	Receiver 155 Mbits/s Data Output
150	RxDGND	I	Supply	Receiver Digital Ground
151	RxQ03P	0	LVPECL	Receiver 155 Mbits/s Data Output
152	RxQ03N	0	LVPECL	Receiver 155 Mbits/s Data Output
153	RxQ01P	0	LVPECL	Receiver 155 Mbits/s Data Output
154	RxQ01N	0	LVPECL	Receiver 155 Mbits/s Data Output
155	RxDGND	I	Supply	Receiver Digital Ground
156	NC			No User Connection Permitted
157	NC			No User Connection Permitted
158	NC	—		No User Connection Permitted
159	NC			No User Connection Permitted
160	FGND	I	Supply	Frame Ground <sup>1</sup>

#### Table 1. TA16-Type Transponder Pinout (continued)

1. Frame ground is connected to the housing and is isolated from all circuit grounds (TxDGND, TxAGND, RxDGND, RxAGND).

#### Table 2. TA16-Type Transponder Input Pin Descriptions

Pin Name	Pin Description
TxD[0:15]P TxD[0:15]N	<b>16-bit Differential LVPECL Parallel Input Data Bus.</b> TxD15P/N is the most significant bit of the input word and is the first bit serialized. TxD00P/N is the least significant bit of the input word and is the last bit serialized. TxD[0:15]P/N is sampled on the rising edge of PICLK.
PICLKP PICLKN	<b>Differential LVPECL Parallel Input Clock</b> . A 155 MHz nominally 50% duty cycle input clock to which TxD[0:15]P/N is aligned. The rising edge of PICLK transfers the data on the 16 TxD inputs into the holding register of the parallel-to-serial converter.
TxRefClkP TxRefClkN	<b>Differential LVPECL Low Jitter 155.520 MHz Input Reference Clock.</b> This input is used as the reference for the internal clock frequency synthesizer which generates the 2.5 GHz bit rate clock used to shift data out of the parallel-to-serial converter and also for the byte-rate clock, which transfers the 16-bit parallel input data from the input holding register into the parallel-to-serial shift register. Input is internally terminated and biased. See discussion on interfacing, page 13.
TxDIS	<b>Transmitter Disable Input</b> . A logic HIGH on this input pin shuts off the transmitter's laser so that there is no optical output.
DLOOP	<b>Diagnostic Loopback Enable (LVTTL)</b> . When the DLOOP input is low, the 2.5 Gbits/s serial data stream from the parallel-to-serial converter is looped back internally to the serial-to-parallel converter along with an internally generated bit synchronous serial clock. The received serial data path from the optical receiver is disabled.
LLOOP	<b>Line Loopback Enable (LVTTL)</b> . When LLOOP is low, the 2.5 Gbits/s serial data and recovered clock from the optical receiver are looped directly back to the optical transmitter. The multiplexed serial data from the parallel-to-serial converter is ignored.
PHINIT	<b>Phase Initialization (LVPECL)</b> . A rising edge on this input will realign the internal timing associated with clocking data into and out of the internal FIFO. For a detailed explanation, see the section on Transmitter Data Input Timing on page 17.
FRAMEN	<b>Frame Enable Input (LVTTL)</b> . Enables the frame detection circuitry to detect A1 A2 byte alignment and to lock to a word boundary. The TA16 transponder will continually perform frame acquisition as long as FRAMEN is held high. When this input is low, the frame-detection circuitry is disabled. Frame-detection process is initiated by rising edge of out-of-frame pulse.
OOF	<b>Out of Frame (LVTTL)</b> . This input indicator is typically generated by external SONET/SDH overhead monitor circuitry in response to a state in which the frame boundaries of the received SONET/SDH signal are unknown, i.e., after system reset or loss of synchronization. The rising edge of the OOF input initiates the frame detection function if FRAMEN is high. The FP output goes high when the frame boundary is detected in the incoming serial data stream from the optical receiver.
RESET	<b>Master Reset (LVTTL)</b> . Reset input for the multiplexer/demultiplexer. A low on this input clears all buffers and registers. During reset, POCLK and PCLK do not toggle.

Table 3.	TA16-Type	Transponder	r Output Pir	n Descriptions
14810 01		manopenae		

Pin Name	Pin Description
RxQ[0:15]P RxQ[0:15]N	<b>16-bit Differential LVPECL Parallel Output Data Bus</b> . RxQ[0:15] is the 155 Mbyte/s 16-bit output word. RxQ15P/N is the most significant bit of the received word and is the first bit serialized. RxQ00P/N is the least significant bit of the received word and is the last bit serialized. RxQ[0:15]P/N is updated on the falling edge of POCLk.
POCLKP POCLKN	<b>Differential LVPECL Parallel Output Clock</b> . A 155 MHz nominally 50% duty cycle, byte rate output clock that is aligned to the RxQ[0:15] byte serial output data. RxQ[0:15] and FP are updated on the falling edge of POCLK.
FP	<b>Frame Pulse (LVPECL).</b> Indicates frame boundaries in the received serial data stream. If framing pattern detection is enabled (FRAMEN high and OOF), FP pulses high for one POCLK cycle when a 32-bit sequence matching the framing pattern is detected in the received serial data. FP is updated on the falling edge of POCLK.
SEARCH	A1 A2 Frame Search Output (LVTTL). A high on this output pin indicates that the frame detection circuit is active and is searching for a new A1 A2 byte alignment. This output will be high during the entire A1 A2 frame search. Once a new alignment is found, this signal will remain high for a minimum of one 155 MHz clock period beyond the third A2 byte before it will be set low.
LOS	<b>Loss of Signal (LVTTL)</b> . A low on this output indicates a loss of lock by the clock recovery circuit in the optical receiver.
LSRBIAS	<b>Laser Bias (Analog)</b> . Provides an indication of the health of the laser in the transmitter. This output changes at the rate of 20 mV/mA of bias current. If this output voltage reaches 1.4 V (70 mA of bias), the automatic power control circuit is struggling to maintain output power. This may indicate that the transmitter has reached an end-of-life condition.
LSRALRM	<b>Laser Degrade Alarm (5 V CMOS).</b> A logic low on this output indicates that the transmitter's automatic power control circuits are unable to maintain the nominal output power. This output becomes active when the optical output power degrades 2 dB below the nominal operating power.
LPM	<b>Laser Power Monitor (Analog)</b> . Provides an indication of the output power level from the transmitter laser. This output is set at 500 mV for the nominal transmitter optical output power. If the optical power decreases by 3 dB, this output will drop to approximately 250 mV, and if the output power should increase by 3 dB, this output will increase to 1000 mV.
PClkP/N	<b>Parallel Byte Clock (Differential LVPECL)</b> . A byte-rate reference clock generated by dividing the internal 2.488 GHz serial bit clock by 16. This output is normally used to synchronize byte-wide transfers from upstream logic into the TA16 transponder. See timing discussion for additional details, page 17.
PHERR	<b>Phase Error Signal (Single-Ended LVPECL)</b> . This signal pulses high during each PCLK cycle for which there is potential setup/hold timing violations between the internal byte clock and the PICLK timing domains. PHERR is updated on the falling edge of the PICLK output. For a detailed explanation, see the section Transmitter Data Input Timing on page 17.
IDPMON	<b>Receiver Photodiode Current Monitor (Analog)</b> . This output provides a current output that is a mirror of the photocurrent generated by the optical receiver's photodiode (APD or PIN).
LOCKDET	<b>Lock Detect (LVTTL).</b> This output goes low after the transmit side PLL has locked to the clock signal provided at the TXREFCLK input pins. LOCKDET is an asynchronous output.

# **Functional Description**

#### Receiver

The optical receiver in the TA16-type transponder is optimized for the particular SDH/SONET application segment in which it was designed to operate and will have either an APD or PIN photodetector. The detected serial data output of the optical receiver is connected to a clock and data recovery circuit (CDR), which extracts a 2488.32 MHz clock signal. This recovered serial bit clock signal and a retimed serial data signal are presented to the 16-bit serial-to-parallel converter and to the frame and byte detection logic.

The serial-to-parallel converter consists of three 16-bit registers. The first is a serial-in parallel-out shift register, which performs serial-to-parallel conversion. The second is an internal 16-bit holding register, which transfers data from the serial-to-parallel register on byte boundaries as determined by the frame and byte detection logic. On the falling edge of the free-running POCLK signal, the data in the holding register is transferred to the output holding register where it becomes available as RxQ[0:15].

The frame and byte boundary detection circuitry searches the incoming data for three consecutive A1 bytes followed immediately by an A2 byte. Framing pattern detection is enabled and disabled by the FRAMEN input. The frame detection process is started by a rising edge on OOF while FRAMEN is active (FRAMEN= high). It is disabled when a framing pattern is detected. When framing pattern detection is enabled (FRAMEN = high), the framing pattern is used to locate byte and frame boundaries in the incoming serial data stream from the CDR circuits. During this time, the parallel output data bus (RxQ[0:15]) will not contain valid data. The timing generator circuitry takes the located byte boundary and uses it to block the incoming serial data stream into bytes for output on the parallel output data bus (RxQ[0:15]). The frame boundary is reported on the framing pulse (FP) output when any 32-bit pattern matching the framing pattern is detected in the incoming serial data stream. When framing detection is disabled (FRAMEN = low), the byte boundary is fixed at the location found when frame detection was previously enabled.

# Transmitter

The optical transmitter in the TA16-type transponder is optimized for the particular SDH/SONET segment in which it is designed to operate. The transmitter will have either a Fabry-Perot or a DFB laser as the optical element and can operate at either 1310 nm or 1550 nm. The transmitter is driven by a serial data stream developed in the parallel-to-serial conversion logic and by a 2488.32 MHz serial bit clock signal synthesized from the 155.52 MHz TxREFCLK input.

The parallel-to-serial converter block shown in Figure 1 is comprised of two byte-wide registers. The first register latches the 16 bits of parallel input data (TxD[0:15]) on the rising edge of PICLK. The second register is a 16-bit parallel-load serial-out shift register that is loaded from the input register. An internally generated byte clock, which is phase aligned to the 2488.32 MHz serial transmit clock, activates the data transfer between the input register and the parallel-to-serial register.

The clock divider and phase detect circuitry shown in Figure 1 generates internal reference clocks and timing functions for the transmitter. Therefore, it is important that the TxREFCLK input is generated from a precise and stable source. To prevent internal timing signals from producing jitter in the transmitted serial data that exceeds the SDH/SONET jitter generation requirements of 0.01 UI, it is required that the TxREFCLK input be generated from a crystal oscillator or other source having a frequency accuracy better than 20 ppm. In order to meet the SDH/SONET requirement, the reference clock jitter must be guaranteed to be less than 1 ps rms over the 12 kHz to 20 MHz bandwidth. When used in SONET network applications, this input clock must be derived from a source that is synchronized to the primary reference clock (stratum 1 clock).

The timing generation circuitry provides two separate functions. It develops a byte rate clock that is synchronized to the 2488.32 MHz transmit serial clock, and it provides a mechanism for aligning the phase between the incoming byte clock (PICLK) and the clock which loads the parallel data from the input register into the parallel-to-serial shift register. The PCLK output is a byte rate (155 MHz) version of the serial transmit clock and is intended for use by upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the parallel data coming into the transmitter and the subsequent parallel-to-serial timing functions. The timing generator also provides a feedback reference clock to the phase detector for use by the transmit serial clock synthesizer (for additional discussions, see transmitter input options, page 17.)

#### Functional Description (continued)

#### **Loopback Modes**

The TA16 transponder is capable of operating in either of two loopback modes: diagnostic loopback or line loopback.

#### Line Loopback

When LLOOP is pulled low, the received serial data stream and recovered 2488.32 MHz serial clock from the optical receiver are connected directly to the serial data and clock inputs of the optical transmitter. This establishes a receive-to-transmit loopback at the serial line rate.

#### **Diagnostic Loopback**

When DLOOP is pulled low, a loopback path is established from the transmitter to the receiver. In this mode, the serial data from the parallel-to-serial converter and the transmit serial clock are looped back to the serialto-parallel converter and the frame and byte detect circuitry, respectively.

#### **Transponder Interfacing**

The TxD[0:15]P/N and PICLKP/N inputs and the RxQ[0:15]P/N, POCLKP/N, and PCLKP/N outputs are high-speed (155 Mbits/s), LVPECL differential data and clock signals. To maintain optimum signal fidelity, these inputs and outputs must be connected to their terminating devices via 50  $\Omega$  controlled-impedance transmission lines. The transmitter inputs (TxD[0:15]P/N, TxREFCLKP/N, and PICLKP/N) must be terminated as close as possible to theTA16 transponder connector with a Thevenin equivalent impedance equal to 50 <sup>3</sup>/<sub>4</sub> terminated to Vcc – 2V. The receiver outputs (RxQ[0:15]P/N, POCLKP/N, and PCLKP/N) must be terminated as close as possible to the device (IC) that these signals interface to with a Thevenin equivalent impedance impedance equal to 50  $\Omega$  terminated to Vcc – 2 V.

Figure 3, below, shows one example of the proper terminations. Other methods may be used, provided they meet the requirements stated above.

**TxREFCLKP/N.** The reference clock input is different than the TxD and PICLK inputs because it is internally terminated, ac-coupled, and self-biased. Therefore, it must be treated somewhat differently than the TxD and PICLK inputs. Figure 14 shows the proper method for connecting the TxREFCLK input.

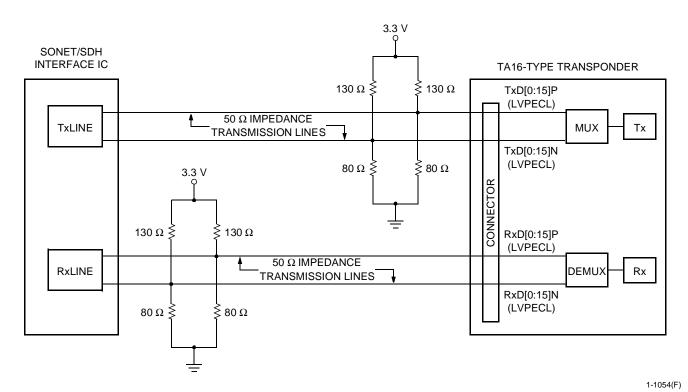


Figure 3. Transponder Interfacing

# **Optical Characteristics**

Minimum and maximum values specified over operating case temperature range at 50% duty cycle data signal. Typical values are measured at room temperature unless otherwise noted.

Table 4. OC48/STM-16 Transmitter Optical Characteristics	(Tc = 0 °C to 65 °C)

Parameter	Symbol	Min	Тур	Max	Unit
Average Output Power: <sup>1</sup>					
Intraoffice (F-P laser)	Po	-10	-5	-3	dBm
Short Haul (DFB laser)	Po	-5	-2	0	dBm
Long Haul:					
1.3 μm DFB Laser	Po	-2	0	2	dBm
1.55 μm DFB Laser	Po	-2	0	3	dBm
Operating Wavelength:					
Intraoffice (F-P laser)	λ	1270		1360	nm
Short Haul (DFB laser)	λ	1270	—	1360	nm
Long Haul (1.3 µm DFB laser)	λ	1280	—	1335	nm
Long Haul (1.55 µm DFB laser)	λ	1500		1580	nm
Spectral Width:					
Intraoffice (F-P laser)	$\Delta\lambda$ rms			4	nm
Short Haul and Long Haul (DFB laser) <sup>2</sup>	Δλ20			1	nm
Side-mode Suppression Ratio (DFB laser) $^3$	SSR	30		_	dB
Extinction Ratio <sup>4</sup>	ľe	8.2		—	dB
Optical Rise and Fall Times	tR, tF	—	—	200	ps
Eye Mask of Optical Output <sup>5, 6</sup>	Compliant with GR-253 and ITU-T G.957				
Jitter Generation	Co	mpliant with	GR-253 ar	nd ITU-T G.	958

1. Output power definitions and measurements per ITU-T Recommendation G.957.

2. Full spectral width measured 20 dB down from the central wavelength peak under fully modulated conditions.

3. Ratio of the average output power in the dominant longitudinal mode to the power in the most significant side mode under fully modulated conditions.

4. Ratio of logic 1 output power to logic 0 output power under fully modulated conditions.

5. GR-253-CORE, Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria.

6. ITU-T Recommendation G.957, Optical Interfaces for Equipment and Systems Relating to the Synchronous Digital Hierarchy.

#### Table 5. OC48/STM-16 Receiver Optical Characteristics (Tc = 0 °C to 65 °C)

Parameter	Symbol	Min	Тур	Max	Unit
Average Receiver Sensitivity <sup>1</sup> : PIN Receiver (intraoffice, short haul) APD Receiver (long haul)	Prmin Prmin	-20 -29	-25 -34	_	dBm dBm
Maximum Optical Power: PIN Receiver APD Receiver (long reach)	Prmax RMAX	1 6		_	dBm dBm
Link Status Switching Threshold Decreasing Light Input: APD PIN	LSTD LSTD		TBD TBD		dBm dBm
Link Status Response Time	—	3	—	100	μs
Optical Path Penalty (1310 nm/1550 nm)	_	_		1/2	dB
Receiver Reflectance	—	—	—	-27	dB
Jitter Tolerance and JitterTransfer	Co	ompliant with	n GR-253 ar	nd ITU-T G.9	58

1. At 1310 nm, 1 x  $10^{-10}$  BER,  $2^{23}$  – 1 pseudorandom data input.

# **Electrical Characteristics**

Table 0. Indistingues Electrical VO characteristics ( $10 = 0$ C (0.05 C, $000 = 3.3$ V $\pm 3.0$	Table 6. Transmitter Electrical I/O Characteristics (	(Tc = 0 °C to 65 °C, Vcc = 3.3 V ± 5%)
---	---	--

Parameter	Symbol	Logic	Min	Тур	Max	Unit
Parallel Input Clock	PICLKP/N	Diff. LVPECL	153.90	155.52	157.00	MHz
Parallel Clock in Duty Cycle	—	_	40		60	%
Reference Clock Frequency Tolerance	TxRefClkP/N	Diff. LVPECL	-20	_	20	ppm
Reference Clock Jitter (in 12 KHz to 20 MHz band)	_	_	—	_	1	ps rms
Reference Clock Input Duty Cycle	_		45	_	55	%
Reference Clock Rise and Fall Times <sup>1</sup>	_		—	_	1.5	ns
Reference Clock Signal Levels: <sup>2</sup> Diff. InputVoltage Swing Single-ended Input Voltage Swing Differential Input Resistance	ΔVindiff ΔVinsingle Rdiff	Diff. LVPECL	300 150 80	  100	1200 600 120	mV mV Ω
Input Data Signal Levels: Input High, Vıн Input Low, Vı∟ Input Voltage Swing, ∆Vıℕ	TxD[0:15]P/N	Diff. LVPECL	Vcc – 1.2 Vcc – 2.0 300		Vcc – 0.3 Vcc – 1.5 —	V V mV
Transmitter Disable Input <sup>3</sup>	TxDis	TTL (5 V)	2.0		5.5	V
Transmitter Enable Input <sup>3</sup>	TxEN	TTL (5 V)	0		0.8	V
Laser Bias Voltage Output <sup>4</sup>	LSRBIAS	Analog	0	200	1600	mV
Laser Power Monitor Output <sup>5</sup>	LPM	Analog	35	500	1000	mV
Laser Degrade Alarm: Output High, Voн Output Low, VoL	LSRALM	5 V CMOS	4.5 0	_	5.2 0.4	V V
Phase Initialization: Input High, Vıн Input Low, Vı∟	PHINIT	Single- Ended LVPECL	Vcc – 1.0 Vcc – 2.3	_	Vcc – 0.57 Vcc – 1.44	V V
Phase Error <sup>6</sup> : Output High, Voн Output Low, VoL	PHERR	Single- Ended LVPECL	Vcc – 1.2 Vcc – 2.2	_	Vcc – 0.65 Vcc – 1.5	V V
Line Loopback Enable: Active-Low: Input High, V⊮ Input Low, V⊫	LLOOP	LVTTL	2.0 0		Vcc + 1.0 0.8	V V

1. 20% to 80%.

2. Internally biased and ac-coupled. See Figure 13.

3. The transmitter is normally enabled and only requires an external voltage to disable.

4. Output conversion factor is 20 mV/mA of laser bias current.

5. Set at 500 mV at nominal output power; will track Po linearly (-3 dB = 250 mV, +3 dB = 1000 mV).

6. Terminated into 220  $\Omega$  to GND with 100  $\Omega$  line-to-line.

# Electrical Characteristics (continued)

#### Table 6. Transmitter Electrical I/O Characteristics (Tc = 0 °C to 65 °C, Vcc = 3.3 V ± 5%) (continued)

Diagnostic Loopback Enable:	DLOOP	LVTTL				
Active-Low:						
Input High, Vін			2.0	—	Vcc + 1.0	V
Input Low, Vı∟			0		0.8	V
Parallel Output Clock: <sup>6</sup>	PCLKP/N	Diff.				
Output High, Voн		LVPECL	Vcc – 1.15		Vcc – 0.6	V
Output Low, Vo∟			Vcc – 1.95		Vcc – 1.45	V
S-E Output Voltage Swing, ΔVSINGLE			400		950	mV
Diff. Voltage Swing, $\Delta V$ DIFF			800		1900	mV

1. 20% to 80%.

2. Internally biased and ac-coupled. See Figure 13.

3. The transmitter is normally enabled and only requires an external voltage to disable.

4. Output conversion factor is 20 mV/mA of laser bias current.

5. Set at 500 mV at nominal output power; will track Po linearly (-3 dB = 250 mV, +3 dB = 1000 mV).

6. Terminated into 220  $\Omega$  to GND with 100  $\Omega$  line-to-line.

#### Table 7. Receiver Electrical I/O Characteristics (Tc = $0 \degree C$ to $65 \degree C$ , Vcc = $3.3 \lor \pm 5\%$ )

Parameter	Symbol	Logic	Min	Тур	Max	Unit
Parallel Output Clock:	POCLKP/N					
Output High, Voн		Diff.	Vcc – 1.3	—	Vcc – 0.7	V
Output Low, Vo∟		LVPECL	Vcc - 2.00	—	Vcc – 1.4	V
POCLk Duty Cycle	—	-	40	—	60	%
Output Data Signal Levels <sup>1</sup> :	RxQ[0:15]P/N	Diff.				
Output High, Voн		LVPECL	2.275	—	2.420	V
Output Low, Vo∟			1.490	—	1.680	V
RxQ[0:15] Rise/Fall Time <sup>2</sup>	—	_	—	—	1.0	ns
Frame Pulse:	FP	LVPECL				
Output High, Voн			Vcc – 1.3	—	Vcc – 0.7	V
Output Low, VoL			Vcc - 2.00	—	Vcc – 1.4	V
Loss-of-Signal Output:	LOS	LVTTL				
Output High, Voн			2.4	—	Vcc	V
Output Low, Vo∟			0	—	0.4	V
Out-of-Frame Input:	OOF	LVTTL				
Input High, Vin			2.00	—	Vcc + 1.0	V
Input Low, Vı∟			0.0	—	0.8	V
Frame Enable Input	FRAMEN	LVTTL				
			2.00	—	Vcc + 1.0	V
			0.0	—	0.8	V

1. Terminated into 330  $\Omega$  to ground.

2. 20% to 80%, 330  $\Omega$  to ground.

#### Table 8. Power Supply Characteristics (Tc = 0 °C to 65 °C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
dc Power Supply Current Drain <sup>1</sup>	Icc	_	1800	2300	mA
Power Dissipation	PDISS		6		W

1. Does not include output termination resistor current drain.

# **Timing Characteristics**

#### **Transmitter Data Input Timing**

The TA16 transponder utilizes a unique FIFO to decouple the internal and external (PICLK) clocks. The FIFO can be initialized, which allows the system designer to have an infinite PCLK-to-PICLK delay through this interfacing logic (ASIC or commercial chip set). The configuration of the FIFO is dependent upon the I/O pins, which comprise the synch timing loop. This loop is formed from PHERR to PHINIT and PCLK to PICLK.

The FIFO can be thought of as a memory stack that can be initialized by PHINT or LOCKDET. The PHERR signal is a pointer that goes high when a potential timing mismatch is detected between PICLK and the internally generated PCLK clock. When PHERR is fed back to PHINIT, it initializes the FIFO so that it does not overflow or underflow.

The internally generated divide-by-16 clock is used to clock out data from the FIFO. PHINIT and LOCKDET signals will center the FIFO after the third PICLK pulse. This is done to ensure that PICLK is stable. This scheme allows the user to have an infinite PCLK to PICLK delay through the ASIC. Once the FIFO is centered, the PCLK and PICLK can have a maximum drift of  $\pm 5$  ns.

During normal operation, the incoming data is passed from the PICLK input timing domain to the internally generated divide-by-16 PCLK timing domain. Although the frequency of PICLK and PCLK are the same, their phase relationship is arbitrary. To prevent errors caused by short setup or hold times between the two domains, the timing generator circuitry monitors the phase relationship between PICLK and PCLK.

When an FIFO timing violation is detected, the phase error (PHERR) signal pulses high. If the condition persists, PHERR will remain high. When PHERR is fed back into the PHINIT input (by shorting them on the printed-circuit board [PCB]), PHINIT will initialize the FIFO if PHINIT is held high for at least two byte clocks. The initialization of the FIFO prevents PCLK and PICLK from concurrently trying to read and write over the same FIFO bank.

During realignment, one to three bytes (16-bits wide) will be lost. Alternatively, the customer logic can take in the PHERR signal, process it, and send an output to the PHINIT input in such a way that only idle bytes are lost during the initialization of the FIFO. Once the FIFO has been initialized, PHERR will go inactive.

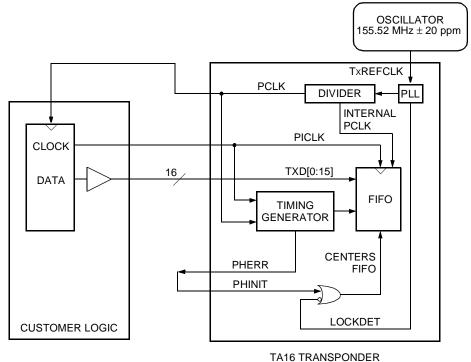
#### **Input Timing Mode 1**

In the configuration shown in Figure 4, PHERR to PHINIT has a zero delay (shorted on the PCB) and the PCLK is used to clock 16-bit-wide data out of the customer ASIC. The FIFO in the multiplexer is 16-bits wide and six registers deep.

The PCLK and PICLK signals respectively control the READ and WRITE counters for the FIFO. The data bank from the FIFO has to be read by the internally

generated clock (PCLK) only once after it has been written by the PICLK input.

Since the delay in the customer ASIC is unknown, the two clocks (PCLK and PICLK) might drift in respect to each other and try to perform the read and writer operation on the same bank in the FIFO at the same time. However, before such a clock mismatch can occur, PHERR goes high and, if externally connected to PHINIT, will initialize the FIFO provided PHINIT remains high for at least two byte clocks. One to three 16-bit words of data will be lost during the initialization of the FIFO.



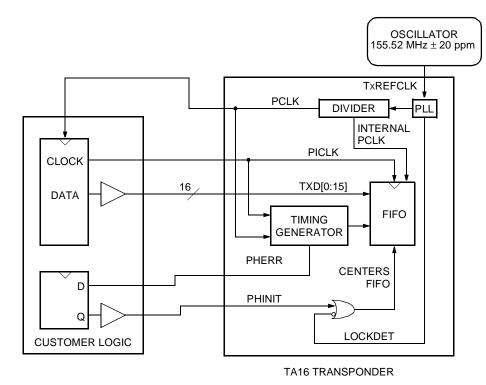
1-1020(F)

Figure 4. Block Diagram Timing Mode 1

#### Input Timing Mode 2

To avoid the loss of data, idle or dummy bytes should be sent on the TxD[0:15] bus whenever PHERR goes high. In the configuration shown in Figure 5, the PHERR signal is used as an input to the customer logic. Upon detecting a high on the PHERR signal, the customer logic should return a high signal, one that remains high for at least two byte-clock cycles, to the PHINIT input of the TA16. Also, when PHERR goes high, the customer logic should start sending idle or dummy bytes to the TA16 on the TxD[0:15] bus. This should continue until PHERR goes low.

The FIFO is initialized two-to-eight byte clocks after PHINIT goes high for two byte clocks. PHERR goes low after the FIFO is initialized. Upon detecting a low on PHERR, the customer logic can start sending real data bytes on TxD[0:15]. The two timing loops (PCLK to PICLK and PHERR to PHINIT) do not have to be of equal length.



1-1021(F)

Figure 5. Block Diagram Timing Mode 2

#### **Forward Clocking**

In some applications, it is necessary to forward-clock the data in a SONET/SDH system. In this application, the reference clock from which the high-speed serial clock is synthesized and the parallel data clock both originate from the same source on the customer application circuit. The timing control logic in theTA16 transponder transmitter automatically generates an internal load signal that has a fixed relationship to the reference clock. The logic takes into account the variation of the reference clock to the internal load signal over temperature and voltage. The connections required to implement this clocking method are shown in Figure 6. The setup and hold times for PICLK to TxD[0:15] must be met by the customer logic.

Possible problems: to meet the jitter generation specifications required by SONET/SDH, the jitter of the reference clock must be minimized. It could be difficult to meet the SONET jitter generation specifications using a reference clock generated from the customer logic.

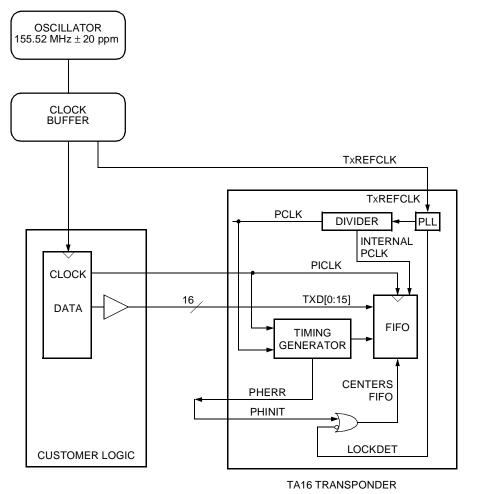


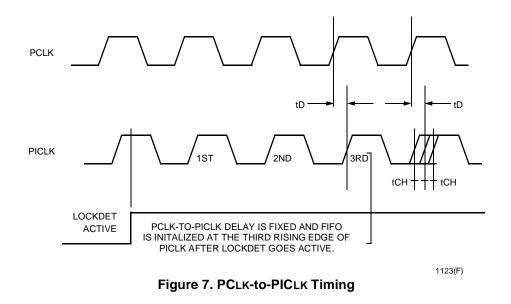
Figure 6. Forward Clocking of the TA16 Transmitter

1-1122(F)

#### PCLK-to-PICLK Timing

After powerup or RESET, the LOCKDET signal will go active, signifying that the PLL has locked to the clock provided on the TXREFCLK input. The FIFO is initialized

on the third PICLK after LOCKDET goes active. The PCLK-to-PICLK delay (tD) can have any value before the FIFO is initialized. The tD is fixed at the third PICLK after LOCKDET goes active. Once the FIFO is initialized, PCLK and PICLK cannot drift more than 5.2 ns; tCH cannot be more than 5.2 ns.



#### PHERR/PHINIT

Case 1— PHERR and PHINIT are shorted on the printed-circuit board:

PHINIT would go high whenever there is a potential timing mismatch between PCLK and PICLK. PHINIT would remain high as long as the timing mismatch between PCLK and PICLK. If PHINIT is high for more than two byte clocks, the FIFO will be initialized. PHINIT will initialize the FIFO two-to-eight byte clocks after it is high for at least two byte clocks, PHERR (and thus PHINIT) goes active once the FIFI is initialized.

Case 2—PHERR signal is input to the customer logic and the customer logic outputs a signal to PHINIT:

Another possible configuration is where the PHERR signal is input into the customer logic and the customer logic sends an output to the PHINIT input. However, the customer logic must ensure that, upon detecting a high on PHERR, the PHINIT signal remains high for more than two byte clocks. If PHINIT is high for less than two byte clocks, the FIFO is not guaranteed to be initialized. Also, the customer logic must ensure that PHINIT goes low after the FIFO is initialized (PHERR goes low).

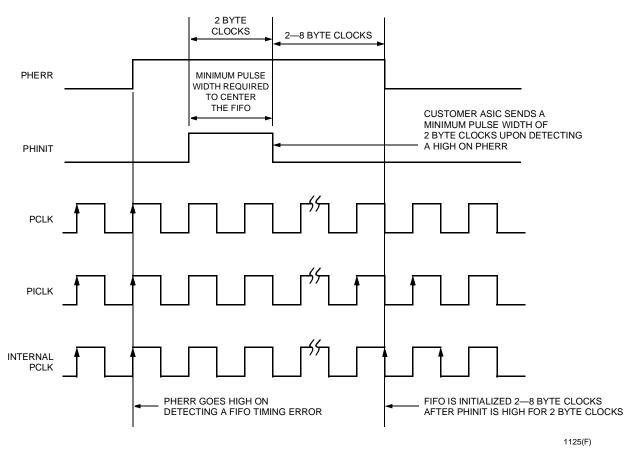


Figure 8. PHERR/PHINIT Timing

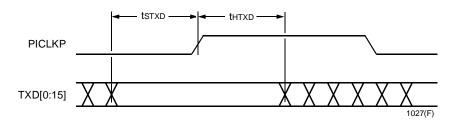


Figure 9. ac Input Timing

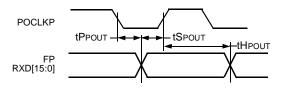
#### Table 9. Transmitter ac Timing Characteristics

Symbol	Description	Min	Мах	Unit
tSTxD	TxD[0:15] Setup Time w. r. t. PICLK	1.5	_	ns
tHTxD	TxD[0:15] Hold Time w. r. t. PICLK	0.5	_	ns
	PCLKP/N Duty Cycle	40	60	%
	PICLKP/N Duty Cycle	40	60	%
tD	PCLK -to-PICLK Drift After FIFO is Centered	—	5.2	ns

#### Table 10. Receiver ac Timing Characteristics

Symbol	Description	Min	Max	Unit
	POCLK Duty Cycle	45	55	%
—	RxD[15:0] Rise and Fall Time <sup>1</sup>	—	1.0	ns
t <b>P</b> POUT	POCLK Low to RxD[15:0] Valid prop. delay	-1	1	ns
tSPOUT	RxD[15:0] and FP Setup Time w.r.t. POCLK	2	_	ns
tHpout	RxD[15:0] and FP Hold Time w. r. t. POCLK	2	_	ns

1. 20% to 80%; 330  $\Omega$  to GND



1-1022(F)

Figure 10. Receiver Output Timing Diagram

#### **Receiver Framing**

Figure 11 shows a typical reframe sequence in which a byte realignment is made. The frame and byte boundary detection is enabled by the rising edge of OOF. Both the frame and byte boundaries are recognized upon receipt of the first A2 byte following three consecutive A1 bytes. The third A2 byte is the first data byte to be reported with the correct byte alignment on the outgoing data bus (RxD[15:0]). Concurrently, the frame pulse (FP) is set high for one POCLK cycle.

The frame and byte boundary detection block is activated by the rising edge of OOF and stays active until the first FP pulse.

Figure 12 shows the frame and byte boundary detection activation by a rising edge of OOF and deactivation by the first FP pulse.

Figure 13 shows the frame and byte boundary detection by the activation of a rising edge of OOF and deactivation by the FRAMEN input.

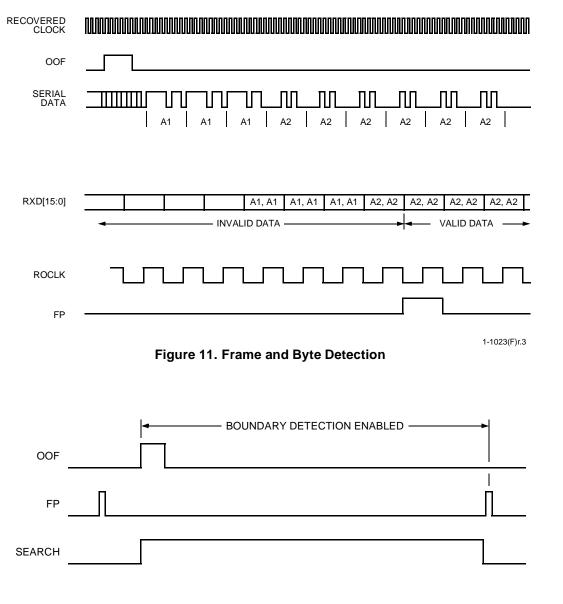


Figure 12. OOF Timing (FRAMEN = High)

1-1024(F)

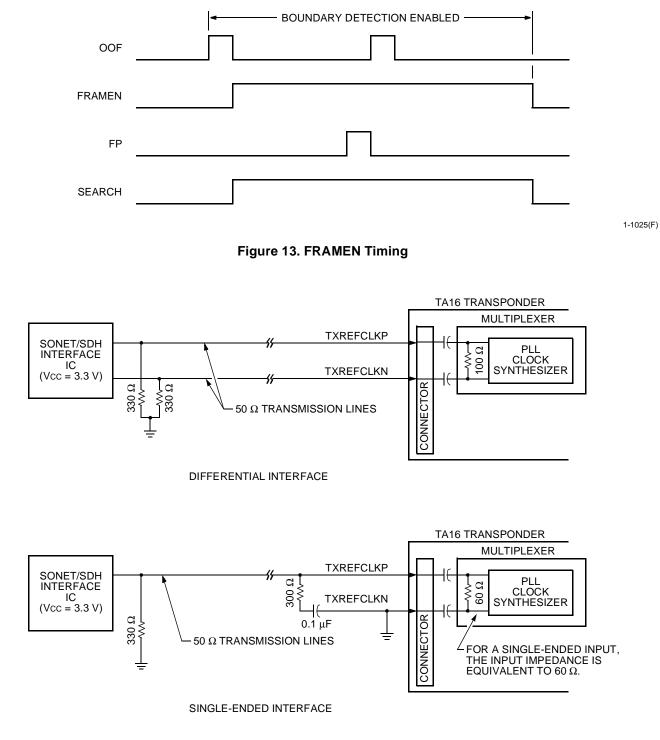


Figure 14. Interfacing to the TxRefClk Input

# **Qualification and Reliability**

To help ensure high product reliability and customer satisfaction, Agere is committed to an intensive quality program that starts in the design phase and proceeds through the manufacturing process. Optoelectronics modules are qualified to Agere internal standards using MIL-STD-883 test methods and procedures and using sampling techniques consistent with *Telcordia Technologies* \* requirements. This qualification program fully meets the intent of *Telcordia Technologies* reliability practices TR-NWT-000468 andTA-TSY-000983. In addition, the Agere Optoelectronics design, development, and manufacturing facility has been certified to be in full compliance with the latest *ISO*<sup>†</sup>-9001 Quality System Standards.

\* Telcordia Technologies is a trademark of Telcordia Technologies, Inc.

† ISO is a registered trademark of the International Organization for Standardization.

# Laser Safety Information

#### **Class I Laser Product**

All versions of theTA16-type transponders are classified as Class I laser products per FDA/CDRH, 21 CFR 1040 Laser Safety requirements. The transponders have been registered/certified with the FDA under Accession Number 8720009. All versions are classified as Class I laser products per  $IEC^{\ddagger}$  60825-1:1993.

# CAUTION: Use of controls, adjustments, and procedures other than those specified herein may result in hazardous laser radiation exposure.

This product complies with 21 CFR 1040.10 and 1040.11.

8.8  $\mu\text{m}/125~\mu\text{m}$  single-mode pigtail with 900  $\mu\text{m}$  tight buffer jacket and connector.

Wavelength = 1.3  $\mu$ m, 1.5  $\mu$ m.

Maximum power = 1.6 mW.

Product is not shipped with power supply.

Because of size constraints, laser safety labeling is not affixed to the module but is attached to the outside of the shipping carton.

NOTICE

Unterminated optical connectors can emit laser radiation.

Do not view with optical instruments.

#### **Electromagnetic Emissions and Immunity**

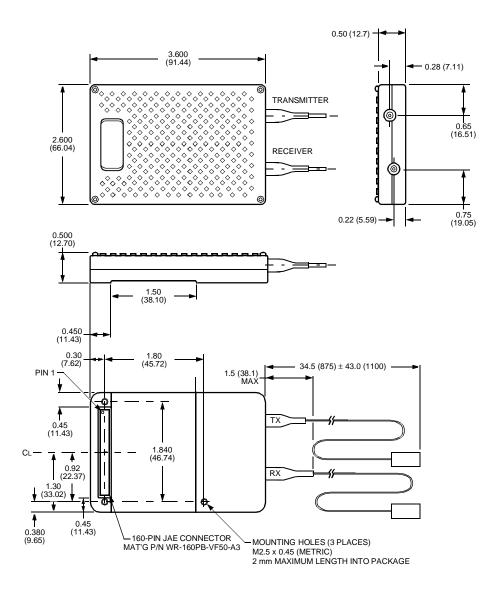
The TA16 transponder will be tested against CENELEC EN50 081 part 1 and part 2, FCC 15, Class B limits for emissions.

The TA16 transponder will be tested against CENELEC EN50 082 part 1 immunity requirements.

*‡ IEC* is a registered trademark of The International Electrotechnical Commission.

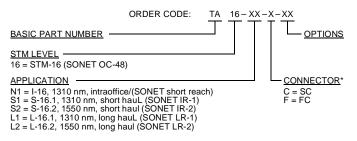
# **Outline Diagram**

Dimensions are in inches and (millimeters).



1-1012(F).d

# **Ordering Information**



\* Other connectors may be made available.

#### Table 11. Ordering Information

Code	Application	Connector	Comcode
TA16N1CAA	1310 nm, Intraoffice	SC	108440066
TA16N1FAA	1310 nm, Intraoffice	FC/PC	108440074
TA16S1CAA	1310 nm, Short Haul	SC	108432907
TA16S1FAA	1310 nm, Short Haul	FC/PC	108432915
TA16S2CAA	1550 nm, Short Haul	SC	108432923
TA16S2FAA	1550 nm, Short Haul	FC/PC	108432931
TA16L1CAA	1310 nm, Long Haul	SC	108432865
TA16L1FAA	1310 nm, Long Haul	FC/PC	108432873
TA16L2CAA	1550 nm, Long Haul	SC	108432881
TA16L2FAA	1550 nm, Long Haul	FC/PC	108432899

# **Related Product Information**

#### **Table 12. Related Product Information**

Description	Document Number
Using the Lucent Technologies Transponder Test Board Application Note	AP00-017OPTO

For additional information, contact your Agere Systems Account Manager or the following: INTERNET: http://www.agere.com	
	docmaster@agere.com
N. AMERICA:	Agere Systems Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18109-3286
	1-800-372-2447, FAX 610-712-4106 (In CANADA: 1-800-553-2448, FAX 610-712-4106)
ASIA:	Agere Systems Hong Kong Ltd., Suites 3201 & 3210-12, 32/F, Tower 2, The Gateway, Harbour City, Kowloon
	Tel. (852) 3129-2000, FAX (852) 3129-2020
	CHINA: (86) 21-5047-1212 (Shanghai), (86) 10-6522-5566 (Beijing), (86) 755-695-7224 (Shenzhen)
	JAPAN: (81) 3-5421-1600 (Tokyo), KORÈA: (82) 2-767-1850 (Seoul), SINGAPORE: (65) 778-8833, TAIWAN: (886) 2-2725-5858 (Taipei)
EUROPE:	Tel. (44) 7000 624624, FAX (44) 1344 488 045

Agere Systems Inc. reserves the right to make changes to the product(s) or information contained herein without notice. No liability is assumed as a result of their use or application.

Copyright © 2001 Agere Systems Inc. All Rights Reserved Printed in U.S.A.

