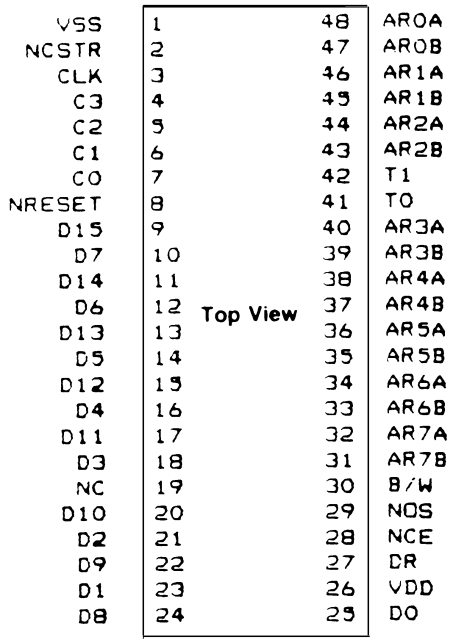
Micro Circuit Engineering

technology applied

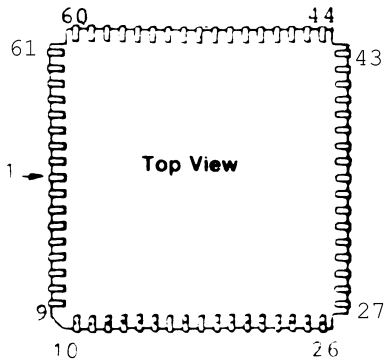
EIGHT CHANNEL ARINC DECODER

- 8/16 bit parallel interface
- 3 channels programmable to HIGH/LOW speed data
- Single 5V supply with low power consumption < 50mW
- Full MIL operating range
- Programmable test I/P to all channels
- Built in parity and word length error detection

PIN CONFIGURATION



48 PIN DIL PACKAGE



1	VSS(0V)	24	D11	47	AR7B
2	NCSTR	25	NC	48	AR7A
3	CLK	26	NC	49	AR6B
4	C3	27	NC	50	AR6A
5	C2	28	NC	51	AR5B
6	NC	29	NC	52	AR5A
7	NC	30	D3	53	AR4B
8	NC	31	D10	54	AR4A
9	NC	32	D2	55	AR3B
10	NC	33	D9	56	AR3A
11	NC	34	D1	57	T0
12	NC	35	D8	58	T1
13	C1	36	DO	59	NC
14	C0	37	VDD(+5V)	60	NC
15	NRESET	38	DR	61	NC
16	D15	39	NCE	62	NC
17	D7	40	NOS	63	AR2B
18	D14	41	NC	64	AR2A
19	D6	42	NC	65	AR1B
20	D13	43	NC	66	AR1A
21	D5	44	NC	67	AR0B
22	D12	45	NC	68	AR0A
23	D4	46	B/W		

68 PIN J LEAD
SURFACE MOUNT PACKAGE

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	- 65ºC to +150ºC
Temperature (Ambient) under Bias	- 55ºC to +125ºC
Supply Voltage VDD	-0.3V to + 7V
DC Input Voltage	-0.3 to VDD +0.3V
Output Current (Single O/P)	10mA
Output Current (Total O/P)	20mA

ELECTRICAL CHARACTERISTICS over operating range

PARAMETER	DESCRIPTION	TEST CONDITIONS		MIN	TYP	MAX	UNITS
IOH	Output High Current	VOH=2.8V	VDD= 4.5V	1.0			mA
IOL	Output Low Current	VOL=0.4V		3.2			mA
VIH	Input High Voltage			2.4		VCC	Volts
VIL	Input Low Voltage			-0.3		0.8	Volts
IIL	Input Load Current	VSS				40	uA
IOZ	Output Leakage Current	0.4V<VO<VCC Output Disabled		-40		40	uA
CI	Input Capacitance	Test Frequency = 1.0 MHZ			2	2.6	pF
CI/O	I/O Capacitance				7	9	pF
ICC	Supply Current	VCC = MAX. All inputs HIGH, All inputs open.				10	mA

ARINC 429 SERIAL INPUT INTERFACE

Interfaces are provided for 8 independent Arinc 429 serial input channels with sufficient digital storage to guarantee no data is lost provided all 8 channels can be accessed within 230μS.

Channels 0,1 & 2 can be programmed for either high or low speed operation. Channels 3 to 7 are configured for interfacing to low speed Arinc buses only.

Digital Filtering is incorporated on each decoder input port to prevent word corruption due to noise spikes. (The duration of reject noise spikes is a function of the basic clock period).

Arinc have suggested that the number of labels available to the user can be increased by either using SDI bits 9 and 10 as extra label bits or by using port identification. Both of these techniques have been accommodated in the design.

DATA DETECTION AND WORD TESTS

Each channel is provided with a 32 bit shift register to hold one complete word. The three channels which are selectable for either high or low speed operation are additionally provided with a 32 bit buffer register.

Each channel contains hardware to test the following parameters:-

(1) Word length of 32 bits.

(2) Parity:- odd on good words.

(3) Gap:- the presence of a 33rd bit is checked for and the output processing is achieved during the remaining gap for a valid word.

(4) Interconnection fault (both I/P's high).

Prioritised error information for each channel is latched into a 3 bit register with the format indicated in Table 1 and made available at the user output port.

Channel servicing is carried out on a rotating priority basis, where the last channel serviced is given the lowest priority, in order to allow full access for each channel.

A facility is provided on the decoder chip to enable individual channels to be tested, which consists of a multi-plexer on the input to each channel to allow test messages (generated external to the chip) to be injected.

TABLE 1

Prioritorised coded error data.

Bit position relative to first output word see fig.2.

15	14	13		
1	1	1	)	Unused
1	1	0	)	
1	0	1		Interconnection fault (highest priority)
1	0	0		Channel overrun (causes corruption of following word in that channel.
0	1	1		Word length error (number of bits not equal to 32).
0	1	0		Parity error (word received with even parity).
0	0	1		Service overrun (not all words or bytes accessed) - lowest priority.
0	0	0		Good word.

USER INTERFACE

Arinc 429 data is read from the decoder chip via an 8 or 16 bit parallel data bus.

Fig 2 illustrates the formatting of the output data relative to the generalised Arinc 429 word format.

Control of the chip is achieved via a four bit control port which provides the user with the facilities outlined in Table 2. The control word is strobed into the chip using the leading edge of the NOT CSTR input providing the required set up and hold times are met.
N.B. NOT CSTR must be high before NOT RESET is removed.

DATA READY signifies to the user that a word is available and can be accessed by pulling NOT CHIP ENABLE low and strobing the NOT OUTPUT SELECT line as illustrated in fig .3.

NOT RESET provides the user with a simple means of asynchronously inhibiting the chip. Activating NOT RESET disables the output buffers and clears DATA READY asynchronously. The internal counters are cleared by holding NOT RESET low for 2 clock periods. Default options are selected which can be overwritten using the control input port. The default options are shown below and are selected by pulsing RESET low or by selecting software reset (see table 2).

- Channel sequencer set to channel 0 for highest priority.
- All channels are set for low speed operation.
- All channels are set for normal reception with no end around test mode.

NOT CSTR and NOT OS must be high during reset but may go low immediately NOT RESET is removed.

NOT CSTR, LOW min = HIGH min = 1.5T for correct operation CO-3, SET UP TIME = 0, HOLD TIME = 2T min after NOT CSTR goes low.

NOT CSTR is synchronised by ∅IN to give a 0.5T interval strobe pulse. This pulse disables the state decoder O/P's allowing 0.5T settling time for the new state to be established before re-enabling the O/P's. This ensures that data I/P's cannot be internally shorted together when changing from test on one channel to another.

*T = $^{1}/_{f}$ = 1 clock cycle time of ∅IN.

A single phase clock must be provided by the user with a frequency in the range of 1.25 - 2.0 MH_Z. The chip will accommodate all the selectable channel speed options available with the clock at any frequency between these limits.

A 3 bit binary code is allocated in the first word of output data to signify which channel has received a message and is being accessed.

The positioning of the code is shown in fig 2 and has the form shown below:-

1st output word bit number

12	11	10	
0	0	0	Channel 0
0	0	1	Channel 1
0	1	0	Channel 2
0	1	1	Channel 3
1	0	0	Channel 4
1	0	1	Channel 5
1	1	0	Channel 6
1	1	1	Channel 7

FIG. 1

TABLE 2 CONTROL WORD CODES

Control bit number

C3	C2	C1	C0	
0	0	0	0	Channels 0 to 7 low speed
0	0	0	1	Channel 0 high speed, channels 1 to 7 low speed
0	0	1	0	Channel 1 high speed, channels 0 and 2 to 7 low speed
0	0	1	1	Channels 0 and 1 high speed, channels 2 to 7 low speed
0	1	0	0 (	Channels 0,1 & 2 high speed (Channels 3 to 7 low speed
0	1	0	1 (	Unused
0	1	1	0 (	
0	1	1	1	Software reset
1	0	0	0	Test Channel 0
1	0	0	1	Test Channel 1
1	0	1	0	Test Channel 2
1	0	1	1	Test Channel 3
1	1	0	0	Test Channel 4
1	1	0	1	Test Channel 5
1	1	1	0	Test Channel 6
1	1	1	1	Test Channel 7

Notes

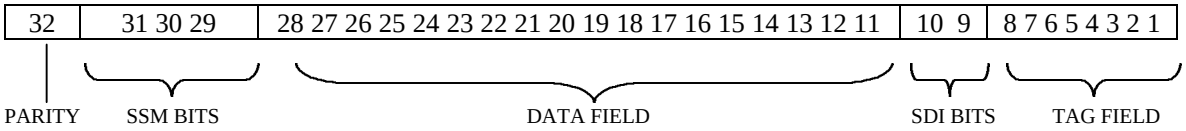
(1) Software reset causes the same action as pulling the RESET line low but once latched into the control register the chip is held in a quiescent mode. Exit from this mode is achieved by latching in the required channel speed option.

(2) Exit from the test mode requires restarting the required speed options (i.e. codes 0 to 4) or loading an unused control mode.

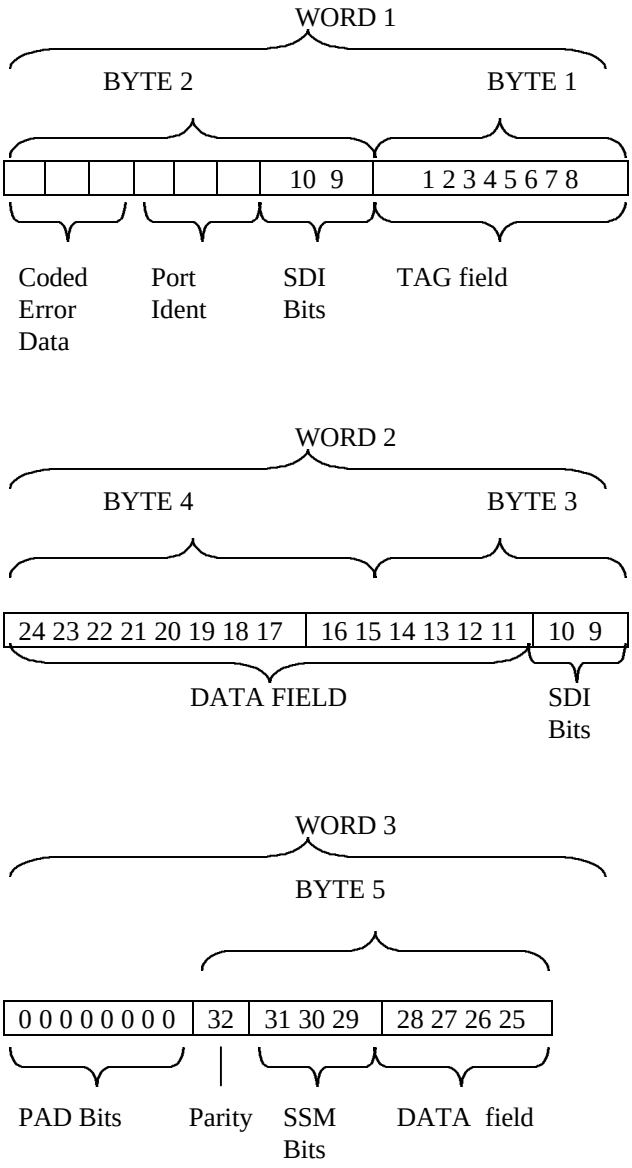
(3) The action of testing a channel does not alter the speed at which is set, also changing between test (i.e. test 1 to test 2) has no effect on channel speed settings.

FIG. 2 MULTICHANNEL ARINC 429 RECEIVER DATA OUTPUT FORMAT

Generalised Arinc 429 word format for BNR data:-



Byte and word output formats:-

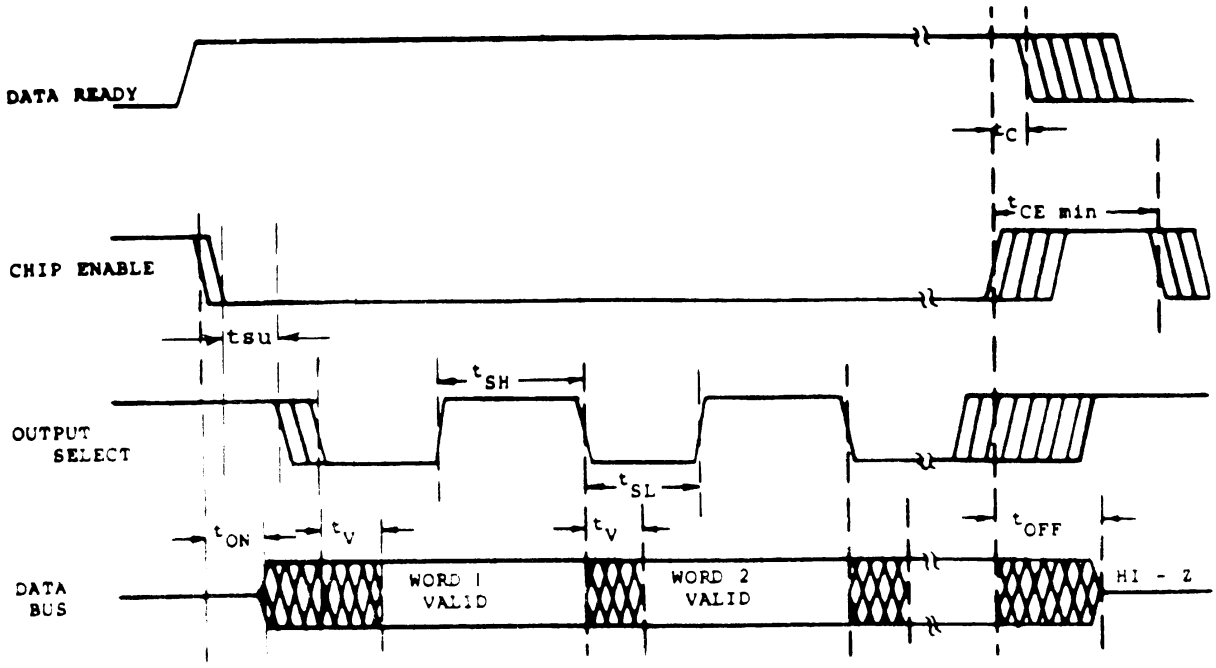


Notes (1) For formats other than BNR see ARINC specification

(2) For byte output formats only 5 bytes are available but for word formats a 6th byte of all zero bits is added to complete the 3rd word.

(3) The coded error data relates to the channel indicated by the port identifier field.

FIG. 3 MULTICHANNEL ARINC 429 RECEIVER OUTPUT TIMING



T	Clock Period (500 - 800nS).	Min	Max
t_{ON}	NOT CHIP ENABLE low to output active time.	10nS	250nS
tv	NOT OUTPUT SELECT low to word valid time.		300nS
$t_{SH\ (MIN)}$	minimum NOT OUTPUT SELECT high time.		400nS
$t_{SL\ (MIN)}$	minimum NOT OUTPUT SELECT low time.		400nS
tc	NOT CHIP ENABLE high to DATA READY low time.	100nS	2T + 500nS
t_{OFF}	NOT CHIP ENABLE high to data bus high impedance time.	20nS	100nS
$t_{CE\ (MIN)}$	minimum time NOT CHIP ENABLE high/low.	2.5T	
t_{CEDRH}	minimum time to select next word (CHIP ENABLE high to DATA READY high).	4T + 20nS	6T + 300nS

Notes:-

(1) The CHIP ENABLE line going high during the select timing resets DATA READY and terminates the read action. Not all 3 words (or 5 bytes) need to be accessed and read termination can take place at any time.

(2) The output timing for the 8 bit parallel bus is similar to the above but with 5 byte accesses required.

(3) The NOT CHIP ENABLE line cannot be held permanently low (see (1)).

(4) All timings are theoretical and are based on a load of 100pF and one standard TTL input.

(5) The NOT OUTPUT SELECT line only affects the chip when NOT CHIP ENABLE is low.

(6) In BYTE mode, NOT CHIP ENABLE low to NOT OUTPUT SELECT low, (tsu) must be > 100nS to ensure correct BYTE output sequence.

ARINC 429
Receiver Subsystem