20 A Step-Down DC-DC Controller

ADP1821

FEATURES

Wide input voltage range: 1 V to 24 V
Wide output voltage range: 0.6 V to 85% of input voltage
1% accuracy, 0.6 V reference voltage
All N-channel MOSFET
300 kHz, 600 kHz, or up to 1.2 MHz synchronized frequency
No current sense resistor required
Power-good output
Programmable soft start with reverse current protection
Current limit protection
Thermal overload protection
Overvoltage protection
Undervoltage lockout
1 μA shutdown supply current
Small, 16-lead QSOP package

APPLICATIONS

Telecom and networking systems
High performance servers
Medical imaging systems
DSP core power supplies
Microprocessor core power supplies
Mobile communication base stations
Distributed power

GENERAL DESCRIPTION

The ADP1821 is a versatile and inexpensive, synchronous PWM step-down controller. It drives an all N-channel power stage to regulate an output voltage as low as 0.6 V with up to a 20 A load current.

The ADP1821 is well suited for a wide range of high power applications, such as DSP and processor core power in telecom, medical imaging, high performance servers, and industrial applications. It operates from a 3.0 V to 5.5 V supply with a power input voltage ranging from 1.0 V to 24 V.

The ADP1821 can operate at any frequency between 300 KHz and 1.2 MHz either by synchronizing with an external source or an internally generated, logic controlled clock of 300 KHz or 600 KHz. It includes an adjustable soft start to allow sequencing and quick power-up while preventing input inrush current. Output reverse-current protection at startup prevents excessive output voltage excursions. The adjustable virtually lossless current limit scheme reduces external part count and improves efficiency.

The ADP1821 operates over the –40°C to +85°C temperature range and is available in a 16-lead QSOP package.

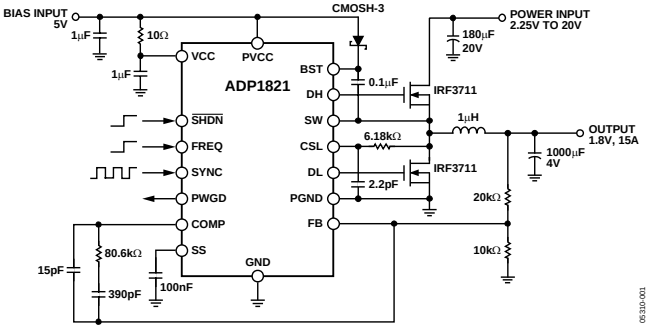

Figure 1. Typical Operating Circuit

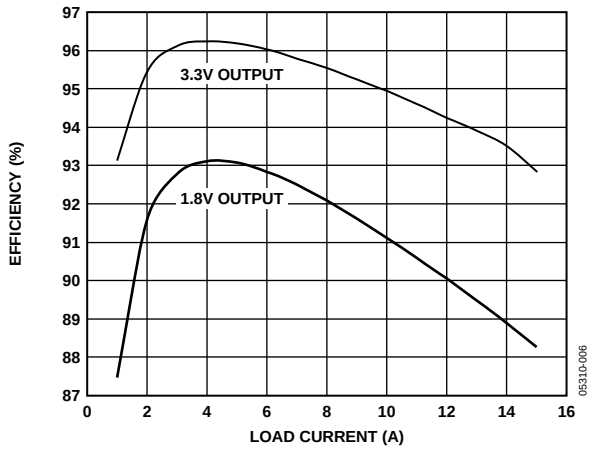

Figure 2. Efficiency vs. Load Current, 5 V Input

Rev. 0

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REVISION HISTORY

7/05—Revision 0: Initial Version

SPECIFICATIONS

See Figure 1. $V_{VCC} = V_{PVCC} = V_{\overline{SHDN}} = V_{FREQ} = 5$ V, SYNC = GND. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC). $T_A = 25°C$, unless otherwise specified.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLY					
Input Voltage		3.0		5.5	V
Undervoltage Lockout Threshold	V_{VCC} rising	2.5	2.7	2.9	V
Undervoltage Lockout Hysteresis	V_{VCC}		0.1		V
Quiescent Current	$I_{VCC} + I_{VCC}$, not switching		1	2	mA
Shutdown Current	$\overline{SHDN}$ = GND			10	µA
Power Stage Supply Voltage		1.0		20	V
ERROR AMPLIFER					
FB Regulation Voltage	$T_A = -40°C$ to $+85°C$	594	600	606	mV
FB Input Bias Current		−100	+1	+100	nA
Error Amplifier Open-Loop Voltage Gain			70		dB
COMP Output Sink Current			600		µA
COMP Output Source Current			110		µA
PWM CONTROLLER					
PWM Peak Ramp Voltage			1.25		V
DL Minimum On-Time	FREQ = VCC (300 kHz)	140	170	200	ns
SOFT START					
SS Pull-Up Resistance	SS = GND		95		kΩ
SS Pull-Down Resistance	$V_{SS} = 0.6$ V	1.65	2.5	4.2	kΩ
OSCILLATOR					
Oscillator Frequency	FREQ = GND, $T_A = -40°C$ to $+85°C$	250	310	375	kHz
	FREQ = VCC, $T_A = -40°C$ to $+85°C$	470	570	720	kHz
Synchronization Range	FREQ = GND	300		600	kHz
	FREQ = VCC	600		1200	kHz
SYNC Minimum Pulse Width				80	ns
CURRENT SENSE					
CSL Threshold Voltage	Relative to PGND	−30	0	+30	mV
CSL Output Current	$V_{CSL} = 0$ V, $T_A = -40°C$ to $+85°C$	42	50	54	µA
Current Sense Blanking Period			160		ns
GATE DRIVERS					
DH Rise Time	$C_{GATE} = 3$ nF, $V_{DH} = V_{IN}$, $V_{BST} - V_{SW} = 5$ V		16		ns
DH Fall Time	$C_{GATE} = 3$ nF, $V_{DH} = V_{IN}$, $V_{BST} - V_{SW} = 5$ V		12		ns
DL Rise Time	$C_{GATE} = 3$ nF, $V_{DL} = V_{IN}$		19		ns
DL Fall Time	$C_{GATE} = 3$ nF, $V_{DL} = 0$ V		13		ns
DL Low to DH High Dead Time			33		ns
DH Low to DL High Dead Time			42		ns
LOGIC THRESHOLDS ($\overline{SHDN}$, SYNC, FREQ)					
$\overline{SHDN}$, SYNC, FREQ Input High Voltage	$V_{VCC} = 3.0$ V to 5.5 V	2.0			V
$\overline{SHDN}$, SYNC, FREQ Input Low Voltage	$V_{VCC} = 3.0$ V to 5.5 V			0.8	V
SYNC, FREQ Input Leakage Current	SYNC = FREQ = GND		0.1	1	µA
$\overline{SHDN}$ Pull-Down Resistance			100		kΩ
THERMAL SHUTDOWN					
Thermal Shutdown Threshold			145		°C
Thermal Shutdown Hysteresis			10		°C

Parameter	Conditions	Min	Typ	Max	Unit
PWGD OUTPUT					
FB Overvoltage Threshold	V_{FB} rising		750		mV
FB Overvoltage Hysteresis			35		mV
FB Undervoltage Threshold	V_{FB} rising		550		mV
FB Undervoltage Hysteresis			35		mV
PWGD Off Current	V_{PWGD} = 5 V			1	μA
PWGD Low Voltage	I_{PWGD} = 10 mA		150	500	mV

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC, $\overline{SHDN}$, SYNC, FREQ, COMP, SS, FB to GND, PVCC to PGND, BST to SW	−0.3 V to +6 V
BST-to-GND	−0.3 V to +30 V
CSL-to-GND	−1 V to +30 V
DH-to-GND	(V_{SW} − 0.3 V) to (V_{BST} + 0.3 V)
DL-to-PGND	−0.3 V to (V_{PVCC} + 0.3 V)
SW-to-GND	−2 V to +30 V
PGND-to-GND	±2 V
θ_{JA}, 2-Layer (SEMI Standard Board)	150°C/W
θ_{JA}, 4-Layer (JEDEC Standard Board)	105°C/W
Operating Ambient Temperature	−40°C to +85°C
Operating Junction Temperature	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Maximum Soldering Lead Temperature	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other condition s above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified all other voltages are referenced to GND.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

SIMPLIFIED BLOCK DIAGRAM

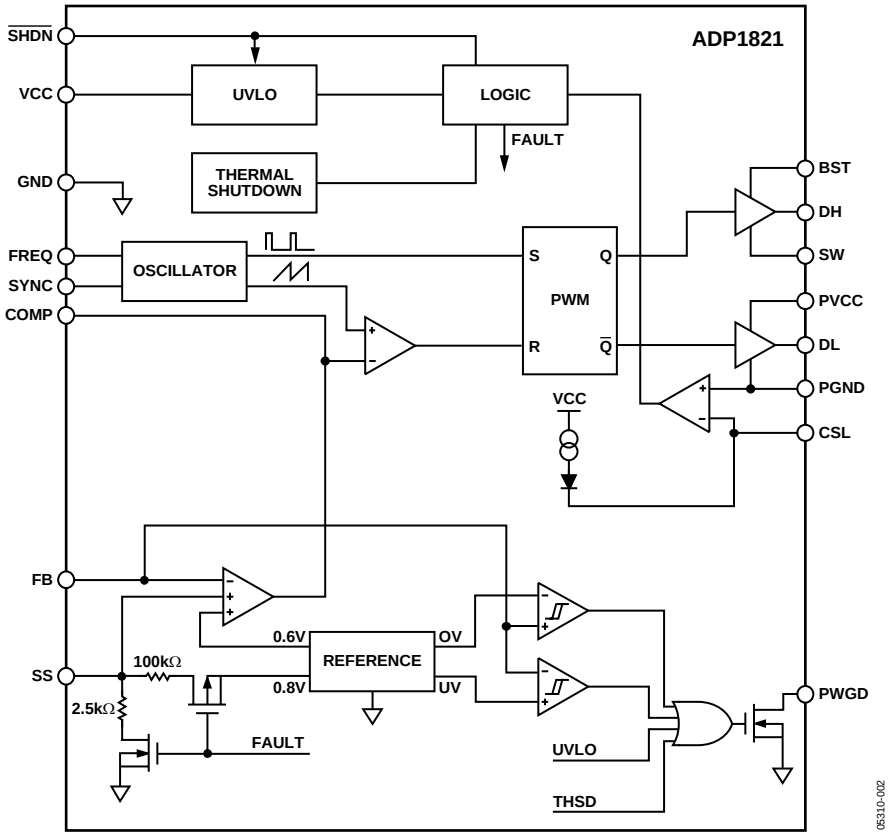


Figure 3.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

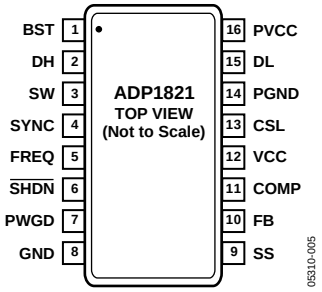


Figure 4. Pin Configuration

Table 3. Pin Function Description

Pin No.	Mnemonic	Description
1	BST	High-Side Gate Driver Boost Capacitor Input. A capacitor between SW and BST powers the high-side gate driver DH. The capacitor is charged through a diode from PVCC when the low-side MOSFET is on. Connect a 0.1 µF or greater ceramic capacitor from BST to SW and a Schottky diode from PVCC to BST to power the high-side gate driver.
2	DH	High-Side Gate Driver Output. Connect DH to the gate of the external high-side, N-channel MOSFET switch. DH is powered from the capacitor between SW and BST and its voltage swings between V_{SW} and V_{BST}.
3	SW	Power Switch Node. SW is the power switching node. Connect the source of the high-side, N-channel MOSFET switch and the drain of the low-side, N-channel MOSFET synchronous rectifier to SW. SW powers the output through the output LC filter.
4	SYNC	Frequency Synchronization Input. Drive SYNC with an external 300 kHz to 1.2 MHz signal to synchronize the converter switching frequency to the applied signal. The maximum SYNC frequency is limited to 2× the nominal internal frequency selected by FREQ. Do not leave SYNC unconnected; when not used, connect SYNC to GND.
5	FREQ	Frequency Select Input. FREQ selects the converter switching frequency. Drive FREQ low to select 300 kHz, or high to select 600 kHz. Do not leave FREQ unconnected.
6	$\overline{\text{SHDN}}$	Active-Low DC-to-DC Shutdown Input. Drive $\overline{\text{SHDN}}$ high to turn-on the converter and drive it low to turn it off. Connect $\overline{\text{SHDN}}$ to VCC for automatic startup.
7	PWGD	Open-Drain Power-Good Output. PWGD sinks current to GND when the output voltage is above or below the regulation voltage. Connect a pull-up resistor from PWGD to VDD for a logical power-good indicator.
8	GND	Analog Ground. Connect GND to PGND at a single point as close as possible to the IC.
9	SS	Soft-Start Control Input. A capacitor from SS to GND controls the soft-start period. When the output is overloaded, SS is discharged to prevent excessive input current while the output recovers. Connect a 1 nF to 1 µF capacitor from SS to GND to set the soft-start period. See the Soft Start section.
10	FB	Voltage Feedback Input. Connect to a resistive voltage divider from the output to FB to set the output voltage. See the Setting the Output Voltage section.
11	COMP	Compensation Node. Connect a resistor-capacitor network from COMP to FB to compensate the regulation control system. See the Compensation section.
12	VCC	Internal Power Supply Input. VCC powers the internal circuitry. Bypass VCC to GND with 0.1 µF or greater capacitor connected as close as possible to the IC.
13	CSL	Low-Side Current Sense Input. Connect CSL to SW through a resistor to set the current limit. See the Setting the Current Limit section.
14	PGND	Power Ground. Connect GND to PGND at a single point as close as possible to the IC.
15	DL	Low-Side Gate Driver Output. Connect DL to the gate of the low-side, N-channel MOSFET synchronous rectifier. The DL voltage swings between PGND and PVCC.
16	PVCC	Internal Gate-Driver Power Supply Input. PVCC powers the low-side, gate driver DL. Bypass PVCC to PGND with 1 µF or greater capacitor connected as close as possible to the IC.

TYPICAL PERFORMANCE CHARACTERISTICS

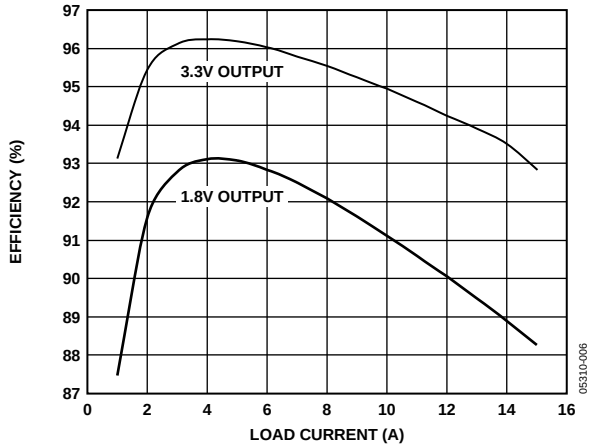


Figure 5. Efficiency vs. Load Current, V_{IN} = 5 V, V_{OUT} = 3.3 V, 1.8 V

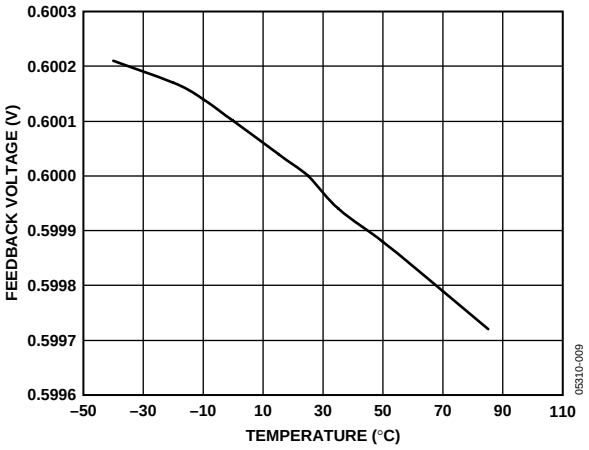


Figure 8. FB Regulation Voltage vs. Temperature

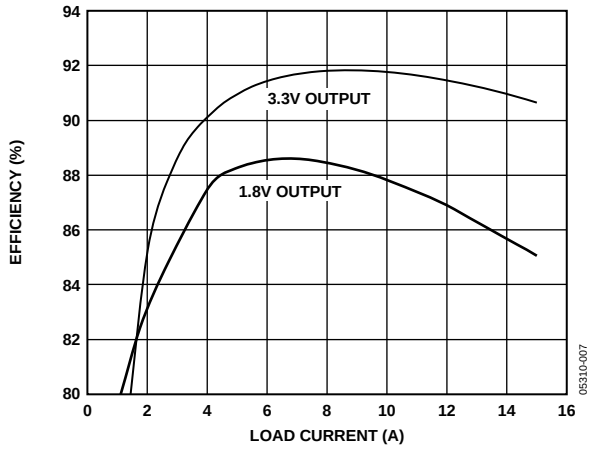


Figure 6. Efficiency vs. Load Current, V_{IN} = 12 V, V_{OUT} = 3.3 V, 1.8 V

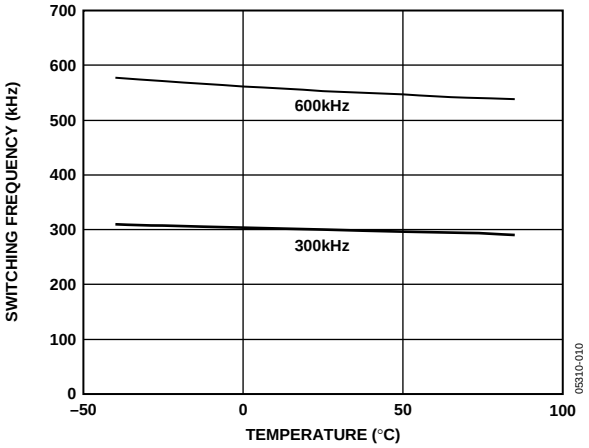


Figure 9. Switching Frequency vs. Temperature

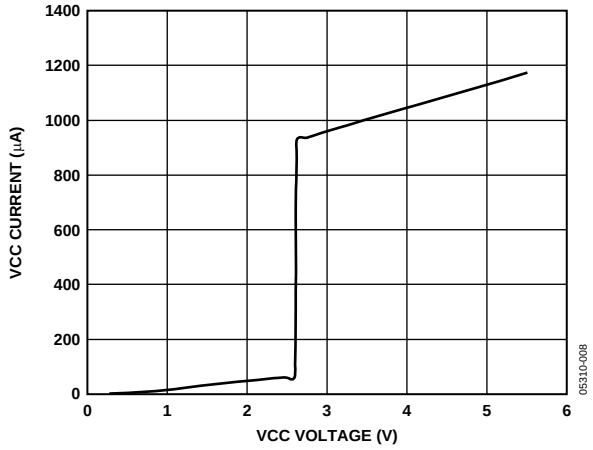


Figure 7. VCC Supply Current vs. Voltage

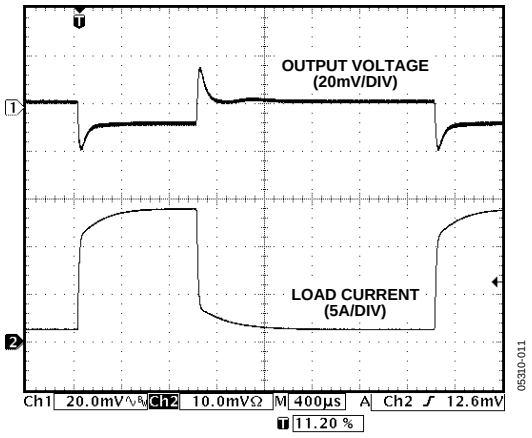


Figure 10. Load Transient Response, 1.5 A to 15 A

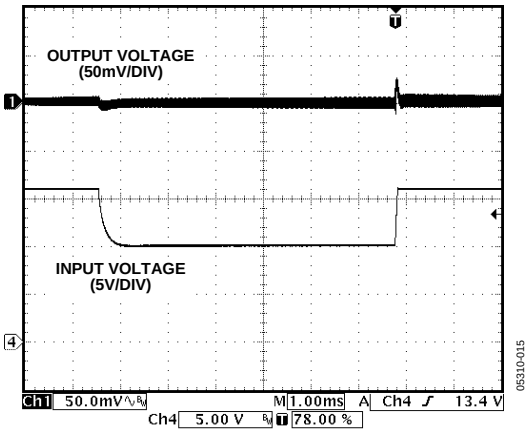


Figure 11. Line Transient Response, 10 V to 16 V

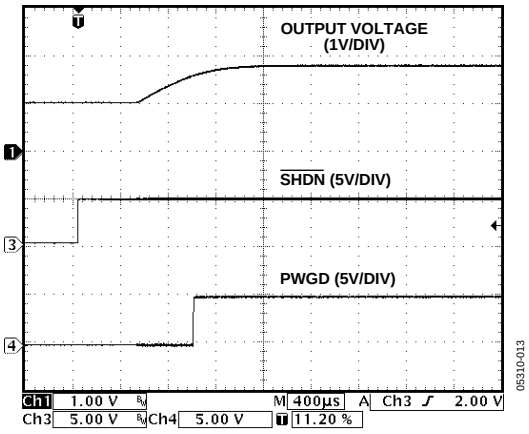


Figure 13. Power-On Response, Prebiased Output

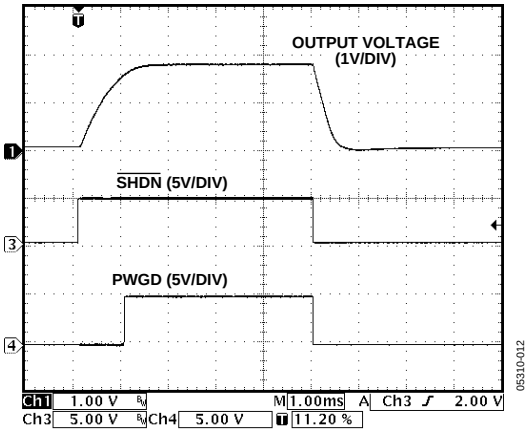


Figure 12. Power-On Response

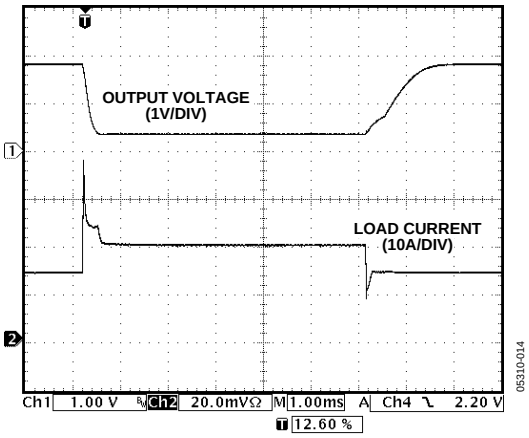


Figure 14. Output Short-Circuit Response and Recovery

THEORY OF OPERATION

The ADP1821 is a versatile, economical, synchronous-rectified, fixed-frequency, pulse width-modulated (PWM) step-down controller capable of generating an output voltage as low as 0.6 V while sourcing up to 20 A to the load. It is ideal for a wide range of high-power applications, such as DSP power and processor core power in telecom, medical imaging, and indus-trial applications. The ADP1821 controller runs from 3.0 V to 5.5 V, and accepts a power input voltage between 1.0 V and 20 V.

The ADP1821 operates at a fixed, internally set 300 kHz or 600 kHz switching frequency that is controlled by the state of the FREQ input. The high frequency reduces external component size and cost while maintaining high efficiency. For noise sensitive applications where the switching frequency needs to be more tightly controlled, synchronize the ADP1821 to an external signal whose frequency is between 300 kHz and 1.2 MHz.

The ADP1821 includes adjustable soft start with output reverse-current protection, and a unique adjustable, lossless current limit. It operates over the −40°C to +85°C temperature range and is available in a space-saving, 16-lead QSOP package.

CURRENT LIMIT SCHEME

The ADP1821 employs a unique, programmable cycle-by-cycle lossless current-sensing scheme that uses an inexpensive high-value resistor to set the current limit. A 50 µA current source is forced out of CSL to a programming resistor connected to SW. The resulting voltage across the current sense resistor sets the current limit threshold. When on-state voltage of the low-side, MOSFET synchronous rectifier exceeds the programmed threshold, the low-side MOSFET remains on, preventing another on cycle and reducing the inductor current. Once the MOSFET voltage, and thus the inductor current, is below the current-sense threshold, the synchronous rectifier is allowed to turn off and another cycle begins.

When the ADP1821 senses an overcurrent condition, SS sinks current from the soft-start capacitor through an internal 2.5 kΩ resistor, reducing the voltage at SS, and thus reducing the regulated output voltage. The ADP1821 remains in this mode for as long as the over-current condition persists. When the over-current condition is removed, operation resumes in soft-start mode. This ensures that when the overload condition is removed, the output voltage smoothly transitions back to regulation while providing protection for overload and short-circuit conditions.

SOFT START

When powering up or resuming operation after shutdown, overload, or short-circuit conditions, the ADP1821 employs an adjustable soft-start feature that reduces input current transients and prevents output voltage overshoot at start-up and overload conditions. The soft-start period is set by the value of the soft-start capacitor, C_{SS}, between SS and GND.

When starting the ADP1821, C_{SS} is initially discharged. It is enabled by either driving $\overline{SHDN}$ high or by bringing VCC above the undervoltage lockout threshold. C_{SS} begins charging to 0.8 V through an internal 100 kΩ resistor. As C_{SS} charges, the regulation voltage at FB is limited to the lesser of either the voltage at SS or the internal 0.6 V reference voltage. As the voltage at SS rises, the output voltage rises proportionally until the voltage at SS exceeds 0.6 V. At this time, the output voltage is regulated to the desired voltage.

If the output voltage is precharged prior to turn-on, the ADP1821 prevents reverse inductor current, which would discharge the output voltage. Once the voltage at SS exceeds the 0.6 V regulation voltage, the reverse current is re-enabled to allow the output voltage regulation to be independent of load current.

To override the soft-start feature, leave SS unconnected. This allows the output voltage to rise as quickly as possible and eliminates the soft-start period.

HIGH-SIDE DRIVER (BST and DH)

Gate drive for the high-side power MOSFET is generated by a flying capacitor boost circuit. This circuit allows the high-side, N-channel MOSFET gate to be driven above the input voltage, allowing full enhancement and low voltage drop across the MOSFET. The circuit is powered from a flying capacitor from SW to BST that in turn is powered from the PVCC gate driver voltage. When the low-side switch is turned on, SW is driven to PGND and the flying capacitor is charged from PVCC through an external Schottky rectifier. The capacitor stores sufficient charge to power BST to drive DH high and to fully enhance the high-side, N-channel MOSFET. Use a flying capacitor value greater than 100× the high-side MOSFET input capacitance.

LOW-SIDE DRIVER (DL)

DL is the gate drive for the low-side, power MOSFET synchronous rectifier. Synchronous rectification reduces conduction losses developed by a conventional rectifier by replacing it with a low-resistance MOSFET switch. DL turns on the synchronous rectifier by driving the gate voltage to PVCC. The MOSFET is turned off by driving the gate voltage to PGND.

An active dead time reduction circuit reduces the break-before-make time of the switching to limit the losses due to current flowing through the synchronous rectifier body diode or external Schottky rectifier.

INPUT VOLTAGE RANGE

The ADP1821 takes its internal power from the VCC and PVCC inputs. PVCC powers the low-side MOSFET gate drive (DL) and VCC powers the internal control circuitry. Both of these inputs are limited to between 3.0 V and 5.5 V. Bypass PVCC to PGND with a 1 µF or greater capacitor. Bypass VCC to GND with a 0.1 µF or greater capacitor.

The power input to the dc-to-dc converter can range between 1.2× the output voltage up to 20 V. Bypass the power input to PGND with a suitably large capacitor. See the Selecting the Input Capacitor section.

SETTING THE OUTPUT VOLTAGE

The output voltage is set using a resistive voltage divider from the output to FB. The voltage divider drops the output voltage to the 0.6 V FB regulation voltage to set the regulation output voltage. The output voltage is set to voltages as low as 0.6 V and as high as 85% of the minimum power input voltage (see the Feedback Voltage Divider section).

SWITCHING FREQUENCY CONTROL

The ADP1821 has a logic controlled frequency select input, FREQ, that sets the switching frequency to 300 kHz or 600 kHz. Drive FREQ low for 300 kHz and drive it high for 600 kHz.

The SYNC input is used to synchronize the converter switching frequency to an external signal. The synchronization range is 300 kHz to 1.2 MHz. The acceptable synchronization frequency range is limited to twice the nominal switching frequency set by FREQ. For lower frequency synchronization, between 300 kHz and 600 kHz, connect FREQ to GND. For higher frequency synchronization, between 480 kHz and 1.2 MHz, connect FREQ to VCC (see the Synchronizing the Converter section for more information).

COMPENSATION

The control loop is compensated by an external series RC network from COMP to FB and sometimes requires a series RC in parallel with the top voltage divider resistor. COMP is the output of the internal error amplifier.

The internal error amplifier compares the voltage at FB to the internal 0.6 V reference voltage. The difference between the two (the feedback voltage error) is amplified by the 1,000 V-to-V gain of the error amplifier. To optimize the ADP1821 for stability and transient response for a given set of external components and input/output voltage conditions, choose the compensation components. For more information on choosing the compensation components, see the Compensating the Regulator section.

POWER-GOOD INDICATOR

The ADP1821 features an open-drain power-good output, (PWGD), that sinks current when the output voltage drops 8.3% below or 25% above the nominal regulation voltage. Two comparators measure the voltage at FB to set these thresholds. The PWGD output also sinks current if an overtemperature or input undervoltage conditions are detected and is operational with VCC voltage as low as 1.0 V.

Use this output as a simple power-good signal by connecting a pull-up resistor from PWGD to an appropriate supply voltage.

SHUTDOWN CONTROL

The ADP1821 dc-to-dc converter features a low-power shutdown mode that reduces quiescent supply current to 1 µA. To shut down the ADP1821, drive $\overline{\text{SHDN}}$ low. To turn it on, drive $\overline{\text{SHDN}}$ high. For automatic startup, connect $\overline{\text{SHDN}}$ to VCC.

APPLICATION INFORMATION

SELECTING THE INPUT CAPACITOR

The input capacitor absorbs the switched input current of the dc-to-dc converter, allowing the input source to deliver smooth dc current. Choose an input capacitor whose impedance at the switching frequency is lower than the input source impedance. Use low equivalent series resistance (ESR) capacitors, such as low-ESR tantalum, ceramic, or organic electrolyte types, such as Sanyo Os-Con. For all types of capacitors, make sure that the current rating of the capacitor is greater than 1/2 of the maximum output load current.

OUTPUT LC FILTER

The output LC filter smoothes the switched voltage at SW making the dc output voltage. Choose the output LC filter to achieve the desired output ripple voltage. Since the output LC filter is part of the regulator negative-feedback control loop, the choice of the output LC filter components affects the regulation control loop stability.

Choose an inductor value such that the inductor ripple current is approximately 1/3 of the maximum dc output load current. Using a larger value inductor results in a physical size larger than required and using a smaller value results in increased losses in the inductor and/or MOSFET switches.

Choose the inductor value by the following equation:

$$L = \frac{1}{(f_{SW})(\Delta I_L)} V_{OUT}\left[1 - \frac{V_{OUT}}{V_{IN}}\right] \quad (1)$$

where:
L is the inductor value.
f_{SW} is the switching frequency.
V_{OUT} is the output voltage.
V_{IN} is the input voltage.
ΔI_L is the inductor ripple current, typically 1/3 of the maximum dc load current.

Choose the output capacitor to set the desired output voltage ripple. The ADP1821 functions with output capacitors that have both high and low equivalent series resistance (ESR). For high-ESR capacitors, such as tantalum or electrolytic types, many parallel connected capacitors might be required to achieve the desired output ripple voltage. When choosing an output capacitor, consider ripple current rating, capacitance, and ESR. Make sure that the ripple current rating is higher than the maximum inductor ripple current (ΔI_L).

The output ripple voltage is a function of the inductor ripple current and the capacitor impedance at the switching frequency. For high ESR capacitors, the impedance is dominated by the ESR, while for low ESR capacitors the impedance is dominated by the capacitance. Determine if the capacitor is high ESR or low ESR be comparing the zero frequency formed by the capacitance and the ESR to the switching frequency.

$$f_{ESRZ} = \frac{1}{2\pi(C_{OUT})(ESR)} \quad (2)$$

where:
f_{ESRZ} is the frequency of the output capacitor ESR zero.
C_{OUT} is the output capacitance.
ESR is the equivalent series resistance of the capacitor.

If f_{ESRZ} is much less than the switching frequency, then the capacitor is high ESR and the ESR dominates the impedance at the switching frequency. If f_{ESRZ} is much greater than the switching frequency, the capacitor is low ESR and the impedance is dominated by the capacitance at the switching frequency.

When using capacitors whose impedance is dominated by ESR at the switching frequency (such as tantalum or aluminum electrolytic capacitors), approximate the output voltage ripple current by the following equation:

$$\Delta V_{OUT} \cong \Delta I_L(ESR) \quad (3)$$

where:
ΔV_{OUT} is the output ripple voltage.
ΔI_L is the inductor ripple current.
ESR is the total equivalent series resistance of the output capacitor (or the parallel combination of ESR of all parallel-connected output capacitors).

Make sure that the ripple current rating of the output capacitor(s) is greater than the maximum inductor ripple current.

For output capacitors whose ESR is much lower than the capacitive impedance at the switching frequency, the capacitive impedance dominates the output ripple current. In this case, determine the ripple voltage by the following equation:

$$\Delta V_{OUT} \cong \frac{\Delta I_L}{8(C_{OUT})(f_{SW})} \quad (4)$$

where:
f_{SW} is the switching frequency.
C_{OUT} is the output capacitance.

When f_{ESRZ} is approximately the same as the switch-ing frequency, the square-root sum of the squares of the two ripples applies or

$$\Delta V_{OUT} \cong \sqrt{\left[\Delta I_L(ESR)\right]^2 + \left[\frac{\Delta I_L}{8(C_{OUT})(f_{SW})}\right]^2} \quad (5)$$

SELECTING THE MOSFETS

The choice of MOSFET directly affects the dc-to-dc converter performance. The MOSFET must have low on resistance to reduce I^2R losses and low gate-charge to reduce transition losses. Also, the MOSFET must have low thermal resistance to ensure that the power dissipated in the MOSFET does not result in excessive MOSFET die temperature.

The high-side MOSFET carries the load current during on-time and carries all the transitions losses of the converter. Typically, the lower the MOSFET on resistance, the higher the gate charge and vice versa. Therefore, it is important to choose a high-side MOSFET that balances the two losses. The conduction loss of the high-side MOSFET is determined by the equation

$$P_C \cong (I_{LOAD})(R_{ON})\left(\frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

where:
P_C = conduction power loss.
R_{ON} = MOSFET on resistance.

The transition loss is approximated by the equation

$$P_T \cong (I_{LOAD})(V_{IN})(Q_G)(f_{SW}) \quad (7)$$

where:
P_T = transition loss power.
Q_G = MOSFET total gate charge.
f_{SW} = converter switching frequency.

The total power dissipation of the high-side MOSFET is the sum of the two losses or

$$P_{HS} \cong (P_C)(P_T) \quad (8)$$

where P_{HS} is the total high-side, MOSFET power loss.

The low-side MOSFET does not carry the transition losses and carries the inductor current when the high-side MOSFET is off. For high input voltage and low output voltage, the low-side MOSFET carries the current most of the time, and therefore to achieve high efficiency it is critical to optimize the low-side MOSFET for low on resistance. In cases where the power loss exceeds the MOSFET rating or lower resistance is required than is available in a single MOSFET, connect multiple low-side MOSFETs in parallel. The equation for low-side MOSFET power loss is

$$P_{LS} \cong (I_{LOAD})^2(R_{ON})\left[1-\frac{V_{OUT}}{V_{IN}}\right] \quad (9)$$

where:
P_{LS} is the low-side MOSFET on resistance.
R_{ON} is the total on resistance of the low-side MOSFET(s).

If multiple low-side MOSFETs are used in parallel, use the parallel combination of the on resistances for determining R_{ON} to solve this equation.

SETTING THE CURRENT LIMIT

The internal current limit circuit measures the voltage across the low-side MOSFET to determine the load current. When the low-side MOSFET current exceeds the current limit, the high-side MOSFET is not allowed to turn on until the current drops below the current limit.

The current limit is set through the current limit resistor, R_{CL}. The current sense pin, CSL, sources 50 µA through R_{CL}. This creates an offset voltage of resistance of R_{CL} multiplied by the 50 µA CSL current. When the low-side MOSFET voltage is equal to or greater than the offset voltage, the ADP1821 is in current limit mode and prevents additional on-time cycles.

Choose the current limit resistor by the equation

$$R_{CL} = \frac{(I_{LPK})(R_{ONWC})}{42\mu A} \quad (10)$$

where:
I_{LPK} is the peak inductor current.
R_{ONWC} is the worst-case (maximium) low-side MOSFET on resistance.

The worst-case, low-side, MOSFET on resistance can be found in the MOSFET data sheet. Note that MOSFETs typically increase on resistance with increasing die temperature. To determine the worst-case MOSFET on resistance, calculate the worst-case MOSFET temperature (based on the MOSFET power loss) and multiply by the ratio between the typical on resistance at that temperature and the on resistance at 25°C, as listed in the MOSFET data sheet.

FEEDBACK VOLTAGE DIVIDER

The output regulation voltage is set through the feedback voltage divider. The output voltage is reduced through the voltage divider and drives the FB feedback input. The regulation threshold at FB is 0.6 V. For the low-side resistor of the voltage divider, R_{BOT}, use 10 kΩ. A larger value resistor can be used, but results in a reduction in output voltage accuracy. Choose RTOP to set the output voltage by the following equation:

$$R_{TOP} = R_{BOT}\left(\frac{V_{OUT} - V_{FB}}{V_{FB}}\right) \quad (11)$$

where:
R_{TOP} is the high-side voltage divider resistance.
R_{BOT} is the low-side voltage divider resistance.
V_{OUT} is the regulated output voltage.
V_{FB} is the feedback regulation threshold, 0.6 V.

COMPENSATING THE REGULATOR

The output of the error amplifier at COMP is used to compensate the regulation control system. Connect a resistor capacitor, RC, and network from COMP to FB to compensate the regulator.

The first step in selecting the compensation components is determining the desired regulation control crossover frequency, f_{CO}. Choose a crossover frequency approximately 1/10 of the switching frequency, or

$$f_{CO} = \frac{f_{SW}}{10} \quad (12)$$

The characteristics of the output capacitor affects the compensation required to stabilize the regulator. The output capacitor acts with its equivalent series resistance (ESR) to form a zero. Calculate the ESR zero frequency by the following equation:

$$f_{ESRZ} = \frac{1}{2\pi(C_{OUT})(ESR)} \quad (13)$$

Note that as similar capacitors are placed in parallel, the ESR zero frequency remains the same.

If $f_{ESRZ} \le \frac{f_{CO}}{2}$, use the ESR zero to stabilize the regulator (see the Compensation Using the ESR Zero section). If $f_{ESRZ} \ge 2\,f_{CO}$, use a feed-forward network to stabilize the regulator (see the Compensation Using Feed Forward section). If $\frac{f_{CO}}{2} < f_{ESRZ} < 2f_{CO}$, use both the ESR zero and feed-forward zeros to stabilize the regulator (see the Compensation Using Both the ESR and Feed-Forward Zeros section).

In all three cases, although not required, it is sometimes beneficial to add an additional compensation capacitor, C_{C2}, from COMP to FB to reduce high frequency noise. This capacitor forms an extra pole in the loop response. Choose this capacitor such that the pole occurs at approximately 1/2 of the switching frequency or

$$F_{PC2} = \frac{f_{SW}}{2} = \frac{1}{2\pi(C_{C2})(R_{COMP})} \quad (14)$$

Solving for C_{C2},

$$C_{C2} = \frac{2}{2\pi(f_{SW})(R_{COMP})} \quad (15)$$

Compensation Using the ESR Zero

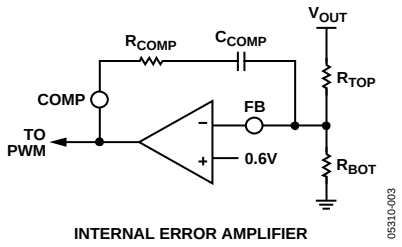


Figure 15. Compensation Using the ESR Zero

If the output capacitor ESR zero is sufficiently low (less-than-or-equal-to ½ of the crossover frequency), use the ESR to stabilize the regulator. In this case, use the circuit shown in Figure 17. Choose the compensation resistor to set the desired crossover frequency, typically 1/10 of the switching frequency or

$$R_{COMP} = \frac{(R_{TOP})(V_{RAMP})(f_{ZESR})(f_{CO})}{V_{IN}(f_{LC})^2} \quad (16)$$

where:
R_{COMP} is the compensation resistor.
V_{RAMP} is the internal ramp peak voltage, 1.25 V.
f_{ZESR} and f_{CO} are the ESR zero and crossover frequencies.
V_{IN} is the dc input voltage.
f_{LC} is the characteristic frequency of the output LC filter or

$$f_{LC} = \frac{1}{2\pi\sqrt{LC}} \quad (17)$$

using known constants

$$R_{COMP} \cong \frac{4.9(R_{TOP})(f_{ZESR})(f_{SW})(L)(C)}{V_{IN}} \quad (18)$$

Choose the compensation capacitor to set the compensation zero, f_{ZC}, to the lesser of 1/4 of the crossover frequency or 1/2 of the LC resonant frequency or

$$f_{ZC} = \frac{f_{CO}}{4} = \frac{f_{SW}}{20} = \frac{1}{2\pi(C_{COMP})(R_{COMP})} \quad (19)$$

or

$$f_{ZC} = \frac{f_{LC}}{2} = \frac{1}{2\pi(C_{COMP})(R_{COMP})} \quad (20)$$

Solving for C_{COMP},

$$C_{COMP} = \frac{4}{2\pi(f_{CO})(R_{COMP})} \quad (21)$$

In terms of the switching frequency and combining the constants,

$$C_{COMP} \cong \frac{6.37}{(f_{SW})(R_{COMP})} \quad (22)$$

or

$$C_{COMP} = \frac{2}{2\pi(f_{LC})(R_{COMP})} \quad (23)$$

or whichever is greater.

Compensation Using Feed Forward

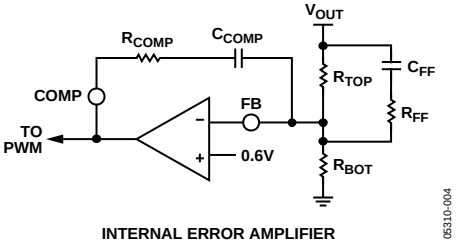


Figure 16. Compensation Using Feed Forward

If the ESR zero is at too high a frequency to be useful in stabilizing the regulator, add a series RC network (as shown in Figure 16) in parallel with the topside voltage divider resistor, R_{TOP}. This adds an additional zero and pole pair that is used to increase the phase at crossover, thus improving stability.

Choose the feed-forward zero frequency for 1/7 of the crossover frequency and the feed-forward pole at 7× the crossover frequency. This sets the ratio of pole-to-zero frequency of approximately 50:1 for optimum stability.

Choose the compensation resistor, R_{COMP}, to set the crossover frequency by the following equation:

$$R_{COMP} = \frac{(R_{TOP})(V_{RAMP})(f_{ZFF})(f_{CO})}{V_{IN}(f_{LC})^2} \quad (24)$$

where f_{ZFF} is the feed-forward zero frequency and is 1/7 of the crossover frequency. Simplifying the following equation:

$$R_{COMP} \cong 0.0705 \frac{(R_{TOP})(f_{SW})^2(L)(C)}{V_{IN}} \quad (25)$$

Choose the compensation capacitor to set the compensation zero, f_{ZC}, to the lesser of 1/4 of the crossover frequency or 1/2 of the LC resonant frequency or

$$f_{ZC} = \frac{f_{CO}}{4} = \frac{f_{SW}}{20} = \frac{1}{2\pi(C_{COMP})(R_{COMP})} \quad (26)$$

or

$$f_{ZC} = \frac{f_{LC}}{2} = \frac{1}{2\pi(C_{COMP})(R_{COMP})} \quad (27)$$

Solving for C_{COMP},

$$C_{COMP} = \frac{4}{2\pi(f_{CO})(R_{COMP})} \quad (28)$$

In terms of the switching frequency and combining the constants,

$$C_{COMP} \cong \frac{6.37}{(f_{SW})(R_{COMP})} \quad (29)$$

or

$$C_{COMP} = \frac{2}{2\pi(f_{LC})(R_{COMP})} \quad (30)$$

or whichever is greater.

Choose the feed-forward capacitor, C_{FF}, to set the feed-forward zero at 1/7 of the crossover frequency

$$f_{ZFF} = \frac{f_{CO}}{7} \quad (31)$$

or

$$f_{CO} = \frac{7}{2\pi(R_{TOP})(C_{FF})} \quad (32)$$

Simplifying and solving for C_{FF},

$$C_{FF} = \frac{11.14}{(R_{TOP})(f_{SW})} \quad (33)$$

Choose the feed-forward resistor, R_{FF}, to set the condition

$$f_{CO} = \frac{1}{7(2\pi)(R_{FF})(C_{FF})} \quad (34)$$

Simplifying and solving for R_{FF},

$$R_{FF} = \frac{0.227}{(f_{SW})(C_{FF})} \quad (35)$$

Compensation Using Both the ESR and Feed-Forward Zeros

If the output capacitor ESR zero frequency falls between 1/2 of the crossover frequency to 2× the crossover frequency, use the circuit shown in Figure 17, such that the ESR zero along with a feed-forward network stabilizes the regulator. In this case, the feed-forward zero is set to 1/7 of the crossover frequency and the feed-forward pole is set to the same frequency as the ESR zero.

Choose the compensation resistor, R_{COMP}, to set the crossover frequency by the following equation:

$$R_{COMP} = \frac{(R_{TOP})(V_{RAMP})(f_{ZFF})(f_{CO})}{V_{IN}(f_{LC})^2} \quad (36)$$

where f_{ZFF} is the feed-forward zero frequency and is 1/7 of the crossover frequency. Simplifying the following equation:

$$R_{COMP} \cong 0.0705 \frac{(R_{TOP})(f_{SW})^2(L)(C)}{V_{IN}} \quad (37)$$

Choose the compensation capacitor to set the compensation zero, f_{ZC}, to ½ of the LC resonant frequency or

$$f_{ZC} = \frac{f_{LC}}{2} = \frac{1}{2\pi(C_{COMP})(R_{COMP})} \quad (38)$$

Solving for C_{COMP},

$$C_{COMP} = \frac{2}{2\pi(f_{LC})(R_{COMP})} \quad (39)$$

Choose the feed-forward capacitor, C_{FF}, to set the feed-forward zero at 1/7 of the crossover frequency

$$f_{ZFF} = \frac{f_{CO}}{7} \quad (40)$$

or

$$f_{CO} = \frac{7}{2\pi(R_{TOP})(C_{FF})} \quad (41)$$

Simplifying and solving for C_{FF},

$$C_{FF} = \frac{11.14}{(R_{TOP})(f_{SW})} \quad (42)$$

Choose the feed-forward resistor, R_{FF}, to set the condition

$$f_{CO} = \frac{1}{7(2\pi)(R_{FF})(C_{FF})} \quad (43)$$

Simplifying and solving for R_{FF},

$$R_{FF} = \frac{0.227}{(f_{SW})(C_{FF})} \quad (44)$$

SETTING THE SOFT START PERIOD

The ADP1821 uses an adjustable soft start to limit the output voltage ramp-up period, limiting the input inrush current. The soft start is set by selecting the capacitor, C_{SS}, from SS to GND.

The ADP1823 charges C_{SS} to 0.8 V through an internal resistor. The voltage on C_{SS} while it is charging is

$$V_{CSS} = 0.8\ V\left(1 - e^{\frac{t}{RC_{SS}}}\right) \quad (45)$$

where R is the internal 100 kΩ resistor. The soft-start period, t_{SS}, is achieved when V_{CSS} = 0.6 V or

$$0.6\ V = 0.8\ V\left(1 - e^{\frac{t_{SS}}{100\ k\Omega(C_{SS})}}\right) \quad (46)$$

or

$$\frac{t_{SS}}{100\ k\Omega(C_{SS})} = -1n\left(1 - \frac{0.6\ V}{0.8\ V}\right) = 1.386 \quad (47)$$

Solving for C_{SS} and combining constants,

$$C_{SS} = (7.213 \times 10^{-6})t_{SS} \quad (48)$$

SYNCHRONIZING THE CONVERTER

The dc-to-dc converter switching can be synchronized to an external signal. This allows multiple ADP1821 converters to be operated at the same frequency to prevent frequency beating or other interactions.

To synchronize the ADP1821 switching to an external signal, drive the sync input with the synchronizing signal. The ADP1821 can only synchronize up to 2× the nominal oscillator frequency. If the frequency is set to 300 kHz (FREQ connected to GND), it can synchronize up to 600 kHz. If the frequency is set to 600 kHz (FREQ connected to VCC), it can synchronize to 1.2 MHz.

The high-side MOSFET turn-on follows the rising edge of the sync input by approximately 320 ns. To prevent erratic switching frequency make sure that the falling edge of the sync input signal does not coincide with the falling edge of the dc-dc converter switching or

$$D_{SYNC} \neq [(320ns)(f_{SW})] + \frac{V_{OUT}}{V_{IN}} \quad (49)$$

where:
D_{SYNC} is the duty cycle of the synchronization waveform.
f_{SW} is the synchronized switching frequency.

Make sure that in all combinations of frequency, input, and output voltages that the sync input fall time does not align with the dc-to-dc converter fall time.

APPLICATION CIRCUITS

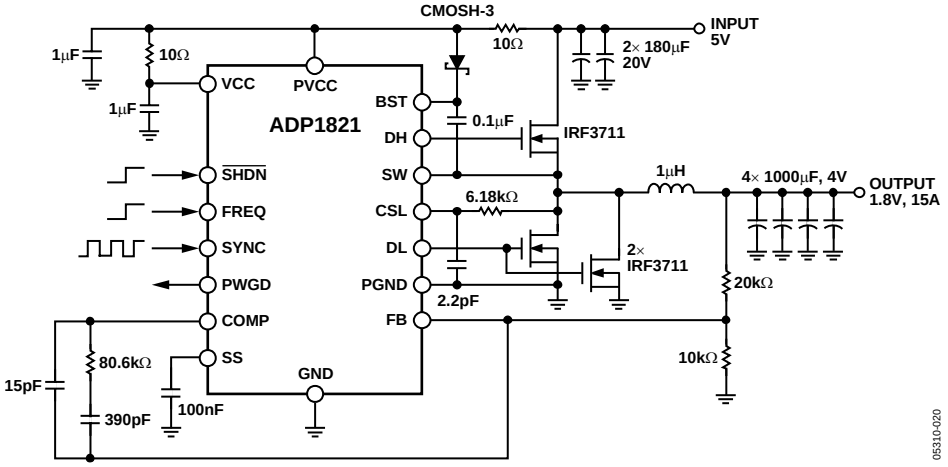


Figure 17. Typical Application Circuit, 5 V Input

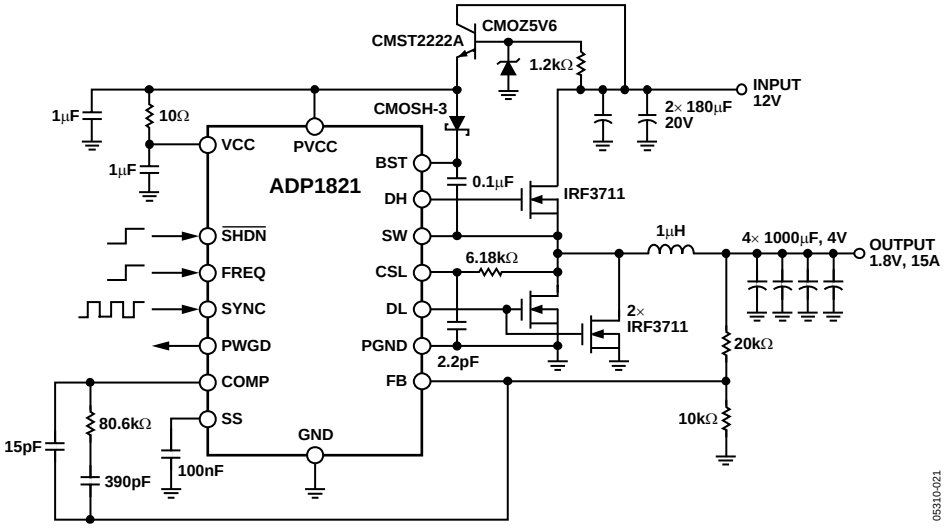
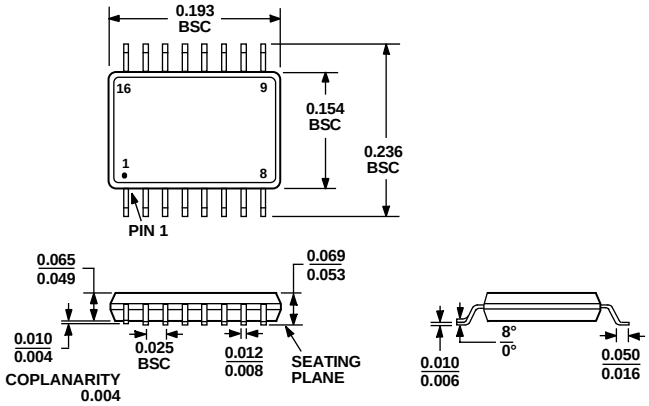


Figure 18. Typical Application Circuit, 12 V Input,
FREQ = SYNC = GND, $\overline{SHDN}$ = VCC, 5 A Load Current,
T_A = 25°C, Unless Otherwise Specified

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-137-AB

Figure 19. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADP1821ARQZ-R7[1]	–40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16

[1] Z = Pb-free part.

NOTES

NOTES

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