FET Drive Simple Sequencers™

Preliminary Technical Data

ADM6819/ADM6820

FEATURES

- Single Chip Enables Power Supply Sequencing of two supplies
- On Board Charge Pump Fully enhances N Channel FET
- Adjustable Primary Supply Monitor monitors down to 0.61V
- Delay from Primary Supply Good to Secondary Supply Enabled
  - Fixed 300ms delay (ADM6819)
  - Capacitor Adjustable Delay (ADM6820)
- Logic / Analog Driven ENABLE Input (ADM6819)
- -40°C to +125°C Operating Range
- Packaged in small 6 Lead SOT-23 Package
- Pin for pin compatible with MAX6819/MAX6820

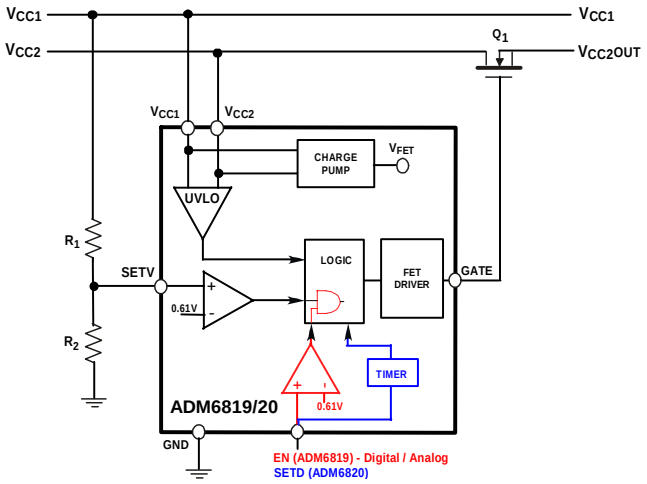
APPLICATIONS

- Multi-Voltage Systems
- Dual Voltage Microprocessors/FPGAs/ASICs/DSPs/ Network Processors
- Telecoms and Datacom s Systems
- PC/Server Applications

GENERAL DESCRIPTION

The ADM6819 and ADM6820 are simple power supply sequencers with FET drive capability for enhancing N Channel MOSFETs. These devices can monitor a primary supply voltage and enable/disable an external N-channel FET for a secondary supply. The ADM6819 has the ability to monitor two supplies. Where more than two voltages require sequencing multiple ADM6819/20 devices can be cascaded to achieve this. The devices operate over a supply range of 2.7V to 5.5V.

Functional Block Diagram



An internal comparator monitors the primary supply using the VSET pin. The input to this comparator is externally set via a resistor divider from the primary supply. When the voltage at the VSET pin rises above the comparator threshold, the secondary supply FET will be enhanced by an internal charge pump on the GATE output. The ADM6819 features an Enable (EN) pin which is fed to the input of an additional comparator and reference circuit. This pin can be used as a digital enable or a secondary power good comparator to monitor a second supply and only enable the GATE if both supplies are valid. When both the internal comparators inputs are above the threshold, a fixed 300ms timeout will occur before the GATE is driven high and the secondary supply is enabled.

The ADM6820 has only one comparator which is on the SETV pin and features a timeout period which is adjustable via a single external capacitor on the SETD pin.

The ADM6819/20 are packaged in small 6-pin SOT-23 packages.

Rev.PrH

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ADM6819/ADM6820—SPECIFICATIONS

Table 1. V_{CC1} or V_{CC2} = +2.7V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = 25°C. (Note1)

Parameter	Min	Typ	Max	Units	Conditions
V_{CC1} , V_{CC2} Pins					(Note 2)
Operating Voltage Range, V_{CC1} or V_{CC2}	2.7		5.5	V	V_{CC1} or V_{CC2} must be >2.7V.
V_{CC1} or V_{CC2} Supply Current, I_{CC}		350	500	µA	V_{CC1} = V_{CC2} = +3.3V
V_{CC1} or V_{CC2} Disable Mode Current		250		µA	V_{CC1} = V_{CC2} = +3.3V, EN = GND
V_{CC1} or V_{CC2} Slew Rate (Note 3)	6			V/s	ADM6819
	$1.2/t_{DEL:AY}$			V/s	ADM6820 (Note 4)
Undervoltage Lockout, V_{UVLO}	2.4	2.525	2.65	V	Vcc Falling
SETV Pin					
SETV Threshold, V_{TH}	0.594	0.610	0.624	V	V_{SETV} rising, enables GATE
SETV Input Current		10	360	nA	(Note 3)
SETV Threshold Hysteresis		-1		%	V_{SETV} falling, disables GATE
SETV to GATE Delay, t_{DELAY}	240	300	340	ms	V_{SETV} > V_{TH} ; V_{EN} > V_{TH} (ADM6819)
SETD Pin					
SETD Ramp Current, I_{SETD}	400	500	600	nA	ADM6820; V_{CC1} or V_{CC2} > +2.5V
SETD Voltage, V_{SETD}	1.295	1.326	1.357	V	ADM6820; V_{CC1} or V_{CC2} > +2.5V
GATE Pin					
GATE Turn-On Time, t_{ON}	0.5	1.5	10	ms	C_{GATE}=1500pF; V_{CC2} = +3.3V; V_{GATE}= +7.8V
GATE Turn-Off Time, t_{OFF}		30		µs	C_{GATE}=1500pF; V_{CC2} = +3.3V; V_{GATE}= +0.5V
GATE Voltage, V_{GATE}	4.5	5.5	6.0	V	With respect to V_{CCx} (Note5); R_{GATE} > 50 MΩ to V_{CCx}
	4.0	5.0	6	V	With respect to V_{CCx} (Note5); R_{GATE} > 5 MΩ to V_{CCx}
	8.5	9.5	10.5	V	With respect to V_{CCx} (Note6); R_{GATE} > 50 MΩ to V_{CCx}
	8	9	10	V	With respect to V_{CCx} (Note6); R_{GATE} > 5 MΩ to V_{CCx}
ENABLE Pin					
EN Input Voltage Low, V_{IL}			0.4	V	V_{CC1} or V_{CC2} must be >2.7V.
EN Input Voltage High, V_{IH}	2.0			V	V_{CC1} or V_{CC2} must be >2.7V.

NOTES:
[1] 100% Production Tested at T_A = +25°C. Specifications over temperature limit are guaranteed by design.
[2] Either V_{CC1} or V_{CC2} must be >2.7V
[3] Guaranteed by design, not production tested.
[4] $_{DELAY}$ (s) = 2.48 X 10^6 X C_{SET}.
[5] Highest supply pin is represented by V_{CCX} = 2.7V
[6] Highest supply pin is represented by V_{CCX} = 5.5V

Absolute Maximum Ratings

Table 2. ADM6819/ADM6820 Absolute Maximum Ratings

Parameter	**Rating**
V_{CC1} , V_{CC2} Pins	-0.3V to 6.0V
SETV, SETD, EN Pins	-0.3V to 30V
Gate Pin	-0.3V to 30V
Power Dissipation	TBD
Storage Temperature	–65°C to +150°C
Operating Temperature Range	–40°C to +125°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

THEORY OF OPERATION

The ADM6819/20 provide local voltage sequencing in multi-supply systems. Figure 1 and Figure 2 show typical application diagrams for these devices.

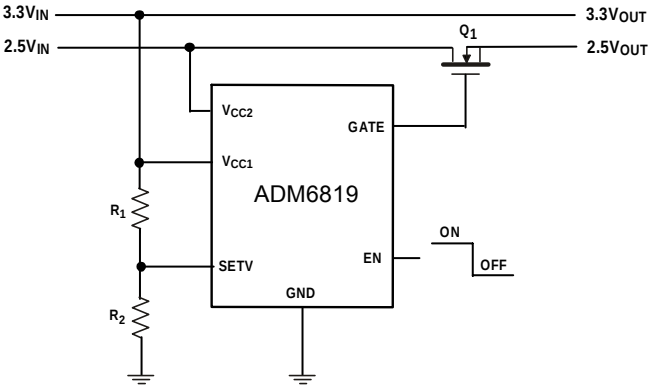


Figure 1. ADM6819 Applications Diagram

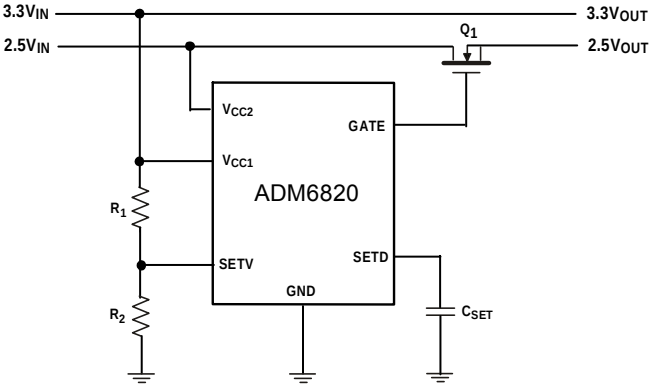


Figure 2. ADM6820 Applications Diagram

The ADM6819/20 is designed to control the N-channel FET in the secondary power path to enable the secondary supply only when the primary supply is above the desired threshold. The GATE pin will be held low while both VCC1 and VCC2 are under the undervoltage threshold, ensuring the FET held off. When either VCC1 or VCC2 is above UVLO and the primary supply is above the desired level dictated by the resistor divider to the VSET pin, the external FET is driven on after the delay has expired. An internal charge pump enhances the external FET. A FET with a low drain-source resistance and low VTH should be chosen to reduce voltage drop across the drain-source of the FET when on. Either supply may act as the primary source provided that VCC1 or VCC2 is greater that 2.7V. A decoupling capacitor of typically 100nF should be used on whichever Vcc is the main supply

.SETV

The ADM6819/ADM6820 will enable a supply after a monitored supply voltage exceeds a programmed threshold. This threshold is programmed by a R1/R2 resistor divider on the SETV pin. Once the voltage on this SETV pin exceeds the threshold of 0.618V, the FET will be switched on after the delay timer has expired. On the ADM6820 this delay is programmable using a capacitor on the SETD pin and on the ADM6819 this delay is fixed at 300ms and the Enable pin must also be valid high to begin the timer. The required turn-on voltage is calculated by the following equation:
R1 = R2 ((VTRIP / VTH) – 1)
Where VTRIP is the minimum turn-on voltage at the supply being monitored and VTH = 0.618V. High value resistor can be used since SETV input current is approximately 10nA.

EN

The ADM6819 has an Enable pin which is connected to the input of a second comparator identical to that on VSET pin. This pin can be used as a digital input provided the signal Vol is below 0.6V. Alternatively the Enable input can be used to validate a second supply. The fixed 300ms timer will not begin to count until both the SETV pin and the EN pin are above the threshold and so the output will not be enabled until after this timer has expired.

GATE

The internal charge pump is capable of driving the gate of an N-Channel MOSFET with no external capacitors. This will ensure that the MOSFET is enhanced to provide a minimum RDS on the MOSFET, thus reducing the voltage drop across the FET. This charge pump is designed to drive the high impedance capacitive load of a MOSFET gate input. The GATE output should not be loaded resistively as this will reduce the gate drive capability. During Undervoltage lockout the GATE is held to GND.

SETD

The ADM6820 features a capacitor adjustable sequencing delay. A capacitor connected to the SETD pin will determine the length of the sequencing delay. The sequencing delay can be calculated as follows:

TDELAY (s) = 2.48 X 106 X CSET

The ADM6819 has a fixed 300ms delay.

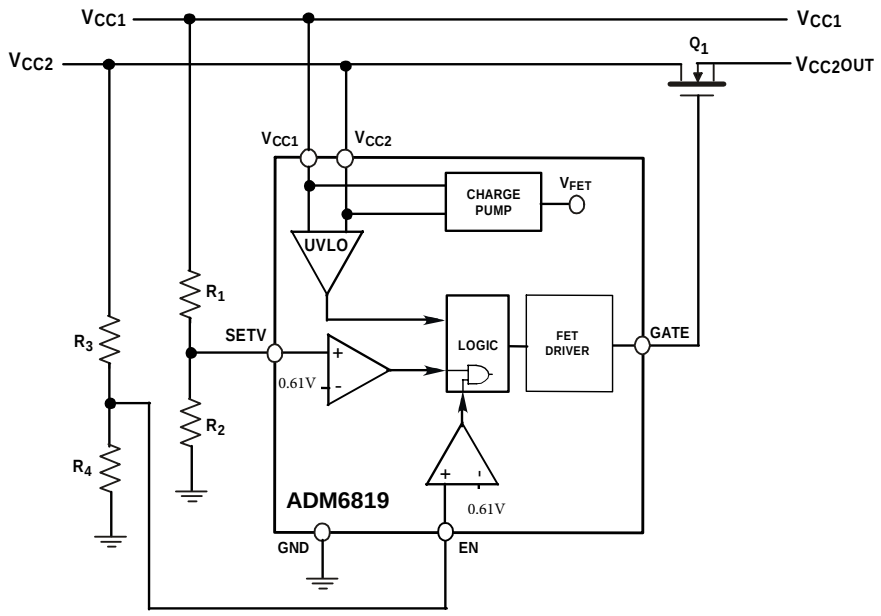


Figure 3. ADM6819 Solution for Validating 2 Supplies before Sequencing

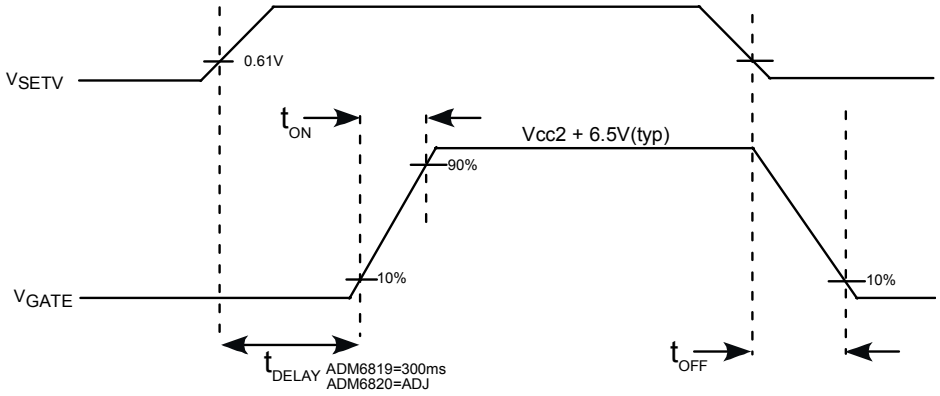


Figure 4. ADM6819/ADM6820 Timing Diagram using SETV for Sequencing

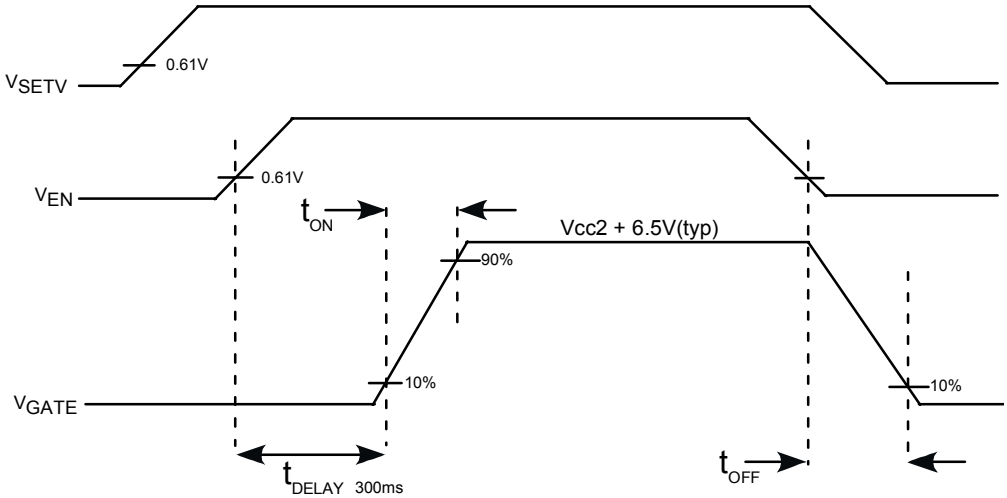


Figure 5. ADM6819 Timing Diagram using both EN and SETV for Sequencing

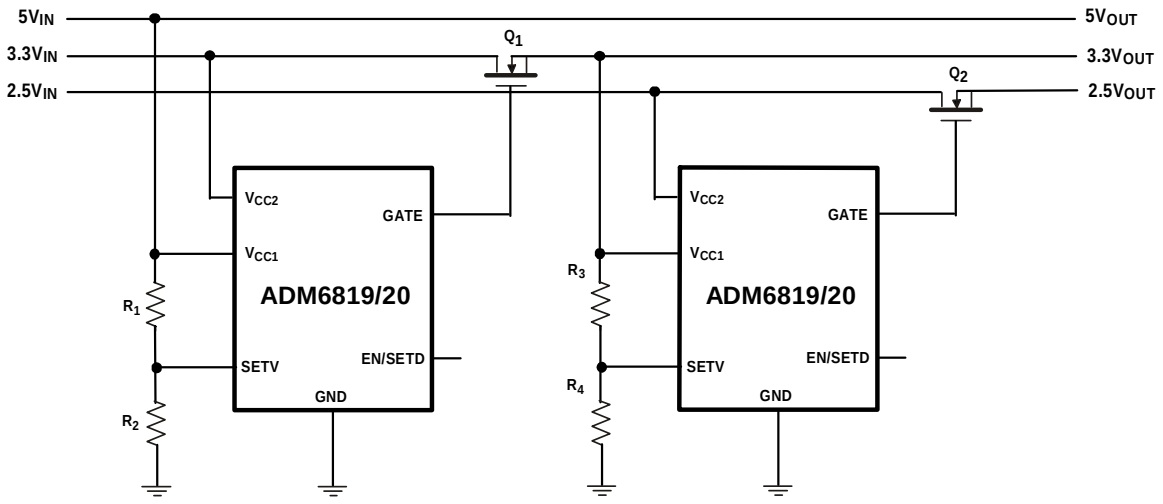
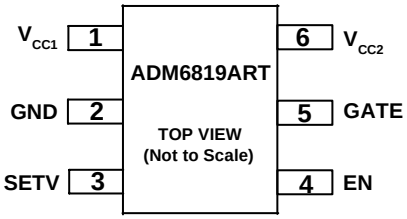
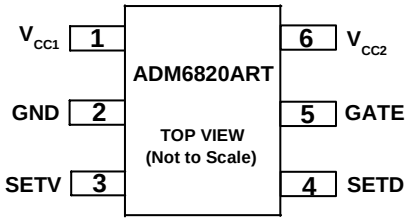


Figure 6. ADM6819/ADM6820 Solution for Sequencing Three Supply Rails

PIN CONFIGURATIONS





PIN FUNCTIONAL DESCRIPTIONS

Pin Number		Name	Description
ADM6819	ADM6820		
1	1	V_{CC1}	Supply Voltage 1. Either V_{CC1} or V_{CC2} must be greater that the UVLO to enable external FET Drive.
2	2	GND	Chip Ground Pin.
3	3	SETV	Sequenced Threshold Set. Connect to an external resistor divider to set the V_{CC1} threshold that enables GATE turn –on. The internal reference is 0.61V.
4	-	EN	Active-High Enable. GATE drive is enabled t_{DELAY} after EN is driven high. GATE drive is immediately disabled when EN is driven low. Connect to the higher of V_{CC1} or V_{CC2} if not used. This pin is internally identical to SETV (0.61V Threshold) and can therefore also be used as a second supply monitor, enabling two supplies to be validated before sequencing begins.
-	4	SETD	GATE Delay Set Input. Connect an external capacitor from SETD to GND to adjust the delay from SETV > V_{TH} to GATE turn-on. T_{DELAY} (s) = 2.484 X 10^6 X C_{SET} (F).
5	5	GATE	GATE Drive Output. GATE drives an external N-channel FET to connect V_{CC2} to the load. GATE drive enables tdelay after SETV exceeds V_{TH} and ENABLE is driven high. GATE drive is immediately disabled when SETV drops below V_{TH} or ENABLE is driven low. When enabled, an internal charge pump drives the GATE above V_{CCX} to fully enhance the external n-channel FET.
6	6	V_{CC2}	Supply Voltage 2. Either V_{CC1} or V_{CC2} must be greater that the UVLO to enable external FET Drive.

OUTLINE DIMENSIONS

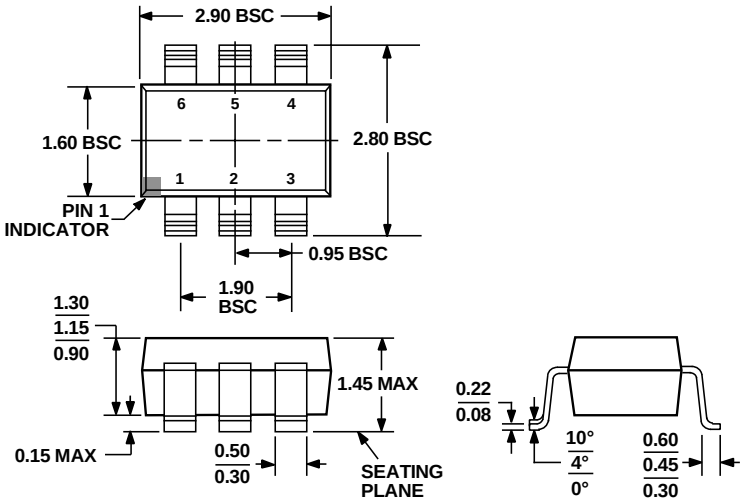


Figure 4. 6-Lead SOT-23 Package (RJ-6)—Dimensions shown in millimeters

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table 3. Ordering Guide

Model	Temperature Range	Package Description	Package Option	Branding
ADM6819WRJZ-REEL7	−40°C to +125°C	6-Lead SOT-23	RJ-6	M2R
ADM6820WRJZ-REEL7	−40°C to +125°C	6-Lead SOT-23	RJ-6	**M2S**

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