

FEATURES

- 1 local and 1 remote temperature channel
- $\pm 1.5^{\circ}\text{C}$ accuracy on local and remote channels
- Automatic series resistance cancellation on remote
- Temperature channels $> 1\text{ k}\Omega$
- Fast (up to 64 measurements per second)
- SMBus 2.0, 1.1, and 1.0 compliant
- SMBus address input/LOCATION input to UDID
- Programmable over-/undertemperature limits
- Programmable fault queue
- SMBusALERT output
- Fail-safe overtemperature comparator output
- Fan speed (RPM) controller

Look-up table for temperature-to-fan-speed control

Linear and discrete options for look-up table

FAN_FAULT output

THERM input, used to time $\overline{\text{PROCHOT}}$ assertions

REF input, used as reference for THERM ($\overline{\text{PROCHOT}}$)

3 V to 5.5 V supply

Small 16-lead QSOP package

APPLICATIONS

Desktop and notebook PCs

Embedded systems

Telecommunications equipment

LCD projectors

FUNCTIONAL BLOCK DIAGRAM

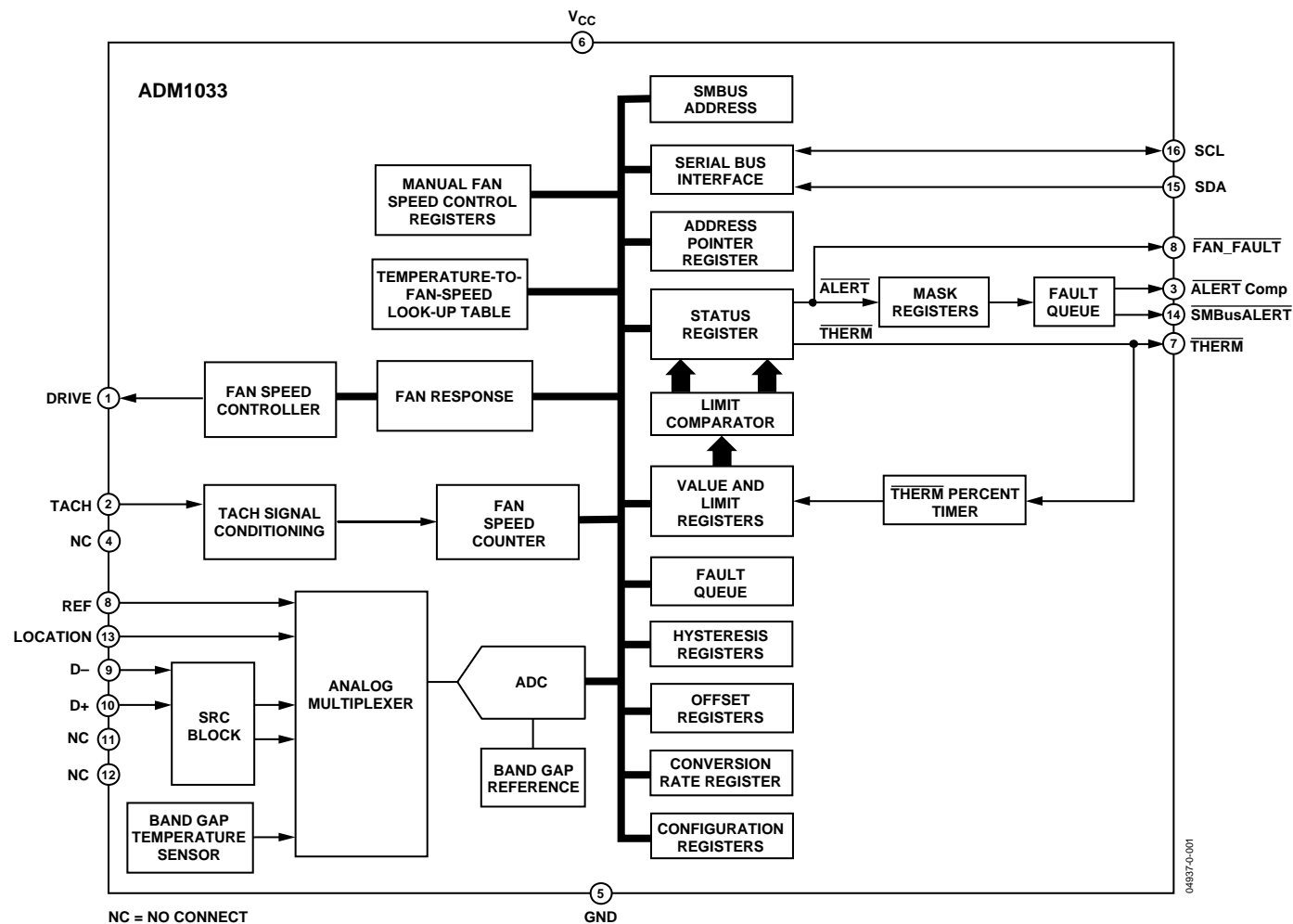


Figure 1.

Rev. 0

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REVISION HISTORY

8/04—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADM1033 is a remote and local temperature sensor and fan controller. Its remote channel accurately monitors the temperature of a remote thermal diode, which can be a discrete 2N3904/6 or located on a microprocessor die. The device can monitor its own ambient temperature as well.

The ADM1033 is also used to monitor and control the speed of a cooling fan. The user can program a target fan speed, or use the look-up table to input a temperature-to-fan speed profile. The look-up table can be configured to run the fan at discrete

speeds (discrete mode) or to ramp the fan speed with temperature (linear mode).

The ADM1033 communicates over a 2-wire SMBus 2.0 interface. An 8-level LOCATION input allows the user to choose between SMBus 1.1 and SMBus 2.0.

The ALERT output indicates error conditions. In addition, the THERM I/O signals overtemperature as an output and times THERM assertions as an input. Pin 8 can be configured as a reference input for the THERM (PROCHOT) input.

SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX} , $V_{CC} = V_{MIN}$ to V_{MAX} , unless otherwise noted.¹

Table 1.

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
POWER SUPPLY					
Supply Voltage, V _{CC} ²	3.0	3.3	3.6	V	Interface inactive, ADC active Standby mode
Supply Current, I _{CC}			3	mA	
			900	μA	
Undervoltage Lockout Threshold		2.5		V	
Power-On Reset Threshold	1		2.4	V	
TEMPERATURE-TO-DIGITAL CONVERTER					
Internal Sensor Accuracy	−4	±1	±2	°C	20°C ≤ T _A ≤ 60°C
			+2	°C	−40°C ≤ T _A ≤ +100°C
Resolution		0.03125		°C	
External Diode Sensor Accuracy		±0.5	±1	°C	−40°C ≤ T _D ≤ +100°C; T _A = +40°C
		±1		°C	−40°C ≤ T _D ≤ +100°C; +20°C ≤ T _A ≤ +60°C
	−3		+2	°C	−40°C ≤ T _D ≤ +100°C; −40°C ≤ T _A ≤ +100°C
Resolution		0.03125		°C	
Remote Sensor Source Current		85		μA	High level
		34		μA	Mid level
		5		μA	Low level
Series Resistance Cancellation			1000	Ω	
Power Supply Sensitivity		±1		%/V	
Conversion Time (Local Temperature)		11		ms	Averaging enabled
Conversion Time (Remote Temperature)		32		ms	Averaging enabled
Total Conversion Time		43		ms	Averaging enabled
OPEN-DRAIN DIGITAL OUTPUTS (ALERT, THERM, FAN_FAULT DRIVE)					
Output Low Voltage, V _{OL}			0.4	V	I _{OUT} = −6.0 mA; V _{CC} = +3 V
High Level Output Leakage Current, I _{OH}		0.1	1	μA	V _{OUT} = V _{CC} ; V _{CC} = 3 V
DIGITAL INPUT LEAKAGE CURRENT (TACH)					
Input High Current, I _{IH}	−1			μA	V _{IN} = V _{CC}
Input Low Current, I _{IL}			1	μA	V _{IN} = 0
Input Capacitance, C _{IN}		7		pF	
DIGITAL INPUT LOGIC LEVELS (TACH)					
Input High Voltage, V _{IH}	2.0		5.5	V	
Input Low Voltage, V _{IL}	−0.3		+0.8	V	
Hysteresis		500		mV p-p	
OPEN-DRAIN SERIAL DATA BUS OUTPUT (SDA)					
Output Low Voltage, V _{OL}			0.4	V	I _{OUT} = −6.0 mA; V _{CC} = +3 V
High Level Output Leakage Current, I _{OH}		0.1	1	μA	V _{OUT} = V _{CC}
SERIAL BUS DIGITAL INPUTS (SCL, SDA)					
Input High Voltage, V _{IH}	2.1			V	
Input Low Voltage, V _{IL}			0.8	V	
Hysteresis		500		mV	
ANALOG INPUTS (LOCATION, REF)					
Input Resistance	80	125	160	kΩ	

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
TACHOMETER ACCURACY					
Fan Speed Measurement Accuracy			±4	%	
AGTL + INPUT (THERM)					
Input High Level		0.75 × REF		V	
Input Low Level			0.4	V	
SERIAL BUS TIMING ³					See Figure 2
Clock Frequency, f_{SCLK}			400	kHz	
Glitch Immunity, t_{SW}		50		ns	
Bus Free Time, t_{BUF}	1.3			μs	
Start Setup Time, $t_{SU:STA}$	0.6			μs	
Start Hold Time, $t_{HD:STA}$	0.6			μs	
Stop Condition Setup Time, $t_{SU:STO}$	0.6			μs	
SCL Low Time, t_{LOW}	1.3			μs	
SCL High Time, t_{HIGH}	0.6			μs	
SCL, SDA Rise Time, t_r			1000	ns	
SCL, SDA Fall Time, t_f			300	ns	
Data Setup Time, $t_{SU:DAT}$	100			ns	
Detect Clock Low Timeout, $t_{TIMEOUT}$	25		35	ms	See Note 4

¹Typicals are at $T_A = 25^\circ\text{C}$ and represent most likely parametric norm. Standby current typ is measured with $V_{CC} = 3.3\text{ V}$. Timing specifications are tested at logic levels of $V_{IL} = 0.8\text{ V}$ for a falling edge and $V_{IH} = 2.1\text{ V}$ for a rising edge.

²Operation at 5.5 V is guaranteed by design, not production tested.

³Guaranteed by design, not production tested.

⁴SMBus timeout disabled by default. See the SMBus Timeout section for more information.

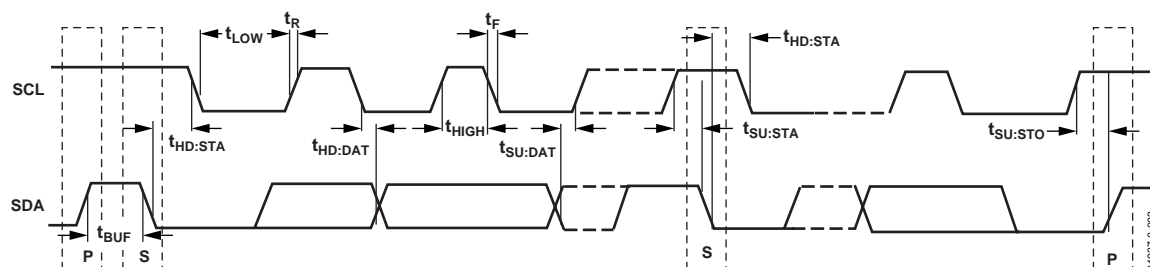


Figure 2. Serial Bus Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Value
Positive Supply Voltage (V_{CC})	–0.3 V to +6.5 V
Voltage on Any Input or Output Pin except FAN_FAULT and LOCATION	–0.3 V to +6.5 V
Voltage on FAN_FAULT ¹	V_{CC}
Voltage on LOCATION	$V_{CC} + 0.3V$
Input Current at Any Pin	± 20 mA
Maximum Junction Temperature (T_{Jmax})	150°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow Peak Temperature	220°C
ESD Rating—All Pins	1500 V

¹ During power-up, the voltage on FAN_FAULT should not be higher than V_{CC} .

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

16-Lead QSOP Package:

$\theta_{JA} = 150^{\circ}\text{C/W}$, $\theta_{JC} = 39^{\circ}\text{C/W}$

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

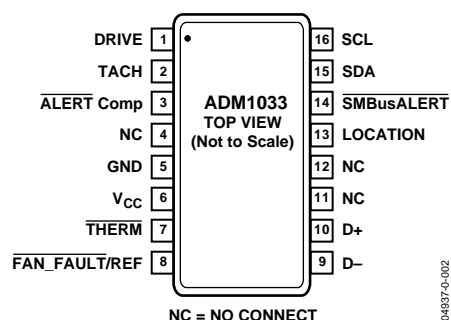


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DRIVE	DRIVE Pin Drives the Fan. Open-drain output. Requires a pull-up resistor.
2	TACH	Fan Speed Measurement Input. Connects to the fan's TACH output to measure the fan speed.
3	ALERT Comp	Open-Drain Active Low Output. Asserts low whenever a measurement goes outside its programmed limits, if not masked. Automatically goes high again when the measured parameter falls back within its limits.
4	NC	No Connect.
5	GND	Ground for Analog and Digital Circuitry.
6	V _{CC}	Power. Can be powered by 3.3 V standby power, if monitoring in low power states is required.
7	THERM	Can be configured as an overtemperature interrupt output, or as an input to monitor PROCHOT output of an INTEL CPU. A timer measures assertion times on the THERM pin (either input or output).
8	FAN_FAULT/REF	FAN_FAULT: Open-Drain Output. Asserts low whenever the fan stalls. REF: Analog Input Reference for THERM input.
9	D-	Cathode Connection for the Thermal Diode or Diode-Connected Transistor.
10	D+	Anode Connection for the Thermal Diode or Diode-Connected Transistor.
11	NC	No Connect.
12	NC	No Connect.
13	LOCATION	8-Level Analog Input. Used to determine the correct SMBus version and the SMBus address (in fixed-and-discoverable mode), and to set the LLL bits in the UDID (in ARP-capable mode).
14	SMBusALERT	Open-Drain Output. Alerts the system in the case of out-of-limit events such as overtemperature. Can be reset only with software.
15	SDA	Serial Bus Bidirectional Data. Connects to the SMBus master's data line. Requires a pull-up resistor, if one is not provided elsewhere in the system.
16	SCL	Serial SMBus Clock Input. Connects to the SMBus master's clock line. Requires a pull-up resistor, if one is not provided elsewhere in the system.

TYPICAL PERFORMANCE CHARACTERISTICS

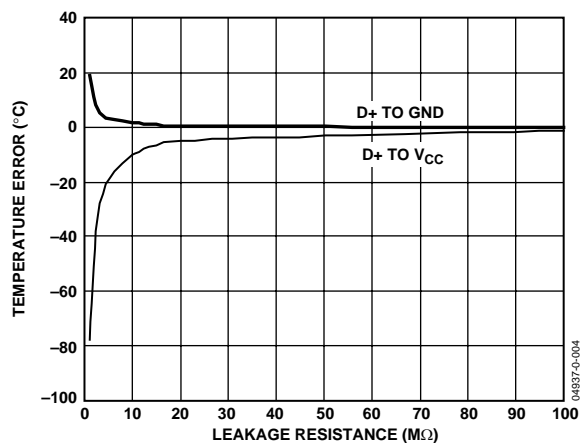


Figure 4. Temperature Error vs. PCB Track Resistance, DXP to GND and VCC

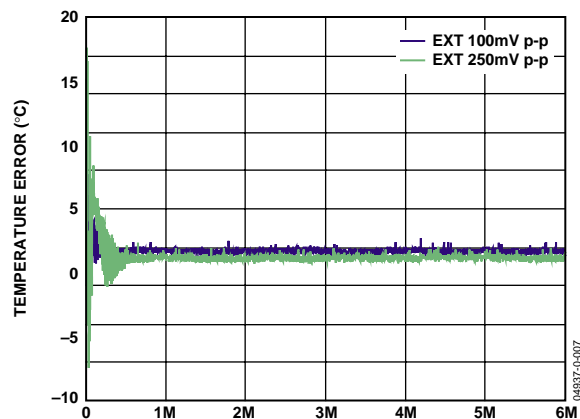


Figure 7. Remote Temperature Error vs. Power Supply Noise Frequency

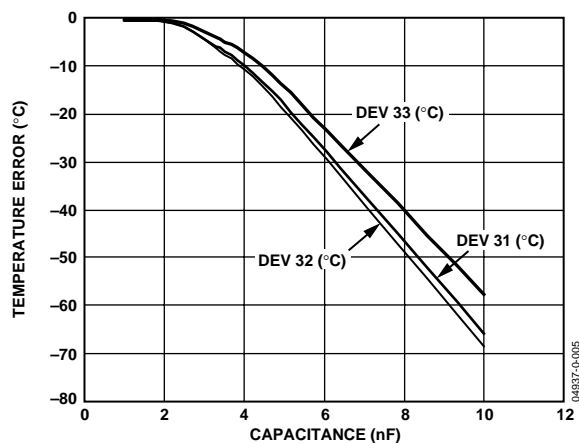


Figure 5. Remote Temperature Error vs. D+, D- Capacitance

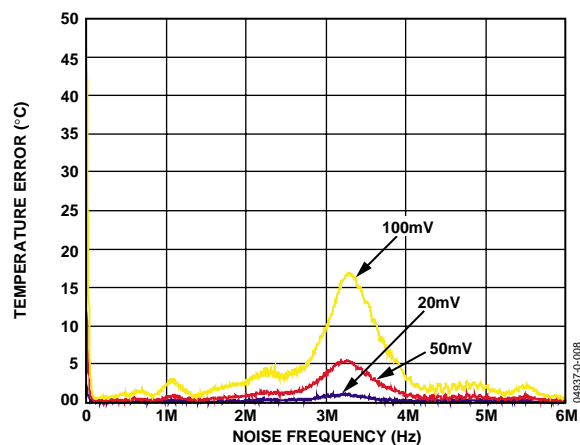


Figure 8. Remote Temperature Error vs. Common-Mode Noise Frequency Coupled on D+ and D-

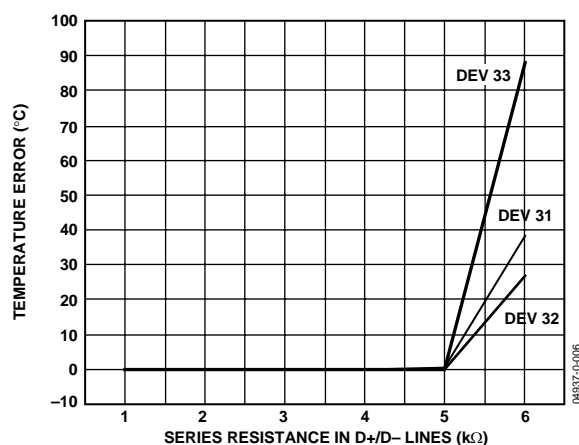


Figure 6. Remote Temperature Error vs. Series Resistance on D+ and D-

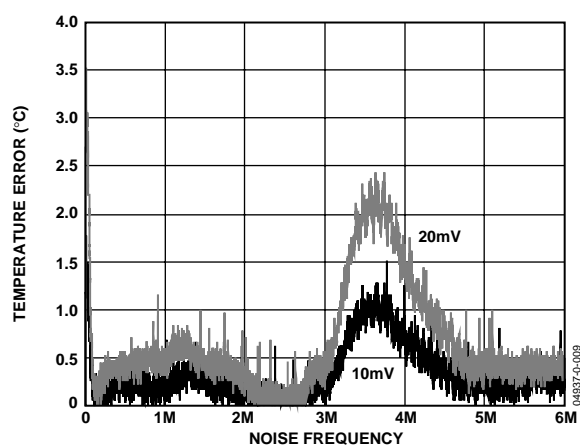


Figure 9. Remote Temperature Error vs. Differential-Mode Noise Frequency Coupled on D+ and D-

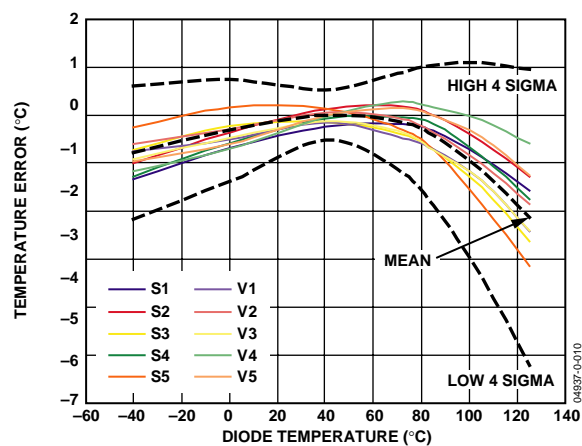


Figure 10. Remote Temperature Error vs. Actual Diode Temperature

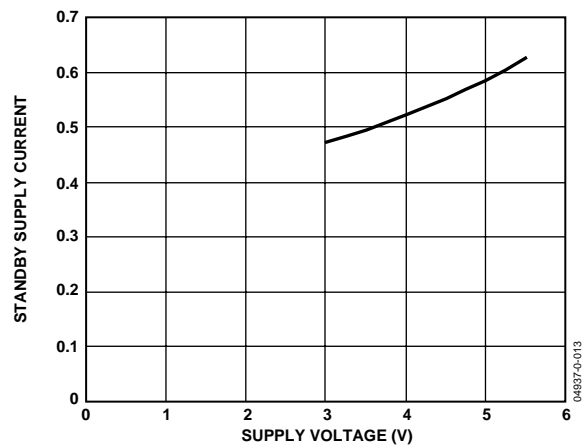


Figure 13. Standby Supply Current vs. Supply Voltage

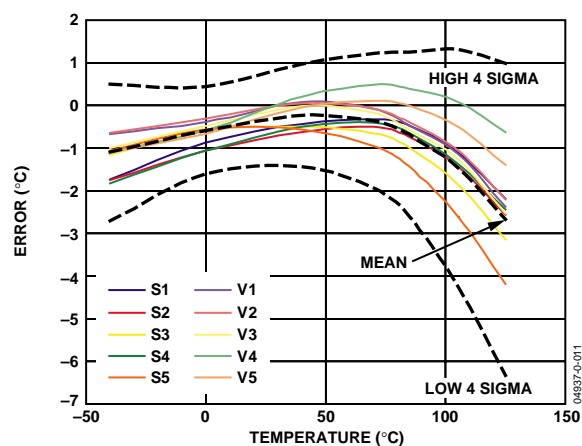


Figure 11. Local Temperature Error vs. Actual Temperature

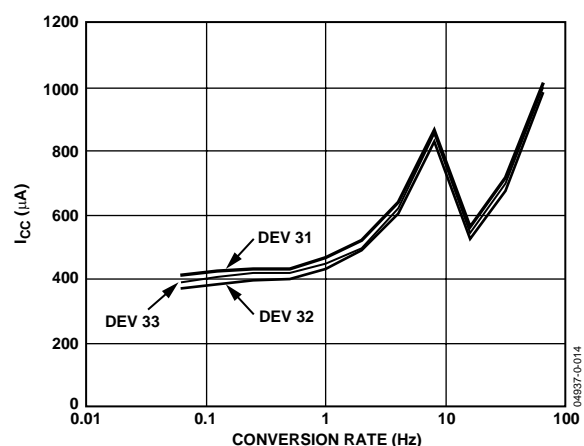


Figure 14. Supply Current vs. Conversion Rate

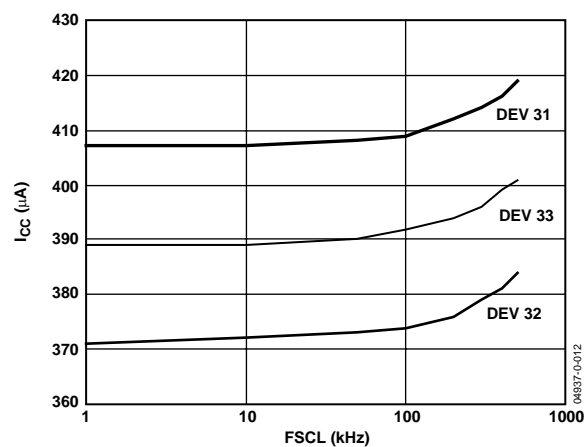


Figure 12. Standby Supply Current vs. SCLK Frequency

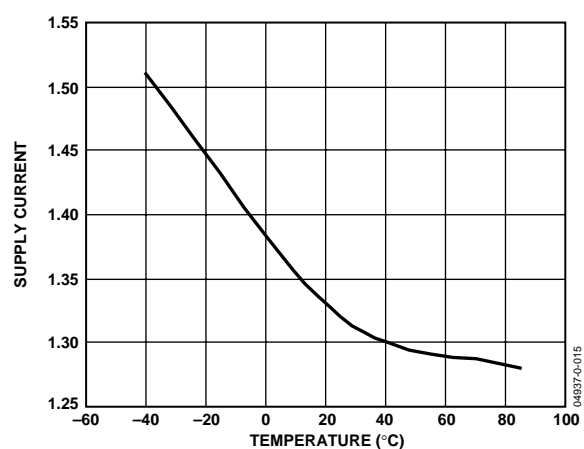


Figure 15. Supply Current vs. ADM1033 Temperature

FUNCTIONAL DESCRIPTION

The ADM1033 is a local and remote temperature monitor and fan controller used in a variety of applications, including microprocessor-based systems. The device accurately monitors remote and ambient temperature and uses that information to quietly control the speed of a cooling fan. Whenever the fan stalls, the device asserts a `FAN_FAULT` output.

The ADM1033 has a `THERM` I/O. As an input, this measures assertions on the `THERM` pin. As an output, it asserts a low signal to indicate when the measured temperature exceeds the programmed `THERM` temperature limits. The ADM1033 communicates over an SMBus 2.0 interface. Its `LOCATION` input determines which version of SMBus to use, as well as the SMBus address (in fixed-and-discoverable mode), and the `LOCATION` bits in the UDID (in ARP-capable mode).

INTERNAL REGISTERS

Table 4 gives a brief description of the ADM1033's principal internal registers. For more detailed information on the function of each register, refer to .

SERIAL BUS INTERFACE

The ADM1033 communicates with the master via the 2-wire SMBus 2.0 interface. It supports two SMBus 2.0 versions, determined by the value of the `LOCATION` input resistors.

The first version is fully ARP-capable. This means that it supports address resolution protocol (ARP), allowing the master to dynamically address the device on power-up. It responds to ARP commands such as "Prepare to ARP."

The second SMBus version, fixed-and-discoverable, is backward-compatible with SMBus 1.0 and 1.1. In this mode, the ADM1033 powers up with a fixed address, which is determined by the state of the `LOCATION` pin on power-up. Note: when using the ADM1033, addresses 0xC2 and 0xCA should not be used by any other device on the bus.

LOCATION INPUT

The `LOCATION` input is a resistor divider input. It has multiple functions and can specify the following: the SMBus version (in fixed-and-discoverable or ARP-capable modes); the SMBus address (in fixed-and-discoverable mode); and the LLL bits (in UDID in ARP-capable mode).

The voltage of this 8-level input is set by a potential divider. The voltage on `LOCATION` is sampled on power-up and digitized by the on-chip ADC to determine the `LOCATION` input value. Because the `LOCATION` input is sampled only at power-up, changes made while power is applied have no effect.

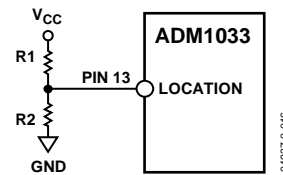


Figure 16. Bootstrapping the `LOCATION` Input

SMBus 2.0 ARP-CAPABLE MODE

In ARP-capable mode, the ADM1033 supports such features as address resolution protocol (ARP) and unique device identifier (UDID). The UDID is a 128-bit message that describes the ADM1033's capabilities to the master. The UDID also includes a vendor-specific ID for functionally equivalent devices.

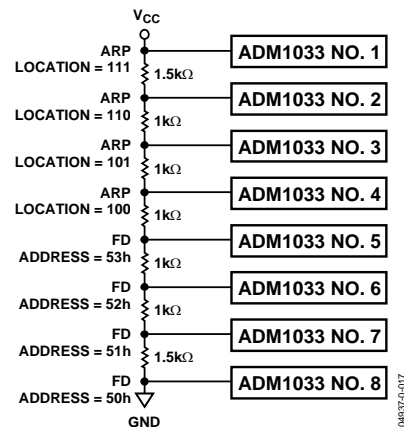


Figure 17. Setting Up Multiple ADM1033 Addresses

In SMBus 2.0 mode, this vendor-specific ID is generated by an on-chip random number generator. This should enable two adjacent ADM1033s in the same system to power-up with a different vendor-specific ID, allowing the master to identify the two separate ADM1033s and assign a different address to each. The state of the `LOCATION` input on power-up is also reflected in the UDID. This is useful when there are more than one ADM1033 in the system, so the master knows which one it is communicating with. The UDID values are listed in Table 6.

The SMBus 2.0 master issues both general and directed ARP commands. A general command is directed at all ARP devices. A directed command is targeted at a single device, once an address has been established. The PEC byte must be used for ARP commands (refer to Packet Error Checking (PEC)). The ADM1033 responds to the following commands:

- Prepare to ARP (general)
- Reset device (general and directed)
- Get UDID (general and directed)
- Assign address (general)

Table 4. Internal Register Descriptions

Register	Description
Configuration	Provides control and configuration of various functions on the device.
Conversion Rate	Determines the number of measurements per second completed by the ADM1033.
Address Pointer	Contains the address that selects one of the other internal registers. When writing to the ADM1033, the first byte of data is always a register address, which is written to the address pointer register.
Status	Provides the status of each limit comparison.
Interrupt Mask	Allows the option to mask $\overline{\text{ALERT}}$ s due to particular out-of-limit conditions.
Value and Limit	Stores the results of temperature and fan speed measurements, along with their limit values.
Offset	Allows the local and remote temperature channel readings to be offset by a twos complement value written to them. These values are automatically added to the temperature values (or subtracted from them if negative). This allows the systems designer to optimize the system, if required, by adding or subtracting up to 15.875°C from a temperature reading.
$\overline{\text{THERM}}$ Limit and Hysteresis	Contains the temperature value at which $\overline{\text{THERM}}$ is asserted and determines the level of hysteresis.
Look-Up Table	Used to program the look-up table for the fan-speed-to-temperature profile.
$\overline{\text{THERM}}$ % Otime and $\overline{\text{THERM}}$ % Limit	Reflects the state of the $\overline{\text{THERM}}$ input and monitors the duration of the assertion time of the signal as a percentage of a time window. The user can program the length of the time window.

Table 5. Resistor Ratios for Setting LOCATION Bits

Ideal Ratio R2/(R1 + R2)	R1 (k Ω)	R2 (k Ω)	Actual R2/(R1 + R2)	Error (%)	SMBus Mode	SMBus Address	UDID LLL
N/A	0	O/C	1	0	ARP ¹	N/A	111
0.8125	18	82	0.82	+0.75	ARP ¹	N/A	110
0.6875	22	47	0.6812	−0.63	ARP ¹	N/A	101
0.5625	12	15	0.5556	−0.69	ARP ¹	N/A	100
0.4375	15	12	0.4444	+0.69	FD ¹	0x53	N/A
0.3125	47	22	0.3188	+0.63	FD ¹	0x52	N/A
0.1875	82	18	0.18	−0.75	FD ¹	0x51	N/A
N/A	O/C	0	0	0	FD ¹	0x50	N/A

¹ FD denotes fixed-and-discoverable mode, ARP denotes ARP-capable mode.

Table 6. UDID Values

Bit No.	Name	Function	Value
<127:120>	Device Capabilities	Describes the ADM1033's capabilities (for instance, that it supports PEC and uses a random number address device)	11000001
<1119:112>	Version/Revision:	UDID version number (Version 1) and silicon revision identification	00001010
<111:96>	Vendor ID	Vendor ID number, assigned by the SBS Implementer's Forum or the PCI SIG	00010001 11010100
<95:80>	Device ID	Device ID	00010000 00110011
<79:64>	Interface	Identifies the protocol layer interfaces supported by the ADM1033. This represents SMBus 2.0 as the Interface version.	00000000 00000100
<63:48>	Subsystem Vendor ID	Subsystem Vendor ID = 0 (subsystem fields are unsupported)	00000000 00000000
<47:32>	Subsystem Device ID	Subsystem Device ID = 0 (subsystem fields are unsupported)	00000000 00000000
<31:0>	Vendor-Specific ID	A unique number per device. Contains the LOCATION Information (LLL) and a 16-bit random number (x). See Table 5 for information on setting the LLL bits.	00000000 00000LLL xxxxxxxx xxxxxxxx

SMBus 2.0 FIXED-AND-DISCOVERABLE MODE

The ADM1033 supports fixed-and-discoverable mode, which is backward-compatible with SMBus 1.0 and 1.1. Fixed-and-discoverable mode supports all the same functionality as ARP-capable mode, except for *assign address*—in which case it powers up with a fixed address and is not changed by the assign address call. The fixed address is determined by the state of the LOCATION pin on power-up.

SMBus 2.0 READ AND WRITE OPERATIONS

The master initiates a data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line (SDA) while the serial clock line (SCL) remains high. This indicates that an address/data stream is to follow. All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, which consist of a 7-bit address (MSB first) plus an $\overline{R/W}$ bit. The last bit determines the direction of the data transfer (whether data is written to or read from the slave device).

1. The peripheral that corresponds to the transmitted address responds by pulling the data line low during the low period before the 9th clock pulse. This pulse is known as the acknowledge bit. All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the $\overline{R/W}$ bit is a 0, the master writes to the slave device. If the $\overline{R/W}$ bit is a 1, the master reads from it.
2. Data is sent over the serial bus in sequences of nine clock pulses—eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low-to-high transition when the clock is high might be interpreted as a stop signal. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.
3. When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the tenth clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as no acknowledge. The master takes the data line low during the low period before the tenth clock pulse, then high during the tenth clock pulse to assert a stop condition.

It is not possible to mix read and write in one operation, because the type of operation is determined at the beginning and cannot be changed without starting a new operation.

To write data to one of the device data registers or read data from it, the address pointer register (APR) must be set so that the correct data register is addressed. The first byte of a write operation always contains an address that is stored in the APR. If data is to be written to the device, the write operation contains a second data byte. The second data byte is written to the register selected by the APR.

As shown in Figure 18, the device address is sent over the bus, followed by $\overline{R/W}$ set to 0. This is followed by two data bytes. The first data byte is the address of the designated internal data register, which is stored in the APR. The second data byte is the data to be written to the internal data register.

When reading data from a register there are two possibilities:

- If the ADM1033's APR value is unknown or incorrect, it must be set to the correct value before data can be read from the desired data register. To do this, perform a write to the ADM1033 as before; but this time send only the data byte containing the register. (See Figure 19.) A read operation is then performed. With the serial bus address and the $\overline{R/W}$ bit set to 1, the data byte is read from the data register. (See Figure 20.)
- If the APR is known to be already at the desired address, data can be read from the corresponding data register without first writing to the APR. In this case, Figure 19 can be omitted.

In Figure 18 to Figure 20, the serial bus address is determined by the state of the LOCATION pin on power-up.

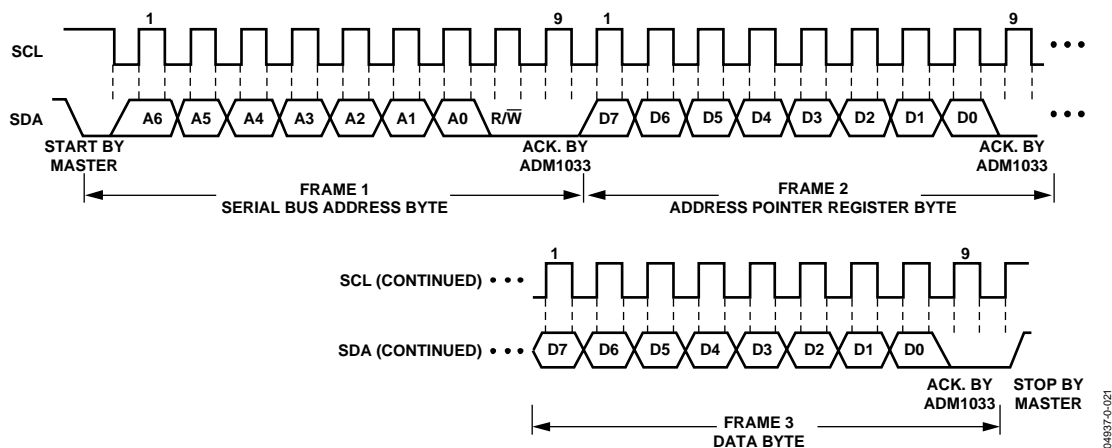


Figure 18. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

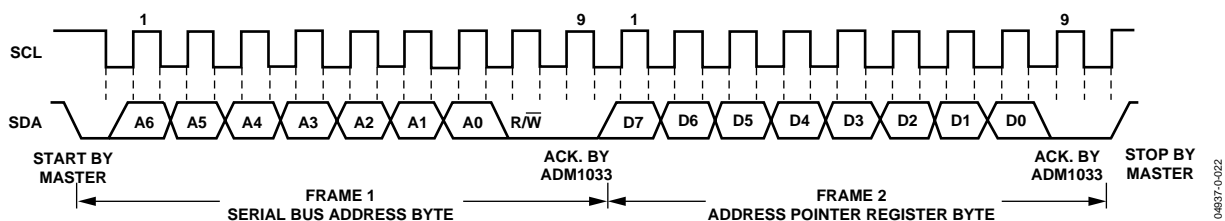


Figure 19. Writing to the Address Pointer Register Only (Send Byte)

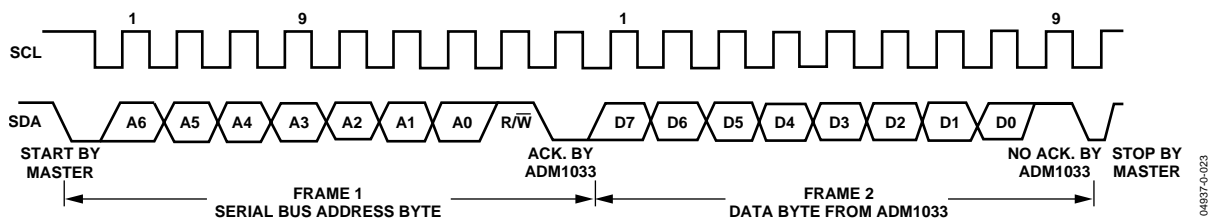


Figure 20. Reading Data from a Previously Selected Register

REGISTER ADDRESSES FOR SINGLE/BLOCK BYTE MODES

The ADM1033 supports single-byte and multiple-byte (block) read and write operations. The register address determines whether a single-byte or block operation is run. For a single-byte operation, the MSB of the register address is set to 0; for a multiple-byte operation, it is set to 1. The number of bytes read from the ADM1033 in a multiple-byte operation is set in the #Bytes/Block Read Register at Address 0x00. The number of bytes written to it is specified in the block-write operation. The addresses quoted in the register map and throughout this data sheet assume single-byte operation. For multiple-byte operations, set the MSB of each register address to 1.

The SMBus specifications define protocols for different types of read and write operations. The ADM1033 supports the following SMBus write protocols: send byte, write byte, block write, receive byte, and block read. The following abbreviations are used in the diagrams:

- S—START
- P—STOP
- R—READ
- W—WRITE
- A—ACKNOWLEDGE
- \overline{A} —NO ACKNOWLEDGE

WRITE OPERATIONS

Send Byte

In this operation, the master device sends a single-command byte to a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends a 7-bit address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends the register address.
5. The slave asserts ACK on SDA.
6. The master asserts a stop condition on SDA, and the transaction ends.

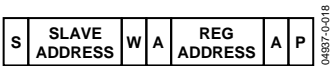


Figure 21. Send Byte

The ADM1033 uses the send-byte operation to write a register address to the APR for a subsequent read from the same address. This is illustrated in Figure 21. The user may be required to read data from the register immediately after setting up the address. If so, the master can assert a repeat start condition immediately after the final ACK and carry out a single-byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends the register address and one data byte to the slave device as follows:

1. The master asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by a write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends the register address. The MSB of the command code should equal 0 for a write-byte operation. If the MSB equals 1, a block-write operation takes place.
5. The slave asserts ACK on SDA.
6. The master sends a data byte.
7. The slave asserts ACK on SDA.
8. The master asserts a stop condition on SDA to end the transaction.

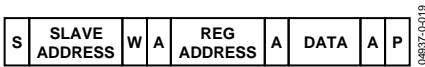


Figure 22. Write Byte

Block Write

In this operation, the master device writes a block of data to a slave address as follows. A maximum number of 32 bytes can be written.

1. The master asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by a write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends the register address. This register address sets up the address pointer register and determines if a block write (MSB = 1) or a byte write (MSB = 0) takes place.
5. The slave asserts ACK on SDA.
6. The master sends the byte count.
7. The slave asserts ACK on SDA.
8. The master sends N data bytes.
9. The slave asserts ACK on SDA after each byte.
10. The master asserts a stop condition on SDA to end the transaction.

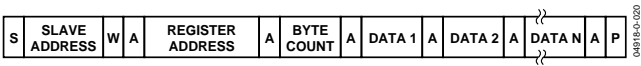


Figure 23. Block Write

READ OPERATIONS

Receive Byte

This operation is useful when repeatedly reading a single register. The register address must be set up prior to this, with the MSB at 0 to read a single byte. In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives a data byte.
5. The master sends NO ACK on SDA.
6. The master asserts a stop condition on SDA and the transaction ends.

In the ADM1033, the receive-byte protocol is used to read a single byte from a register whose address has previously been set by a send-byte or write-byte operation.



Figure 24. Receive Byte

Block Read

In this operation, the master reads a block of data from a slave device. The number of bytes to be read must be set in advance. To do this, use a write-byte operation to the #Bytes/Block Read Register at Address 0x00. The register address determines whether a block-read or a read-byte operation is to be completed (set MSB to 1 to specify a block-read operation). A maximum number of 32 bytes can be read.

1. The master asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends the register address (MSB = 1).
5. The slave asserts ACK on SDA.
6. The master asserts a repeated start on SDA.
7. The master sends the 7-bit slave address followed by the read bit (high).
8. The slave asserts ACK on SDA.
9. The slave sends the byte count.
10. The master asserts ACK on SDA.
11. The slave sends N data bytes.
12. The master asserts ACK on SDA after each data byte.
13. The master does not acknowledge after the Nth data byte.
14. The master asserts a stop condition on SDA to end the transaction.

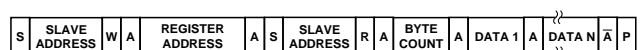


Figure 25. Block Read from RAM

SMBus TIMEOUT

The ADM1033 has a programmable SMBus timeout feature. When this is enabled, the SMBus typically times out after 25 ms of no activity. The timeout is disabled by default. It prevents SMBus hangups by releasing the bus after a period of inactivity.

To enable the SDA timeout, set the SDA timeout bit (Bit 5) of Configuration Register 1 (Address 0x01) to 1.

To enable the SCL timeout, set the SCL timeout bit (Bit 4) of Configuration Register 1 (Address 0x01) to 1.

PACKET ERROR CHECKING (PEC)

The ADM1033 supports packet error checking (PEC). This optional feature is triggered by the extra clock for the PEC byte. The PEC byte is calculated using CRC-8. The frame check sequence (FCS) conforms to CRC-8 by the following:

$$C(x) = x^8 + x^2 + x + 1$$

For more information, consult www.SMBus.org.

ALERT RESPONSE ADDRESS (ARA)

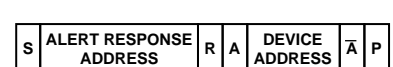


Figure 26. Alert Response Address

When multiple devices exist on the same bus, the alert response address (ARA) feature allows an interrupting device to identify itself to the host. The ALERT output can be used as an interrupt output or as an SMBALERT. One or more ALERT outputs can be connected to a common SMBALERT line, which is connected to the master. If a device's ALERT line goes low, the following procedure occurs:

1. SMBALERT is pulled low.
2. The master initiates a receive-byte operation and sends the alert response address (ARA 0001 100). This is a general call address that must not be used as a specific device address.
3. The device with the low ALERT output responds to the ARA, and the master reads its device address. Once the address is known, it can be interrogated in the usual way.
4. If low ALERT output is detected in more than one device, the one with the lowest device address has priority, in accordance with normal SMBus arbitration.
5. Once the ADM1033 has responded to the ARA, it resets its ALERT output. If the error persists, the ALERT is re-asserted on the next monitoring cycle.

TEMPERATURE MEASUREMENT SYSTEM

INTERNAL TEMPERATURE MEASUREMENT

The ADM1033 contains an on-chip band gap temperature sensor. The on-chip ADC performs conversions on the sensor's output and outputs the temperature data in 13-bit format. The resolution of the local temperature sensor is 0.03125°C.

Table 7 shows the format of the temperature data MSBs. Table 8 shows the local and remote sensor extended resolution data for the LSBs. To ensure accurate readings, the LSBs should be read first. This locks the current LSBs and MSBs until the MSBs are read. They then start to update again. (Reading only the MSBs does not lock the registers.) Temperature updates to the look-up table take place in parallel, so fan speeds can be updated even if the MSBs are locked.

Table 7. Temperature Data Format for Local and Remote Temperature High Bytes

Temperature (°C)	Digital Output
–64	0000 0000
–40	0001 1000
–32	0010 0000
–2	0011 1110
–1	0011 1111
0	0100 0000
1	0100 0001
2	0100 0010
10	0100 1010
20	0101 0100
50	0111 0010
75	1000 1011
100	1010 0100
125	1011 1101
150	1101 0110
191	1111 1111

Table 8. Local and Remote Sensor Extended Resolution

Extended Resolution (°C)	Temperature Low Bits
0.0000	00000
0.03125	00001
0.0625	00010
0.125	00100
0.250	01000
0.375	01100
0.500	10000
0.625	10100
0.750	11000
0.875	11100

$$\text{Temperature (°C)} = (\text{MSB} - 64^\circ\text{C}) + (\text{LSB} \times 0.03125)$$

Example: $\text{MSB} = 0101\ 0100 = 84$

$\text{LSB} = 11100 = 14$

$$\text{Temperature } ^\circ\text{C} = (84 - 64) + (28 \times 0.03125) = 20.875$$

REMOTE TEMPERATURE MEASUREMENT

The ADM1033 measures the temperature of one external diode sensor or diode-connected transistor, which is connected to Pins 9 and 10. These pins are dedicated temperature input channels. The series resistance cancellation (SRC) feature can automatically cancel out the effect of up to 1 kΩ of resistance in series with the remote thermal diode.

The forward voltage of a diode or diode-connected transistor, operated at a constant current, exhibits a negative temperature coefficient of about –2 mV/°C. Unfortunately, the absolute value of V_{BE} varies from device to device, and individual calibration is required to null this out. Therefore, the technique is unsuitable for mass production.

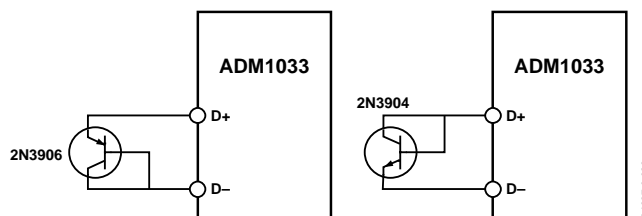


Figure 27. Measuring Temperature Using Discrete Transistors

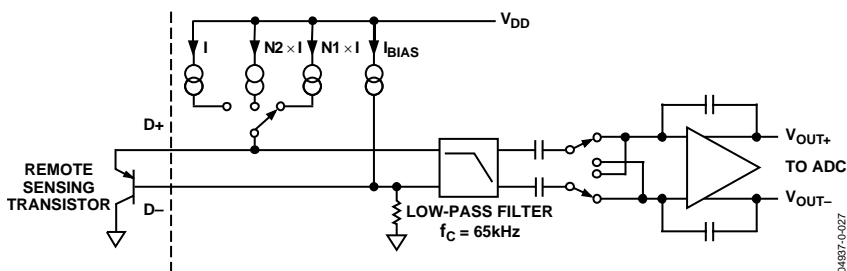


Figure 28. ADM1033 Signal Conditioning

The ADM1033 operates at three different currents to measure the change in V_{BE} .

Figure 28 shows the input signal conditioning used to measure the output of an external temperature sensor. It also shows the external sensor as a substrate transistor, provided for temperature monitoring on some microprocessors. The external sensor works equally well as a discrete transistor.

If a discrete transistor is used, the collector is not grounded and should be linked to the base. If a PNP transistor is used, the base is connected to the D– input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D– input and the base to the D+ input.

If the sensor is used in a very noisy environment, a capacitor value of up to 1000 pF can be placed between the D+ and D– inputs to filter the noise. However, additional parasitic capacitance on the lines between D+, D–, and the thermal diode should also be considered. The total capacitance should never be greater than 1000 pF.

To measure each ΔV_{BE} , the sensor is switched between operating currents of I , $(N1 \times I)$, and $(N2 \times I)$. The resulting waveform is passed through a 65 kHz low-pass filter to remove noise, then to a chopper-stabilized amplifier that amplifies and rectifies the waveform. This produces a dc voltage proportional to ΔV_{BE} . These measurements are used to determine the temperature of the thermal diode, while automatically compensating for any series resistance on the D+ and/or D– lines. The temperature is stored in two registers as a 13-bit word.

To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles at conversion rates of less than 16 Hz. An external temperature measurement takes nominally 32 ms when averaging is enabled and 6 ms when averaging is disabled.

One LSB of the ADC corresponds to 0.03125°C. The ADM1033 can theoretically measure temperatures from –64°C to +191.96875°C, although –64°C and +191°C are outside its operating range. The extended temperature resolution data format is shown in Table 8. The extended temperature resolution for the local and remote channels is stored in the extended temperature resolution registers (Reg. 0x40 = Local, Reg. 0x42 = Remote).

Table 9. Temperature Measurement Registers

Register	Description	Default
0x40	Local Temperature, LSBs	0x00
0x41	Local Temperature, MSBs	0x00
0x42	Remote Temperature, LSBs	0x00
0x43	Remote Temperature, MSBs	0x00

High and low temperature limit registers are associated with each temperature measurement channel. The appropriate status bit is set when the high and low limits are exceeded. Exceeding either limit can cause an $\overline{\text{SMBALERT}}$ interrupt.

Table 10. Temperature Measurement Limit Registers

Register	Description	Default
0x0B	Local High Limit	0x8B (75°C)
0x0C	Local Low Limit	0x54 (20°C)
0x0D	Local $\overline{\text{THERM}}$ Limit	0x95 (85°C)
0x0E	Remote High Limit	0x8B (75°C)
0x0F	Remote Low Limit	0x54 (20°C)
0x10	Remote $\overline{\text{THERM}}$ Limit	0x95 (85°C)

ADDITIONAL FUNCTIONS

Several other temperature measurement functions available on the ADM1033 offer the systems designer added flexibility.

Turn-Off Averaging

The ADM1033 performs averaging at conversion rates of less than or equal to eight conversions per second. This means that the value in the measurement register is the average of 16 measurements. For faster measurements, set the conversion rate to 16 conversions per second or greater. (Averaging is not carried out at these conversion rates.) Or, to switch off averaging at the slower conversion rates, set Bit 1 (AVG) of Configuration 1 Register (Address 0x01).

Single-Channel ADC Conversions

In normal operating mode, the ADM1033 converts on both the local temperature and remote channels. However, the user can set the ADM1033 to convert on one channel only. To enable single-channel mode, set the round robin bit (Bit 7) in Configuration Register 2 (Address 0x02) to 0. When the round robin bit equals 1, the ADM1033 converts on both temperature channels. In single-channel mode, it converts on one channel only, to be determined by the state of the channel selector bit (Bit 4) of Configuration Register 2 (Address 0x02).

Table 11. Channel Selector

Bit 4	Channel Selector (Configuration 2)
0	Local Channel (default)
1	Remote Channel

Removing Temperature Errors

As CPUs run faster and faster, it becomes more difficult to avoid high frequency clocks when routing the D+ and D– traces around a system board. Even when recommended layout guidelines are followed, temperature errors attributed to noise coupled onto the D+ and D– lines remain. High frequency noise generally gives temperature measurements that are too high by a constant amount. The ADM1033 has local and remote temperature offset registers at Addresses 0x16 and 0x17—one for each channel. By completing a one-time calibration, the user can determine the offset caused by the system board noise and remove it using the offset registers. The registers automatically add a twos complement word to the remote temperature measurements, ensuring correct readings in the value registers.

Table 12. Offset Registers

Registration	Description	Default
0x16	Local Offset	0x00
0x17	Remote Offset	0x00

Table 13. Offset Register Values

Code	Offset Value
0 0000 000	0°C (Default)
0 0000 001	0.125°C
0 0000 111	0.875°C
0 0001 111	1.875°C
0 0111 111	7.875°C
0 1111 111	15.875°C
1 0000 000	–16°C
1 1111 000	–0.875°C

LAYOUT CONSIDERATIONS

Digital boards can be electrically noisy environments. Be sure to protect the analog inputs from noise, particularly when measuring the very small voltages from a remote diode sensor. Take the following precautions:

- Place the ADM1033 as close as possible to the remote sensing diode. A distance of 4 inches to 8 inches is adequate, provided that the worst noise sources such as clock generators, data/address buses, and CRTs are avoided.
- Route the D+ and D– tracks close together, in parallel, with grounded guard tracks on each side. Provide a ground plane under the tracks if possible.
- Use wide tracks to minimize inductance and reduce noise pickup. A minimum of 5 mil track width and spacing is recommended.
- Try to minimize the number of copper/solder joints, which can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D– path and at the same temperature. Thermocouple effects should not be a major problem because 1°C corresponds to about 200 μV , and thermocouple voltages are about 3 $\mu\text{V}/^\circ\text{C}$ of temperature difference. Unless there are two thermocouples with a big temperature differential between them, thermocouple voltages should be much less than 200 μV .



Figure 29. Arrangement of Signal Tracks

- Place a 0.1 μF bypass capacitor close to the ADM1033.

- If the distance to the remote sensor is more than 8 inches, twisted pair cable is recommended. This works up to about 6 feet to 12 feet.
- For very long distances (up to 100 feet), use shielded twisted pair such as Belden #8451 microphone cable. Connect the twisted pair to D+ and D– and the shield to GND, close to the ADM1033. Leave the remote end of the shield unconnected to avoid ground loops.

Because the measurement technique uses switched current sources, excessive cable and/or filter capacitance can affect the measurement. When using long cables, the filter capacitor C1 may be reduced or removed. In any case, the total shunt capacitance should never exceed 1000 pF.

Noise Filtering

For temperature sensors operating in noisy environments, common practice is to place a capacitor across the D+ and D– pins to help combat the effects of noise. However, large capacitances affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1000 pF. While this capacitor reduces the noise, it does not eliminate it, making it difficult to use the sensor in a very noisy environment.

The ADM1033 has a major advantage over other devices when it comes to eliminating the effects of noise on the external sensor. The series resistance cancellation feature allows a filter to be constructed between the external temperature sensor and the part. The effect of any filter resistance seen in series with the remote sensor is automatically cancelled from the temperature result.

The construction of a filter allows the ADM1033 and the remote temperature sensor to operate in noisy environments. Figure 30 shows a low-pass R-C-R filter with the following values: $R = 100\ \Omega$ and $C = 1\ \text{nF}$. This filtering reduces both common-mode noise and differential noise.

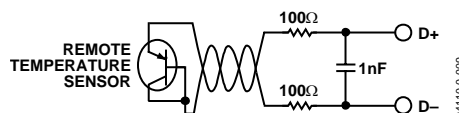


Figure 30. Filter Between Remote Sensor and ADM1033

LIMITS, STATUS REGISTERS, AND INTERRUPTS

High and low limits are associated with each measurement channel on the ADM1033 and form the basis of system status monitoring. The user can set a status bit for any out-of-limit condition and detect it by polling the device. Alternatively, SMBusALERTs can be generated to flag a processor or microcontroller of an out-of-limit condition.

8-BIT LIMITS

Table 14 and Table 15 list all the 8-bit limits on the ADM1033:

Table 14. Temperature Limit Registers

Register	Description	Default
0x0B	Local High Limit	0x8B (75°C)
0x0C	Local Low Limit	0x54 (20°C)
0x0D	Local <u>THERM</u> Limit	0x95 (85°C)
0x0E	Remote High Limit	0x8B (75°C)
0x0F	Remote Low Limit	0x54 (20°C)
0x10	Remote <u>THERM</u> Limit	0x95 (85°C)

Table 15. THERM Limit Register

Register	Description	Default
0x19	<u>THERM</u> % Limit	0xFF

OUT-OF-LIMIT COMPARISONS

The ADM1033 measures all parameters in a round-robin format and sets the appropriate status bit for out-of-limit conditions. Comparisons are made differently, depending on whether the measured value is compared to a high or low limit.

High Limit: \geq Comparison Performed

Low Limit: $<$ Comparison Performed

ANALOG MONITORING CYCLE TIME

The analog monitoring cycle time begins on power-up or, if monitoring has been disabled, by writing a 1 to the monitor/STBY bit of Configuration Register 1 (Address 0x01). The ADC measures each one of the analog inputs in turn; as each measurement is completed, the result is automatically stored in the appropriate value register. The round-robin monitoring cycle continues, unless it is disabled. To disable the cycle, write a 0 to the monitor/STBY bit (Bit 0) of Configuration Register 1 (Address 0x01).

The ADC performs round-robin conversions and takes 11 ms for the local temperature measurement and 32 ms for each remote temperature measurement with averaging enabled.

The total monitoring cycle time for the average temperatures is, therefore, nominally

$$32 + 11 = 43 \text{ ms}$$

Once the conversion time elapses, the round robin starts again. For more information, refer to the Conversion Rate Register section.

Fan TACH measurements take place in parallel and are not synchronized with the temperature measurements.

STATUS REGISTERS

The results of limit comparisons are stored in the status registers. A 1 represents an out-of-limit measurement; a 0 represents an in-limit measurement. The status registers are located at Addresses 0x4F to 0x51.

If the measurement is outside its limits, the corresponding status register bit is set to 1. It remains set at 1 until the measurement falls back within its limits and either the status register is read or an ARA is completed.

To poll the state of the various measurements, read the status registers over the serial bus. If Bit 0 (ALERT low) of Status Register 3 (Address 0x51) is set, this means the ADM1033 has pulled the ALERT output low.

Pin 14 is an SMBusALERT output. This pin automatically notifies the system supervisor of an out-of-limit condition. Reading the status register clears the status bit, as long as the error condition has been cleared.

Pin 3 is an ALERT Comp output. This pin asserts low when ever an unmasked measurement goes outside its limit. Unlike SMBusALERT, it automatically resets once the measurement falls back within the programmed limits.

Status register bits are sticky. Whenever a status bit is set due to an out-of-limit condition, it remains set—even after the triggering event has cleared. The only way to clear the status bit is to read the status register (after the triggering event has cleared). Interrupt mask registers (Reg. 0x08, Reg. 0x09, Reg. 0x0A) allow individual interrupt sources to be masked from causing an ALERT. If one of these masked interrupt sources goes out of limit, its associated status bit is set in the status register.

Table 16. Status Register 1 (Reg. 0x4F)

Bit No.	Name	Description
7	LH	1 = Local high temperature limit has been exceeded.
6	LL	1 = Local low temperature limit has been exceeded.
5	RH	1 = Remote high temperature limit has been exceeded.
4	RL	1 = Remote low temperature limit has been exceeded.
3	RD	1 = Remote diode error; indicates an open or short on the D1+/D1– pins.
2	Unused	Reserved.
1	Unused	Reserved.
0	Unused	Reserved.

Table 17. Status Register 2 (Reg. 0x50)

Bit No.	Name	Description
7	LT	1 = Local THERM temperature limit has been exceeded.
6	RT	1 = Remote THERM temperature limit has been exceeded.
5	Unused	Reserved.
4	T%	1 = THERM timer limit has been exceeded.
3	TA	1 = One of the THERM limits has been exceeded; and the THERM output signal has been asserted.
2	TS	1 = THERM pin is active. Clears on a read, if THERM is not active.
1	Res	Reserved.
0	Res	Reserved.

Table 18. Status Register 3 (Reg. 0x51)

Bit No.	Name	Description
7	FS	1 = Fan has stalled.
6	FA	1 = Fan ALARM speed, indicates fan is running at alarm speed.
5	Res	Reserved.
4	Res	Reserved.
3	Res	Reserved.
2	Res	Reserved.
1	Res	Reserved.
0	ALERT	1 = SMBusALERT low, indicates the ADM1033 has pulled the SMBusALERT line low.

ALERT INTERRUPT BEHAVIOR

The ADM1033 generates an ALERT to signal out-of-limit conditions. Out-of-limit conditions can also be detected by polling the status registers. The ADM1033 has two ALERT outputs, called ALERT Comp and SMBusALERT.

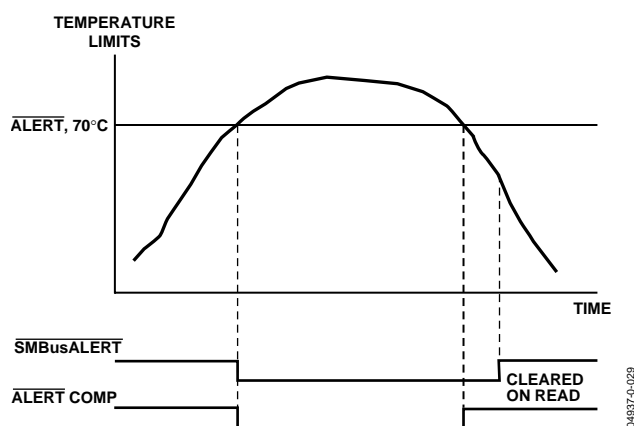
In SMBusALERT mode, the output remains low until the following combination of conditions occur: the measurement falls back within its programmed limits, and either the status register is read or an ARA is completed.

In ALERT Comp mode, the output automatically resets once the temperature measurement falls back within the programmed limits.

For the SMBusALERT output, a status bit is set when a measurement goes outside its programmed limit. If the corresponding mask bit is not set, the SMBusALERT output is pulled low. If the measured value falls back within the limits, the SMBusALERT output remains low until the corresponding status register is read or until an ARA is completed, as long as no other measurement is outside its limits.

On the other hand, the ALERT Comp output is automatically pulled low when a measurement goes outside its programmed limits. Once the measurement falls back within its limits, the ALERT output is automatically pulled back high again, assuming no other measurement channel is outside its limits.

The main difference between the two outputs is that the SMBusALERT does not reset without software intervention, while the ALERT Comp output automatically resets itself. Note: In this data sheet, an ALERT refers to both the ALERT Comp and SMBusALERT, unless otherwise stated.

Figure 31. How ALERT Comparator and SMBusALERT Outputs Work

04837-Q-029

HANDLING SMBUSALERT INTERRUPTS

To prevent tie-ups due to service interrupts, follow these steps:

1. Detect an SMBus assertion.
2. Enter the interrupt handler.
3. Read the status register to identify the interrupt source.
4. Mask the interrupt source by setting the appropriate mask bit in the interrupt mask registers (Reg. 0x08 to Reg. 0x0A).
5. Take the appropriate action for a given interrupt source.
6. Exit the interrupt handler.
7. Periodically poll the status register. If the interrupt status bit has cleared, reset the corresponding interrupt mask bit to 0. This causes the $\overline{\text{SMBusALERT}}$ output and status bits to behave as shown in Figure 32.

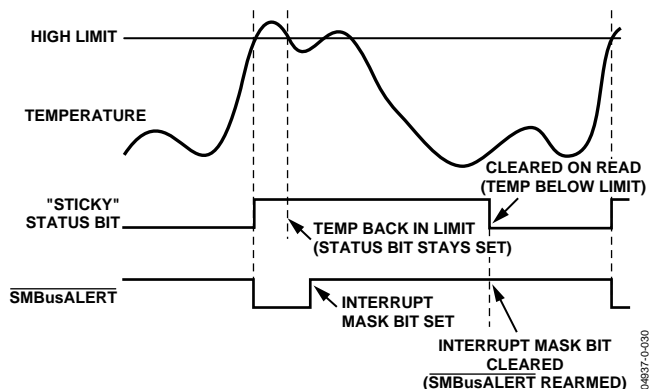


Figure 32. Handling $\overline{\text{SMBusALERT}}$ s

INTERRUPT MASKING REGISTER

Mask Registers 1, 2, and 3 are located at Addresses 0x08, 0x09, and 0x0A. These registers allow individual interrupt sources to be masked out to prevent the $\overline{\text{ALERT}}$ interrupts. Note that masking the interrupt source prevents only the $\overline{\text{ALERT}}$ from being asserted; the appropriate status bit is set as normal.

Table 19. Mask Register 1 (Reg. 0x08)

Bit No.	Name	Description
7	LH	1 masks the $\overline{\text{ALERT}}$ for the local high temperature.
6	LL	1 masks the $\overline{\text{ALERT}}$ for the local low temperature.
5	RH	1 masks the $\overline{\text{ALERT}}$ for the remote high temperature.
4	RL	1 masks the $\overline{\text{ALERT}}$ for the remote low temperature.
3	RD	1 masks the $\overline{\text{ALERT}}$ for the remote diode errors.
2	Res	Reserved.
1	Res	Reserved.
0	Res	Reserved.

Table 20. Mask Register 2 (Reg. 0x09)

Bit No.	Name	Description
7	Res	Reserved.
6	Res	Reserved.
5	Res	Reserved.
4	T%	1 masks the $\overline{\text{ALERT}}$ for the $\overline{\text{THERM}}$ timer limit.
3	TA	1 masks the $\overline{\text{ALERT}}$ for the $\overline{\text{THERM}}$ limit being exceeded and the $\overline{\text{THERM}}$ output signal being asserted.
2	TS	1 masks the $\overline{\text{ALERT}}$ for a transition on $\overline{\text{THERM}}$; has no effect on $\overline{\text{ALERT}}$ in ALERT Comp mode.
1	Res	Reserved.
0	Res	Reserved.

Table 21. Mask Register 3 (Reg. 0x0A)

Bit No.	Name	Description
7	FS	1 masks the $\overline{\text{ALERT}}$ for fan stalling.
6	FA	1 masks the $\overline{\text{ALERT}}$ for fan running at ALARM speed.
5	Res	Reserved.
4	Res	Reserved.
3	Res	Reserved.
2	Res	Reserved.
1	Res	Reserved.
0	Res	Reserved.

FAN_FAULT OUTPUT

The $\overline{\text{FAN_FAULT}}$ output signals when the fan stalls. Pin 8, a dual-function pin, defaults to a $\overline{\text{FAN_FAULT}}$ output. It can also be reconfigured as an analog input reference for the $\overline{\text{THERM}}$ input. To configure the pin, set the $\overline{\text{FAN_FAULT/REF}}$ bit (Bit 7) in Configuration Register 4 (Address 0x04) to 1.

FAULT QUEUE

The ADM1033 has a programmable fault queue option that lets the user program the number of out-of-limit measurements allowable before generating an $\overline{\text{SMBusALERT}}$. The fault queue affects only temperature measurement channels and is operational only in $\overline{\text{SMBusALERT}}$ mode. It performs some simple filtering, which is particularly useful at the higher conversion rates (16, 32, and 64 conversions per second), where averaging is not carried out.

There is a queue for each of the temperature channels. If L (the value programmed to the fault queue) or more consecutive out-of-limit measurements are made on the same temperature channel, the fault queue fills and the $\overline{\text{SMBusALERT}}$ output triggers. To fill the fault queue, the user needs L or more consecutive out-of-limit measurements on the local, or L or more consecutive out-of-limit measurements on the remote channel. The fault queue is independent of the state of the bits in the status register.

Table 22. Fault Queue (Address 0x06)

Bits <3:0>	Fault Queue
000x	1
001x	2
01xx	3
1xxx	4

To reset the fault queue, do one of the following:

- $\overline{\text{SMBus}}$ ARA command
- Read Status Register 1
- Power-on reset

The $\overline{\text{SMBusALERT}}$ clears, even if the condition that caused the $\overline{\text{SMBusALERT}}$ remains. The $\overline{\text{SMBusALERT}}$ is reasserted, if the fault queue fills up.

CONVERSION RATE REGISTER

The ADM1033 makes up to 64 measurements per second. However, for the sake of reduced power consumption and better noise immunity, users can run the ADM1033 at a slower conversion rate. Averaging does not occur at rates of 16, 32, and 64 conversions per second. Table 23 lists the available rates. The conversion rate register is located at Address 0x05. Note that the current round-robin loop must be completed before the newly programmed conversion rate can take effect.

Table 23. Conversion Rates

Code	Conversion Rate
0x00	0.0625
0x01	0.125
0x02	0.25
0x03	0.5
0x04	1
0x05	2
0x06	4
0x07	8
0x08	16
0x09	32
0x0A	64
0x0B to 0xFF	Reserved

THERM I/O TIMER AND LIMITS

Pin 7 can be configured as either an input or output. As an output, it is asserted low to signal that the measured temperature has exceeded preprogrammed temperature limits. The output is automatically pulled high again when the temperature falls below the ($\overline{\text{THERM}}$ – Hysteresis) limit. The value of hysteresis is programmable in Register 0x1A. $\overline{\text{THERM}}$ is enabled as an output by default on power-up.

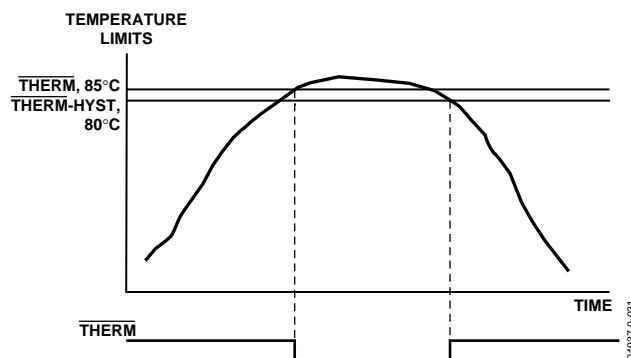


Figure 33. $\overline{\text{THERM}}$ Behavior

Once the $\overline{\text{THERM}}$ limits are exceeded, the fans are boosted to full speed—that is, as long as the boost disable bit (Bit 1) is not set in Configuration Register 2 (Address 0x02).

To configure $\overline{\text{THERM}}$ as an input, set the $\overline{\text{THERM}}$ timer bit (Bit 2) of Configuration Register 1 (Address 0x01) to 1. (It no longer operates as an output.) The ADM1033 can then detect whenever the $\overline{\text{THERM}}$ input is asserted low. This can be connected to a trip point temperature sensor or to the $\overline{\text{PROCHOT}}$ output of a CPU. With processor core voltages reducing all the time, the threshold for the $\text{ADTL} + \overline{\text{PROCHOT}}$ output also reduces as new processors become available. The default threshold on $\overline{\text{THERM}}$ is the normal CMOS threshold. However, Pin 8 ($\overline{\text{FAN_FAULT/REF}}$) can be reconfigured as a REF input. This is done by setting Bit 7 ($\overline{\text{FAN_FAULT/REF}}$) in Configuration Register 4 (Address 0x04) to 1. The processor V_{CCP} should be connected to this input to provide a reference for the $\overline{\text{THERM}}$ input. The resulting $\overline{\text{THERM}}$ threshold is $0.75 \times V_{\text{CCP}}$, the correct threshold for an AGTL+ signal.

The ADM1033 can also measure assertion times on the $\overline{\text{THERM}}$ input as a percentage of an on-time window. This window is programmable in Configuration Register 4 (Address 0x04) using Bits <6:4> ($\overline{\text{THERM}}$ % on-time window). Values of between 0.25 and 8 are programmable. The assertion time, as a percentage of the time window, is stored in the $\overline{\text{THERM}}$ % on-time register (Address 0x4E).

A $\overline{\text{THERM}}$ % (0x19) limit is also associated with this register. Once the measured percentage exceeds the percentage limit, the $\overline{\text{THERM}}$ % exceeded bit (Bit 4) in Status Register 2 (Address 0x50) is asserted and an $\overline{\text{ALERT}}$ is generated, as long as the mask bit is not set. If the limit is set to 0x00, an $\overline{\text{ALERT}}$ is generated on the first assertion. If the limit is set to 0xFF, an $\overline{\text{ALERT}}$ is never generated. This is because 0xFF corresponds to the $\overline{\text{THERM}}$ input, which is asserted all the time.

Table 24. $\overline{\text{THERM}}$ % On-Time Window

Code	$\overline{\text{THERM}}$ % On-Time Window
000	0.25 s
001	0.5 s
010	1 s
011	2
100	4 s
101	8 s
110	8 s
111	8 s

When $\overline{\text{THERM}}$ is configured as an input only, set the enable $\overline{\text{THERM}}$ events bits in Configuration Register 4 (Address 0x04) to allow Pin 7 to operate as an I/O.

To configure the $\overline{\text{THERM}}$ pin to be pulled low as an output whenever the local temperature exceeds the local $\overline{\text{THERM}}$ limit, set the enable local $\overline{\text{THERM}}$ events bit (Bit 0) of Configuration Register 4 (Address 0x04).

To configure the $\overline{\text{THERM}}$ pin to be pulled low as an output whenever the remote temperature exceeds the remote $\overline{\text{THERM}}$ limit, set the enable remote $\overline{\text{THERM}}$ events bit (Bit 1) of Configuration Register 4 (Address 0x04).

$\overline{\text{THERM}}$ % LIMIT REGISTER

The $\overline{\text{THERM}}$ % limit is programmed to Register 0x19. An $\overline{\text{ALERT}}$ is generated if the $\overline{\text{THERM}}$ is asserted for longer than the programmed percentage limit. The limit is programmed as a percentage of the chosen time window.

$$0x00 = 0\%$$

$$0xFF = 100\%$$

$$\text{Therefore, } 1 \text{ LSB} = 0.39\%$$

Example

If a time window of 8 seconds is chosen, and an $\overline{\text{ALERT}}$ is to be generated if $\overline{\text{THERM}}$ is asserted for more than 1 second, program the following value to the limit register:

$$\% \text{ Limit} = 1/8 \times 100 = 12.5\%$$

$$12.5\% / 0.39\% = 32d = 0x20 = 0010 \ 0000$$

An $\overline{\text{ALERT}}$ is generated if the $\overline{\text{THERM}}$ limit is exceeded after the time window has elapsed, assuming it is not masked.

FAN DRIVE SIGNAL

The ADM1033 controls the speed of a cooling fan. Varying the duty cycle (on/off time) of a square wave applied to the fan varies the speed of the fan. The ADM1033 uses a control method called synchronous speed control, in which the PWM drive signal applied to the fan is synchronized with the fan's TACH signal. See the Synchronous Speed Control section.

The external circuitry required to drive the fan is simple. A single N-channel MOSFET is the only drive device required. The specifications of the MOSFET depend on the maximum current required by the fan and the gate voltage drive ($V_{GS} < 3\text{ V}$ for direct interfacing to the drive pin). V_{GS} can be greater than 3 V, as long as the pull-up on the gate is tied to 5 V. The MOSFET should also have a low on resistance to ensure that there is no significant voltage drop across the FET. A high on resistance reduces the voltage applied across the fan and, therefore, the maximum operating speed of the fan. Figure 34 shows a scheme for driving a 3-wire fan.

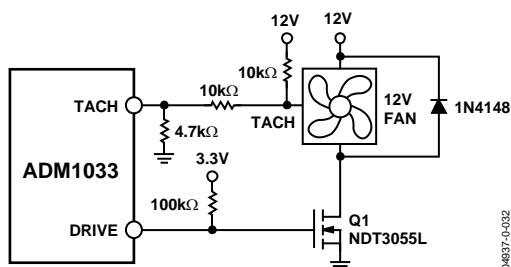


Figure 34. Interfacing a 3-Wire Fan to the ADM1033 Using an N-Channel MOSFET

Figure 34 uses a 10 kΩ pull-up resistor for the TACH signal. This assumes that the TACH signal is an open collector from the fan. In all cases, the fan's TACH signal must be kept below 5 V maximum to prevent damaging the ADM1033.

If in doubt as to whether a fan has an open collector or totem-pole TACH output, use one of the input signal conditioning circuits shown in the Fan Inputs section.

When designing drive circuits with transistors and FETs, make sure that the drive pins are not required to source current and that they sink less than the maximum current specified.

SYNCHRONOUS SPEED CONTROL

The ADM1033 drives the fan using a control scheme called synchronous speed control. In this scheme, the PWM drive signal applied to the fan is synchronized with the TACH signal. Accurate and repeatable fan speed measurements are the main benefits. The fan is allowed to run reliably at speeds as low as 30 % of the full capability.

The drive signal applied to the fan is synchronized with the TACH signal. The ADM1033 switches on the drive signal and waits for a transition on the TACH signal. When a transition takes place on the TACH signal, the PWM drive is switched off for a period of time called t_{OFF} . The drive signal is then switched on again. The t_{OFF} time is varied in order to vary the fan speed.

If the fan runs too fast, the t_{OFF} time is increased. If the fan runs too slow, the t_{OFF} time is decreased.

Because the drive signal is synchronized with the TACH signal, the frequency with which the fan is driven depends on the current speed of the fan and the number of poles in it.

Figure 35 shows how the synchronous speed drive signal works. The ideal TACH signal is the signal that would be output from the fan, if power were applied 100% of the time. It is representative of the actual speed of the fan. The actual TACH signal is the signal seen on the TACH output from the fan, if using a scope. In effect, the actual TACH signal is the ideal TACH signal chopped with the drive signal.

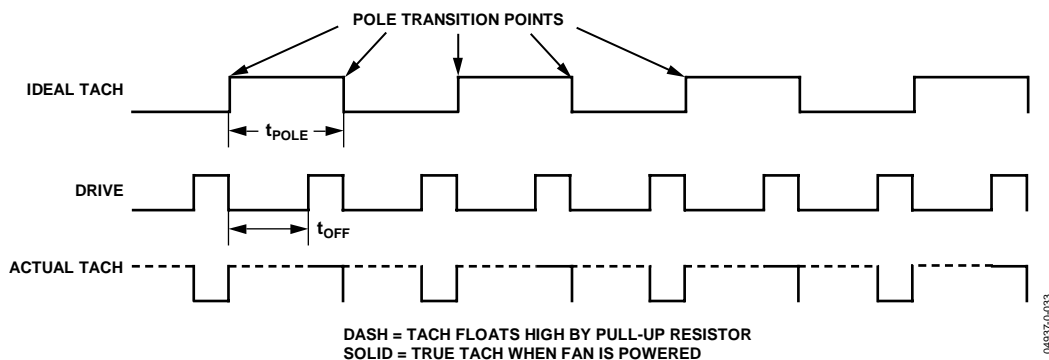


Figure 35. Drive Signal by Using Synchronous Control

ADM1033

FAN INPUTS

Pin 2 is the TACH input intended for fan speed measurement. This input is open-drain.

Signal conditioning on the ADM1033 accommodates the slow rise and fall time of typical tachometer outputs. The maximum input signal range is from 0 V to 5 V, even when V_{CC} is less than 5 V. If these inputs are supplied from fan outputs that exceed 0 V to 5 V, either resistive attenuation of the fan signal or diode clamping must be used to keep the fan inputs within an acceptable range.

Figure 36 to Figure 38 show examples of possible fan input circuits.

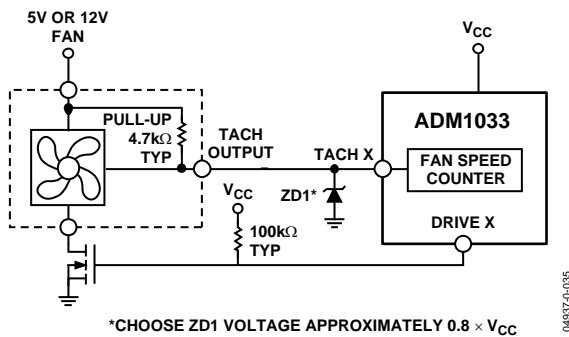


Figure 36. Fan with TACH Pull-Up to Voltage > 5 V, Clamped with Zener Diode

If the fan output has a resistive pull-up to 12 V (or another voltage greater than 5 V), the fan output can be clamped with a Zener diode, as shown in Figure 36. Select a Zener voltage that is greater than V_{IH} but less than 5 V, allowing for the voltage tolerance of the Zener. A value of between 3 V and 5 V is suitable.

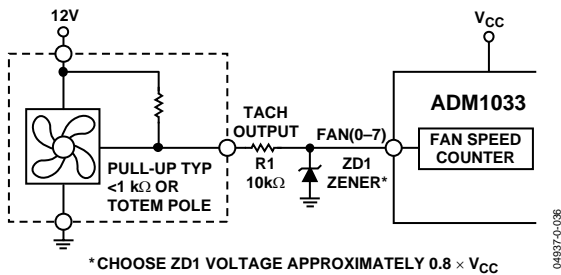


Figure 37. Fan with Strong TACH Pull-Up to Voltage > V_{CC} or Totem Pole Output, Clamped with Zener and Resistor

If the fan has a strong pull-up (less than 1 kΩ to 12 V) or a totem-pole output, then a series resistor can be added to limit the Zener current, as shown in Figure 37.

Or, resistive attenuation can be used, as shown in Figure 38.

$R1$ and $R2$ should be chosen such that

$$2\text{ V} < V_{PULL-UP} \times R2 / (R_{PULL-UP} + R1 + R2) < 5\text{ V}$$

The fan inputs have an input resistance of about 160 kΩ to ground. Consider this when calculating resistor values.

With a pull-up voltage of 12 V and pull-up resistor of less than 1 kΩ, suitable values for $R1$ and $R2$ would be 100 kΩ and 47 kΩ. This gives a high input voltage of 3.83 V.

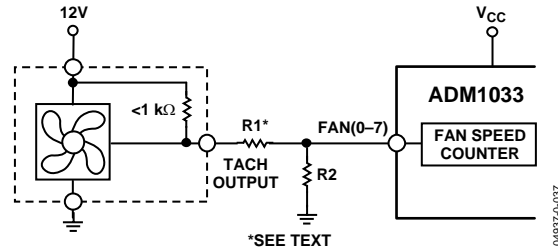


Figure 38. Fan with Strong TACH Pull-Up to Voltage > V_{CC} to Totem Pole Output, Attenuated with $R1/R2$

FAN SPEED MEASUREMENT

The fan counter does not count the fan TACH output pulses directly. This is because the fan may be spinning at less than 1,000 rpm and it would take several seconds to accumulate a large and accurate count. Instead, the period of the fan revolution is measured by gating an on-chip 81.92 kHz oscillator into the input of a 16-bit counter for one complete revolution of the fan. Therefore, the accumulated count value is actually proportional to the fan tachometer period and inversely proportional to the fan speed.

The number of poles in the fan must be programmed in Configuration Register 3 (Address 0x03). This number must be an even number only, because there cannot be an uneven number of poles in a fan. A TACH period is output for every two poles. Therefore, the number of poles must be known so that the ADM1033 can measure for a full revolution.

Figure 39 shows the fan speed measurement period, assuming that the fan outputs an ideal TACH signal. In reality, the TACH signal output by the fan is chopped by the drive signal. However, because the drive signal and TACH signal are synchronized, there is enough information available for the ADM1033 to measure the fan speed accurately.

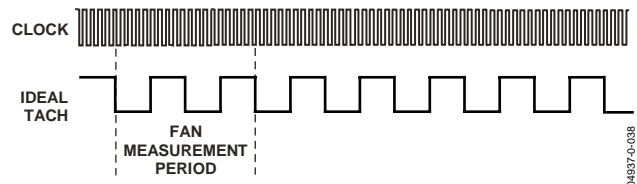


Figure 39. Fan Speed Measurement for a 4-Pole Fan

FAN SPEED MEASUREMENT REGISTERS

The 16-bit measurements listed in Table 25 are stored in the TACH value registers.

Table 25. TACH Value Registers

Register	Description	Default
0x4A	TACH Period, LSB	0xFF
0x4B	TACH Period, MSB	0xFF

READING FAN SPEED

Reading back the fan speed involves a 2-register read for each measurement. The low byte should be read first. This freezes the high byte until both high and low byte registers have been read, preventing erroneous fan speed measurement readings.

The fan tachometer reading registers report back the number of 12.20 μ s period clocks (81.92 kHz oscillator) gated to the fan speed counter for one full rotation of the fan (assuming the correct number of poles is programmed). Because the ADM1033 essentially measures the fan TACH period, the higher the count value, the slower the fan's actual speed. A 16-bit fan TACH reading of 0xFFFF indicates that the fan has stalled or is running very slowly (<75 rpm).

CALCULATING FAN SPEED

Fan speed in rpm is calculated as follows. This calculation assumes the number of poles programmed in Configuration Register 3 (Address 0x03) is correct for the fan used.

$$\text{Fan Speed (rpm)} = (81920 \times 60) / \text{Fan TACH Reading}$$

where the Fan TACH Reading is the 16-bit Fan Tachometer Reading.

Example:

$$\text{TACH High Byte (Reg. 0x28)} = 0x7$$

$$\text{TACH Low Byte (Reg. 0x29)} = 0xFF$$

What is the fan speed in rpm?

$$\text{Fan TACH Reading} = 0x17FF = 6143d$$

$$\text{rpm} = (f \times 60) / \text{Fan TACH Reading}$$

$$\text{rpm} = (81920 \times 60) / 6143$$

$$\text{Fan Speed} = 800 \text{ rpm}$$

ALARM SPEED

The fan ALARM speed (Bit 6) in Status Register 3 (Address 0x51) is set whenever the fan runs at alarm speed. This occurs if the device is programmed to run the fan at full speed whenever the THERM temperature limits are exceeded. The device runs at alarm speed, for example, if the Boost Disable bit (Bit 1) of the Configuration 2 Register (Address 0x02) is not set to 1.

Fan Response Register

The ADM1033 fan speed controller operates by reading the current fan speed, comparing it with the programmed fan speed, and then updating the drive signal applied to the fan. The fan response register determines the rate at which the ADM1033 looks at and updates the drive signal. Different fans have different inertias and respond to a changing drive signal more or less quickly than others. The fan's response register allows the user to tailor the ADM1033 to a particular fan, to prevent situations like overshoot.

The user selects the number of updates to the drive signal per second. Table 26 lists the available options.

Table 26. Fan Response Codes

Code	Update Rate
000	1.25 updates/s
001	2.5 updates/s = default
010	5 updates/s
011	10 updates/s
100	20 updates/s
101	40 updates/s
110	80 updates/s
111	160 updates/s

Table 27. Fan Response Register (Address 0x3C)

Bit	Function
<7:3>	Unused
<2:0>	Fan Response

LOOK-UP TABLE: MODES OF OPERATION

The ADM1033 look-up table has two modes of operation used to determine the behavior of the system:

- Manual mode
- Look-up table

Manual Mode

In manual mode, the ADM1033 is under software control. The software programs the required fan speed value or target rpm value. The ADM1033 then outputs that fan speed.

Programming Target Fan Speed

In this mode, the user programs the target rpm as a TACH count for N poles or a TACH count for one full rotation of the fan. This assumes that the number of poles is programmed correctly in Configuration 3 Register (Address 0x03).

Follow these steps to program the target fan speed:

1. Place the ADM1033 in manual mode. Set Bit 7 (Table/SW) of Configuration Register 1 (Address 0x01) = 0.
2. Program the target TACH count (fan speed) using the following equation:

$$TACH\ Count = (f \times 60) / R$$

where:

$$f = \text{clock frequency} = 81.92\text{ kHz}$$

R = required rpm value

Example 1: If the desired value is 5,000 rpm, program the following value to the TACH pulse period registers:

$$TACH\ Pulse\ Period = (f \times 60) / 5000$$

$$TACH\ Pulse\ Period = 983d = 0x03D7$$

Example 2: If the desired value is 3,500 rpm, program the following value to the TACH pulse period registers:

$$TACH\ Pulse\ Period = (f \times 60) / 3500$$

$$TACH\ Pulse\ Period = 1404d = 0x057C$$

Table 28. Registers to be Programmed

Fan	Description	Address	Value
Example 1	Look-Up Table LSB	0x2A	0xD7
Example 1	Look-Up Table MSB	0x2B	0x03
Example 2	Look-Up Table LSB	0x2C	0x7C
Example 2	Look-Up Table MSB	0x2D	0x05

LOOK-UP TABLE

The ADM1033 allows the user to program a temperature-to-fan-speed profile. There are 24 registers in the look-up table, eight for temperature and 16 for target fan speed (each target fan speed is two registers). In total, there are eight available points.

There are two options when programming the look-up table. It can be programmed to make the fan run at discrete speeds and jump to the new speed once the temperature threshold is crossed. Or, it can linearly ramp the TACH count between the two temperature thresholds.

Figure 40 and Figure 41 show what the look-up table looks like, if all eight points are used on the one curve for both fans.

Figure 40 shows the transfer curve when the fan is programmed to run at discrete speeds. The ADM1033 spins the fan at its new speed once a threshold is crossed.

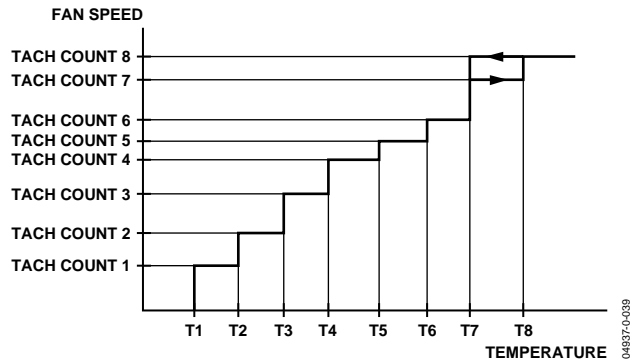


Figure 40. Programming the Look-Up Table in Discrete RPM Mode

Figure 41 shows the transfer curve if the linear fan speeds option is chosen. At temperature T1, the fan runs at Fan Speed 1. As the temperature increases, the fan speed increases until it reaches Fan Speed 2 at T2.

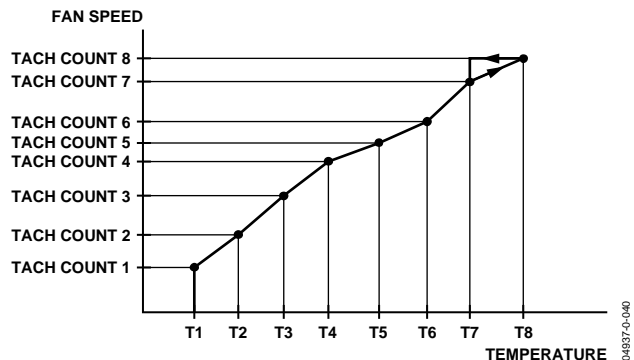


Figure 41. Programming the Look-Up Table in Linear Fan Speeds Mode

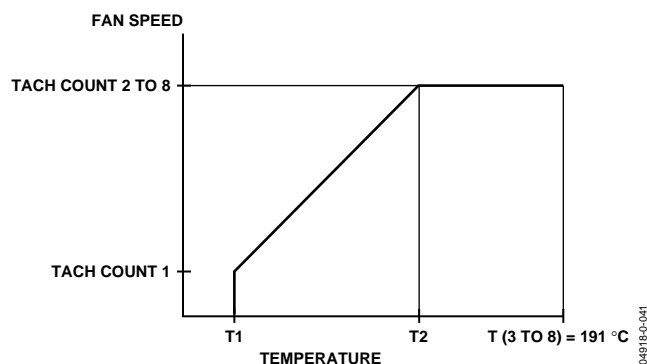


Figure 42. Programming Two Points on the Look-Up Table

Once the temperature exceeds the highest temperature point in the look-up table, the fan speed remains at the highest speed until the temperature drops below the T7 temperature value.

If the temperatures in T1 to T8 are not programmed in succession, the fan speed moves to the next highest programmed temperature as the temperature increases. Similarly, when the temperature decreases, it ignores programmed higher temperatures and jumps to the next lower temperature. Therefore, the temperature-to-fan-speed profile for increasing and decreasing temperature can be different.

When programming the look-up table, the user has the option to use between two and eight points for the fan (eight points only if the same curve is to be used for both fans).

If the user wants to program only the transfer curve and knows the starting temperature, minimum fan speed, maximum temperature, and maximum fan speed, then only four parameters are required: T1, T2, FS1, and FS2. The remaining look-up temperature thresholds should remain at their default values of +191°C. FS 3 to FS8 should be programmed with the same value as FS2 to give the flat curve, if required, or, they can be left at the default value of 0.

However, it is normal to program a $\overline{\text{THERM}}$ limit as well. Once this temperature is exceeded and the boost bit is set, the fan runs to full speed. This overrides the table.

Table 29. Look-Up Table Register Addresses

x	Temperature, x	RPMx, LSB	RPMx, MSB
1	0x22	0x2A	0x2B
2	0x23	0x2C	0x2D
3	0x24	0x2E	0x2F
4	0x25	0x30	0x31
5	0x26	0x32	0x33
6	0x27	0x34	0x35
7	0x28	0x36	0x37
8	0x29	0x38	0x39

SETTING UP THE LOOK-UP TABLE IN LINEAR MODE

When discrete/linear speed (Bit 2) is set to 1 (default), the TACH count decreases linearly and the fan speed increases with temperature. At temperature T_X , the fan runs at FS_X and speed increases with temperature to FS_{X+1} at temperature T_{X+1} .

Alternatively, the fan can be run at discrete fan speeds. When discrete/linear speed (Bit 2) is set to 0, the fan runs at a new speed once the temperature threshold is exceeded.

SELECTING WHICH TEMPERATURE CHANNEL CONTROLS A FAN

Fan Behavior Register (Address 0x07)

Bits <1:0> = DRIVE Behavior

The ADM1033 can be configured so that either the local temperature or the remote temperature controls the fan. In default, the remote temperature controls the fan.

Table 30. Drive BHVR Bits

Bits	Drive x BHVR
00	Local Temperature Controls the Fan
01	Remote Temperature Controls the Fan
10	Remote Temperature Controls the Fan
11	Fan Runs at Full Speed

LOOK-UP TABLE HYSTERESIS

The user can program a hysteresis to be applied to the look-up table. The advantage of this is apparent, if the temperature is cycling around one of the threshold temperatures, particularly when the look-up table is configured in discrete mode. It is not as important in linear mode.

Table 31. Programming the Hysteresis

Code	Hysteresis Value
0000 0000	0°C
0000 0001	1°C
0000 0010	2°C
0000 0101	5°C
0000 1000	8°C
0000 1111	15°C

The hysteresis register of the look-up table is at Address 0x3A. A hysteresis value of between 0°C and 15°C can be programmed with a resolution of 1°C and applied to all the temperature thresholds. Table 31 gives sample values for programming.

PROGRAMMING THE THERM LIMIT FOR TEMPERATURE CHANNELS

THERM is the absolute maximum temperature allowed on a temperature channel. Above this temperature, a component such as the CPU or VRM might operate beyond its safe operating limit. When the temperature exceeds THERM, all fans are driven at full speed to provide critical system cooling. The fans remain running at 100% until the temperature drops below THERM – Hysteresis. The hysteresis value can be programmed; its default is 5°C. If the boost disable bit (Bit 1) is set in Configuration Register 2, the fans do not run to full speed.

The THERM limit is considered the maximum worst-case operating temperature of the system. Exceeding any THERM limit runs all fans at full speed, a condition with very negative acoustic effects. This limit should be set up as a fail-safe and not exceeded under normal system operating conditions. The THERM temperature limit registers are listed in Table 32.

Table 32. THERM Hysteresis Registers

Address	Description	Default
0x0D	Local <u>THERM</u> Limit	0x95 (85°C)
0x10	Remote <u>THERM</u> Limit	0x95 (85°C)

The THERM hysteresis register is at Address 0x1A. A value is programmed and applied to both temperature channels—local and remote. A THERM hysteresis value of between 0°C and 15°C can be programmed with a resolution of 1°C. See Table 33.

Table 33. Programming THERM Hysteresis

Code	Hysteresis Value
0000 0000	0°C
0000 0001	1°C
0000 0010	2°C
0000 0101	5°C
0000 1000	8°C
0000 1111	15°C

XOR TREE TEST MODE

The ADM1033 includes an XOR tree test mode. This mode is useful for in-circuit test equipment at board-level testing. By applying stimulus to the pins included in the XOR test, it is possible to detect opens or shorts on the system board. Figure 43 shows the signals exercised in this mode.

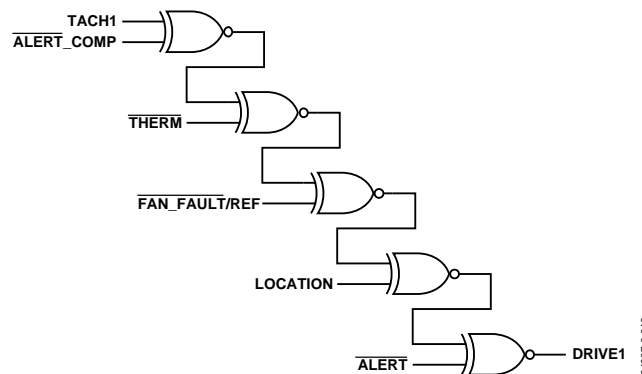


Figure 43. XOR Tree Test

LOCK BIT

Setting the lock bit (Bit 6) of Configuration Register 1 (Address 0x01) makes all the lockable registers read-only. These registers remain read only until the ADM1033 is powered down and back up again. For more information on which registers are lockable, see Table 33.

SW RESET

Setting the software reset bit (Bit 0) of Configuration Register 1 (Address 0x01) resets all software-resettable bits to their default value. For more information on resetting registers and their default values, see Table 34 to Table 68.

Table 34. ADM1033 Registers

Address	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Lockable
0x00/80	R/W	#Bytes/Block Read	7	6	5	4	3	2	1	0	0x20	Y
0x01/81	R/W	Configuration 1	Table/SW	Lock	SDA	SCL	ALERT	TIMER	AVG	MON	0x01	Y
0x02/82	R/W	Configuration 2	RR	RES	RES	CS	LUT	D/L	BD	Reset	0x84	Y
0x03/83	R/W	Configuration 3	RES	RES	RES	RES	#FP	#FP	#FP	#FP	0x44	Y
0x04/84	R/W	Configuration 4	FF/REF	%T	%T	%T	XOR	RES	RTM	LTM	0x00	Y
0x05/85	R/W	Conversion Rate	RES	RES	RES	RES	Conv	Conv	Conv	Conv	0x07	Y
0x06/86	R/W	Fault Queue	RES	F1 Off	RES	RES	FQ	FQ	FQ	FQ	0x01	Y
0x07/87	R/W	Fan Behavior	RES	RES	RES	RES	RES	RES	DB	DB	0x09	Y
0x08/88	R/W	Mask 1	LH	LL	RH	RL	RD	RES	RES	RES	0x52	N
0x09/89	R/W	Mask 2	RES	RES	RES	%T	TA	TS	RES	RES	0x10	N
0x0A/8A	R/W	Mask 3	FS	FA	RES	RES	RES	RES	RES	RES	0x00	N
0x0B/8B	R/W	Local High Limit	7	6	5	4	3	2	1	0	0x8B	N
0x0C/8C	R/W	Local Low Limit	7	6	5	4	3	2	1	0	0x54	N
0x0D/8D	R/W	Local THERM Limit	7	6	5	4	3	2	1	0	0x95	Y
0x0E/8E	R/W	Remote High Limit	7	6	5	4	3	2	1	0	0x8B	N
0x0F/8F	R/W	Remote Low Limit	7	6	5	4	3	2	1	0	0x54	N
0x10/90	R/W	Remote THERM Limit	7	6	5	4	3	2	1	0	0x95	Y
0x16/96	R/W	Local Offset	7	6	5	4	3	2	1	0	0x00	Y
0x17/97	R/W	Remote Offset	7	6	5	4	3	2	1	0	0x00	Y
0x19/99	R/W	THERM % Limit	7	6	5	4	3	2	1	0	0x00	Y
0x1A/9A	R/W	THERM Hysteresis	RES	RES	RES	RES	Hys	Hys	Hys	Hys	0x05	N
0x22/A2	R/W	Look-Up Table T1	7	6	5	4	3	2	1	0	0xFF	Y
0x23/A3	R/W	Look-Up Table T2	7	6	5	4	3	2	1	0	0xFF	Y
0x24/A4	R/W	Look-Up Table T3	7	6	5	4	3	2	1	0	0xFF	Y
0x25/A5	R/W	Look-Up Table T4	7	6	5	4	3	2	1	0	0xFF	Y
0x26/A6	R/W	Look-Up Table T5	7	6	5	4	3	2	1	0	0xFF	Y
0x27/A7	R/W	Look-Up Table T6	7	6	5	4	3	2	1	0	0xFF	Y
0x28/A8	R/W	Look-Up Table T7	7	6	5	4	3	2	1	0	0xFF	Y
0x29/A9	R/W	Look-Up Table T8	7	6	5	4	3	2	1	0	0xFF	Y
0x2A/AA	R/W	Look-Up Table, FS1	7	6	5	4	3	2	1	0	0xFF	Y
0x2B/AB	R/W	Look-Up Table, FS1	15	14	13	12	11	10	9	8	0xFF	Y
0x2C/AC	R/W	Look-Up Table, FS2	7	6	5	4	3	2	1	0	0xFF	Y
0x2D/AD	R/W	Look-Up Table, FS2	15	14	13	12	11	10	9	8	0xFF	Y
0x2E/AE	R/W	Look-Up Table, FS3	7	6	5	4	3	2	1	0	0xFF	Y
0x2F/AF	R/W	Look-Up Table, FS3	15	14	13	12	11	10	9	8	0xFF	Y
0x30/B0	R/W	Look-Up Table, FS4	7	6	5	4	3	2	1	0	0xFF	Y
0x31/B1	R/W	Look-Up Table, FS4	15	14	13	12	11	10	9	8	0xFF	Y
0x32/B2	R/W	Look-Up Table, FS5	7	6	5	4	3	2	1	0	0xFF	Y
0x33/B3	R/W	Look-Up Table, FS5	15	14	13	12	11	10	9	8	0xFF	Y
0x34/B4	R/W	Look-Up Table, FS6	7	6	5	4	3	2	1	0	0xFF	Y
0x35/B5	R/W	Look-Up Table, FS6	15	14	13	12	11	10	9	8	0xFF	Y
0x36/B6	R/W	Look-Up Table, FS7	7	6	5	4	3	2	1	0	0xFF	Y
0x37/B7	R/W	Look-Up Table, FS7	15	14	13	12	11	10	9	8	0xFF	Y
0x38/B8	R/W	Look-Up Table, FS8	7	6	5	4	3	2	1	0	0xFF	Y
0x39/B9	R/W	Look-Up Table, FS8	15	14	13	12	11	10	9	8	0xFF	Y
0x3A/BA	R/W	Look-Up Table Hysteresis	RES	RES	RES	RES	HYS	HYS	HYS	HYS	0x00	Y
0x3C/BC	R/W	Fan Response	RES	RES	RES	RES	RES	FR	FR	FR	0x00	Y
0x3D\BD	R	Device ID	7	6	5	4	3	2	1	0	0x33	N
0x3E\BE	R	Company ID	7	6	5	4	3	2	1	0	0x41	N

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Address	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Lockable
0x3F\BF	R	Revision Register	7	6	5	4	3	2	1	0	0x02	N
0x40\C0	R	Local Temperature	4	3	2	1	0	RES	RES	RES	0x00	N
0x41\C1	R	Local Temperature	12	11	10	9	8	7	6	5	0x00	N
0x42\C2	R	Remote Temperature	4	3	2	1	0	RES	RES	RES	0x00	N
0x43\C3	R	Remote Temperature	12	11	10	9	8	7	6	5	0x00	N
0x4A\CA	R	TACH Period	7	6	5	4	3	2	1	0	0xFF	N
0x4B\CB	R	TACH Period	15	14	13	12	11	10	9	8	0xFF	N
0x4E\CE	R	THERM % On-Time	7	6	5	4	3	2	1	0	0x00	N
0x4F\CF	R	Status 1	LH	LL	RH	RL	RTH	RES	RES	RES	0x00	N
0x50\D0	R	Status 2	LT	RT	RES	%T	TA	TS	RES	RES	0x00	N
0x51\D1	R	Status 3	FS	FA	RES	RES	RES	RES	RES	ALERT	0x00	N

Table 35. Register 0x00, # Bytes/Block Read, Power-On Reset = 0x20, Lock = Y, S/W Reset = Y

Bit	Name	R/W	Description
<7:0>	# Bytes Block Read	R/W	Block reads are # bytes/block read long. The maximum is 32 bytes, the SMBus transaction limit.

Table 36. Register 0x01, Configuration Register 1, Power-On Default = 0x01, Lock = Y, SW Reset = Y

Bit	Name	R/W	Description
7	SW Con	R/W	Set to 1 to have look-up table control the fan speed. Set to 0 to put ADM1033 in software/manual control mode. Default = 0.
6	Lock Bit	R/W	Set to 1 to prevent the user from writing to the ADM1033 registers. 1 = ADM1033 registers locked. 0 = ADM1033 registers unlocked. Default = 0.
5	SDA Timeout	R/W	1 = SDA timeout enabled. 0 = SDA timeout disabled. Default = 0.
4	SCL Timeout	R/W	1 = SCL timeout enabled. 0 = SDL timeout disabled. Default = 0.
3	Reserved	R/W	Reserved.
2	Enable THERM Timer	R/W	1 = timer enabled, 0 = timer disabled. Enables THERM as an input. Default = 0.
1	Averaging Off	R/W	Disables averaging at the slower conversion rates (8 Hz and slower). Averaging is automatically disabled at the higher (16, 32, and 64) conversion rates. Default = Averaging On = 0.
0	Monitor/STBY	R/W	Set to 1 to enable monitoring of temperature. Set to 0 to disable temperature monitoring. Power-On Default = 1.

Table 37. Register 0x02, Configuration Register 2, Power-On Default = 0x84, Lock = Y, SW Reset = Y

Bit	Name	R/W	Description
7	Round Robin	R/W	Enables round-robin mode. Set to 0 for single-channel mode. (The ADC converts on only one channel, which is determined by the channel selector bits.) Default = Round Robin = 1.
<6:5>	Reserved	R/W	Reserved.
4	Channel Selector	R/W	0 = local temperature measurements, 1 = remote temperature measurements.
3	Reserved	R/W	Reserved.
2	Discrete/Linear RPM	R/W	Determines whether the fans run at discrete speeds or whether the fan speed increases with temperature between the two thresholds. Default = 1 = linear.
1	Boost Disable	R/W	Set to 1 to prevent fans from being boosted, if either THERM temperature or THERM timer limits are exceeded. Under these conditions, the fans run at the previously calculated speed. Default = 0.
0	SW Reset	R/W	Set this bit to 1 to reset the ADM1033 registers to their default values, excluding the limit registers, offset registers, and look-up table registers. This bit self-clears. Default = 0.

Table 38. Register 0x03, Configuration Register 3, Power-On Default = 0x44, Lock = Y, SW Reset = Y

Bit	Name	R/W	Description
<7:4>	Unused	R/W	Reserved.
<3:0>	#Poles Fan	R/W	Write the number of poles in the fan to this register. Power-On Default = 4 poles = 100. This value should be an even number only.

Table 39. Register 0x04, Configuration Register 4, Power-On Default = 0x00, Lock = Y, SW Reset = Y

Bit	Name	R/W	Description
7	FAN_FAULT REF	R/W	Sets the function for Pin 8. 0 = Default = FAN_FAULT Output (THERM Input is CMOS). 1 = Reference Input for THERM.
<6:4>	THERM % Time Window	R/W	These bits set the time window over which THERM % is calculated. 000 = 0.25 s 001 = 0.5 s 010 = 1 s 011 = 2 s 100 = 4 s 101 = 8 s 110 = 8 s 111 = 8 s
3	XOR Test	R/W	Set this bit to 1 to enable the XOR connectivity test.
2	Unused	R/W	Reserved.
1	Enable Remote THERM Events	R/W	This bit enables THERM assertions as an output. Functions when the THERM timer is enabled and the remote temperature exceeds its THERM limit.
0	Enable Local THERM Events	R/W	This bit enables THERM assertions as an output. Functions when the THERM timer is enabled and the local temperature exceeds its THERM limit.

Table 40. Register 0x05, Conversion Rate Register, Power-On Default = 0x0A, Lock = Y, SW Reset = Y

Bit	Name	R/W	Description
7	Reserved	R/W	Reserved. Do not write a 1 to this bit.
<6:4>	Unused	R	Reserved.
<3:0>	Conversion Rate	R/W	These 4 bits set the conversion rates of the ADM1033. Changing these bits does not update the conversion rate until the start of the next round robin. 0000 = 0.0625 conversions/s 0001 = 0.125 conversions/s 0010 = 0.25 conversions/s 0011 = 0.5 conversions/s 0100 = 1 conversion/s 0101 = 2 conversions/s 0110 = 4 conversions/s 0111 = 8 conversions/s 1000 = 16 conversions/s 1001 = 32 conversions/s 1010 = 64 conversions/s

Table 41. Register 0x06, Fault Queue, Power-On Default = 0x01, Lock = Y, SW Reset = Y

Bit	Name	R/W	Description
<7:4>	Unused	R	Reserved.
<3:0>	Fault Queue Length	R/W	These 4 bits set the fault queue (the number of out-of-limit measurements made before an ALERT is generated). 000x = 1 001x = 2 01xx = 3 1xxx = 4

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Table 42. Register 0x07, Fan BHVR Register, Power-On Default = 0x09, Lock = Y, SW Reset = Y

Bit	Name	R/W	Description
7	Reserved	R	Reserved.
6	Fan Off	R/W	When this bit is set to 1, the fan switches off, regardless of programmed target fan speed. Default = 0.
<5:2>	Reserved	R	Reserved.
<1:0>	DRIVE BHVR	R/W	Determine which temperature source controls the DRIVE Output. 00 = local temp controls the DRIVE. 01 = remote temperature controls the DRIVE. 10 = remote temperature controls the DRIVE. 11 = DRIVE at full speed.

Table 43. Register 0x08, Mask Register 1, Power-On Default = 0x52, Lock = N, SW Reset = Y

Bit	Name	R/W	Description
7	Local Temp High	R/W	A 1 disables the corresponding interrupt status bit from causing the interrupt output to be set. The status bit is not affected. Default = 0.
6	Local Temp Low	R/W	A 1 disables the corresponding interrupt status bit from causing the interrupt output to be set. The status bit is not affected. Default = 1.
5	Remote High	R/W	A 1 disables the corresponding interrupt status bit from causing the interrupt output to be set. The status bit is not affected. Default = 0.
4	Remote Low	R	A 1 disables the corresponding interrupt status bit from causing the interrupt output to be set. The status bit is not affected. Default = 1.
3	Remote Diode Error	R	A 1 disables the corresponding interrupt status bit from causing the interrupt output to be set. The status bit is not affected. Default = 0.
2	Unused	R	Reserved.
1	Unused	R	Reserved.
0	Unused	R	Reserved.

Table 44. Register 0x09, Mask Register 2, Power-On Default = 0x10, Lock = N, SW Reset = Y

Bit	Name	R/W	Description
<7:5>	Unused	R	Unused.
4	<u>THERM</u> %	R/W	A 1 disables the corresponding interrupt status bit from setting the interrupt output. The status bit is not affected. Default = 0.
3	<u>THERM</u> Assert	R/W	A 1 disables the corresponding interrupt status bit from setting the interrupt output. The status bit is not affected. Default = 0.
2	<u>THERM</u> _State	R/W	A 1 disables the corresponding interrupt status bit from setting the interrupt output. The status bit is not affected. Default = 0. This bit has no effect for the ALERT Comp output.
<1:0>	Unused	R	Unused.

Table 45. Register 0x0A, Mask Register 3, Power-On Default = 0x00, Lock = N, SW Reset = Y

Bit	Name	R/W	Description
7	Fan Stalled	R/W	A 1 disables the corresponding interrupt status bit from setting the interrupt output. The status bit is not affected. Default = 0.
6	Fan Alarm Speed	R/W	A 1 disables the corresponding interrupt status bit from setting the interrupt output. The status bit is not affected. Default = 0.
5	Reserved	R	Reserved. Default = 0.
4	Reserved	R	Reserved. Default = 0.
3	Reserved	R	Reserved. Default = 0.
2	Reserved	R	Reserved. Default = 0.
1	Reserved	R	Reserved. Default = 0.
0	Reserved	R	Reserved. Default = 0.

Table 46. Register 0x0B, Local High Limit, Power-On Default = 0x8B, Lock = N, SW Reset = N

Bit	Name	R/W	Description
<7:0>	Local High Limit	R/W	When the local temperature exceeds this point, the corresponding interrupt status bit is set.

Table 47. Register 0x0C, Local Low Limit, Power-On Default = 0x54, Clock = N, SW Reset = N

Bit	Name	R/W	Description
<7:0>	Local Low Limit	R/W	When the local temperature falls below this point, the corresponding interrupt status bit is set.

Table 48. Register 0x0D, Local THERM Limit, Power-On Default = 0x95, Lock = Y, SW Reset = N

Bit	Name	R/W	Description
<7:0>	Local <u>THERM</u> Limit	R/W	When the local temperature exceeds this point, the corresponding status bit is set and the <u>THERM</u> output is activated.

Table 49. Register 0x0E, Remote High Limit, Power-On Default = 0x8B, Lock = N, SW Reset = N

Bit	Name	R/W	Description
<7:0>	Remote High Limit	R/W	When the remote temperature exceeds this point, the corresponding interrupt status bit is set.

Table 50. Register 0x0F, Remote Low Limit, Power-On Default = 0x54, Lock = N, SW Reset = N

Bit	Name	R/W	Description
<7:0>	Remote Low Limit	R/W	When the remote temperature falls below this point, the corresponding interrupt status bit is set.

Table 51. Register 0x10, Remote THERM Limit, Power-On Default = 0x95, Lock = Y, SW Reset = N

Bit	Name	R/W	Description
<7:0>	Remote <u>THERM</u> Limit	R/W	When the temperature exceeds this point, the corresponding status bit is set and the <u>THERM</u> output is activated.

Table 52. Register 0x16, Local Offset Register, Power-On Default = 0x00, Lock = Y, SW Reset = N

Bit	Name	R/W	Description
<7:0>	Local Offset	R/W	Allows a twos complement offset to be automatically added to or subtracted from the local temperature measurement. Resolution = 0.125°C. Maximum offset = –16°C to +15.875°C. Default = 0.

Table 53. Register 0x17, Remote Offset Register, Power-On Default = 0x00, Lock = Y, SW Reset = N

Bit	Name	R/W	Description
<7:0>	Remote Offset	R/W	Allows a twos complement offset to be automatically added to or subtracted from the remote temperature measurement. Resolution = 0.125°C. Maximum offset = –16°C to +15.875°C. Default = 0.

Table 54. Register 0x19, THERM Timer % Limit, Power-On Default = 0xFF, Lock = Y, SW Reset = N

Bit	Name	R/W	Description
<7:0>	<u>THERM</u> Timer on % Limit	R/W	If the <u>THERM</u> is asserted for greater than or equal to the <u>THERM</u> timer on % limit of the time window, then the corresponding status bit is set.

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Table 55. Register 0x1A, $\overline{\text{THERM}}$ Hysteresis, Power-On Default = 0x05, Lock = Y, SW Reset = N

Bit	Name	R/W	Description
<7:4>	Reserved	R	Reserved.
<3:0>	$\overline{\text{THERM}}$ Hysteresis	R/W	An unsigned $\overline{\text{THERM}}$ hysteresis value, LSB = 1°C. Once $\overline{\text{THERM}}$ has been activated on a temperature channel, if the temperature drops below the $\overline{\text{THERM}}$ limit – hysteresis, the $\overline{\text{THERM}}$ is deactivated.

Table 56. Look-Up Table Registers, Lock = Y, SW Reset = Y

Register Address	R/W	Description	Power-On Default
0x22	R/W	Look-Up Table, T1	0xFF
0x23	R/W	Look-Up Table, T2	0xFF
0x24	R/W	Look-Up Table, T3	0xFF
0x25	R/W	Look-Up Table, T4	0xFF
0x26	R/W	Look-Up Table, T5	0xFF
0x27	R/W	Look-Up Table, T6	0xFF
0x28	R/W	Look-Up Table, T7	0xFF
0x29	R/W	Look-Up Table, T8	0xFF
0x2A	R/W	Look-Up Table, RPM1, LSB	0xFF
0x2B	R/W	Look-Up Table, RPM1, MSB	0xFF
0x2C	R/W	Look-Up Table, RPM2, LSB	0xFF
0x2D	R/W	Look-Up Table, RPM2, MSB	0xFF
0x2E	R/W	Look-Up Table, RPM3, LSB	0xFF
0x2F	R/W	Look-Up Table, RPM3, MSB	0xFF
0x30	R/W	Look-Up Table, RPM4, LSB	0xFF
0x31	R/W	Look-Up Table, RPM4, MSB	0xFF
0x32	R/W	Look-Up Table, RPM5, LSB	0xFF
0x33	R/W	Look-Up Table, RPM5, MSB	0xFF
0x34	R/W	Look-Up Table, RPM6, LSB	0xFF
0x35	R/W	Look-Up Table, RPM6, MSB	0xFF
0x36	R/W	Look-Up Table, RPM7, LSB	0xFF
0x37	R/W	Look-Up Table, RPM7, MSB	0xFF
0x38	R/W	Look-Up Table, RPM8, LSB	0xFF
0x39	R/W	Look-Up Table, RPM8, MSB	0xFF

Table 57. Register 0x3A, Look-Up Table Hysteresis, Power-On Default = 0x02, Lock = Y, SW Reset = Y

Bit	Name	R/W	Description
<7:4>	Reserved	R	Reserved.
<3:0>	Look-Up Table Hysteresis	R/W	These bits determine the hysteresis applied to the temperature thresholds in the look-up table. LSB size = 1°C.

Table 58. Register 0x3, Fan Response Register, Power-On Default = 0x11, Lock = Y, SW Reset = Y

Bit	Name	R/W	Description
<7:3>	Reserved	R	Reserved.
<2:0>	Fan Response	R/W	These bits set the fan's response in the rpm control mode. 000 = 1.25 updates/s 001 = 2.5 updates/s (default) 010 = 5 updates/s 011 = 10 updates/s 100 = 20 updates/s 101 = 40 updates/s 110 = 80 updates/s 111 = 160 updates/s

Table 59. Register 0x3D, Device ID, Power-On Default = 0x33, Lock = N, SW Reset = N

Bit	Name	R/W	Description
<7:0>	Device ID	R	This read-only value contains the device ID, which is 0x33.

Table 60. Register 0x3E, Company ID, Power-On Default = 0x41, Lock = N, SW Reset = N

Bit	Name	R/W	Description
<7:0>	Company ID	R	This read-only value contains the company ID, which is 0x41.

Table 61. Register 0x3D, Revision Register, Power-On Default = 0x02, Lock = N, SW Reset = N

Bit	Name	R/W	Description
<7:0>	Revision ID	R	This read-only value contains the revision ID.

Table 62. Register 0x40/41, Local Temperature Registers, Power-On Default = 0x02, Lock = N, SW Reset = Y

Bit	Name	R/W	Description
<4:0>	Local Temperature LSB	R	Contains the LSBs of the last measured local temperature value. Resolution = 0.03125°C.
<12:5>	Local Temperature MSB	R	Contains the MSBs of the last measured local temperature value. Resolution = 1°C.

Table 63. Register 0x42/43, Remote Temperature Registers, Power-On Default = 0x00, Lock = N, SW Reset = Y

Bit	Name	R/W	Description
<4:0>	Remote Temperature LSB	R	Contains the LSBs of the last measured remote temperature value. Resolution = 0.03125°C.
<12:5>	Remote Temperature MSB	R	Contains the MSBs of the last measured remote temperature value. Resolution = 1°C.

Table 64. Register 0x4A/4B, TACH Period, Power-On Default = 0xFF, Lock = N, SW Reset = Y

Bit	Name	R/W	Description
<7:0>	Fan Period Count, LSB	R	This register contains the LSBs of the last measured fan revolution count.
<15:8>	Fan Period Count, MSB	R	This register contains the MSBs of the last measured fan revolution count.

Table 65. Register 0x4E, $\overline{\text{THERM}}$ % On-Time; Power-On Default = 0x00, Lock = N, SW Reset = Y

Bit	Name	R/W	Description
<7:0>	$\overline{\text{THERM}}$ % On Time	R	This value represents the % on time of $\overline{\text{THERM}}$ activity within the time window set by the configuration bits.

Table 66. Register 0x4F, Status 1, Power-On Default = 0x00, Lock = N, SW Reset = Y

Bit	Name	R/W	Description
7	Local Temp High	R	A 1 indicates the local high limit has been tripped.
6	Local Temp Low	R	A 1 indicates the local low limit has been tripped.
5	Remote Temp High	R	A 1 indicates the remote high limit has been tripped.
4	Remote Temp Low	R	A 1 indicates the remote low limit has been tripped.
3	Remote Diode Error	R	A 1 indicates a short or an open has been detected on the remote temperature channel. This test is completed once on each conversion.
<2:0>	Reserved	R	Reserved.

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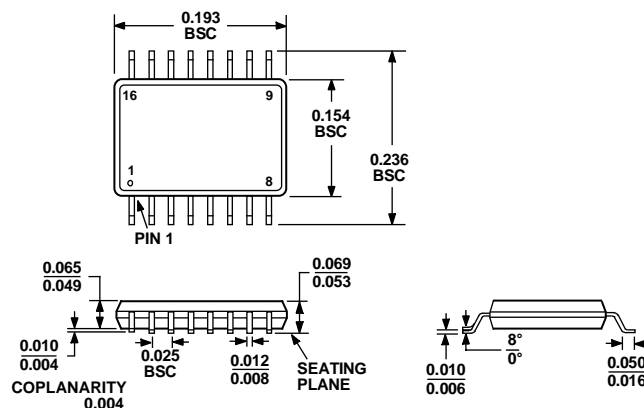
Table 67. Register 0x50, Status 2, Power-On Default = 0x00, Lock = N, SW Reset = Y

Bit	Name	R/W	Description
7	Local $\overline{\text{THERM}}$	R	A 1 indicates the local $\overline{\text{THERM}}$ limit has been tripped.
6	Remote $\overline{\text{THERM}}$	R	A 1 indicates the remote $\overline{\text{THERM}}$ limit has been tripped.
5	Reserved	R	Reserved for future use.
4	$\overline{\text{THERM}}$ % Exceeded	R	A 1 indicates the $\overline{\text{THERM}}$ signal has been asserted for longer than the programmed limit. Clear on read. If $\overline{\text{THERM}}$ % Limit = 0x00 and $\overline{\text{THERM}}$ is asserted, it reasserts immediately.
3	$\overline{\text{THERM}}$ Asserted	R	A 1 indicates the $\overline{\text{THERM}}$ signal has been asserted low, as an input only.
2	$\overline{\text{THERM_State}}$	R	A 1 indicates the $\overline{\text{THERM}}$ pin has been asserted low as an output.
1	Reserved	R	Reserved.
0	Reserved	R	Reserved.

Table 68. Register 0x51, Status Register 3, Power-On Default = 0x00, Lock = N, SW Reset = Y

Bit	Name	R/W	Description
7	Fan Stalled	R	A 1 indicates the fan has stalled.
6	Fan Alarm Speed	R	A 1 indicates the fan is running at full speed, due to an ALARM condition (for instance, if the $\overline{\text{THERM}}$ temperature limit is exceeded).
5	Reserved	R	Reserved.
4	Reserved	R	Reserved.
3	Reserved	R	Reserved.
2	Reserved	R	Reserved.
1	Reserved	R	Reserved.
0	$\overline{\text{ALERT}}$ Low	R	A 1 indicates the ADM1033 has pulled the $\overline{\text{ALERT}}$ output pin low. Allows polling of a single status register to determine if an $\overline{\text{ALERT}}$ condition has occurred in any of the status registers.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-137AB

Figure 44. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)

Dimensions shown in inches

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM1033ARQ	−40°C to +125°C	16-Lead QSOP	RQ-16
ADM1033ARQ-REEL	−40°C to +125°C	16-Lead QSOP	RQ-16
ADM1033ARQ-REEL7	−40°C to +125°C	16-Lead QSOP	RQ-16
ADM1033ARQZ ¹	−40°C to +125°C	16-Lead QSOP	RQ-16
ADM1033ARQZ-REEL ¹	−40°C to +125°C	16-Lead QSOP	RQ-16
ADM1033ARQZ-REEL7 ¹	−40°C to +125°C	16-Lead QSOP	RQ-16

¹ Z = Pb-free part.

ADM1033

NOTES