50 MHz to 4 GHz TruPwr™ Detector

PRELIMINARY TECHNICAL DATA

ADL5501

FEATURES

True rms response
Excellent temperature stability
Up to 30 dB input dynamic range at 4 GHz
50 Ω input impedance
1.25 V rms, +15 dBm, maximum input
Single-supply operation: 2.7 V to 5.5 V
Low power: 3 mW at 3 V supply
RoHS Compliant

APPLICATIONS

Measurement of CDMA, CDMA2000, W-CDMA, and QPSK/QAM-based OFDM, and other complex modulation waveforms
RF transmitter or receiver power measurement

FUNCTIONAL BLOCK DIAGRAM

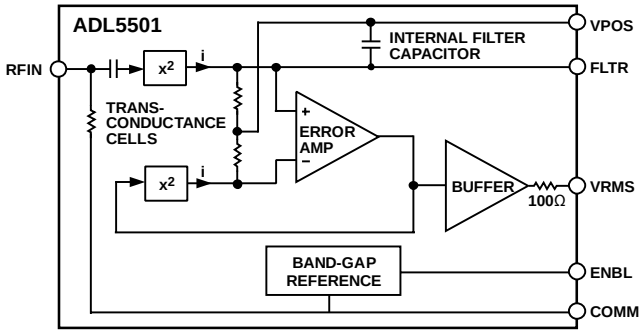

Figure 1.

GENERAL DESCRIPTION

The ADL5501 is a mean-responding power detector for use in high frequency receiver and transmitter signal chains from 50 MHz to 4 GHz. It is easy to apply, requiring only a single supply between 2.7 V and 5.5 V and a power supply decoupling capacitor. The input is internally ac-coupled and has a nominal input impedance of 50 Ω. The output is a linear-responding dc voltage with a conversion gain of 6.6 V/V rms at 900 MHz.

The ADL5501 is intended for true power measurement of simple and complex waveforms. The device is particularly useful for measuring high crest factor (high peak-to-rms ratio) signals, such as CDMA, CDMA2000, W-CDMA, and QPSK/QAM-based OFDM waveforms. The on-chip modulation filter provides adequate averaging for most waveforms. The on-chip, 100 Ω series resistance at the output combined with an external shunt capacitor creates a low-pass filter response that reduces the residual ripple in the dc output voltage. For more complex waveforms, an external capacitor at the FLTR pin can be used for supplementary signal demodulation.

The ADL5501 offers excellent temperature stability across a 30 dB range and near 0 dB measurement error across temperature over the top portion of the dynamic range. In addition to its temperature stability, the ADL5501 offers low process variations which further reduces calibration complexity.

The ADL5501 operates from −40°C to +85°C and is available in a 6-lead, 2.0 mm × 2.1 mm SC-70 package. It is fabricated on a proprietary high f_T silicon bipolar process.

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TARGET SPECIFICATIONS

T_A = 25°C, V_S = 3.0 V, C_{FLTR} = Open, C_{OUT} = 100 nF, unless otherwise noted.

Table 1.

Parameter	Condition	Min	Typ	Max	Unit
FREQUENCY RANGE	(Input RFIN)	50		4000	MHz
RMS CONVERSION (f = 100 MHz)	(Input RFIN to output VRMS)				
Input Impedance			77||4.7		Ω||pF
Input Return Loss			12.5		dB
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±1 dB Error[2]	V_S = 3 V		TBD		dB
	V_S = 5 V		30		dB
Conversion Gain	VOUT = (Gain × V_{IN}) + Intercept	TBD	7.4	TBD	V/V rms
Output Intercept[3]		TBD	0.03	TBD	V
Output Voltage—High Power In	P_{IN} = +5 dBm, 400 mV rms		3.06		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, 20 mV rms		0.17		V
Temperature Sensitivity	P_{IN} = −5 dBm				
	25°C ≤ T_A ≤ 85°C		0.0026		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0023		dB/°C
RMS CONVERSION (f = 900 MHz)	(Input RFIN to output VRMS)				
Input Impedance			40||0.7		Ω||pF
Input Return Loss			16.5		dB
Dynamic Range	CW input, −40°C < T_A < +85°C				
±1 dB Error	V_S = 3 V		TBD		dB
	V_S = 5 V		26		dB
Conversion Gain	VOUT = (Gain × V_{IN}) + Intercept		6.6		V/V rms
Output Intercept			0.03		V
Output Voltage—High Power In	P_{IN} = +5 dBm, 400 mV rms		2.69		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, 20 mV rms		0.15		V
Temperature Sensitivity	P_{IN} = −5 dBm				
	25°C ≤ T_A ≤ 85°C		0.0039		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0046		dB/°C
RMS CONVERSION (f = 1900 MHz)	(Input RFIN to output VRMS)				
Input Impedance			64||-0.5		Ω||pF
Input Return Loss			13.5		dB
Dynamic Range	CW input, −40°C < T_A < +85°C				
±1 dB Error	V_S = 3 V		TBD		dB
	V_S = 5 V		33		dB
Conversion Gain	VOUT = (Gain × V_{IN}) + Intercept		5.7		V/V rms
Output Intercept			0.02		V
Output Voltage—High Power In	P_{IN} = +5 dBm, 400 mV rms		2.36		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, 20 mV rms		0.13		V
Temperature Sensitivity	P_{IN} = −5 dBm				
	25°C ≤ T_A ≤ 85°C		0.0049		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0076		dB/°C

Parameter	Condition	Min	Typ	Max	Unit
RMS CONVERSION (f = 2350 MHz)	(Input RFIN to output VRMS)				
Input Impedance			83||-0.06		Ω||pF
Input Return Loss			12		dB
Dynamic Range	CW input, −40°C < T_A < +85°C				
±1 dB Error	V_S = 3 V		TBD		dB
	V_S = 5 V		32		dB
Conversion Gain	VOUT = (Gain × V_{IN}) + Intercept		5.1		V/V rms
Output Intercept			0.02		V
Output Voltage—High Power In	P_{IN} = +5 dBm, 400 mV rms		2.11		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, 20 mV rms		0.12		V
Temperature Sensitivity	P_{IN} = −5 dBm				
	25°C ≤ T_A ≤ 85°C		0.0051		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0142		dB/°C
OUTPUT OFFSET	No signal at RFIN		50	TBD	mV
ENABLE INTERFACE	(Pin ENBL)				
Logic Level to Enable Power, HI Condition	2.7 ≤ V_S ≤ 5.5 V, −40°C < T_A < +85°C	1.8		V_{POS}	V
Input Current when HI	2.7 V at ENBL, −40°C ≤ T_A ≤ +85°C		0.2	TBD	µA
Logic Level to Disable Power, LO Condition	2.7 ≤ V_S ≤ 5.5 V, −40°C < T_A < +85°C	−0.5		0.8	V
Power-Up Response Time[4]	C_{FLTR} = C_{OUT} = Open, 0 dBm at RFIN		5		µs
	C_{FLTR} = 100nF, C_{OUT} = Open, 0 dBm at RFIN		TBD		µs
POWER SUPPLY					
Operating Range	−40°C < T_A < +85°C	2.7		5.5	V
Quiescent Current	No signal at RFIN, ENBL Input HI[5]		1.0		mA
Total Supply Current when Disabled	No signal at RFIN, ENBL Input LO		<1	TBD	µA

[1] The available output swing, and hence the dynamic range, is altered by the supply voltage; see TDB.
[2] Error referred to best-fit line at 25°C
[3] Calculated using linear regression.
[4] The response time is measured from 10%–90% of settling level; see TDB.
[5] Supply current is input level dependant; see TBD.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage V_S	5.5 V
VRMS	0 V, V_S
RFIN	1.25 V rms
Equivalent Power, re 50 Ω	15 dBm
Internal Power Dissipation	TBD mW
θ_{JA} (SC-70)	TBD°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

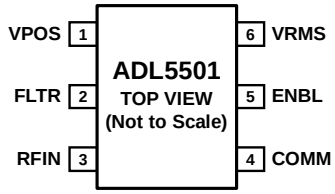

Figure 2. 6-Lead SC-70 Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VPOS	Supply Voltage Pin. Operational range 2.7 V to 5.5 V.
2	FLTR	Modulation Filter Pin. Connection for an External Capacitor to lower the corner frequency of the modulation filter. Capacitor is connected between FLTR and V_S. The on-chip filter is approximately TBD pF. For simple waveforms, no further filtering of the demodulated signal is required.
3	RFIN	Signal Input Pin. Internally ac-coupled after internal termination resistance. Nominal 50 Ω input impedance.
4	COMM	Device Ground Pin.
5	ENBL	Enable Pin. Connect Pin to V_S for Normal Operation. Connect pin to ground for disable mode for a supply current less than 1 µA.
6	VRMS	Output Pin. Rail-to-rail voltage output with limited 3 mA current drive capability. The output has an internal 100 Ω series resistance. High resistive loads are recommended to preserve output swing.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = 5.0 V, C_{FLTR} = Open, C_{OUT} = 100 nF, Colors: black = +25°C, blue = −40°C, red = +85°C, unless otherwise noted.

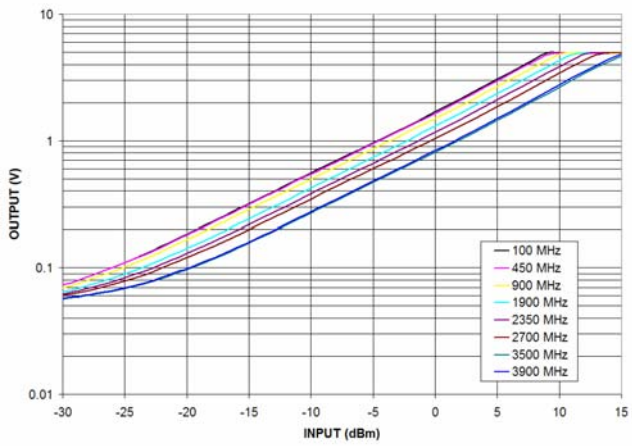

Figure 3. Output vs. Input Level, Frequencies 100 MHz, 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2700 MHz, 3500 MHz, and 3900 MHz, Supply 5.0 V

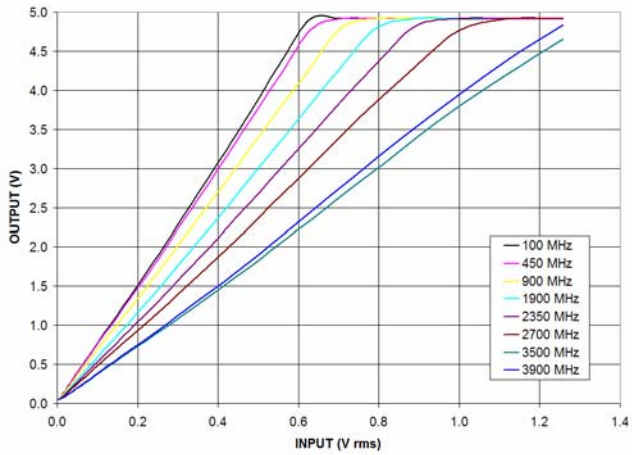

Figure 4. Output vs. Input Level (Linear Scale), Freq 100 MHz, 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2700 MHz, 3500 MHz, and 3900 MHz, Supply 5.0 V

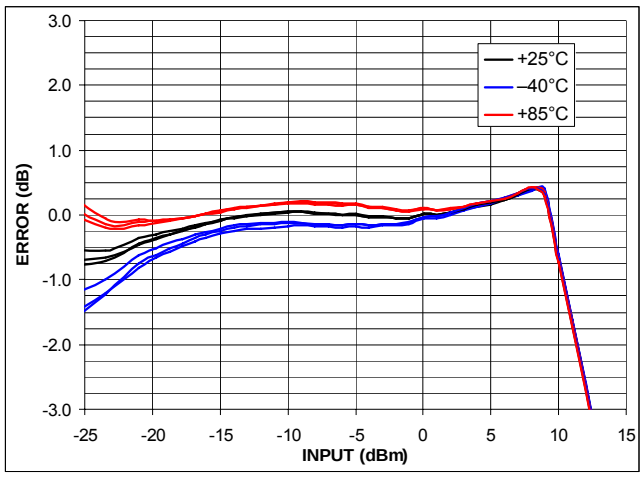

Figure 5. Temperature Drift Distributions for 3 Devices at −40°C, +25°C, and +85°C vs. +25°C Linear Reference, Frequency 100 MHz, Supply 5.0 V

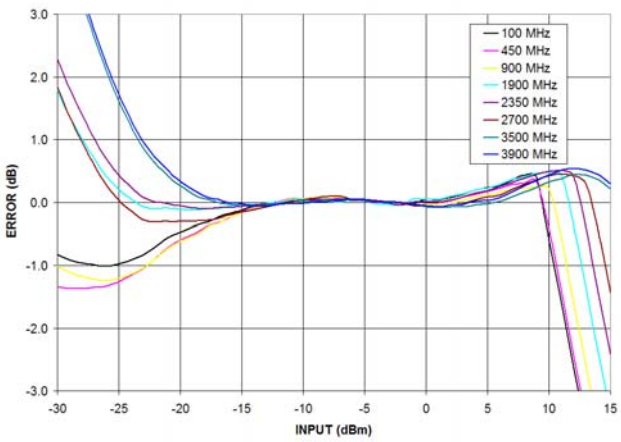

Figure 6. Linearity Error vs. Input Level, Freq 100 MHz, 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2700 MHz, 3500 MHz, and 3900 MHz, Supply 5.0 V

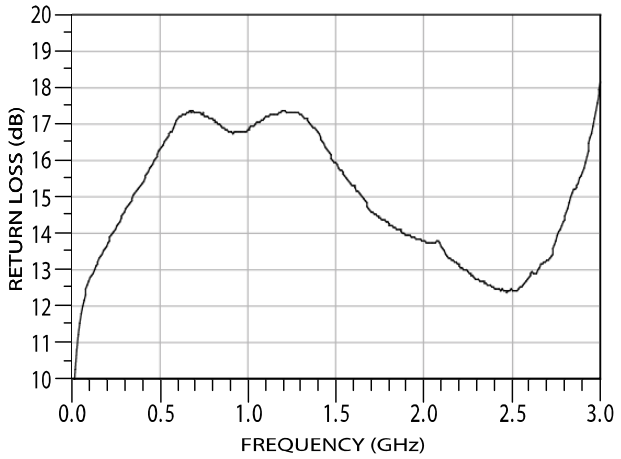

Figure 7. Return Loss vs. Frequency

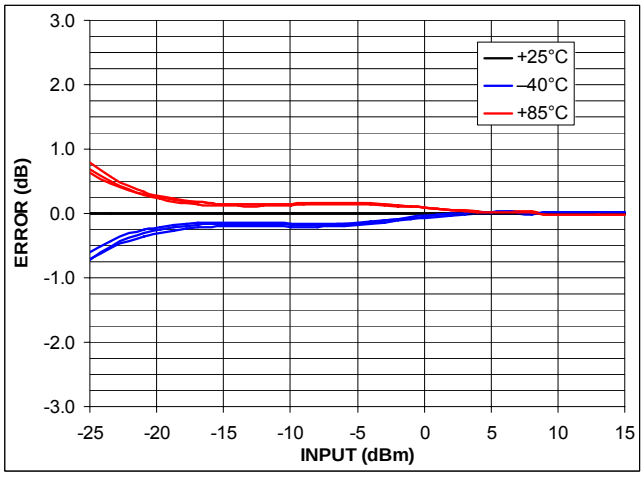

Figure 8. Output Delta from +25°C Output Voltage for 3 Devices at −40°C and +85°C, Frequency 100 MHz, Supply 5.0 V

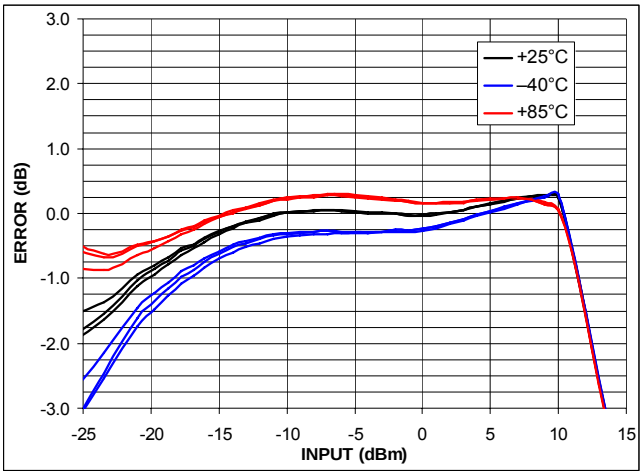

Figure 9. Temperature Drift Distributions for 3 Devices at –40°C, +25°C, and +85°C vs. +25°C Linear Reference, Frequency 900 MHz, Supply 5.0 V

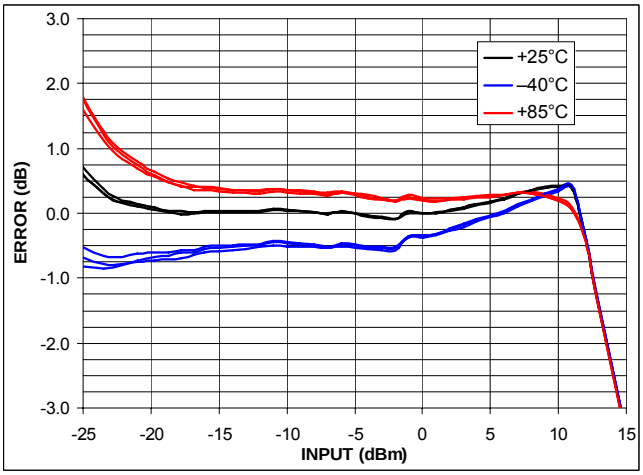

Figure 10. Temperature Drift Distributions for 3 Devices at –40°C, +25°C, and +85°C vs. +25°C Linear Reference, Frequency 1900 MHz, Supply 5.0 V

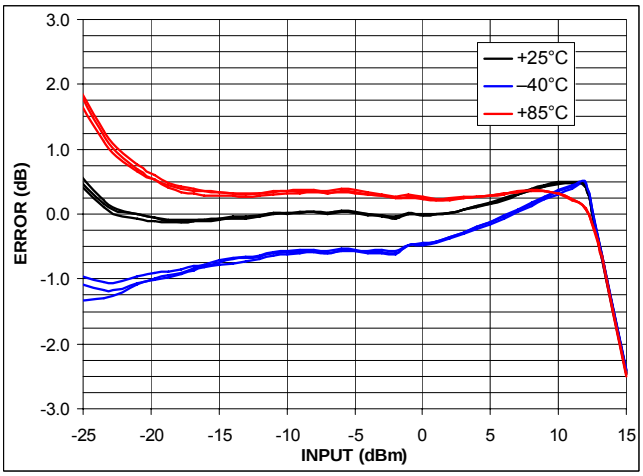

Figure 11. Temperature Drift Distributions for 3 Devices at –40°C, +25°C, and +85°C vs. +25°C Linear Reference, Frequency 2350 MHz, Supply 5.0 V

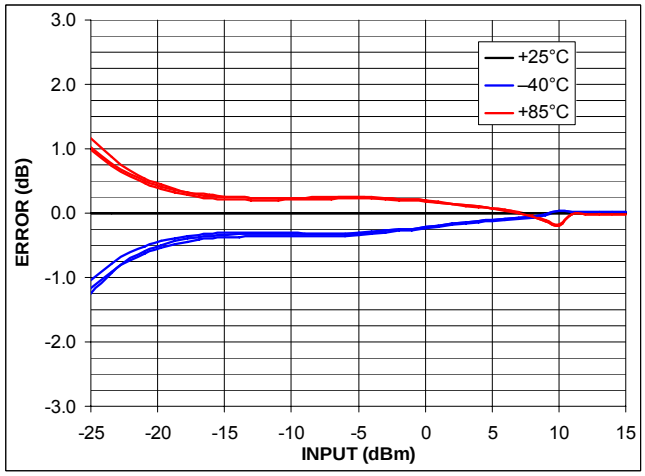

Figure 12. Output Delta from +25°C Output Voltage for 3 Devices at –40°C and +85°C, Frequency 900 MHz, Supply 5.0 V

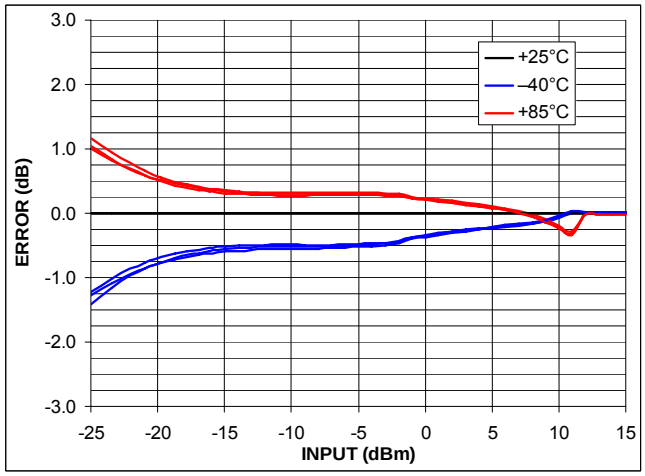

Figure 13. Output Delta from +25°C Output Voltage for 3 Devices at –40°C and +85°C, Frequency 1900 MHz, Supply 5.0 V

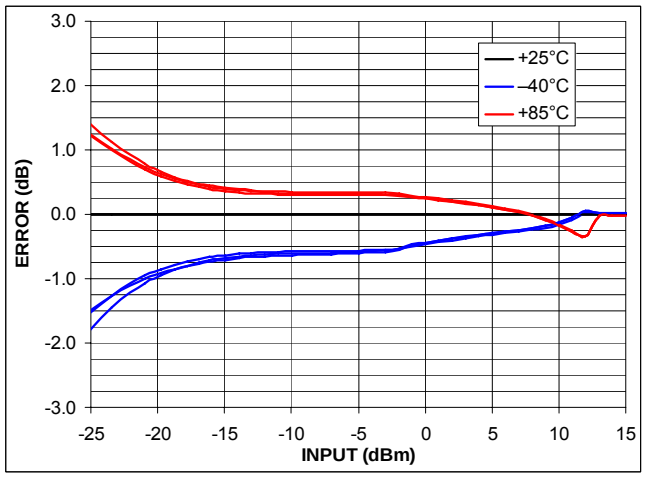

Figure 14. Output Delta from +25°C Output Voltage for 3 Devices at –40°C and +85°C, Frequency 2350 MHz, Supply 5.0 V

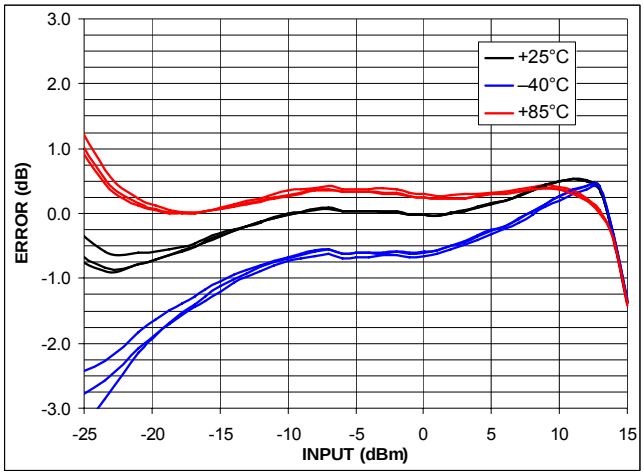

Figure 15. Temperature Drift Distributions for 3 Devices at −40°C, +25°C, and +85°C vs. +25°C Linear Reference, Frequency 2700 MHz, Supply 5.0 V

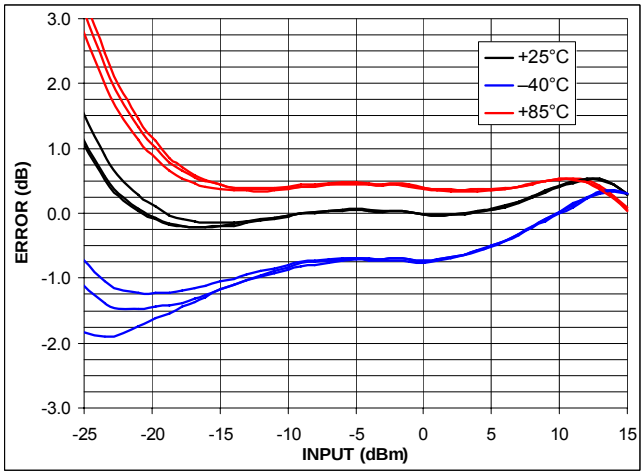

Figure 16. Temperature Drift Distributions for 3 Devices at −40°C, +25°C, and +85°C vs. +25°C Linear Reference, Frequency 3500 MHz, Supply 5.0 V

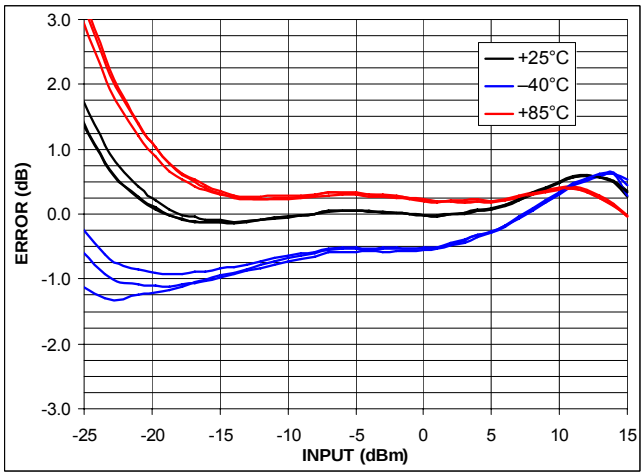

Figure 17. Temperature Drift Distributions for 3 Devices at −40°C, +25°C, and +85°C vs. +25°C Linear Reference, Frequency 3900 MHz, Supply 5.0 V

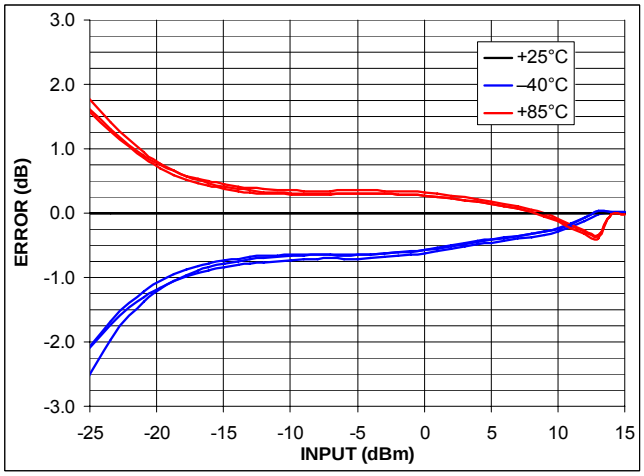

Figure 18. Output Delta from +25°C Output Voltage for 3 Devices at −40°C and +85°C, Frequency 2700 MHz, Supply 5.0 V

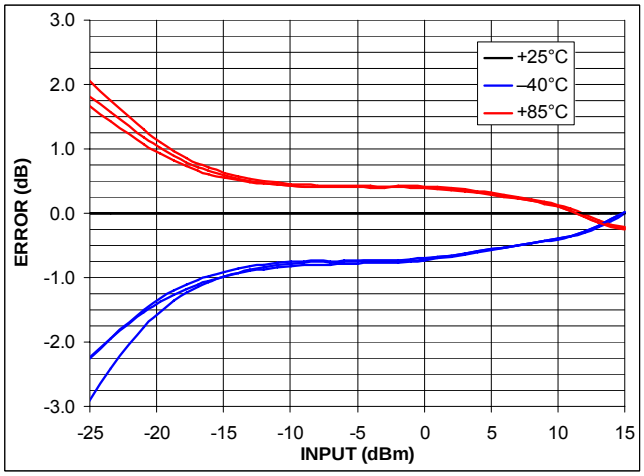

Figure 19. Output Delta from +25°C Output Voltage for 3 Devices at −40°C and +85°C, Frequency 3500 MHz, Supply 5.0 V

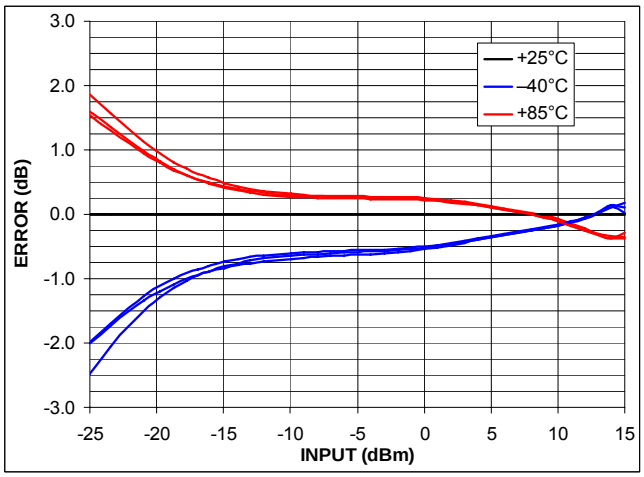

Figure 20. Output Delta from +25°C Output Voltage for 3 Devices at −40°C and +85°C, Frequency 3900 MHz, Supply 5.0 V

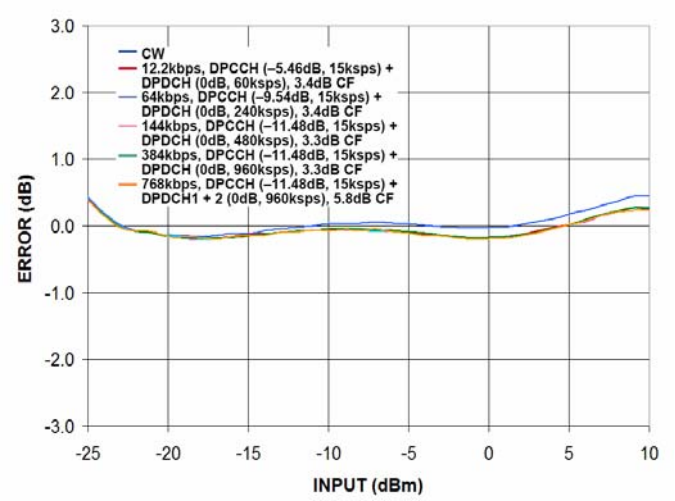

Figure 21. Error from CW Linear Reference vs. Input with Various WCDMA Up Link Waveforms at 1900 MHz, C_{FLTR} = Open, C_{OUT} = 100 nF

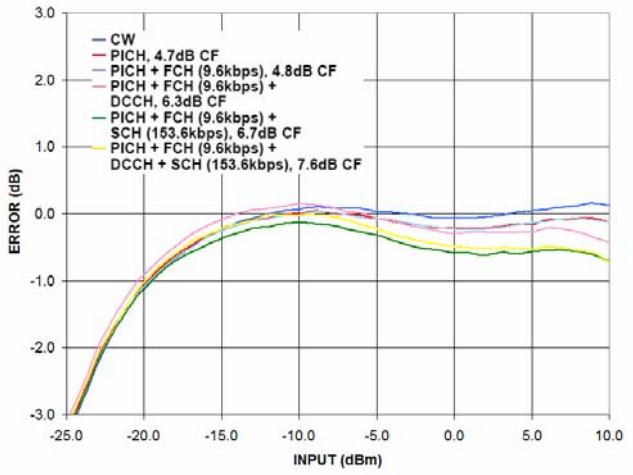

Figure 22. Error from CW Linear Reference vs. Input with Various CDMA2000 Reverse Link Waveforms at 900 MHz, C_{FLTR} = 1 nF, C_{OUT} = 100 nF

EVALUATION BOARD

Figure 23 shows the schematic of the ADL5501 evaluation board. The layout and silkscreen of the evaluation board layers are shown in Figure 24 to Figure 27. The board is powered by a single supply in the 2.7 V to 5.5 V range. The power supply is decoupled by 100 pF and 0.1 µF capacitors. Table 4 details the various configuration options of the evaluation board.

Problems caused by impedance mismatch can arise using the evaluation board to examine the ADL5501 performance. One way to reduce these problems is to put a coaxial 3 dB attenuator on the RFIN SMA connector. Mismatches at the source, cable, and cable interconnection, as well as those occurring on the evaluation board, can cause these problems.

A simple (and common) example of such a problem is triple travel due to mismatch at both the source and the evaluation board. Here the signal from the source reaches the evaluation board and mismatch causes a reflection. When that reflection reaches the source mismatch, it causes a new reflection, which travels back to the evaluation board, adding to the original signal incident at the board. The resultant voltage varies with both cable length and frequency dependence on the relative phase of the initial and reflected signals. Placing the 3 dB pad at the input of the board improves the match at the board and thus reduces the sensitivity to mismatches at the source. When such precautions are taken, measurements are less sensitive to cable length and other fixture issues. In an actual application when the distance between ADL5501 and source is short and well-defined, this 3 dB attenuator is not needed.

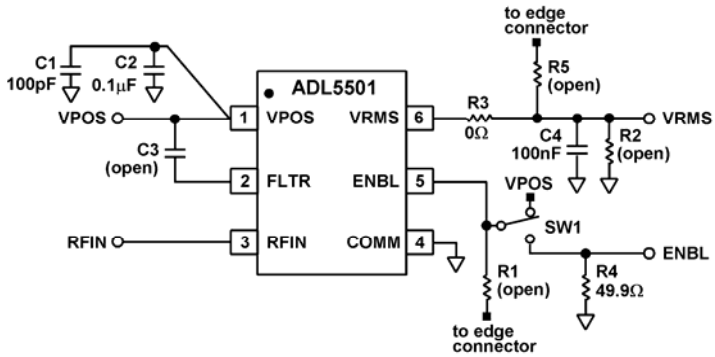

Figure 23. Evaluation Board Schematic

Table 4. Evaluation Board Configuration Options

Component	Description	Default Condition
VPOS, GND	Ground and Supply Vector Pins.	Not Applicable
C1, C2	Power Supply Decoupling. The nominal supply decoupling of 0.01 µF and 100 pF.	C1 = 0.1 µF (Size 0402) C2 = 100 pF (Size 0402)
C3	Filter Capacitor. The internal averaging capacitor can be augmented by placing additional capacitance in C3.	C3 = Open (Size 0402)
R2, R3, C4	Output Filtering. The combination of the internal 100 Ω output resistance and C4 produce a low-pass filter to reduce output ripple. The output can also be scaled down using the resistor divider pads, R3 and R8. In addition, resistors and capacitors can be placed in C4 and R8 to load test VRMS.	R2 = Open (Size 0402) R3 = 0 Ω (Size 0402) C4 = 100 nF (Size 0402)
R4, SW1	Device Enable. When the switch is set towards the "SW1" label, the ENBL pin is connected to VPOS and the ADL5501 is in operating mode. In the opposite switch position, the ENBL pin is grounded (through the 49.9 Ω resistor) putting the device in power-down mode. While in this switch position, the ENBL pin can be driven by a signal generator via the SMA labeled ENBL. In this case, R4 serves as a termination resistor for generators requiring a 50 Ω match.	R4 = 49.9 Ω (Size 0402) SW1 = towards "SW1" label
R1, R5	Alternate Interface. R6 allows VOUT to be accessible from the edge connector, which is only used for characterization.	R1 = Open (Size 0402) R5 = Open (Size 0402)

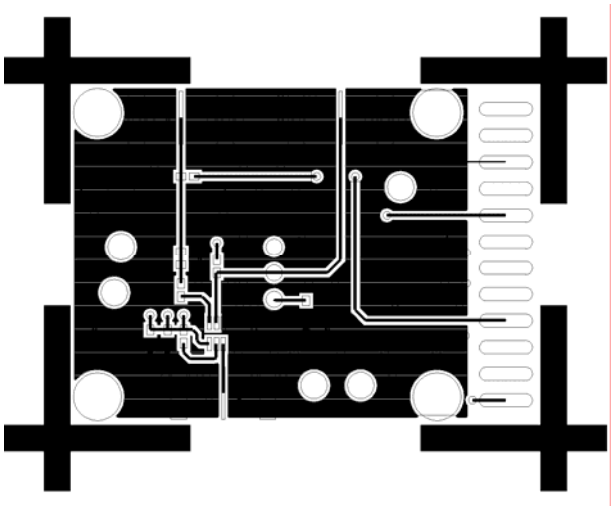

Figure 24. Layout of Component Side

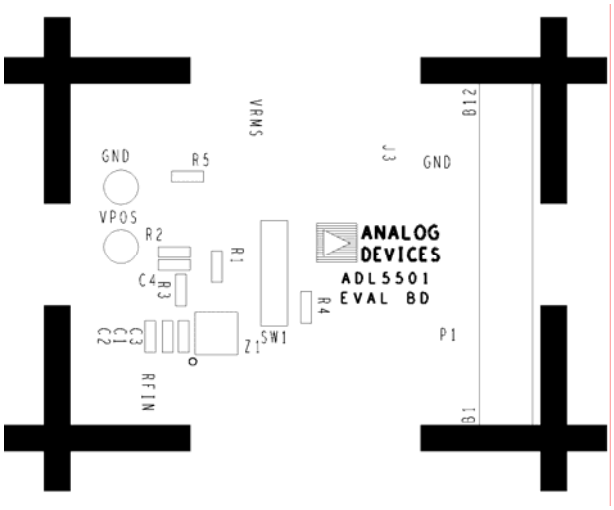

Figure 26. Silkscreen of Component Side

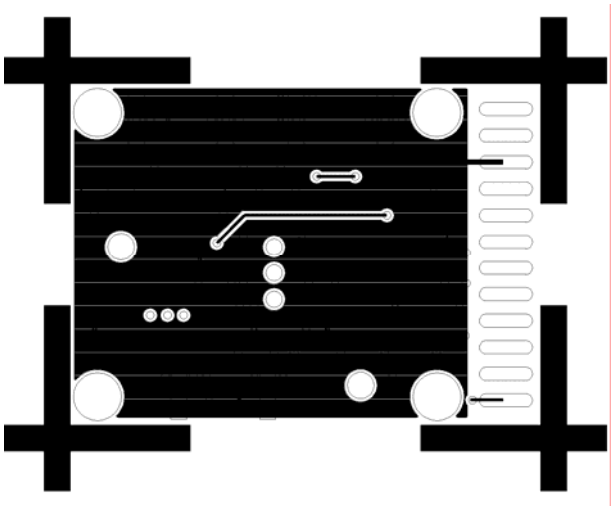

Figure 25. Layout of Circuit Side

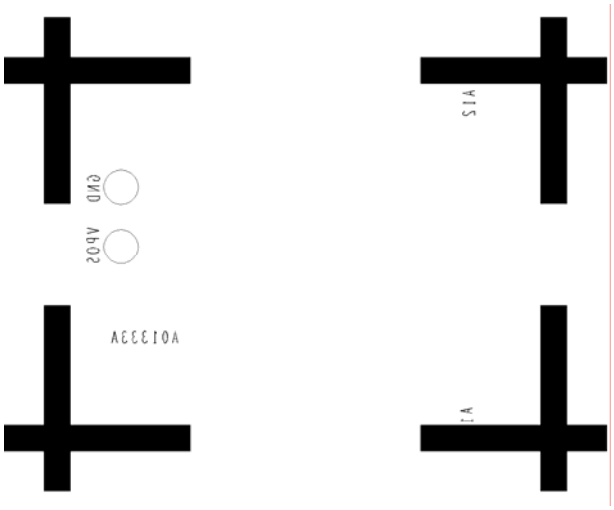

Figure 27. Silkscreen of Circuit Side

OUTLINE DIMENSIONS

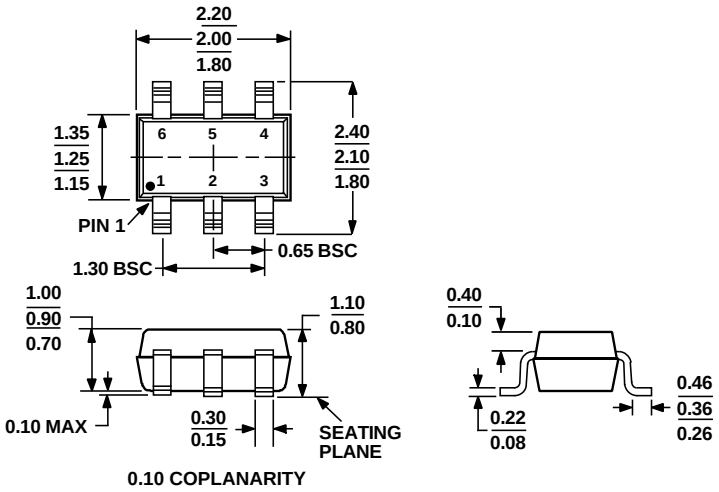

Figure 28. 6-Lead Thin Shrink Small Outline Transistor Package [SC-70] (KS-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Outline	Branding	Ordering Quantity
ADL5501AKSZ-R7[1]	–40°C to +85°C	6-Lead SC-70, 7″Tape and Reel	KS-6	Q0Z	3,000
ADL5501AKSZ-R2[1]	–40°C to +85°C	6-Lead SC-70, 7″Tape and Reel	KS-6	Q0Z	250
ADL5501-EVAL		Evaluation Board			

[1] Z = Pb-free part.

NOTES

PR06056-0-5/06(PrB)