Precision Wide-range (3 nA - 3 mA) High-Side Current Mirror

Preliminary Technical Data

ADL5315

FEATURES

Accurately mirrors input current (1:1 ratio) over 6 decades
Linearity 1% from 3 nA to 3 mA
Stable mirror input voltage
Voltage held 1 V below supply using internal reference or may be set externally
Adjustable input current limit
2.7 V to 8 V single-supply operation
Miniature 8-lead chip scale package (LFCSP 2 mm × 3 mm)

APPLICATIONS

Optical power monitoring from a single photodiode
General voltage biasing with precision current monitoring
Voltage-to-current conversion

GENERAL DESCRIPTION

The ADL5315* is a wide input current range precision high-side current mirror featuring a stable and user-adjustable input voltage. It is optimized for use with PIN photodiodes, but its flexibility and wide operating range make it suitable for a broad array of additional applications. The current sourced from the INPT pin, over a range of 3 nA to 3 mA, is accurately mirrored with a 1:1 ratio and sourced from the IOUT output pin. In a typical photodiode application, the output drives a current-input logarithmic amplifier to produce a linear-in-dB output representing the optical power incident upon the photodiode. For linear voltage output a single resistor to ground is all that is required. The photodiode anode may be connected to a high-speed transimpedance amplifier for the extraction of the data stream. The voltage at the INPT pin is temperature stable with respect to the voltage at the VSET input pin, which it tracks. A temperature stable reference voltage is provided at pin SREF, which, when tied to VSET, fixes the voltage at INPT 1.0 V below VPOS. VSET may also be driven from an external source. The VSET input has very low input current and may be driven as low as the bottom rail, facilitating non-loading voltage-to-current conversion as well as minimizing dark current in photodiode applications.

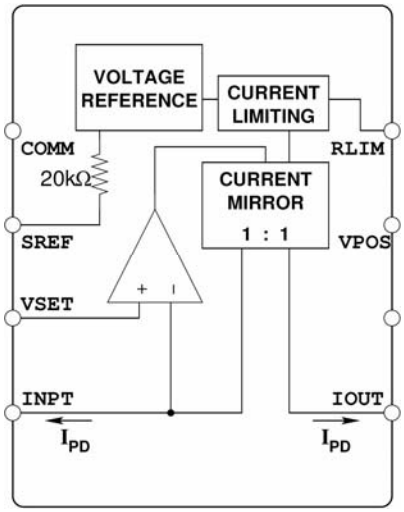

Figure 1. Functional Block Diagram

The ADL5315 also features adjustable input current limiting using an external resistor from RLIM to VPOS. The maximum current sourced by INPT (and IOUT) can be set between 1 mA and 16 mA, beyond which the voltage at INPT falls rapidly from its setpoint. Connecting RLIM directly to VPOS provides basic input short circuit protection with the default current limit of 16 mA typical.

The ADL5315 is available in a 2 x 3 mm 8-lead LFCSP package and is specified for operation from −40°C to +85°C.

Rev. PrC

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ADL5315—Specifications

Table 1. V_{POS} = 5 V, I_{PD} = 3 μA, T_A = 25°C, unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
CURRENT MIRROR OUTPUT	IOUT (Pin 8)				
Current Gain from INPT to IOUT	−40°C < T_A < +85°C	TBD	1.00	TBD	A/A
Nonlinearity	3 nA < I_{PD} < 3 mA		1	TBD	%
Small-signal Bandwidth	I_{PD} = 3 nA		2		kHz
	I_{PD} = 3 μA		2		MHz
Wideband Noise at IPDM	I_{PD} = 3 μA		20		nArms
Output Voltage Range		0		V_{POS} - 1	V
$I_{OUT} \cdot R_{OUT}$ Product	I_{PD} = 3 μA		1500		V
MIRROR INPUT, VOLTAGE CONTROL	INPT (Pin1), VSET (Pin 2), SREF (Pin 3)				
Specified Input Current Range, I_{PD}	Flows from INPT pin	3n		3m	A
VSET Voltage Range	2.7 V < V_{POS} < 6.5 V	0		V_{POS} – 1	V
	6.5 V < V_{PHV} < 8 V	V_{POS} – 6.5		V_{POS} – 1	V
Incremental Gain from VSET to INPT	0.2 V < V_{SET} < 8.0 V	TBD	1	TBD	V/V
Incremental Input Resistance at VSET	V_{SET} = 4.0 V	500			MOhms
Input Bias Current at VSET	V_{SET} = 4.0 V			0.1	nA
SREF Voltage, relative to V_{POS}	2.7 V < V_{POS} < 8 V	TBD	-1.0	TBD	V
OVERCURRENT PROTECTION					
INPT Current Compliance Limit	V_{INPT} deviation of 200 mV , R_{LIM} = 0	TBD	16	TBD	mA
	V_{INPT} deviation of 200 mV , R_{LIM} = 9 kohm	TBD	4	TBD	mA
POWER SUPPLY	VPOS (Pin 6)				
Supply Voltage Range		2.7		8	V
Quiescent Current	I_{PD} = 3 μA		1.8	TBD	mA
	I_{PD} = 3 mA		8.3	TBD	mA

ABSOLUTE MAXIMUM RATINGS

Table 2. ADL5315 Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	8 V
Input Current at INPT	20 mA
Internal Power Dissipation	400 mW
θ_{JA} (soldered exposed paddle)	80°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

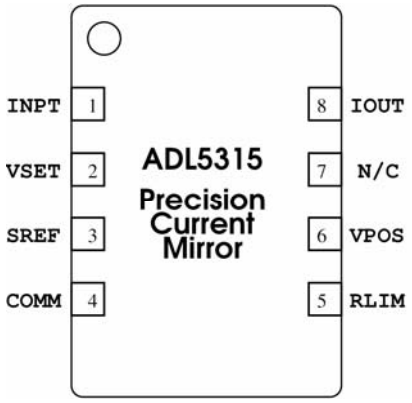

Figure 2. 8-Lead Leadframe Chip Scale Package (LFCSP) and 6-Lead SOT23

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	**INPT**	Input Current. Pin sources current only.
2	**VSET**	Sets voltage at INPT (gain=1). Range 0 V to VPOS -1.0 V. Optional shielding of INPT trace.
3	**SREF**	Reference voltage for VSET. Internally generated at VPOS – 1.0 V through 20 KΩ. May be shorted to VSET for standard mirror operation.
4	**COMM**	Analog Ground.
5	**RLIM**	External resistor to VPOS sets current limit at INPT from 1 mA to 16 mA. I_{LIM} = 48 V / (R_{LIM} + 3 KΩ).
6	**VPOS**	Positive Supply (2.7 V to 8.0 V).
7	**N/C**	Optional shielding of IOUT trace. No connection to die.
8	**IOUT**	Output Current. Mirrors current at INPT with a gain of 1.0. Sources current only.

TYPICAL PERFORMANCE CHARACTERISTICS

(V_P = 5 V, V_{SET} = 4 V, T_A = 25°C, unless otherwise noted.

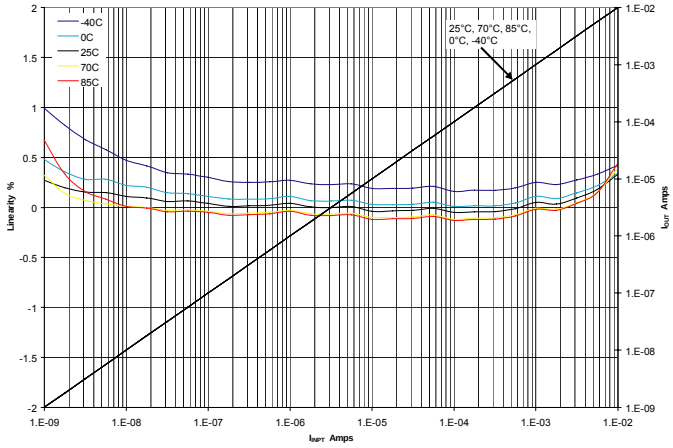

Figure 3. I_{OUT} Error vs. I_{INPT} for Multiple Temperatures, Normalized to 25°C and I_{INPT} = 3uA

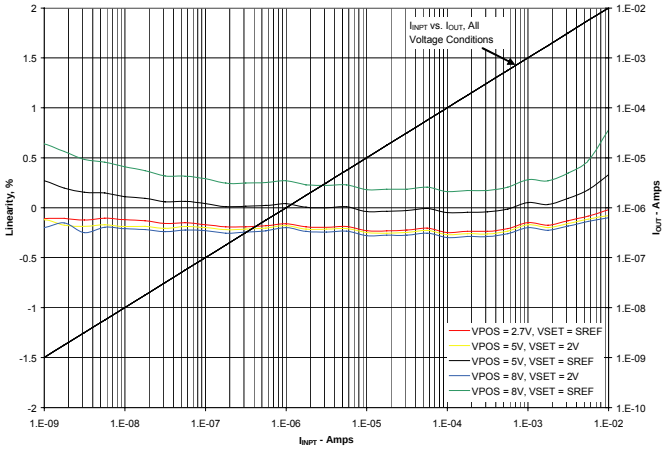

Figure 6. I_{OUT} Linearity vs. I_{INPT} for Multiple Supply Conditions, Normalized to I_{INPT} = 3uA

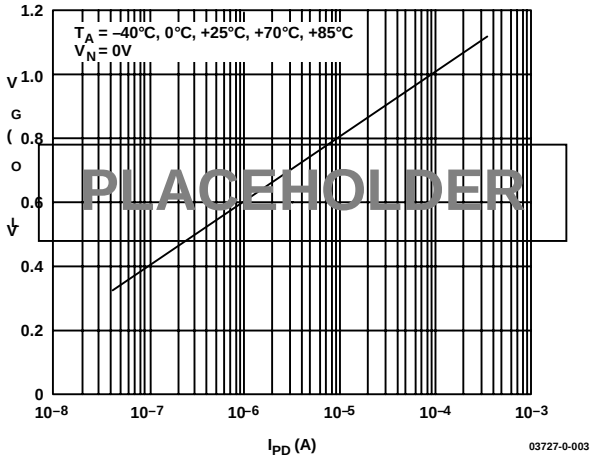

Figure 4.

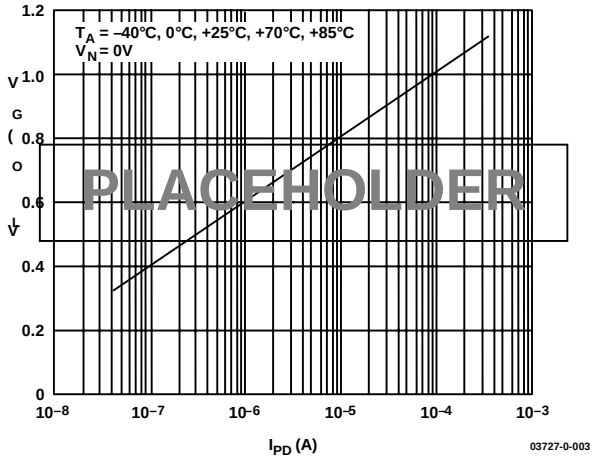

Figure 7.

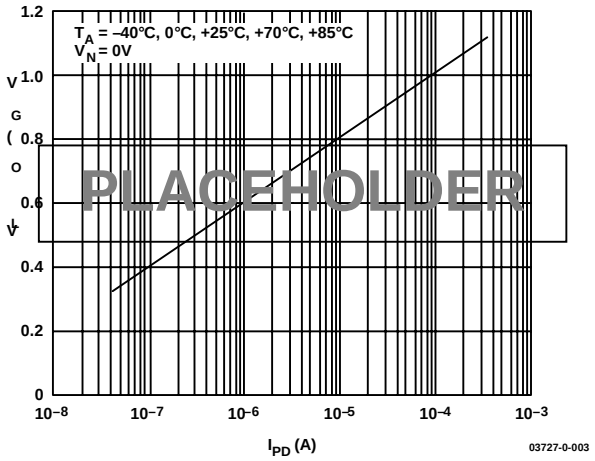

Figure 5.

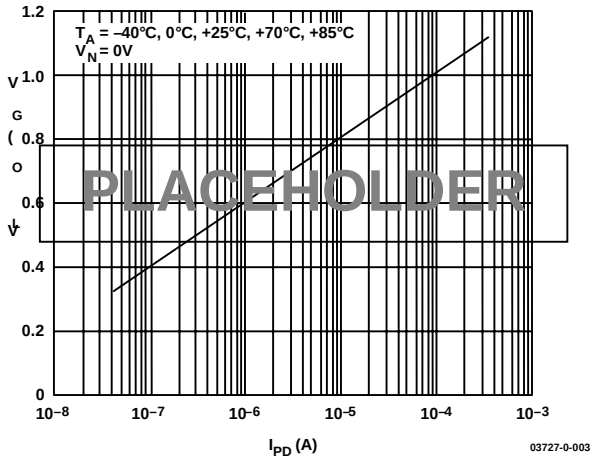

Figure 8.

APPLICATIONS

The ADL5315 is primarily designed for wide dynamic range applications simplifying power monitoring designs where access is only permitted to the cathode of a PIN photodiode or receiver module. Figure 9 shows a typical application when the ADL5315 is used to provide an accurate bias to a PIN diode while simultaneously mirroring the diode current to be measured by a translinear logarithmic amplifier.

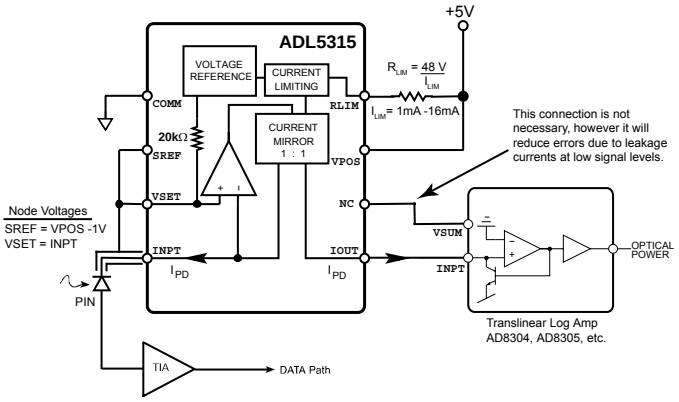

Figure 9. Typical Application Using the ADL5315

In this application, the ADL5315 sets the bias voltage on the PIN diode. This voltage is delivered at Pin INPT and is controlled by the voltage at Pin VSET. VSET is driven by the onboard reference available at Pin SREF which is equal to VPOS – 1 V.

The input current, I_{PD}, is precisely mirrored at a ratio of 1:1 to Pin IOUT. This interface is optimized for use with any of the Analog Devices translinear logarithmic amplifiers (for example, the AD8304 or AD8305) to offer a precise, wide dynamic range measurement of the optical power incident upon the PIN.

If a linear voltage output is preferred at IOUT, a single external resistor to ground is all that is necessary to perform the conversion.

AVERAGE POWER MONITORING

In those applications where a modulated signal is incident upon the photodiode it may be desired to measure the average power of the signal. Figure 10 shows the connections necessary for using the ADL5315 in such a measurement system.

The value of the capacitor to ground should be selected in order to eliminate errors due to modulation of the ADL5315 input current.

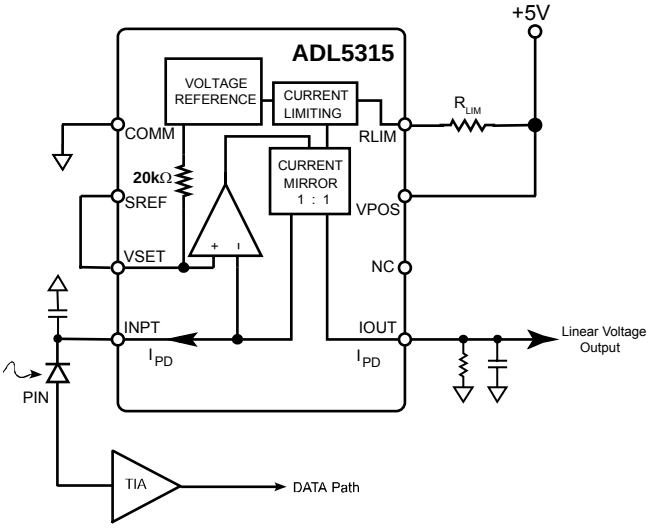

Figure 10. Average Power Monitoring using the ADL5315

TRANSLINEAR LOG AMP INTERFACING

The mirror current output, IOUT, of the ADL5315 is designed to interface directly to an Analog Devices translinear logarithmic amplifier, such as the AD8304, AD8305, or ADL5306. Figure 11 shows the basic connections necessary for interfacing the ADL5315 to the AD8305. In this configuration, the designer can use the full current mirror range of the ADL5315 for high accuracy power monitoring.

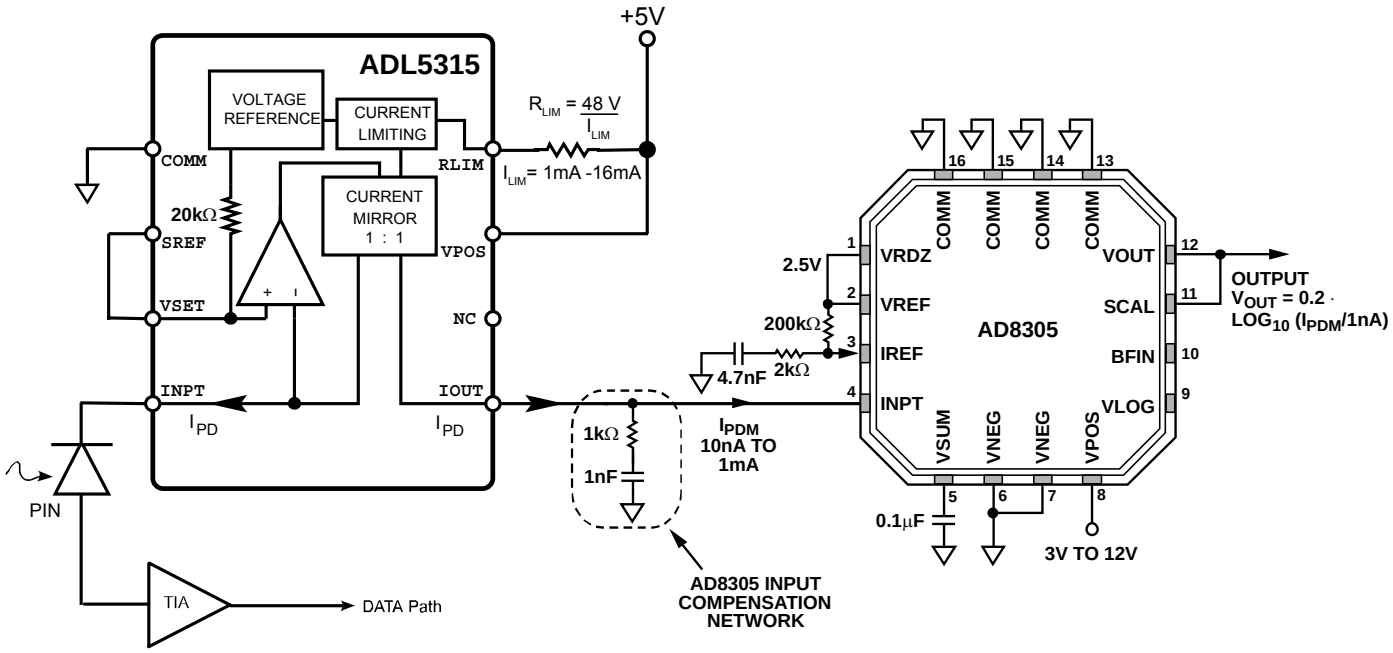

Figure 11. Interfacing the ADL5315 to the AD8305 for High Accuracy PIN Power Monitoring

Measured rms noise voltage at the output of the AD8305 vs. input current is shown in Figure 12 for the AD8305 by itself and in cascade with the ADL5315. The relatively low noise produced by the ADL5315, combined with the additional noise filtering inherent in the frequency response characteristics of the AD8305 result in minimal degradation to the noise performance of the AD8305.

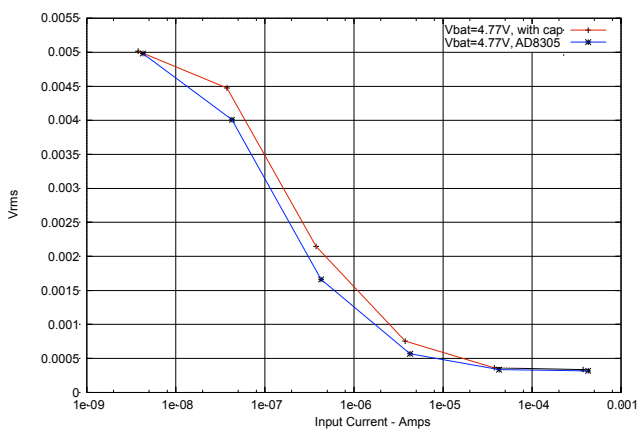

Figure 12. Measured RMS Noise of AD8305 vs. AD8305 Cascaded with ADL5315

EVALUATION BOARD

Table 4. Evaluation Board (Rev A) Configuration Options

Component	Function	Default Conditions
VPOS, GND	**Supply and Ground Connections**	Not Applicable
INPUT, L1, C4	**Input Interface:** The evaluation board is configures to accept an input current at the SMA connector labeled INPUT. Filtering of this current can be done using L1 and C4.	L1 = 0 Ω (Size 0805) C4 = open (Size 00603)
R4, C3	**PIN Input Compensation:** Provides essential HF compensation at the INPT pin.	C3 = 390 pF (size 0805) R4 = 4.02 kΩ (size 0402)
SREF, VSET, SW1, R1, R6, R7	**INPT Bias Voltage:** The dc voltage applied to VSET determines the voltage at INPT, VSET = INPT. Connecting SREF to VSET sets the bias at INPT to be 1V below VPOS. Opening SW1 allows for VSET to be driven externally via the SMA connector.	SW1 = closed R1 = 100 Ω (size 0402) R6 = R7 = 0 Ω (size 0402)
IOUT, R5	**Output/Mirror Current Interface:** The output current at the SMA connector labeled IOUT is equal to the value at INPT. R5 allows a resistor to be installed for applications where a scaled voltage referenced to I_{PD} is desirable instead of a current.	R5 = open (size 0603)
R2	**Current Limiting:** An external resistor to VPOS sets the current limit at INPT from 1 mA to 16 mA. I_{LIM} = 48 V / R_{LIM}. The eval board is configured such that I_{LIM} = 4.8mA.	R2 = 10 kΩ (size 0402)
C1, C2, R3	**Supply Filtering/Decoupling**	C1 = 0.01 µF (Size 0402) C2 = 0.1 µF (Size 0603) R3 = 0 Ω (Size 0805)

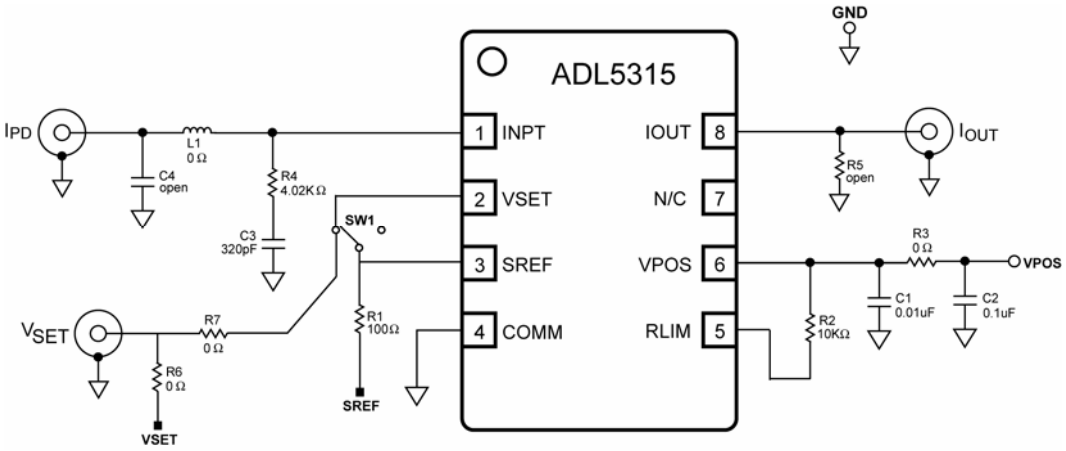

Figure 13. Evaluation Board Schematic (Rev A)

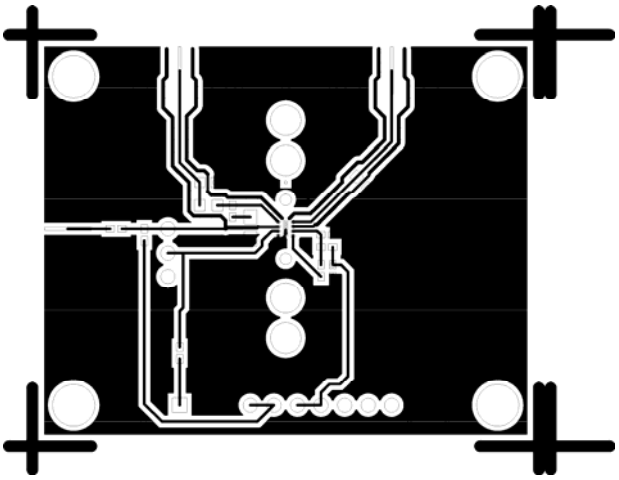

Figure 14. Component Side Layout

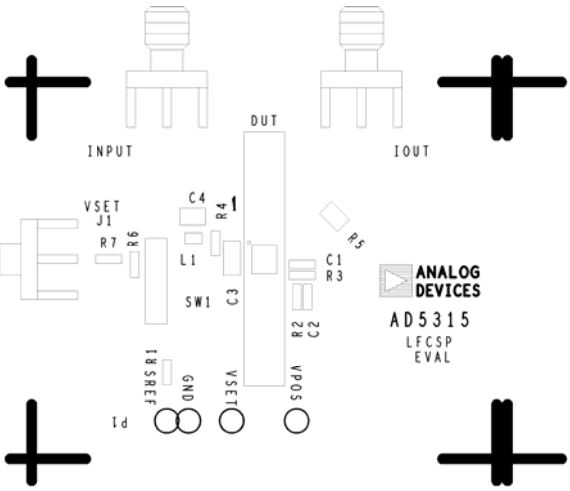

Figure 15. Component Side Silkscreen

OUTLINE DIMENSIONS

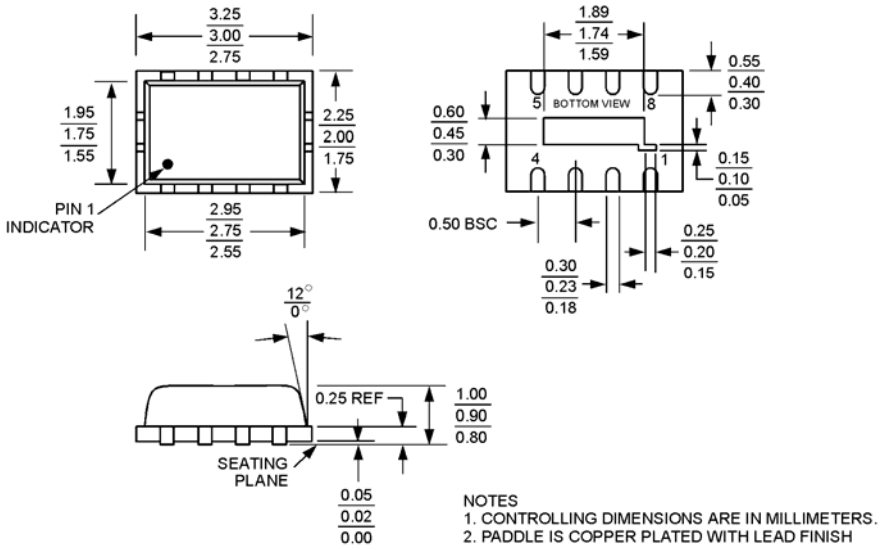

Figure 16. 8-Lead Lead Frame Chip Scale Package

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADL5315 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table 5. Ordering Guide

ADL5315 Products	Temperature Package	Package Description	Package Outline	Branding
ADL5315XCP	–40°C to +85°C	8-Lead LFCSP		
ADL5315-EVAL		Evaluation Board		

PR05694-0-8/05(PrC)

ANALOG DEVICES

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