# Low Voltage 1.15 V to 5.5 V, Single-Channel Bidirectional Logic Level Translator

Preliminary Technical Data

# ADG3301

## FEATURES

**Bidirectional level translation**
**Operates from 1.15 V to 5.5 V**
**Low quiescent current < 1 µA**
**No direction pin**

## APPLICATIONS

**SPI®, MICROWIRE® level translation**
**Low voltage ASIC level translation**
**Smart card readers**
**Cell phones and cell phone cradles**
**Portable communication devices**
**Telecommunications equipment**
**Network switches and routers**
**Storage systems (SAN/NAS)**
**Computing/server applications**
**GPS**
**Portable POS systems**
**Low cost serial interfaces**

## FUNCTIONAL BLOCK DIAGRAM

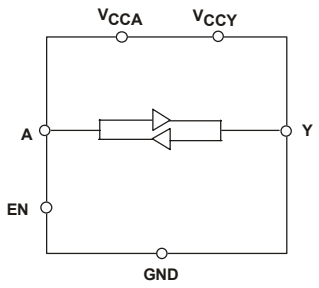


*Figure 1.*

## GENERAL DESCRIPTION

The ADG3301 is a single channel bidirectional logic level translator. It can be used in multivoltage digital system applications such as data transfer between a low voltage DSP/controller and a higher voltage device. The internal architecture allows the device to perform bidirectional logic level translation without an additional signal to set the direction in which the translation takes place.

The voltage applied to $V_{CCA}$ sets the logic levels on the A side of the device, while $V_{CCY}$ sets the levels on the Y side. For proper operation, $V_{CCA}$ must always be less than $V_{CCY}$. The $V_{CCA}$-compatible logic signals applied to the A pin appear as $V_{CCY}$-compatible levels on the Y pin. Similarly, $V_{CCY}$-compatible logic levels applied to the Y pin appear as $V_{CCA}$-compatible logic levels on the A pin.

The enable pin (EN) provides three-state operation on both the A-side and the Y-side pins. When the device enable pin is pulled low, the terminals on both sides of the device are in the high impedance state. The EN pin is referred to the $V_{CCA}$ supply voltage and driven high for normal operation.

The ADG3301 is available in compact 6 lead SC70 package and is guaranteed to operate over the 1.15 V to 5.5 V supply voltage range and extended −40°C to +85°C temperature range.

## PRODUCT HIGHLIGHTS

1. Bidirectional level translation.
2. Fully guaranteed over the 1.15 V to 5.5 V supply range.
3. No direction pin.
4. Compact 6 lead SC70 package.

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# SPECIFICATIONS[1]

$V_{CCY}$ = 1.65 V to 5.5 V, $V_{CCA}$ = 1.15 V to $V_{CCY}$, GND = 0 V. All specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Conditions | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|---|
| LOGIC INPUTS/OUTPUTS | | | | | | |
| A Side | | | | | | |
| Input High Voltage[3] | $V_{IHA}$ | $V_{CCA}$ = 1.15 V | $V_{CCA}$ – 0.3 | | | V |
| | $V_{IHA}$ | $V_{CCA}$ = 1.2 V to 5.5 V | $V_{CCA}$ – 0.4 | | | |
| Input Low Voltage[3] | $V_{ILA}$ | | | | 0.4 | V |
| Output High Voltage | $V_{OHA}$ | $V_Y = V_{CCY}$, $I_{OH}$ = 20 µA, Figure 27 | $V_{CCA}$ – 0.4 | | | V |
| Output Low Voltage | $V_{OLA}$ | $V_Y$ = 0 V, $I_{OL}$ = 20 µA, Figure 27 | | | 0.4 | V |
| Capacitance[3] | $C_A$ | f = 1 MHz, EN = 0, Figure 32 | | 9 | | pF |
| Leakage Current | $I_{LA, HiZ}$ | $V_A$ = 0 V/$V_{CCA}$, EN = 0, Figure 29 | | | ±1 | µA |
| Y Side | | | | | | |
| Input Low Voltage[3] | $V_{IHY}$ | | $V_{CCY}$ – 0.4 | | | V |
| Input High Voltage[3] | $V_{ILY}$ | | | | 0.4 | V |
| Output High Voltage | $V_{OHY}$ | $V_A = V_{CCA}$, $I_{OH}$ = 20 µA, Figure 28 | $V_{CCY}$ – 0.4 | | | V |
| Output Low Voltage | $V_{OLY}$ | $V_A$ = 0 V, $I_{OL}$ = 20 µA, Figure 28 | | | 0.4 | V |
| Capacitance[3] | $C_Y$ | f = 1 MHz, EN = 0, Figure 33 | | 6 | | pF |
| Leakage Current | $I_{LY, HiZ}$ | $V_Y$ = 0 V/$V_{CCY}$, EN = 0, Figure 30 | | | ±1 | µA |
| Enable (EN) | | | | | | |
| Input High Voltage[3] | $V_{IHEN}$ | $V_{CCA}$ = 1.15 V | $V_{CCA}$ – 0.3 | | | V |
| | $V_{IHEN}$ | $V_{CCA}$ = 1.2 V to 5.5 V | $V_{CCA}$ – 0.4 | | | V |
| Input Low Voltage[3] | $V_{ILEN}$ | | | | 0.4 | V |
| Leakage Current | $I_{LEN}$ | $V_{EN}$ = 0 V/$V_{CCA}$, $V_A$ = 0 V, Figure 31 | | | ±1 | µA |
| Capacitance[3] | $C_{EN}$ | | | 3 | | pF |
| Enable Time[3] | $t_{EN}$ | $R_S = R_T$ = 50 Ω, $V_A$ = 0 V/$V_{CCA}$(A→Y), $V_Y$ = 0 V/$V_{CCY}$(Y→A), Figure 34 | | 1 | 1.8 | µs |
| SWITCHING CHARACTERISTICS[3] | | | | | | |
| 3.3 V ± 0.3V≤ $V_{CCA}$≤ $V_{CCY}$,, $V_{CCY}$ = 5 V ± 0.5 V | | | | | | |
| A→Y Level Translation | | $R_S = R_T$ = 50 Ω, $C_L$ = 50 pF, Figure 35 | | | | |
| Propagation Delay | $t_{P, A-Y}$ | | | 6 | 10 | ns |
| Rise Time | $t_{R, A-Y}$ | | | 2 | 3.5 | ns |
| Fall Time | $t_{F, A-Y}$ | | | 2 | 3.5 | ns |
| Maximum Data Rate | $D_{MAX, A-Y}$ | | 50 | | | Mbps |
| Channel-to-Channel Skew | $t_{SKEW, A-Y}$ | | | 2 | 4 | ns |
| Part-to-Part Skew | $t_{PPSKEW, A-Y}$ | | | | 3 | ns |
| Y→A Level Translation | | $R_S = R_T$ = 50 Ω, $C_L$ = 15 pF, Figure 36 | | | | |
| Propagation Delay | $t_{P, Y-A}$ | | | 4 | 7 | ns |
| Rise Time | $t_{R, Y-A}$ | | | 1 | 3 | ns |
| Fall Time | $t_{F, Y-A}$ | | | 3 | 7 | ns |
| Maximum Data Rate | $D_{MAX, Y-A}$ | | 50 | | | Mbps |
| Channel-to-Channel Skew | $t_{SKEW, Y-A}$ | | | 2 | 3.5 | ns |
| Part-to-Part Skew | $t_{PPSKEW, Y-A}$ | | | | 2 | ns |
| 1.8 V ± 0.15 V≤ $V_{CCA}$ ≤$V_{CCY}$, $V_{CCY}$= 3.3 V ± 0.3 V | | | | | | |
| A→Y Translation | | $R_S = R_T$ = 50 Ω, $C_L$ = 50 pF, Figure 35 | | | | |
| Propagation Delay | $t_{P, A-Y}$ | | | 8 | 11 | ns |
| Rise Time | $t_{R, A-Y}$ | | | 2 | 5 | ns |
| Fall Time | $t_{F, A-Y}$ | | | 2 | 5 | ns |
| Maximum Data Rate | $D_{MAX, A-Y}$ | | 50 | | | Mbps |
| Channel-to-Channel Skew | $t_{SKEW, A-Y}$ | | | 2 | 4 | ns |
| Part-to-Part Skew | $t_{PPSKEW, A-Y}$ | | | | 4 | ns |

| Parameter | Symbol | Conditions | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|---|
| Y→A Translation | | $R_S = R_T = 50\ \Omega$, $C_L = 15$ pF, Figure 36 | | | | |
| Propagation Delay | $t_{P, Y-A}$ | | | 5 | 8 | ns |
| Rise Time | $t_{R, Y-A}$ | | | 2 | 3.5 | ns |
| Fall Time | $t_{F, Y-A}$ | | | 2 | 3.5 | ns |
| Maximum Data Rate | $D_{MAX, Y-A}$ | | 50 | | | Mbps |
| Channel-to-Channel Skew | $t_{SKEW, Y-A}$ | | | 2 | 3 | ns |
| Part-to-Part Skew | $t_{PPSKEW, Y-A}$ | | | | 3 | ns |
| 1.15 V to 1.3 V≤ $V_{CCA}$ ≤$V_{CCY}$, $V_{CCY}$= 3.3 V ± 0.3 V | | | | | | |
| A→Y Translation | | $R_S = R_T = 50\ \Omega$, $C_L = 50$ pF, Figure 35 | | | | |
| Propagation Delay | $t_{P, A-Y}$ | | | 9 | 18 | ns |
| Rise Time | $t_{R, A-Y}$ | | | 3 | 5 | ns |
| Fall Time | $t_{F, A-Y}$ | | | 2 | 5 | ns |
| Maximum Data Rate | $D_{MAX, A-Y}$ | | 40 | | | Mbps |
| Channel-to-Channel Skew | $t_{SKEW, A-Y}$ | | | 2 | 5 | ns |
| Part-to-Part Skew | $t_{PPSKEW, A-Y}$ | | | | 10 | ns |
| Y→A Translation | | $R_S = R_T = 50\ \Omega$, $C_L = 15$ pF, Figure 36 | | | | |
| Propagation Delay | $t_{P, Y-A}$ | | | 5 | 9 | ns |
| Rise Time | $t_{R, Y-A}$ | | | 2 | 4 | ns |
| Fall Time | $t_{F, Y-A}$ | | | 2 | 4 | ns |
| Maximum Data Rate | $D_{MAX, Y-A}$ | | 40 | | | Mbps |
| Channel-to-Channel Skew | $t_{SKEW, Y-A}$ | | | 2 | 4 | ns |
| Part-to-Part Skew | $t_{PPSKEW, Y-A}$ | | | | 4 | ns |
| 1.15 V to 1.3 V≤ $V_{CCA}$ ≤$V_{CCY}$, $V_{CCY}$ = 1.8 V ± 0.3 V | | | | | | |
| A→Y Translation | | $R_S = R_T = 50\ \Omega$, $C_L = 50$ pF, Figure 35 | | | | |
| Propagation Delay | $t_{P, A-Y}$ | | | 12 | 25 | ns |
| Rise Time | $t_{R, A-Y}$ | | | 7 | 12 | ns |
| Fall Time | $t_{F, A-Y}$ | | | 3 | 5 | ns |
| Maximum Data Rate | $D_{MAX, A-Y}$ | | 25 | | | Mbps |
| Channel-to-Channel Skew | $t_{SKEW, A-Y}$ | | | 2 | 5 | ns |
| Part-to-Part Skew | $t_{PPSKEW, A-Y}$ | | | | 15 | ns |
| Y→A Translation | | $R_S = R_T = 50\ \Omega$, $C_L = 15$ pF, Figure 36 | | | | |
| Propagation Delay | $t_{P, Y-A}$ | | | 14 | 35 | ns |
| Rise Time | $t_{R, Y-A}$ | | | 5 | 16 | ns |
| Fall Time | $t_{F, Y-A}$ | | | 2.5 | 6.5 | ns |
| Maximum Data Rate | $D_{MAX, Y-A}$ | | 25 | | | Mbps |
| Channel-to-Channel Skew | $t_{SKEW, Y-A}$ | | | 3 | 6.5 | ns |
| Part-to-Part Skew | $t_{PPSKEW, Y-A}$ | | | | 23.5 | ns |
| 2.5 V ± 0.2 V ≤ $V_{CCA}$ ≤$V_{CCY}$, $V_{CCY}$ = 3.3 V ± 0.3 V | | | | | | |
| A→Y Translation | | $R_S = R_T = 50\ \Omega$, $C_L = 50$ pF, Figure 35 | | | | |
| Propagation Delay | $t_{P, A-Y}$ | | | 7 | 10 | ns |
| Rise Time | $t_{R, A-Y}$ | | | 2.5 | 4 | ns |
| Fall Time | $t_{F, A-Y}$ | | | 2 | 5 | ns |
| Maximum Data Rate | $D_{MAX, A-Y}$ | | 60 | | | Mbps |
| Channel-to-Channel Skew | $t_{SKEW, A-Y}$ | | | 1.5 | 2 | ns |
| Part-to-Part Skew | $t_{PPSKEW, A-Y}$ | | | | 4 | ns |
| Y→A Translation | | $R_S = R_T = 50\ \Omega$, $C_L = 15$ pF, Figure 36 | | | | |
| Propagation Delay | $t_{P, Y-A}$ | | | 5 | 8 | ns |
| Rise Time | $t_{R, Y-A}$ | | | 1 | 4 | ns |
| Fall Time | $t_{F, Y-A}$ | | | 3 | 5 | ns |
| Maximum Data Rate | $D_{MAX, Y-A}$ | | 60 | | | Mbps |
| Channel-to-Channel Skew | $t_{SKEW, Y-A}$ | | | 2 | 3 | ns |
| Part-to-Part Skew | $t_{PPSKEW, Y-A}$ | | | | 3 | ns |

| Parameter | Symbol | Conditions | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|---|
| POWER REQUIREMENTS | | | | | | |
| Power Supply Voltages | $V_{CCA}$ | $V_{CCA} \leq V_{CCY}$ | 1.15 | | 5.5 | V |
| | $V_{CCY}$ | | 1.65 | | 5.5 | V |
| Quiescent Power Supply Current | $I_{CCA}$ | $V_A$ = 0 V/$V_{CCA}$, $V_Y$ = 0 V/$V_{CCY}$, $V_{CCA}$ = $V_{CCY}$ = 5.5 V, EN = 1 | | 0.17 | 1 | µA |
| | $I_{CCY}$ | $V_A$ = 0 V/$V_{CCA}$, $V_Y$ = 0 V/$V_{CCY}$, $V_{CCA}$ = $V_{CCY}$ = 5.5 V, EN = 1 | | 0.27 | 1 | µA |
| Three-State Mode Power Supply Current | $I_{HiZA}$ | $V_{CCA}$ = $V_{CCY}$ = 5.5 V, EN = 0 | | 0.1 | 1 | µA |
| | $I_{HiZY}$ | $V_{CCA}$ = $V_{CCY}$ = 5.5 V, EN = 0 | | 0.1 | 1 | µA |

[1] Temperature range is a follows: B version: −40°C to +85°C.
[2] All typical values are at $T_A$ = 25°C, unless otherwise noted.
[3] Guaranteed by design; not subject to production test.

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 2.**

| Parameter | Rating |
|---|---|
| $V_{CCA}$ to GND | −0.3 V to +7 V |
| $V_{CCY}$ to GND | $V_{CCA}$ to +7 V |
| Digtal Inputs (A) | −0.3 V to ($V_{CCA}$ + 0.3 V) |
| Digtal Inputs (Y) | −0.3 V to ($V_{CCY}$ + 0.3 V) |
| EN to GND | −0.3 V to +7 V |
| Operating Temperature Range | |
| Industrial (B Version) | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| $\theta_{JA}$ Thermal Impedance (4-Layer Board) | |
| 6 Lead SC70 | 332°C/W |
| Lead Temperature, Soldering (10 sec) | 300°C |
| IR Reflow, Peak Temperature (< 20 sec) | 260°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

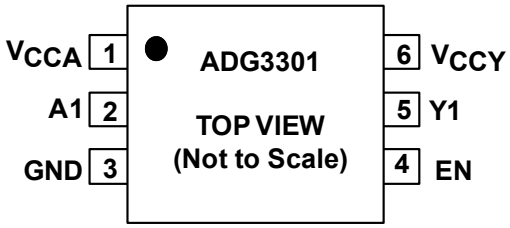



*Figure 2. 6-Lead SC70*

**Table 3 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | $V_{CCA}$ | Power Supply Voltage Input for the A I/O Pin (1.15 V ≤ $V_{CCA}$ ≤ $V_{CCY}$). |
| 2 | A | Input/Output A. Referenced to $V_{CCA}$. |
| 3 | GND | Ground. |
| 4 | EN | Active High Enable input. |
| 5 | Y | Input/Output A4. Referenced to $V_{CCA}$. |
| 6 | $V_{CCY}$ | Power Supply Voltage Input for the Y I/O Pin (1.65 V ≤ $V_{CCY}$ ≤ 5.5V). |

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## TYPICAL PERFORMANCE CHARACTERISTICS

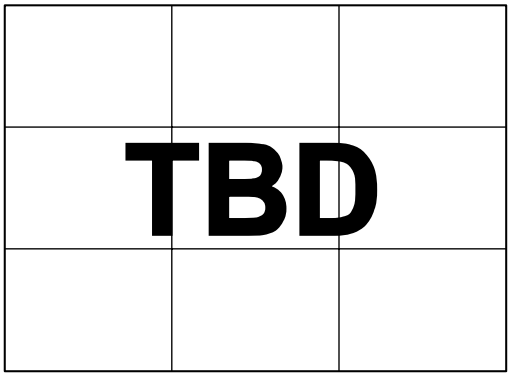



*Figure 3. $I_{CCA}$ vs. Data Rate (A→Y Level Translation)*

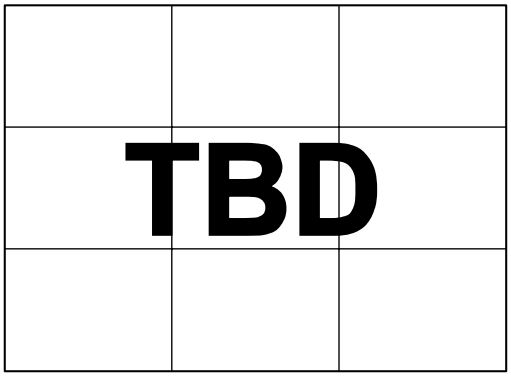



*Figure 6. $I_{CCY}$ vs. Data Rate (Y→A Level Translation)*

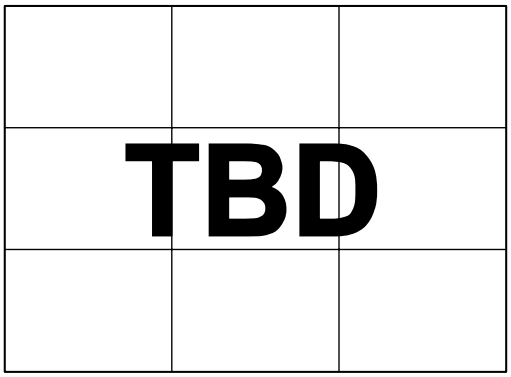



*Figure 4. $I_{CCY}$ vs. Data Rate (A→Y Level Translation)*

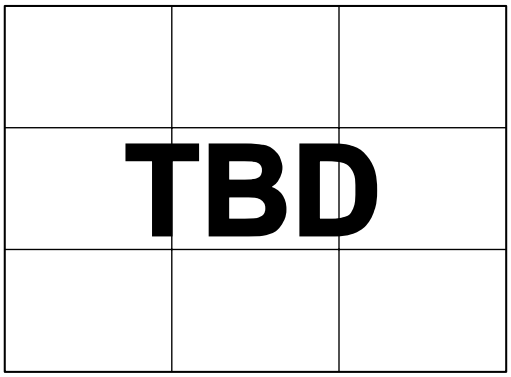



*Figure 7. $I_{CCY}$ vs. Capacitive Load at Pin Y for A→Y (1.2 V→1.8 V) Level Translation*

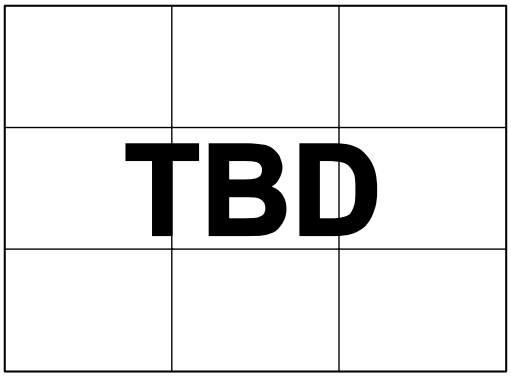



*Figure 5. $I_{CCA}$ vs. Data Rate (Y→A Level Translation)*

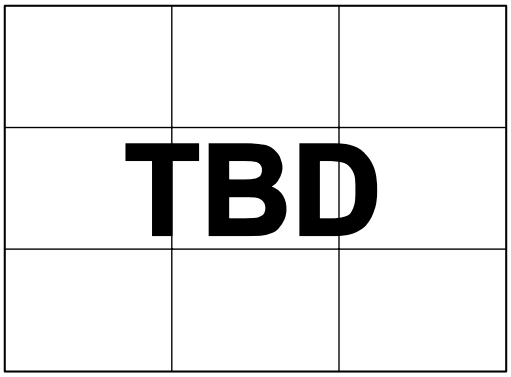



*Figure 8. $I_{CCA}$ vs. Capacitive Load at Pin A for Y→A (1.8 V→1.2 V) Level Translation*

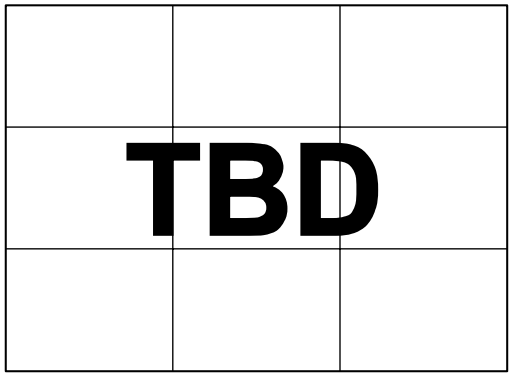



*Figure 9. $I_{CCY}$ vs. Capacitive Load at Pin Y for A→Y (1.8 V→3.3 V) Level Translation*

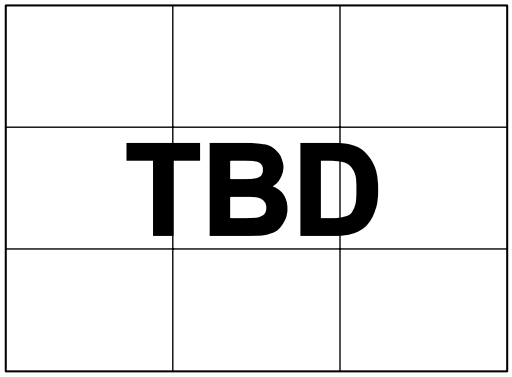



*Figure 10.$I_{CCA}$ vs. Capacitive Load at Pin A for Y→A (3.3 V→1.8 V) Level Translation*

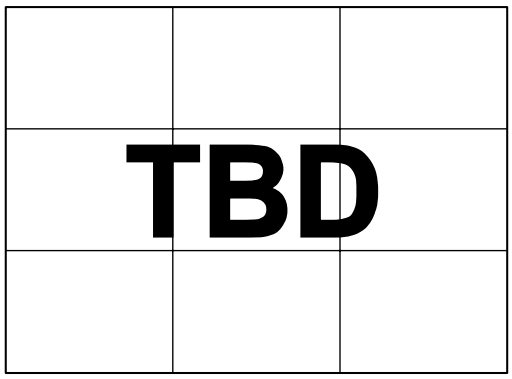



*Figure 11. $I_{CCY}$ vs. Capacitive Load at Pin Y for A→Y (3.3 V→5 V) Level Translation*

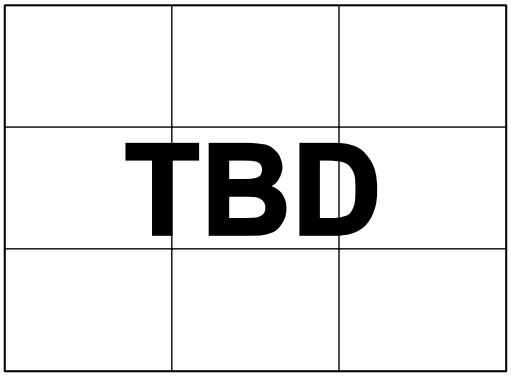



*Figure 12. $I_{CCA}$ vs. Capacitive Load at Pin A for Y→A (5 V→3.3 V) Level Translation*

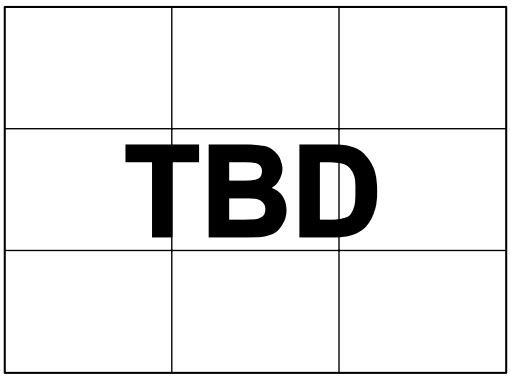



*Figure 13. Rise Time vs. Capacitive Load at Pin Y (A→Y Level Translation)*

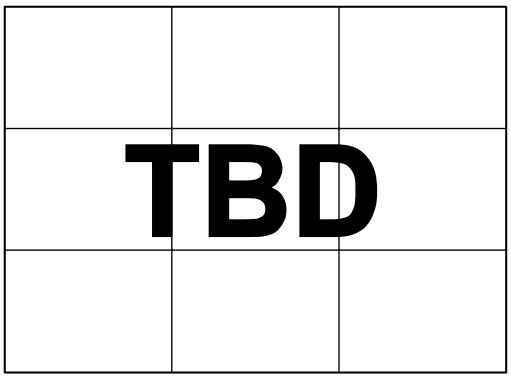



*Figure 14. Fall Time vs. Capacitive Load at Pin Y (A→Y Level Translation)*

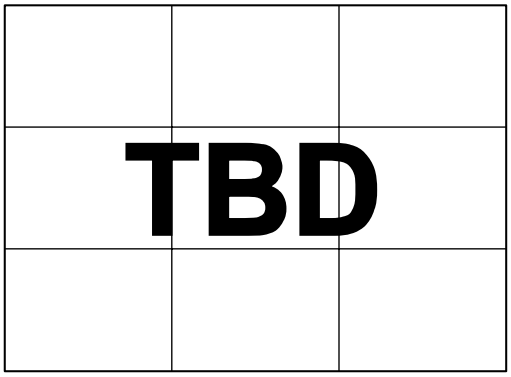



*Figure 15. Rise Time vs. Capacitive Load at Pin A (Y→A Level Translation)*

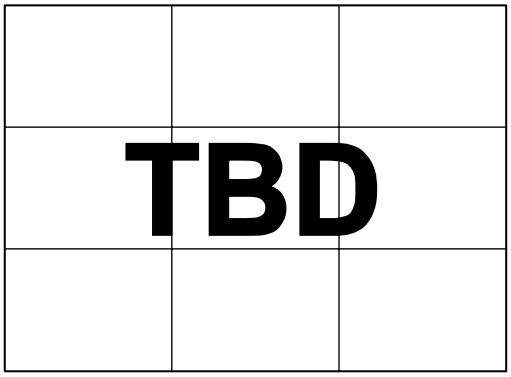



*Figure 16. Fall Time vs. Capacitive Load at Pin A (Y→A Level Translation)*

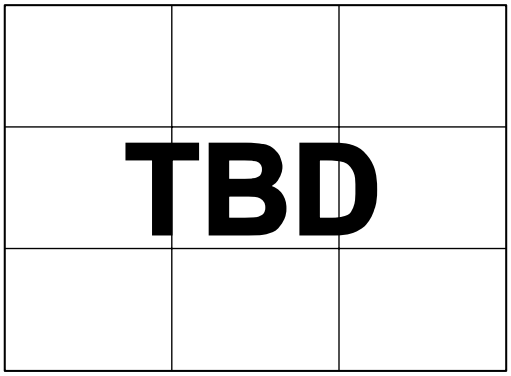



*Figure 17. Propagation Delay ($t_{PLH}$) vs. Capacitive Load at Pin Y (A→Y Level Translation)*

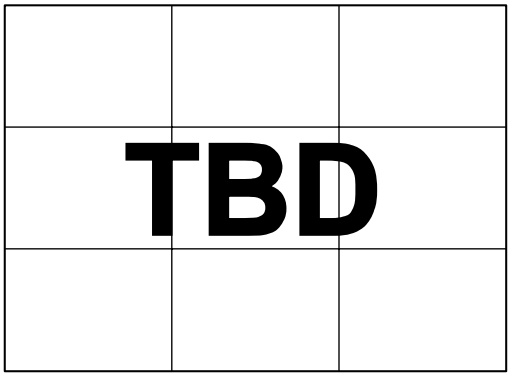



*Figure 18. Propagation Delay ($t_{PHL}$) vs. Capacitive Load at Pin Y (A→Y Level Translation)*

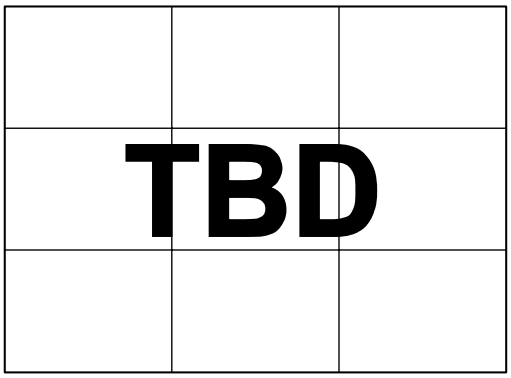



*Figure 19. Propagation Delay ($t_{PLH}$) vs. Capacitive Load at Pin A (Y→A Level Translation)*

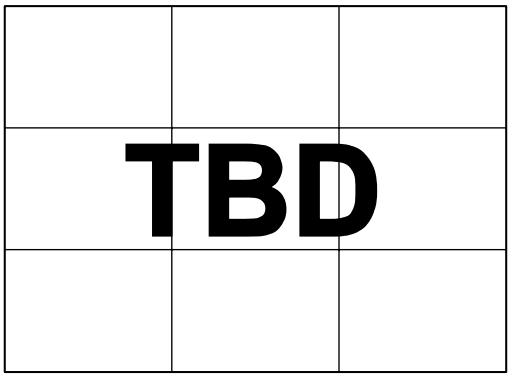



*Figure 20. Propagation Delay ($t_{PHL}$) vs. Capacitive Load at Pin A (Y→A Level Translation)*

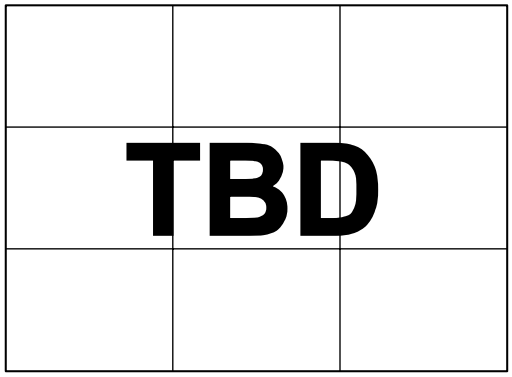



*Figure 21. Eye Diagram at Y Output (1.2 V to 1.8 V Level Translation, 25 Mbps)*

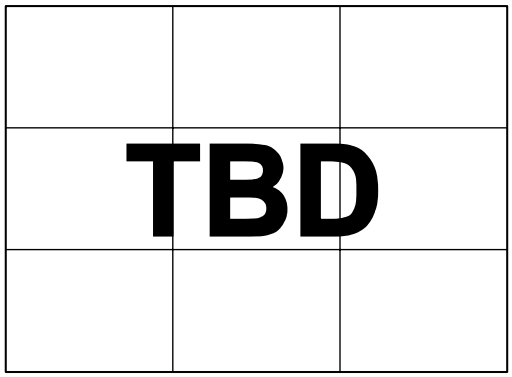



*Figure 22. Eye Diagram at A Output (1.8 V to 1.2 V Level Translation, 25 Mbps)*

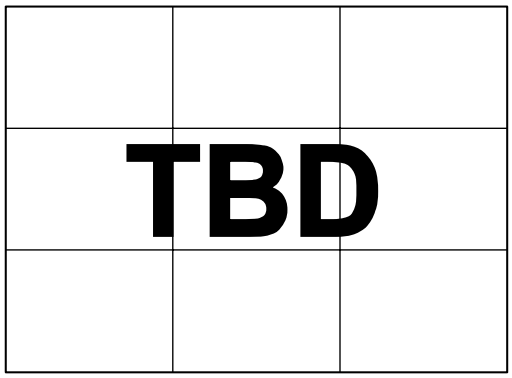



*Figure 23. Eye Diagram at Y Output (1.8 V to 3.3 V Level Translation, 50 Mbps)*

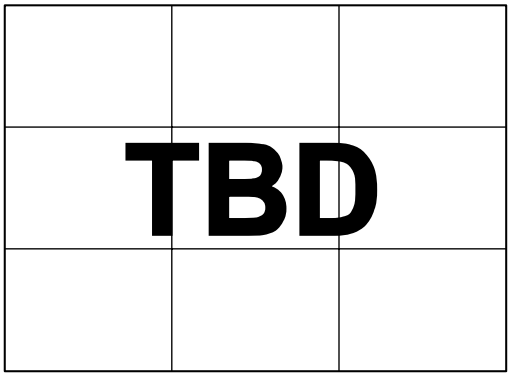



*Figure 24. Eye Diagram at A Output (3.3 V to 1.8 V Level Translation, 50 Mbps)*

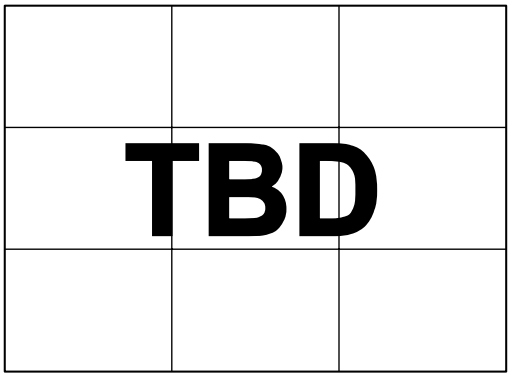



*Figure 25. Eye Diagram at Y Output (3.3 V to 5 V Level Translation, 50 Mbps)*

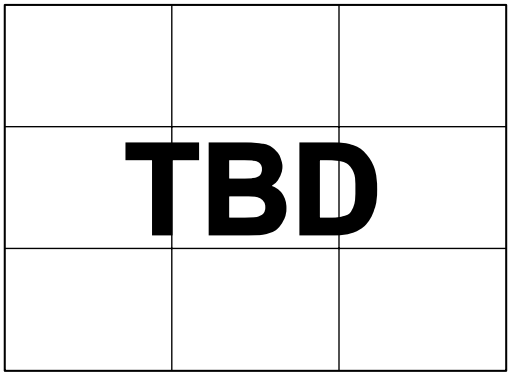



*Figure 26. Eye Diagram at A Output (5 V to 3.3 V Level Translation, 50 Mbps)*

# TEST CIRCUITS

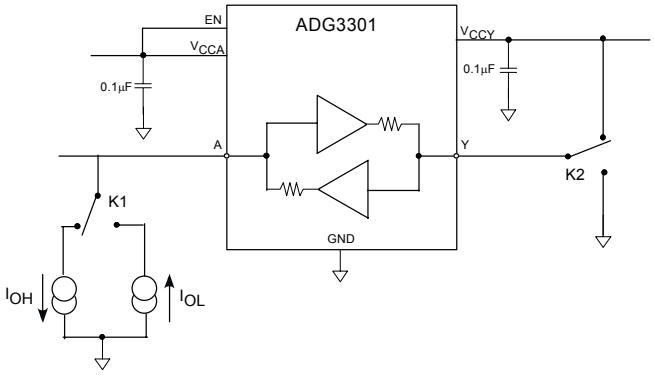



*Figure 27. $V_{OH}/V_{OL}$ Voltages at Pin A*

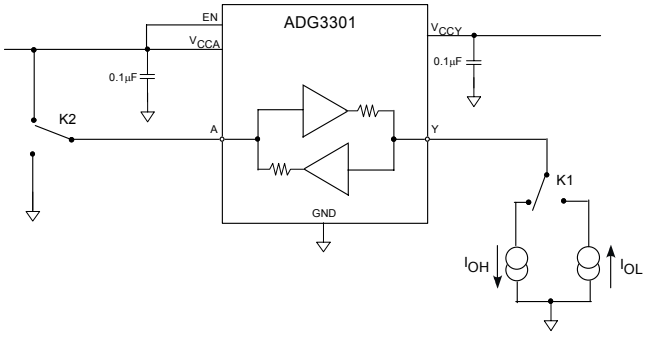



*Figure 28. $V_{OH}/V_{OL}$ Voltages at Pin Y*

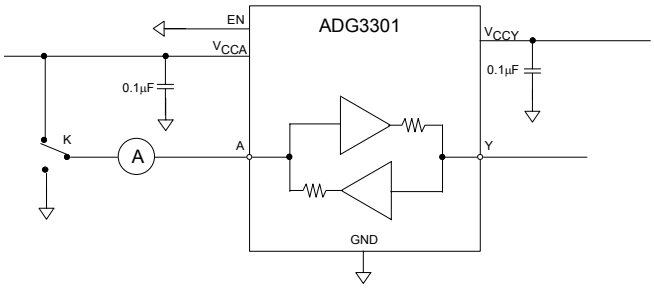



*Figure 29. Three-State Leakage Current at Pin A*

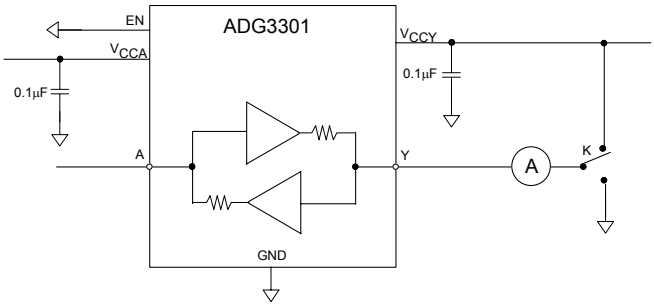



*Figure 30. Three-State Leakage Current at Pin Y*

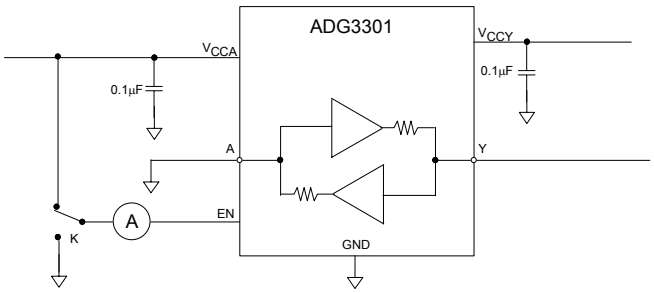



*Figure 31. EN Pin Leakage Current*

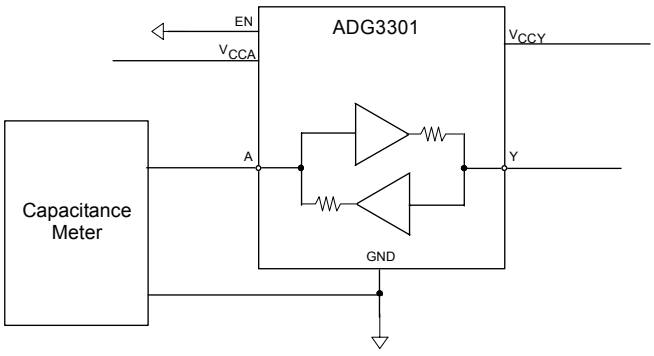



*Figure 32. Capacitance at Pin A*

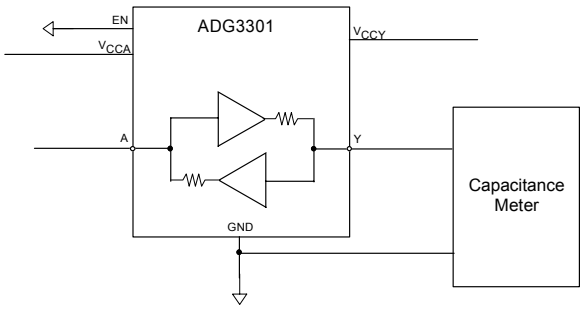
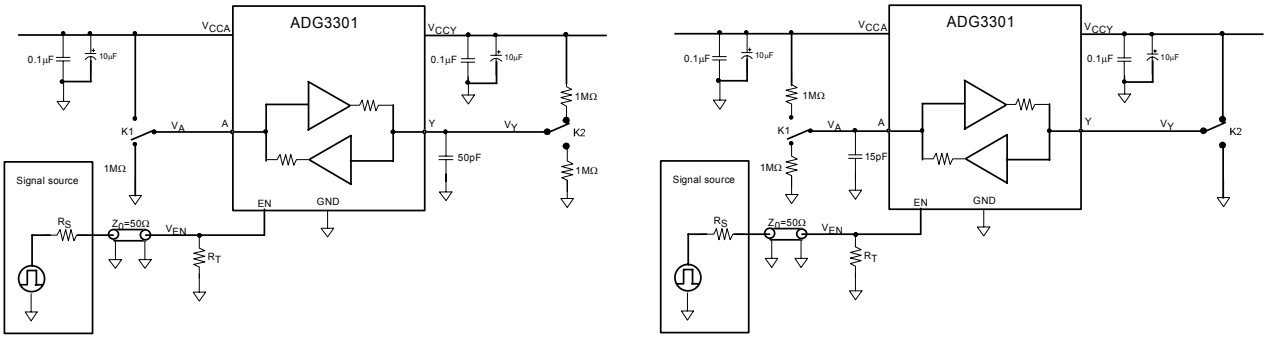
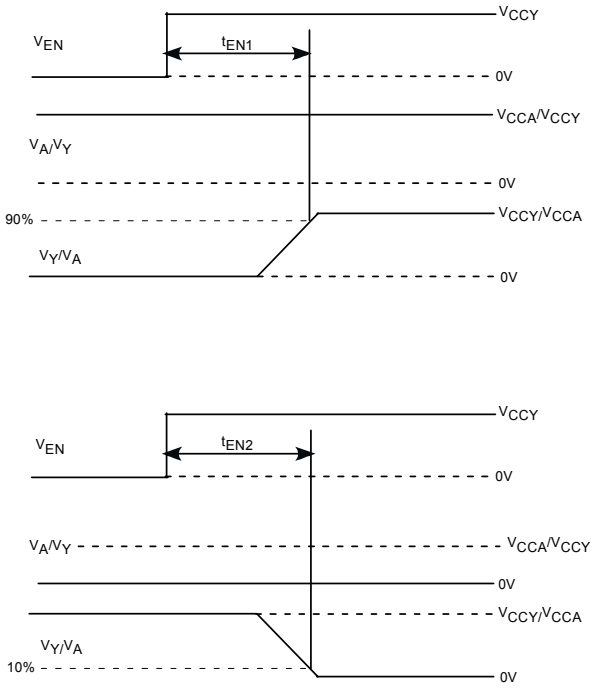



*Figure 33. Capacitance at Pin Y*




A-Y direction

Y-A direction




Note: $t_{EN}$ is whichever is larger between $t_{EN1}$ and $t_{EN2}$ in either A->Y and Y->A directions

*Figure 34. Enable Time*

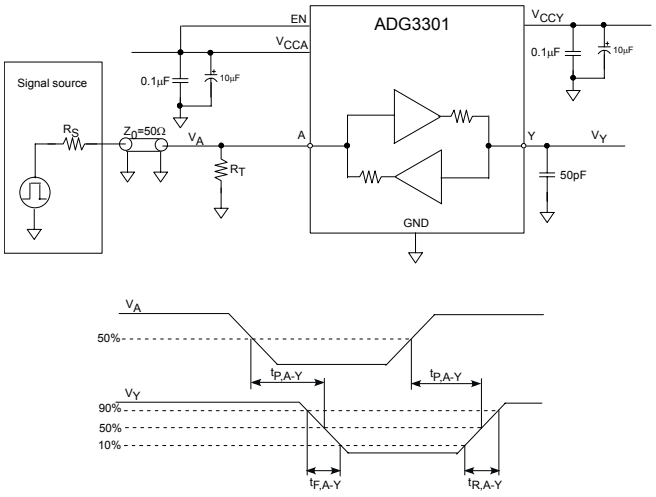



*Figure 35. Switching Characteristics (A→Y Level Translation)*

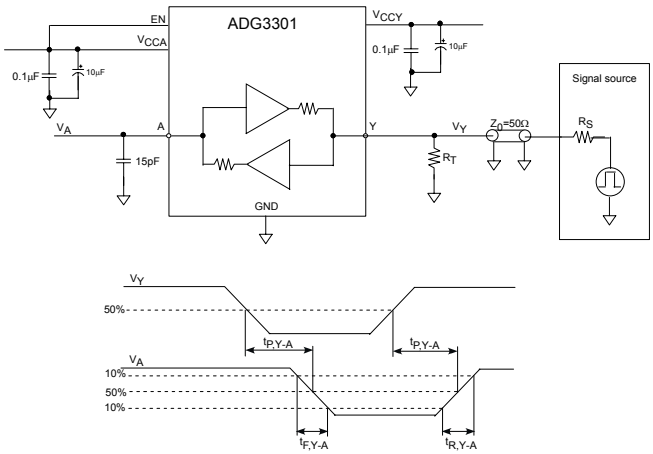



*Figure 36. Switching Characteristics (Y→A Level Translation)*

# TERMINOLOGY

**Table 4.**

| Symbol | Description |
|---|---|
| $V_{IHA}$ | Logic input high voltage at Pin A. |
| $V_{ILA}$ | Logic input low voltage at Pin A. |
| $V_{OHA}$ | Logic output high voltage at Pin A. |
| $V_{OLA}$ | Logic output low voltage at Pin A. |
| $C_A$ | Capacitance measured at Pin A (EN = 0). |
| $I_{LA, HiZ}$ | Leakage current at Pin A when EN = 0 (Pin A three-stated). |
| $V_{IHY}$ | Logic input high voltage at Pin Y. |
| $V_{ILY}$ | Logic input low voltage at Pin Y. |
| $V_{OHY}$ | Logic output high voltage at Pin Y. |
| $V_{OLY}$ | Logic output low voltage at Pin Y. |
| $C_Y$ | Capacitance measured at Pin Y (EN = 0). |
| $I_{LY, HiZ}$ | Leakage current at Pin Y when EN = 0 (Pin Y three-stated). |
| $V_{IHEN}$ | Logic input high voltage at the EN pin. |
| $V_{ILEN}$ | Logic input low voltage at the EN pin. |
| $C_{EN}$ | Capacitance measured at EN pin. |
| $I_{LEN}$ | Enable (EN) pin leakage curent. |
| $t_{EN}$ | Three-state enable time for Pins A /Y. |
| $t_{P, A-Y}$ | Propagation delay when translating logic levels in the A→Y direction. |
| $t_{R, A-Y}$ | Rise time when translating logic levels in the A→Y direction. |
| $t_{F, A-Y}$ | Fall time when translating logic levels in the A→Y direction. |
| $D_{MAX, A-Y}$ | Guaranteed data rate when translating logic levels in the A→Y direction under the driving and loading conditions specified in Table 1. |
| $t_{SKEW, A-Y}$ | Difference between propagation delays on any two channels when translating logic levels in the A→Y direction. |
| $t_{PPSKEW, A-Y}$ | Difference in propagation delay between any one channel and the same channel on a different part (under same driving/loading conditions) when translating in the A→Y direction. |
| $t_{P, Y-A}$ | Propagation delay when translating logic levels in the Y→A direction. |
| $t_{R, Y-A}$ | Rise time when translating logic levels in the Y→A direction. |
| $t_{F, Y-A}$ | Fall time when translating logic levels in the Y→A direction. |
| $D_{MAX, Y-A}$ | Guaranteed data rate when translating logic levels in the Y→A direction under the driving and loading conditions specified in Table 1. |
| $t_{SKEW, Y-A}$ | Difference between propagation delays on any two channels when translating logic levels in the Y→A direction. |
| $t_{PPSKEW, Y-A}$ | Difference in propagation delay between any one channel and the same channel on a different part (under same driving/loading conditions) when translating in the Y→A direction. |
| $V_{CCA}$ | Power supply voltage at the $V_{CCA}$ pin. |
| $V_{CCY}$ | Power supply voltage at the $V_{CCY}$ pin. |
| $I_{CCA}$ | $V_{CCA}$ supply current. |
| $I_{CCY}$ | $V_{CCY}$ supply current. |
| $I_{HiZA}$ | $V_{CCA}$ supply current during three-state mode (EN = 0). |
| $I_{HiZY}$ | $V_{CCY}$ supply current during three-state mode (EN = 0). |

# THEORY OF OPERATION

The ADG3301 level translator allows the level shifting necessary for data transfer in a system where multiple supply voltages are used. The device requires two supplies, $V_{CCA}$ and $V_{CCY}$ ($V_{CCA} \leq V_{CCY}$). These supplies set the logic levels on each side of the device. When driving the A pin, the device translates the $V_{CCA}$ compatible logic levels to $V_{CCY}$ compatible logic levels available at the Y pin. Similarly, since the device is capable of bidirectional translation, when driving the Y pin the $V_{CCY}$ compatible logic levels are translated to $V_{CCA}$-compatible logic levels available at the A pin. When EN = 0, the A and Y pins are three-stated. When EN is driven high, the ADG3301 goes into normal operation mode and performs level translation.

## LEVEL TRANSLATOR ARCHITECTURE

The ADG3301 consists of a single bidirectional channel that can translate logic levels in either the A→Y or the Y→A direction. It uses a one-shot accelerator architecture, which ensures excellent switching characteristics. Figure 37 shows a simplified block diagram of the ADG3301 level translator.

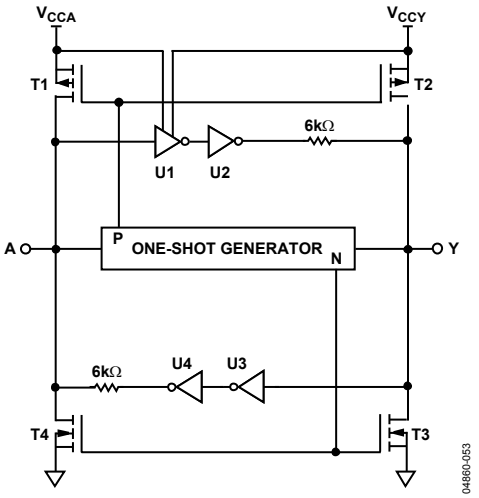



*Figure 37. Simplified Block Diagram of an ADG3301 Channel*

The logic level translation in the A→Y direction is performed using a level translator (U1) and an inverter (U2), while the translation in the Y→A direction is performed using the inverters U3 and U4. The one-shot generator detects a rising or falling edge present on either the A side or the Y side of the channel. It sends a short pulse that turns on the PMOS transistors (T1–T2) for a rising edge, or the NMOS transistors (T3–T4) for a falling edge. This charges/discharges the capacitive load faster, which results in fast rise and fall times.

## INPUT DRIVING REQUIREMENTS

To ensure correct operation of the ADG3301, the circuit that drives the input of an ADG3301 channels must have an output impedance of less than or equal to 150 Ω and a minimum peak current driving capability of 36 mA.

## OUTPUT LOAD REQUIREMENTS

The ADG3301 level translator is designed to drive CMOS-compatible loads. If current driving capability is required, it is recommended to use buffers between the ADG3301 outputs and the load.

## ENABLE OPERATION

The ADG3301 provides three-state operation at the A and Y I/O pins by using the enable (EN) pin as shown in Table 5.

**Table 5. Truth Table**

| EN | Y I/O Pin | A I/O Pin |
|---|---|---|
| 0 | Hi-Z[1] | Hi-Z[1] |
| 1 | Normal operation[2] | Normal operation[2] |

[1] High impedance state.
[2] In normal operation, the ADG3301 performs level translation.

While EN = 0, the ADG3301 enters into tri-state mode. In this mode, the current consumption from both the $V_{CCA}$ and $V_{CCY}$ supplies is reduced, allowing the user to save power, which is critical, especially on battery-operated systems. The EN input pin can be driven with either $V_{CCA}$- or $V_{CCY}$-compatible logic levels.

## POWER SUPPLIES

For proper operation of the ADG3301, the voltage applied to the $V_{CCA}$ must be always less than or equal the voltage applied to $V_{CCY}$. To meet this condition, the recommended power-up sequence is $V_{CCY}$ first and then $V_{CCA}$. The ADG3301 operates properly only after both supply voltages reach their nominal values. It is not recommended to use the part in a system where, during power-up, $V_{CCA}$ may be greater than $V_{CCY}$ due to significant increase in the current taken from the $V_{CCA}$ supply For optimum performance, the $V_{CCA}$ and $V_{CCY}$ pins should be decoupled to GND, and placed as close as possible to the device.

## DATA RATE

The maximum data rate at which the device is guaranteed to operate is a function of the $V_{CCA}$ and $V_{CCY}$ supply voltage combination and the load capacitance. It is given by the maximum frequency of a square wave that can be applied to the device, which meets the $V_{OH}$ and $V_{OL}$ levels at the output and does not exceed the maximum junction temperature (see the Absolute Maximum Ratings).Table 6 shows the guaranteed data rates at which the ADG3301 can operate in both directions (A→Y or Y→A level translation) for various $V_{CCA}$ and $V_{CCY}$ supply combinations.

**Table 6. Guaranteed Data Rate (Mbps)[1]**

| | $V_{CCY}$ | | | |
|---|---|---|---|---|
| **$V_{CCA}$** | **1.8 V (1.65 V to 1.95 V)** | **2.5 V (2.3 V to 2.7 V)** | **3.3 V (3.0 V to 3.6 V)** | **5 V (4.5 V to 5.5 V)** |
| **1.2 V (1.15 V to 1.3 V)** | 25 | 30 | 40 | 40 |
| **1.8 V (1.65 V to 1.95 V)** | - | 45 | 50 | 50 |
| **2.5 V (2.3 V to 2.7 V)** | - | - | 60 | 50 |
| **3.3 V (3.0 V to 3.6 V)** | - | - | - | 50 |
| **5 V (4.5 V to 5.5 V)** | - | - | - | - |

[1] The load capacitance used is 50 pF when translating in the A→Y direction and 15 pF when translating in the Y→A direction.

# APPLICATIONS

The ADG3301 is designed for digital circuits that operate at different supply voltages; therefore, logic level translation is required. The lower voltage logic signals are connected to the A pin, and the higher voltage logic signals to the Y pin. The ADG3301 can provide level translation in both directions from A→Y or Y→A, eliminating the need for a level translator IC for each direction. The internal architecture allows the ADG3301 to perform bidirectional level translation without an additional signal to set the direction in which the translation is made. It also allows simultaneous data flow in both directions on the same part, for example, two channels translate in A→Y direction while the other two translate in Y→A direction. This simplifies the design by eliminating the timing requirements for the direction signal and reduces the number of ICs used for level translation.

Figure 38 shows an application where a 1.8V microprocessors transfers data to or from a 3.3V peripheral device using the ADG3301 level translator.

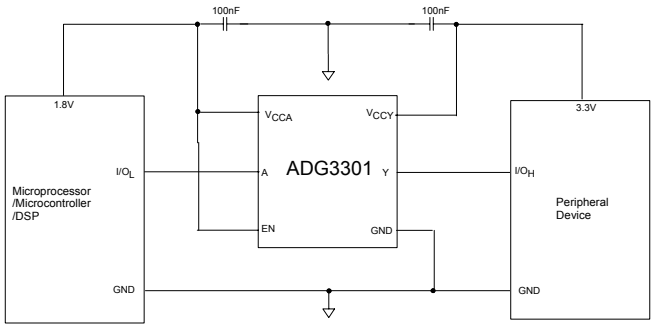


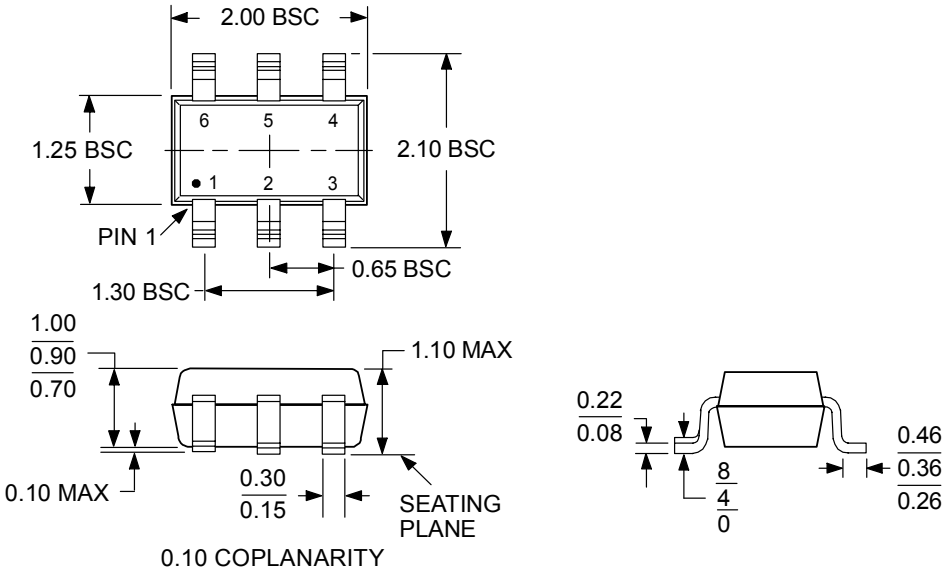

*Figure 39. 1.8V to 3.3V level translation circuit*

## LAYOUT GUIDELINES

As with any high speed digital IC, the printed circuit board layout is important for the overall performance of the circuit. Care should be taken to ensure proper power supply bypass and return paths for the high speed signals. Each $V_{CC}$ pin ($V_{CCA}$ and $V_{CCY}$) should be bypassed using low effective series resistance (ESR) and effective series inductance (ESI) capacitors placed as close as possible to the $V_{CCA}$ and $V_{CCY}$ pins. The parasitic inductance of the high speed signal track might cause significant overshoot. This effect can be reduced by keeping the length of the tracks as short as possible. A solid copper plane for the return path (GND) is also recommended.

# OUTLINE DIMENSIONS

6-Lead Plastic Surface Mount Package [SC70]
(KS-6)
Dimensions shown in millimeters




COMPLIANT TO JEDEC STANDARDS MO-203AB

*Figure 40. 6 Lead SC 70 package*

PR05517-0-7/05(PrA)