

FEATURES

- New, fast settling, fractional-N PLL architecture**
- Single PLL replaces ping-pong synthesizers**
- 0.5 degree rms phase error at 2 GHz RF output**
- Digitally programmable output phase**
- RF input range up to 3.5 GHz**
- 3-wire serial interface**
- On-chip, low noise differential amplifier**
- Phase noise figure of merit: -216 dBc/Hz**
- Loop filter design possible using ADI SimPLL**

APPLICATIONS

- GSM/EDGE base stations**
- PHS base stations**
- Instrumentation and test equipment**

GENERAL DESCRIPTION

The ADF4193 frequency synthesizer can be used to implement local oscillators in the up conversion and down conversion sections of wireless receivers and transmitters. Its architecture is specifically designed to meet the GSM/EDGE lock time requirements for base stations. It consists of a low noise, digital phase frequency detector (PFD), and a precision differential charge pump. There is also a differential amplifier to convert the differential charge pump output to a single ended voltage for the external voltage controlled oscillator (VCO). The Σ - Δ based fractional interpolator, working with the N divider, allow programmable modulus fractional-N division. Additionally, the 4-bit reference (R) counter and on-chip frequency doubler allows selectable reference signal (REF_{IN}) frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and a VCO. The switching architecture ensures that the PLL settles inside the GSM time slot guard period, removing the need for a second PLL and associated isolation switches. This decreases cost, complexity, PCB area, shielding, and characterization on previous ping-pong GSM PLL architectures.

FUNCTIONAL BLOCK DIAGRAM

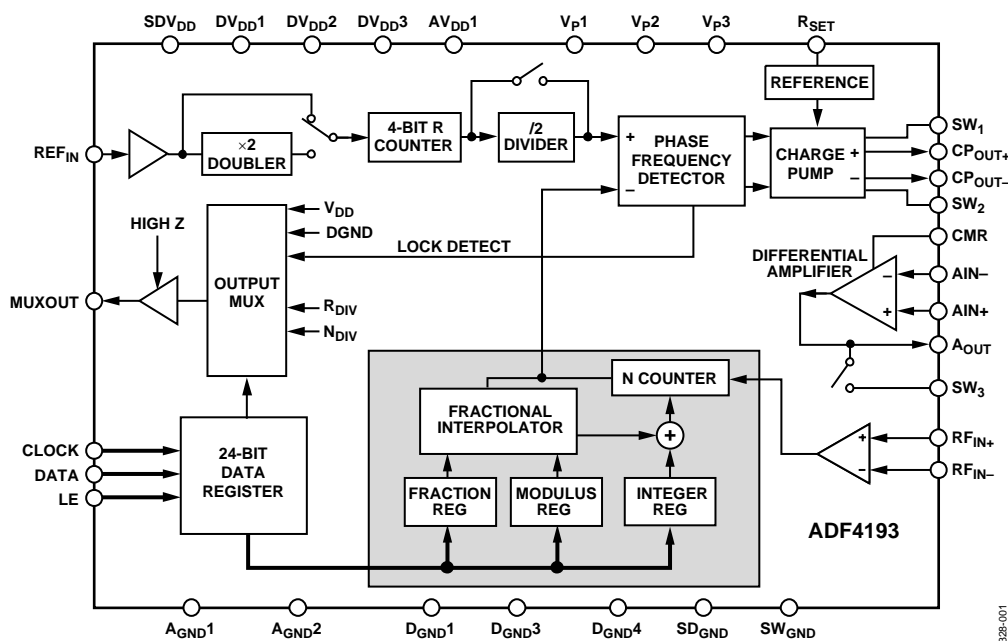


Figure 1.

Rev. 0

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REVISION HISTORY**4/05—Revision 0: Initial Version**

SPECIFICATIONS

$AV_{DD} = DV_{DD} = SDV_{DD} = 3\text{ V} \pm 10\%$, $V_{P1}, V_{P2} = 5\text{ V} \pm 10\%$, $V_{P3} = 5.35\text{ V} \pm 5\%$, $AGND = DGND = GND = 0\text{ V}$, $R_{SET} = 2.4\text{ k}\Omega$, dBm referred to $50\ \Omega$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Operating temperature range (B version): -40°C to $+85^\circ\text{C}$.

Table 1.

Parameter	B Version	Unit	Test Conditions/Comments
RF CHARACTERISTICS			
RF Input Frequency (RF_{IN})	0.4/3.5	GHz min/max	See Figure 21 for input circuit.
RF Input Sensitivity	-10/0	dBm min/max	
Maximum Allowable Prescaler Output Frequency ¹	470	MHz max	
REF_{IN} CHARACTERISTICS			
REF _{IN} Input Frequency	300	MHz max	For $f > 120\text{ MHz}$, set REF/2 bit = 1.
REF _{IN} Edge Slew Rate	350	V/ μs min	
REF _{IN} Input Sensitivity	0.7/ V_{DD} 0 to V_{DD}	V p-p min/max V max	AC-coupled. CMOS-compatible.
REF _{IN} Input Capacitance	10	pF max	
REF _{IN} Input Current	± 100	μA max	
PHASE DETECTOR			
Phase Detector Frequency	26	MHz max	
CHARGE PUMP			
I_{CP} Up/Down			
High Value	6.6	mA typ	With $R_{SET} = 2.4\text{ k}\Omega$.
Low Value	104	μA typ	With $R_{SET} = 2.4\text{ k}\Omega$.
Absolute Accuracy	5	% typ	Nominally $R_{SET} = 2.4\text{ k}\Omega$.
R_{SET} Range	1/4	k Ω min/max	
I_{CP} Three-State Leakage	1	nA typ	$0.75\text{ V} \leq V_{CP} \leq V_P - 1.5\text{ V}$.
I_{CP} Up vs. Down Matching	0.1	% typ	
I_{CP} vs. V_{CP}	1	% typ	
I_{CP} vs. Temperature	1	% typ	$0.75\text{ V} \leq V_{CP} \leq V_P - 1.5\text{ V}$.
Differential Amplifier			
Input Current	1	nA typ	@ 20 kHz offset.
Output Voltage Range	1.5/($V_{P3} - 0.5$)	V min/max	
VCO Tuning Range	1.8/($V_{P3} - 0.8$)	V min/max	
Output Noise	7	nV/ $\sqrt{\text{Hz}}$ typ	
LOGIC INPUTS			
V_{IH} , Input High Voltage	1.4	V min	
V_{IL} , Input Low Voltage	0.7	V max	
I_{INH} , I_{INL} , Input Current	± 1	μA max	
C_{IN} , Input Capacitance	10	pF max	
LOGIC OUTPUTS			
V_{OH} , Output High Voltage	$V_{DD} - 0.4$	V min	$I_{OH} = 500\ \mu\text{A}$.
V_{OL} , Output Low Voltage	0.4	V max	$I_{OL} = 500\ \mu\text{A}$.
POWER SUPPLIES			
AV_{DD}	2.7/3.3	V min/V max	$AV_{DD} \leq V_{P1}, V_{P2} \leq 5.5\text{ V}$.
DV_{DD}	AV_{DD}		
V_{P1}, V_{P2}	4.5/5.5	V min/V max	$V_{P1}, V_{P2} \leq V_{P3} \leq 5.65\text{ V}$.
V_{P3}	5.0/5.65	V min/V max	
I_{DD} ($AV_{DD} + DV_{DD} + SDV_{DD}$)	27	mA max	22 mA typ.
I_{DD} ($V_{P1} + V_{P2}$)	27	mA max	22 mA typ.
I_{DD} (V_{P3})	30	mA max	24 mA typ.
I_{DD} Power-Down	10	μA typ	

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Parameter	B Version	Unit	Test Conditions/Comments
SW1, SW2, and SW3			
R_{ON} (SW1 and SW2)	65	Ω typ	
R_{ON} SW3	90	Ω typ	
NOISE CHARACTERISTICS			
900 MHz Output ²	-108	dBc/Hz typ	@ 5 kHz offset and 26 MHz PFD frequency.
1800 MHz Output ³	-102	dBc/Hz typ	@ 5 kHz offset and 13 MHz PFD frequency.
Phase Noise Floor ⁴	-145	dBc/Hz typ	@ 13 MHz PFD frequency.
Phase Noise Figure of Merit ⁵	-216	dBc/Hz typ	@ VCO output with dither off.

¹ The prescaler value should be chosen to ensure that the RF input is divided down to a frequency that is less than this value.

² $f_{REFIN} = 26$ MHz; $f_{step} = 200$ kHz; $f_{RF} = 900$ MHz; Loop BW = 40 kHz.

³ $f_{REFIN} = 13$ MHz; $f_{step} = 200$ kHz; $f_{RF} = 1850$ MHz; Loop BW = 60 kHz.

⁴ The phase noise is measured with the EVAL-ADF4193EB1 evaluation board and the Agilent E5500 phase noise system.

⁵ Calculated from phase noise measured at 5 kHz with a 60 kHz loop BW. Increased noise contribution from the differential amplifier if the loop BW is reduced.

TIMING CHARACTERISTICS

$AV_{DD} = DV_{DD} = 3\text{ V} \pm 10\%$, $V_{P1}, V_{P2} = 5\text{ V} \pm 10\%$, $V_{P3} = 5.35\text{ V} \pm 5\%$, $AGND = DGND = GND = 0\text{ V}$, $R_{SET} = 2.4\text{ k}\Omega$, dBm referred to $50\ \Omega$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Operating temperature (B version): -40°C to $+85^\circ\text{C}$.

Table 2.

Parameter	Limit (B Version)	Unit	Test Conditions/Comments
t_1	10	ns min	LE setup time
t_2	10	ns min	DATA to CLOCK setup time
t_3	10	ns min	DATA to CLOCK hold time
t_4	15	ns min	CLOCK high duration
t_5	15	ns min	CLOCK low duration
t_6	10	ns min	CLOCK to LE setup time
t_7	15	ns min	LE pulse width

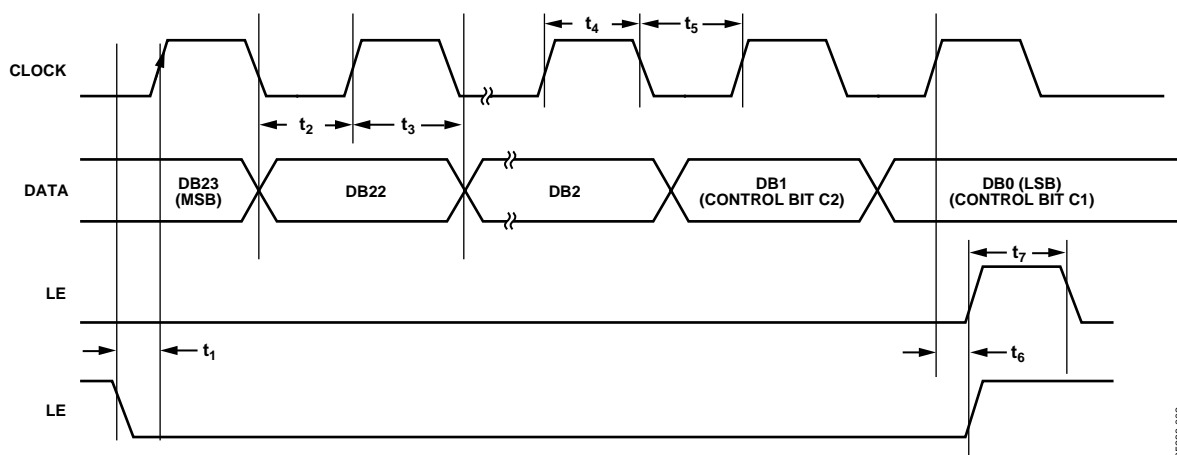


Figure 2. Timing Diagram

05238-002

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.

Table 3.

Parameter	Rating
AV _{DD} to GND	-0.3 V to +3.6 V
AV _{DD} to DV _{DD} , SDV _{DD}	-0.3 V to +0.3 V
V _P to GND	-0.3 V to +5.8 V
V _P to AV _{DD}	-0.3 V to +5.8 V
Digital I/O Voltage to GND	-0.3 V to V _{DD} + 0.3 V
Analog I/O Voltage to GND	-0.3 V to V _P + 0.3 V
REF _{IN} , RF _{IN+} , RF _{IN-} to GND	-0.3 V to V _{DD} + 0.3 V
Operating Temperature Range Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +125°C
Maximum Junction Temperature	150°C
LFCSP θ_{JA} Thermal Impedance (Paddle-Soldered)	27.3°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

Transistor Count

75,800 (MOS), 545 (BJT)

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

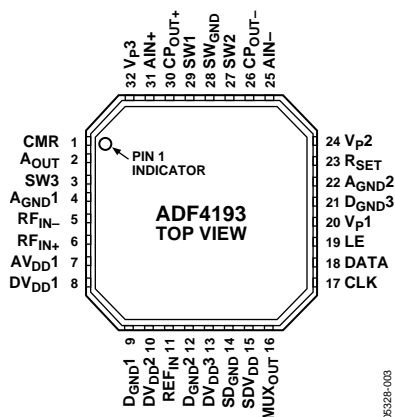


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	CMR	Common-Mode Reference Voltage for the Differential Amplifier's Output Voltage Swing. Internally biased to three-fifths of V_{P3} . Requires a 0.1 μF capacitor to ground.
2	AOUT	Differential Amplifier Output to Tune the External VCO.
3	SW3	Fast-Lock Switch 3. Closed while SW3 timeout counter is active.
4	AGND1	Analog Ground. This is the ground return pin for the differential amplifier and the RF section.
5	RFIN-	Complementary Input to the RF Prescaler. This point must be decoupled to the ground plane with a small bypass capacitor, typically 100 pF.
6	RFIN+	Input to the RF Prescaler. This small signal input is ac-coupled to the external VCO.
7	AVDD1	Power Supply Pin for the RF Section. Nominally 3 V. A 100 pF decoupling capacitor to the ground plane should be placed as close as possible to this pin.
8	DVDD1	Power Supply Pin for the N Divider. Should be the same voltage as AVDD1. A 0.1 μF decoupling capacitor to ground should be placed as close as possible to this pin.
9	DGND1	Ground Return Pin for DVDD1.
10	DVDD2	Power Supply Pin for the REF _{IN} Buffer and R Divider. Nominally 3V. A 0.1 μF decoupling capacitor to ground should be placed as close as possible to this pin.
11	REF _{IN}	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and a dc equivalent input resistance of 100 k Ω . See Figure 15. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac-coupled.
12	DGND2	Ground Return Pin for DVDD2 and DVDD3.
13	DVDD3	Power Supply Pin for the Serial Interface Logic. Nominally 3 V.
14	SDGND	Ground Return Pin for the Σ - Δ Modulator.
15	SDVDD	Power Supply Pin for the Digital Σ - Δ Modulator. Nominally 3 V. A 0.1 μF decoupling capacitor to the ground plane should be placed as close as possible to this pin.
16	MUX _{OUT}	This multiplexer output allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally. See Figure 35.
17	CLK	Serial Clock Input. Data is clocked into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
18	DATA	Serial Data Input. The serial data is loaded MSB first with the three LSBs as the control bits. This input is a high impedance CMOS input.
19	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift register is loaded into the register that is selected by the three LSBs.
20	V _{P1}	Power Supply Pin for the Phase Frequency Detector (PFD). Nominally 5 V, should be at the same voltage at V _{P2} . A 0.1 μF decoupling capacitor to ground should be placed as close as possible to this pin.
21	DGND3	Ground Return Pin for V _{P1} .

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Pin No.	Mnemonic	Function
22	AGND2	Ground Return Pin for V _{P2} .
23	R _{SET}	Connecting a resistor between this pin and GND sets the charge pump output current. The nominal voltage bias at the R _{SET} pin is 0.55 V. The relationship between I _{CP} and R _{SET} is $I_{CP} = \frac{0.25}{R_{SET}}$ So, with R _{SET} = 2.4 kΩ, I _{CP} = 104 μA.
24	V _{P2}	Power Supply Pin for the Charge Pump. Nominally 5 V, should be at the same voltage at V _{P1} . A 0.1 μF decoupling capacitor to ground should be placed as close as possible to this pin.
25	AIN-	Differential Amplifier's Negative Input Pin.
26	CP _{OUT-}	Differential Charge Pump's Negative Output Pin. Should be connected to AIN- and the loop filter.
27	SW2	Fast Lock Switch 2. This switch is closed to SW _{GND} while the SW1/2 timeout counter is active.
28	SW _{GND}	Common for SW1 and SW2 switches. Should be connected to the ground plane.
29	SW1	Fast Lock Switch 1. This switch is closed to SW _{GND} while the SW1/2 timeout counter is active.
30	CP _{OUT+}	Differential Charge Pump's Positive Output Pin. Should be connected to AIN+ and the loop filter.
31	AIN+	Differential Amplifier's Positive Input Pin.
32	V _{P3}	Power Supply Pin for the Differential Amplifier. This may range from 5.0 V to 5.5 V. A 0.1 μF decoupling capacitor to ground should be placed as close as possible to this pin. Also requires a 10 μF decoupling capacitor to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

FREQ.	UNIT	GHz	KEYWORD	R	
PARAM	TYPE	S	IMPEDANCE	50	
DATA	FORMAT	MA			
FREQ.	MAGS11	ANGS11	FREQ.	MAGS11	ANGS11
0.5	0.8897	-16.6691	2.3	0.67107	-75.8206
0.6	0.87693	-19.9279	2.4	0.66556	-77.6851
0.7	0.85834	-23.561	2.5	0.6564	-80.3101
0.8	0.85044	-26.9578	2.6	0.6333	-82.5082
0.9	0.83494	-30.8201	2.7	0.61406	-85.5623
1.0	0.81718	-34.9499	2.8	0.5977	-87.3513
1.1	0.80229	-39.0436	2.9	0.5655	-89.7605
1.2	0.78917	-42.3623	3.0	0.5428	-93.0239
1.3	0.77598	-46.322	3.1	0.51733	-95.9754
1.4	0.75578	-50.3484	3.2	0.49909	-99.1291
1.5	0.74437	-54.3545	3.3	0.47309	-102.208
1.6	0.73821	-57.3785	3.4	0.45694	-106.794
1.7	0.7253	-60.695	3.5	0.44698	-111.659
1.8	0.71365	-63.9152	3.6	0.43589	-117.986
1.9	0.70699	-66.4365	3.7	0.42472	-125.62
2.0	0.7038	-68.4453	3.8	0.41175	-133.291
2.1	0.69284	-70.7986	3.9	0.41055	-140.585
2.2	0.67717	-73.7038	4.0	0.40983	-147.97

Figure 4. S Parameter Data for the RF Input

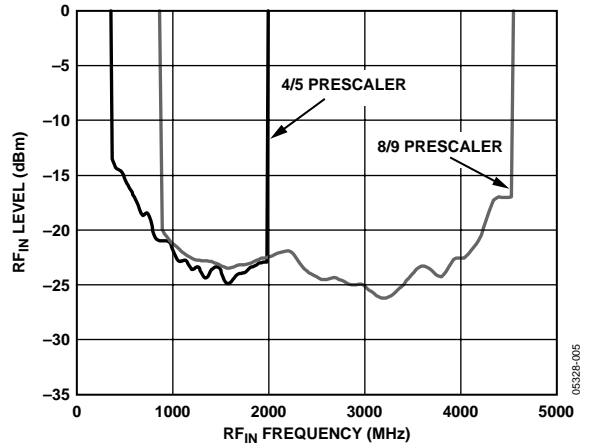


Figure 7. RF Input Sensitivity

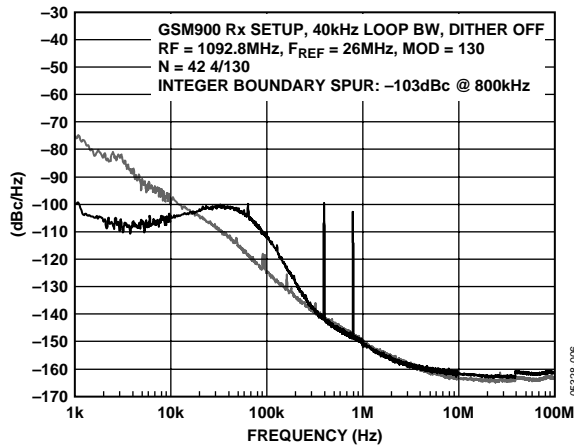


Figure 5. SSB Phase Noise Plot at 1092.8 MHz (GSM900 Rx Setup) vs. Free Running VCO Noise

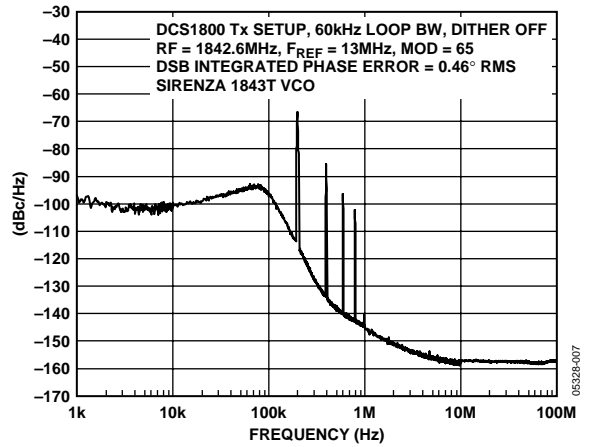


Figure 8. SSB Phase Noise Plot at 1842.6 MHz (DCS1800 Tx Setup) vs. Free Running VCO Noise

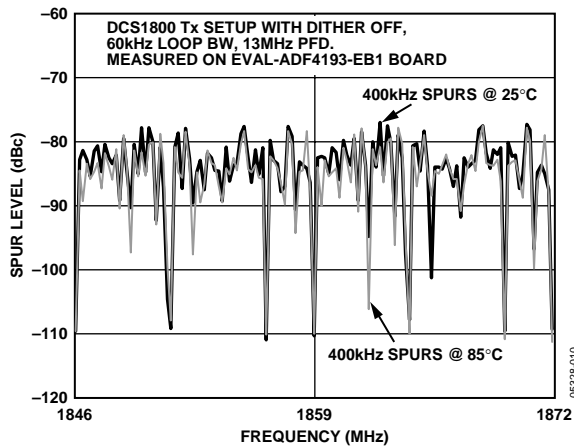


Figure 6. 400 kHz Fractional Spur Levels Across all DCS1800 Tx Channels over Two Integer Multiples of the PFD Reference

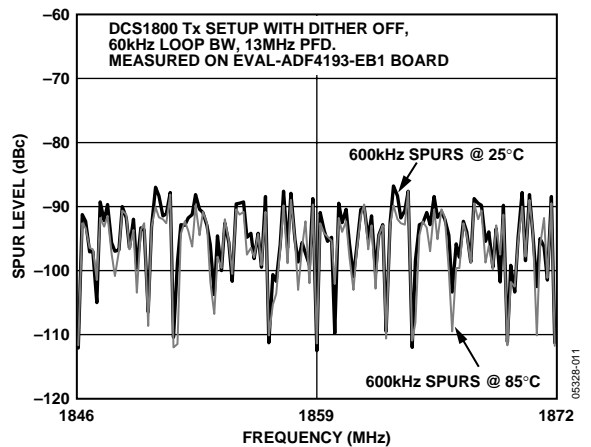


Figure 9. 600 kHz Fractional Spur Levels Across all DCS1800 Tx Channels over Two Integer Multiples of the PFD Reference

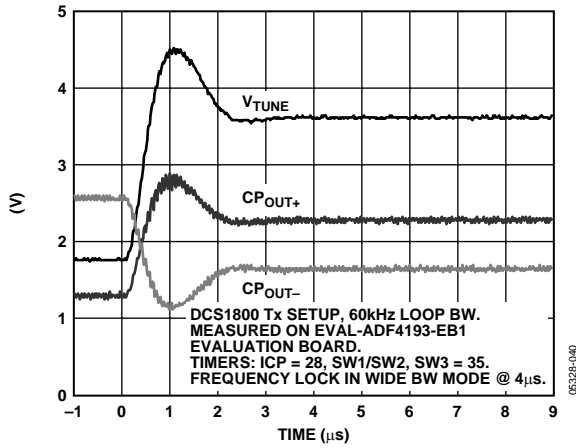


Figure 10. V_{TUNE} Settling Transient for a 75 MHz Jump from 1818 MHz to 1893 MHz with Sirenza 1843T VCO

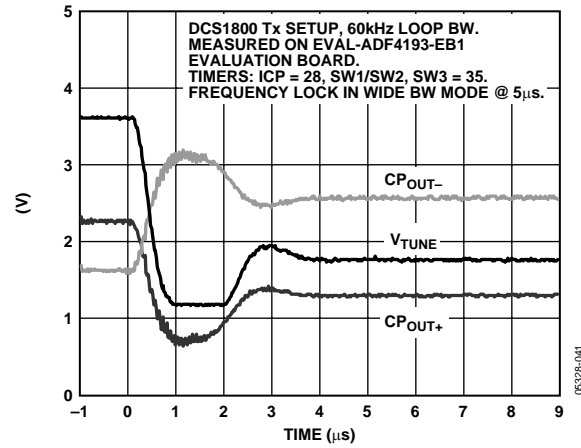


Figure 13. V_{TUNE} Settling Transient for a 75 MHz Jump Down from 1893 MHz to 1818 MHz, the Bottom of the Allowed Tuning Range with the Sirenza 1843T VCO

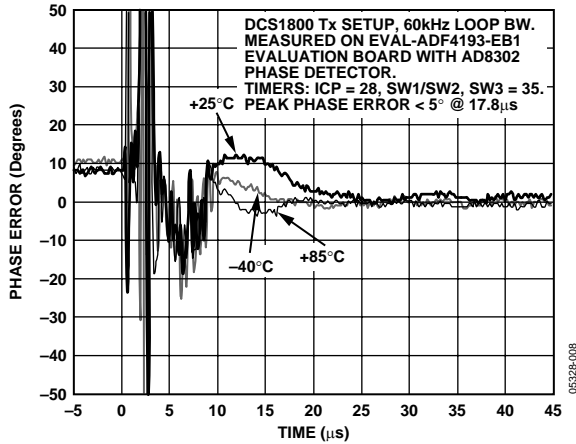


Figure 11. Phase Settling Transient for a 75 MHz Jump From 1818 MHz to 1893 MHz (V_{TUNE} 1.8 V to 3.7 V with Sirenza 1843T VCO)

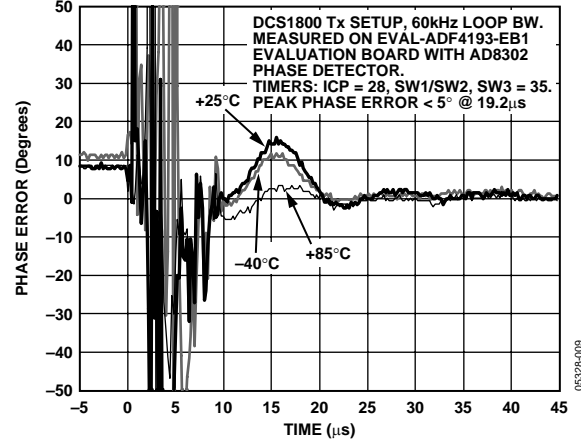


Figure 14. Phase Settling Transient for a 75 MHz Jump from 1893 MHz to 1818 MHz (V_{TUNE} = 3.7 V to 1.8 V with Sirenza 1843T VCO)

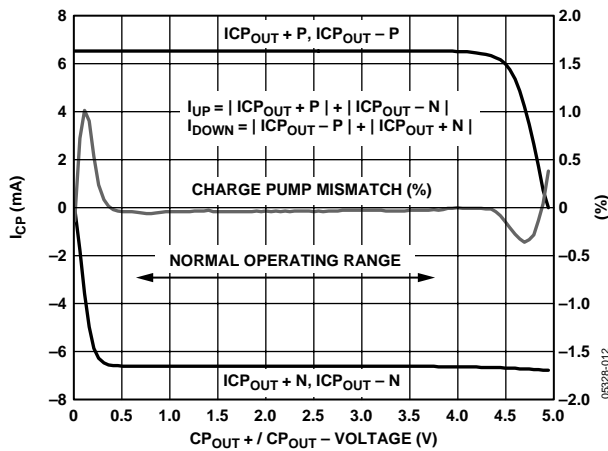


Figure 12. Differential Charge Pump Output Compliance Range and Charge Pump Mismatch with $V_{p1} = V_{p2} = 5V$

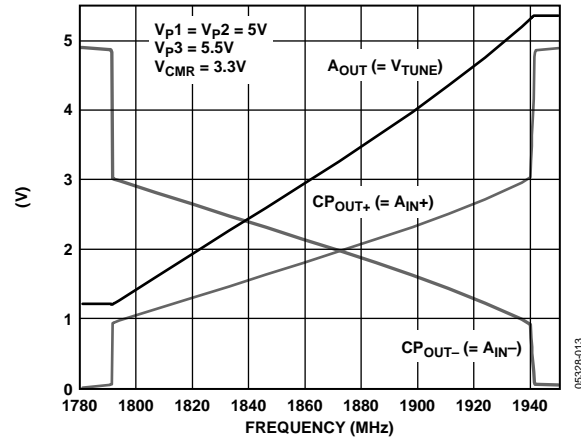


Figure 15. Tuning Range with a Sirenza 1843T VCO and a 5.5 V Differential Amplifier Power Supply Voltage

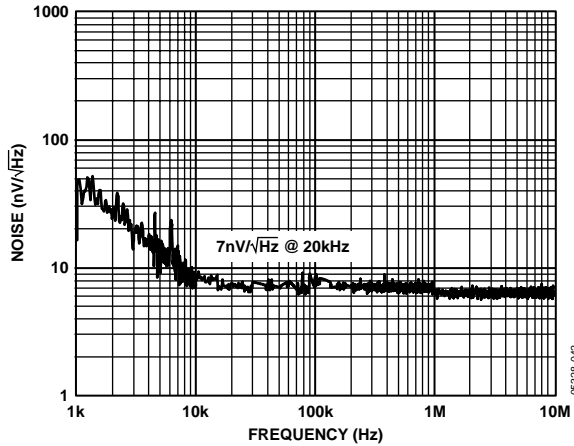


Figure 16. Voltage Noise Density Measured at the Differential Amplifier Output

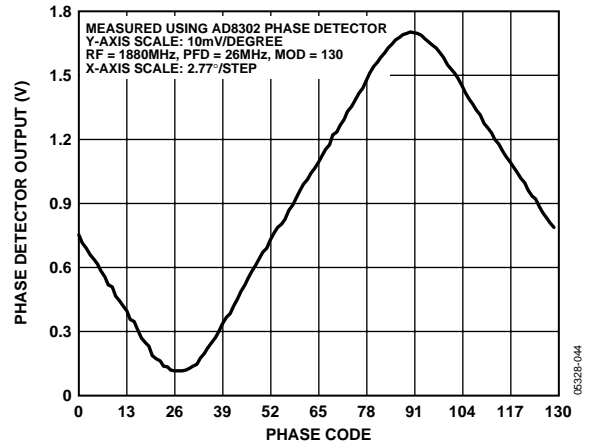


Figure 18. Detected RF Output Phase for Phase Code Sweep from 0 to MOD

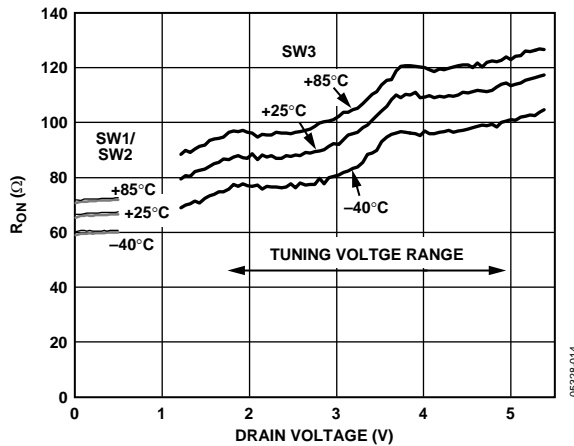
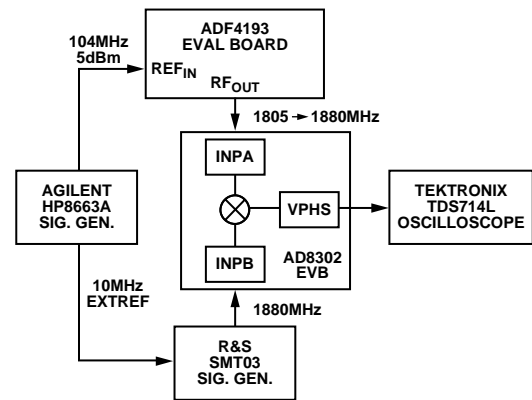


Figure 17. On Resistance of Loop Filter Switches SW1/SW2 and SW3



INTERVAL BETWEEN R0 WRITES SHOULD BE A MULTIPLE OF MOD REFERENCE CYCLES ($5_{\mu s}$) FOR COHERENT PHASE MEASUREMENTS

Figure 19. Test Setup for Phase Lock Time Measurements

GENERAL DESCRIPTION

The ADF4193 is targeted at GSM base station requirements, specifically to eliminate the need for ping-pong solutions. It works on the basis of fast lock, using a wide loop bandwidth during a frequency change and narrowing the loop bandwidth once frequency lock has been achieved. Widening the loop bandwidth is achieved by increasing the charge pump current. Switches are included to change the loop filter component values to maintain stability with the changing charge pump current. The narrow loop bandwidth ensures that phase noise and spur specifications are met. A differential charge pump and loop filter topology are used to ensure that the fast lock time benefit from widening the loop bandwidth is maintained when the loop is restored to narrow bandwidth mode for normal operation.

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 20. Switches S1 and S2 are normally closed switches. S3 is normally open. When power-down is initiated, S3 is closed and S1 and S2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

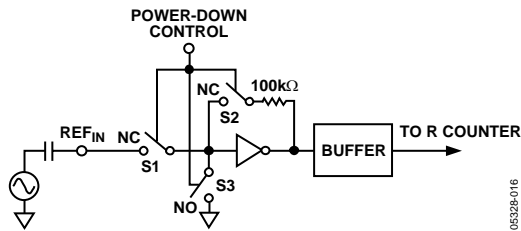


Figure 20. Reference Input Stage

R Counter and Doubler

The 4-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). A toggle flip-flop can be optionally inserted after the R counter to give a further divide by 2. Using this option has the additional advantage of ensuring that the PFD reference clock has a 50/50 mark-space ratio. This ratio gives the maximum separation between the fast lock timer clock, which is generated off the falling edge of the PFD reference, and the rising edge, which is the active edge in the PFD. It is recommended that this toggle flip-flop be enabled for all even R divide values. It must be enabled if dividing down a REF_{IN} frequency that is greater than 120 MHz.

An optional doubler before the 4-bit R counter can be used for low REF_{IN} frequencies, up to 20 MHz. With these programmable options, reference division ratios from 0.5 to 30 between REF_{IN} and the PFD are possible.

RF INPUT STAGE

The RF input stage is shown in Figure 21. It is followed by a two stage limiting amplifier to generate the CML clock levels needed

for the prescaler. Two prescaler options are selectable: a 4/5 and an 8/9. The 8/9 prescaler should be selected for N divider values greater than 80.

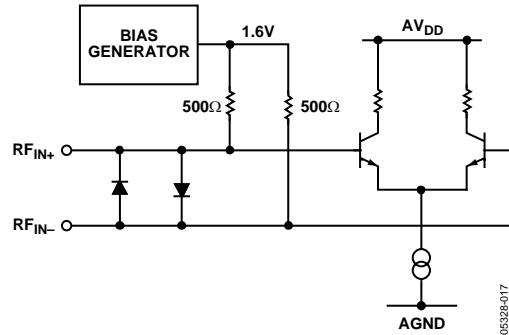


Figure 21. RF Input Stage

RF N Divider

The RF N divider allows a fractional division ratio in the PLL feedback path. The integer and fractional parts of the division are programmed using separate registers, as shown in Figure 22 and described in the next section. Integer division ratios from 23 to 255 are allowed and a 3rd order Σ-Δ modulator interpolates the fractional value between the integer steps.

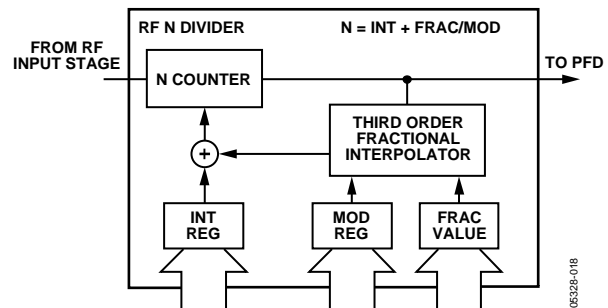


Figure 22. Fractional-N Divider

INT, FRAC, and MOD Relationship

The INT, FRAC, and MOD values, programmed through the serial interface, make it possible to generate RF output frequencies that are spaced by fractions of the PFD reference frequency. The N divider value, shown inside the square brackets of the following equation for the RF VCO frequency (RF_{OUT}), is made up of an integer part (INT) and a fractional part (FRAC/MOD):

$$RF_{OUT} = F_{PFD} \times [INT + (FRAC/MOD)] \quad (1)$$

where RF_{OUT} is the output frequency of the external VCO and F_{PFD} is the PFD reference frequency.

The value of MOD is chosen to give the desired channel step with the available reference frequency. Thereafter program the INT and FRAC words for the desired RF output frequency. See the Worked Example in the Programming section for more information.

PFD and Charge Pump

The PFD takes inputs from the R divider and N divider and produces up and down outputs with a pulse width difference proportional to the phase difference between the inputs. The charge pump outputs a net up or down current pulse of a width equal to this difference, to pump up or pump down the voltage that is integrated onto the loop filter, which in turn increases or decreases the VCO output frequency. If the N divider phase lags the R divider phase, a net up current pulse is produced that increases the VCO frequency (and thus the phase). If the N divider phase leads the R divider edge, then a net down pulse is produced to reduce the VCO frequency and phase. Figure 23 is a simplified schematic of the PFD and charge pump. The charge pump is made up of an array of 64 identical cells, each of which is fully differential. All 64 cells are active during fast lock and only one is active during normal operation. Since a single-ended control voltage is required to tune the VCO, an on-chip differential to single-ended amplifier is provided for this purpose. In addition, because the phase-lock loop only controls the differential voltage generated across the charge pump outputs, an internal common-mode feedback (CMFB) loop biases the charge pump outputs at a common-mode voltage of approximately 2 V.

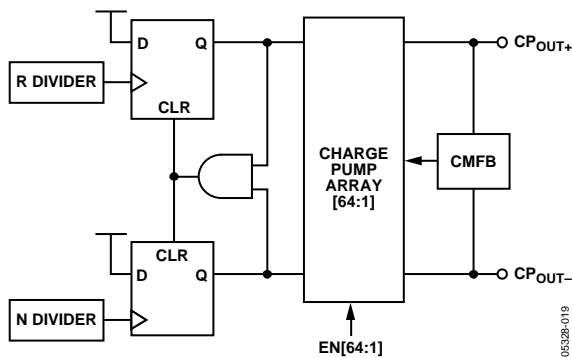


Figure 23. PFD and Differential Charge Pump Simplified Schematic

Differential Charge Pump

The charge pump cell (see Figure 24) has a fully differential design for best up-to-down current matching. Good matching is essential to minimize the phase offset created when switching the charge pump current from its high value (in fast lock mode) to its nominal value (in normal mode).

To pump up, the up switches are on and PMOS current is sourced out through CP_{OUT+}, which increases the voltage on the external loop filter capacitors connected to CP_{OUT+}. Similarly the NMOS current sink on CP_{OUT-} decreases the voltage on the external loop filter capacitors connected to CP_{OUT-}. Hence, the differential voltage between CP_{OUT+} and CP_{OUT-} increases. To pump down, PMOS current sources out through CP_{OUT-} and NMOS current sinks in through CP_{OUT+}, which decreases the (CP_{OUT+}, CP_{OUT-}) differential voltage. The charge pump up/down matching is improved by an order of magnitude over the conventional single-ended charge pump that depended on the

matching of two different device types. The up/down matching in this structure depends on how a PMOS matches a PMOS and an NMOS matches an NMOS.

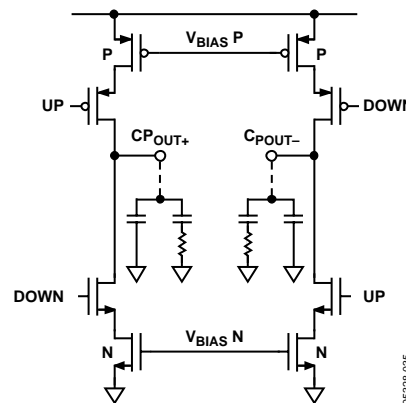


Figure 24. Differential Charge Pump Cell with External Loop Filter Components

Fast Lock Timeout Counters

Timeout counters, clocked at one quarter the PFD reference frequency, are provided to precisely control the fast locking operation (see Figure 25). Whenever a new frequency is programmed, the fast lock timers start and the PLL locks into wide BW mode with the 64 identical 100 μA charge pump cells active (6.4 mA total). When the ICP counter times out, the charge pump current is reduced to 1X by deselecting cells in binary steps over the next six timer clock cycles, until just one 100 μA cell is active. The charge pump current switching from 6.4 mA to 100 μA equates to an 8 to 1 change in loop bandwidth. The loop filter must be changed to ensure stability when this happens. That is the job of the SW1, SW2, and SW3 switches. The application circuit shown in Figure 36 shows how they can be used to reconfigure the loop filter time constants. They close to short out external loop filter resistors during fast lock and open when their counters time out to restore the filter time constants to their normal values for the 100 μA charge pump current. Since it takes six timer clock cycles to reduce the charge pump current to 1X, it is recommended that both switch timers be programmed to the value of the ICP timer plus 7.

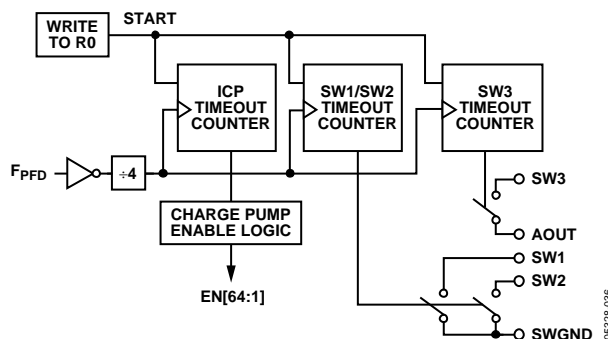


Figure 25. Fast Lock Timeout Counters

Differential Amplifier

The internal, low noise, differential to single-ended amplifier is used to convert the differential charge pump output to a single-ended control voltage for the tuning port of the VCO. Figure 26 shows a simplified schematic of the differential amplifier. The output voltage is equal to the differential voltage, offset by the voltage on the CMR pin according to the following equation:

$$V_{AOUT} = (V_{AIN+} - V_{AIN-}) + V_{CMR}$$

The CMR offset voltage is internally biased to three-fifths of V_{P3} , the differential amplifier power supply voltage, as shown in Figure 26. Connect a 0.1 μ F capacitor to ground to the CMR pin to roll off the thermal noise of the biasing resistors.

As can be seen in Figure 15, the differential amplifier output voltage behaves according to the previous equation over a 4 V range from approximately 1.2 V min up to $V_{P3} - 0.3$ V. However, fast settling is guaranteed only over a tuning voltage range from 1.8 V up to $V_{P3} - 0.8$ V. This is to allow sufficient room for overshoot in the PLL frequency settling transient.

Noise from the differential amplifier is suppressed inside the PLL loop bandwidth. For loop bandwidths >20 kHz, the $1/f$ noise has a negligible effect on the PLL output phase noise. Outside the loop bandwidth, the differential amplifier's noise FM modulates the VCO. The passive filter network following the differential amplifier, shown in the application circuit of Figure 36, suppresses this noise contribution to below the VCO noise from offsets of 400 kHz and above. This network has a negligible effect on lock time since it is bypassed when SW3 is closed while the loop is locking.

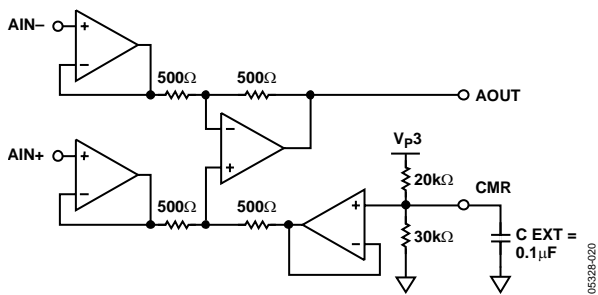


Figure 26. Differential Amplifier Block Diagram

MUX_{OUT} and Lock Detect

The output multiplexer on the ADF4193 allows the user to access various internal points on the chip. The state of MUX_{OUT} is controlled by M4 to M1 in the MUX register. Figure 35 shows the full truth table. Figure 27 shows the MUX_{OUT} section in block diagram form.

Lock Detect

MUX_{OUT} can be programmed to provide a digital lock detect signal. Digital lock detect is active high. Its output goes high if there are 40 successive PFD cycles with an input error of less than 15 ns. It stays high until a new channel is programmed or until the error at the PFD input exceeds 30 ns for one or more cycles.

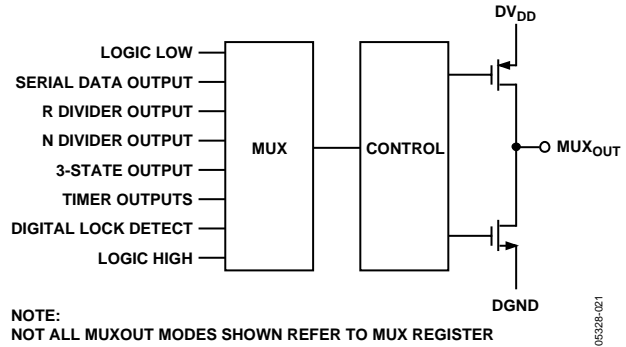


Figure 27. MUX_{OUT} Circuit

Input Shift Register

The ADF4193 serial interface section includes a 24-bit input shift register. Data is clocked in MSB first on each rising edge of CLK. Data from the shift register is latched into one of eight control registers, R0 to R7, on the rising edge of latch enable (LE). The destination register is determined by the state of the three LSBs (C3, C2, and C1) in the shift register. The three LSBs are DB2, DB1, and DB0, as shown in the timing diagram of Figure 2. The truth table for these bits is shown in Table 5. Figure 28 shows a summary of how the registers are programmed.

Table 5. C3, C2, and C1 Truth Table

Control Bits			Name	Register
C3	C2	C1		
0	0	0	FRAC/INT	R0
0	0	1	MOD/R	R1
0	1	0	Phase	R2
0	1	1	Function	R3
1	0	0	Charge Pump	R4
1	0	1	Power-Down	R5
1	1	0	MUX	R6
1	1	1	Test Mode	R7

REGISTER MAP

FRAC/INT REGISTER (R0)

RESERVED	8-BIT RF INT VALUE								12-BIT RF FRAC VALUE										CONTROL BITS				
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C3 (0)	C2 (0)	C1 (0)

MOD/R REGISTER (R1)

DBB	DBB	RESERVED	PRESCALER	DBB	DBB				12-BIT MODULUS										DBB	CONTROL BITS			
CP ADJ	REF/2			DOUBLER ENABLE	4-BIT RF R COUNTER				DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
F5	F4	0	F2	F1	R4	R3	R2	R1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C3 (0)	C2 (0)	C1 (1)

PHASE REGISTER (R2)

RESERVED	12-BIT PHASE											DBB	CONTROL BITS		
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	C3 (0)	C2 (1)	C1 (0)

FUNCTION REGISTER (R3)

RESERVED										CPO GND	RESERVED	PPD POLARITY	CONTROL BITS		
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	1	F3	1	F1	C3 (0)	C2 (1)	C1 (1)

CHARGE PUMP REGISTER (R4)

RESERVED										9-BIT TIME OUT COUNTER							TIMER SELECT	CONTROL BITS					
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1	C9	C8	C7	C6	C5	C4	C3	C2	C1	F2	F1	C3 (1)	C2 (0)	C1 (0)

POWER-DOWN REGISTER (R5)

PD DIFF AMP		PD CHARGE PUMP	CP 3-STATE	COUNTER RESET	CONTROL BITS		
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
F5	F4	F3	F2	F1	C3 (1)	C2 (0)	C1 (1)

MUX REGISTER (R6)

RESERVED	SIGMA-DELTA DITHER	RESERVED					MUXOUT				CONTROL BITS				
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	M11	M10	0	0	0	0	0	M4	M3	M2	M1	C3 (1)	C2 (1)	C1 (0)

TEST MODE REGISTER (R7)

RESERVED												CONTROL BITS			
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	C3 (1)	C2 (1)	C1 (1)

DBB = DOUBLE BUFFERED BIT(S)

Figure 28.

FRAC/INT REGISTER (R0)

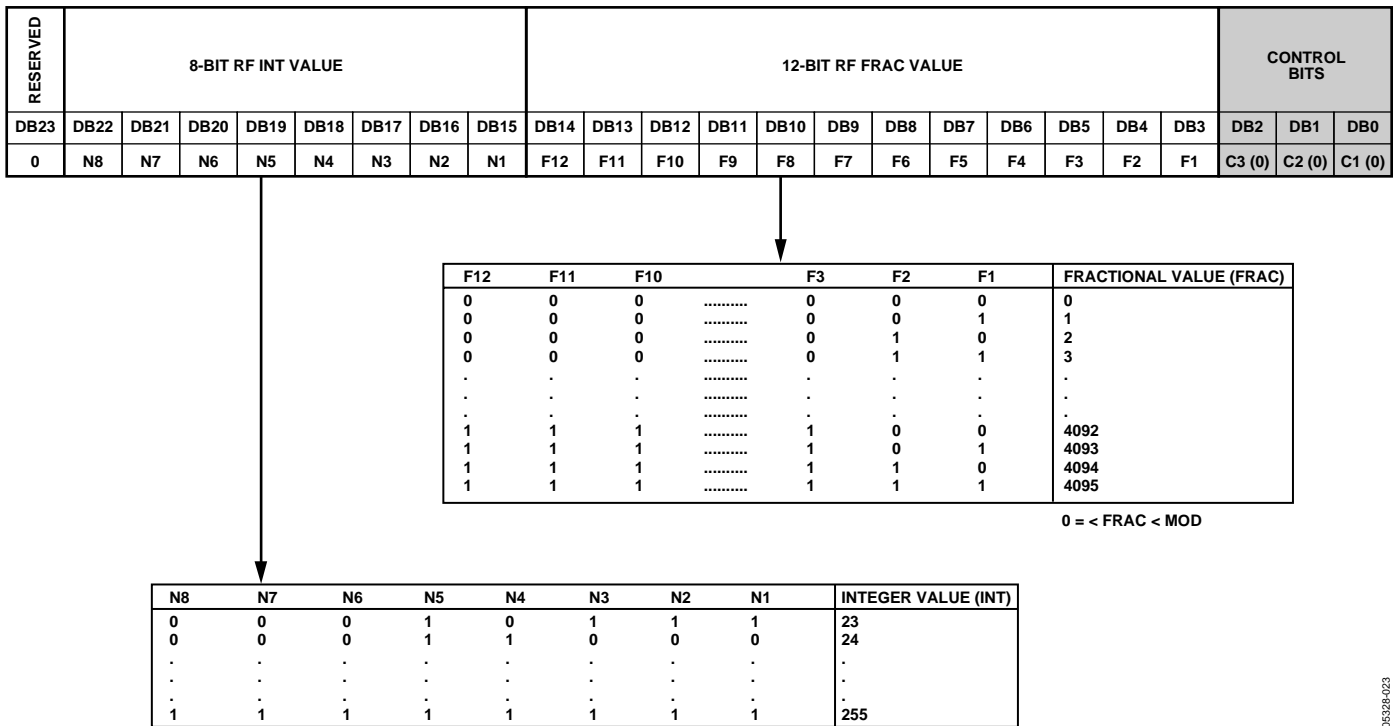


Figure 29.

R0, the INT/FRAC register, is used to program the synthesizer output frequency. On the next PFD cycle, following a write to R0, the N divider section is updated with the new INT and FRAC values, the PLL automatically enters fast lock mode; the charge pump current is increased to its maximum value and stays at this value until the ICP timeout counter times out, and switches SW1, SW2, and SW3 close and remain closed until the SW1/2 and SW3 timeout counters time out.

Once all registers have been programmed during the initialization sequence (see Table 8), all that is required thereafter to program a new channel is a write to R0. However, as described in the Programming section, it may be desirable to also program R1 and R2 register settings on a channel by channel basis. These settings are double buffered by the write to R0. This means that while the data is loaded through the serial interface on the respective R1 and R2 write cycles, the synthesizer is not updated with their data until the next write to Register R0.

Control Bits

The three LSBs, C3, C2, and C1, should be set to 0, 0, 0, respectively, to select R0, the INT/FRAC register.

Reserved Bit

DB23 is reserved and must be set to 0.

8-Bit INT Value

These eight bits set the INT value, which determines the integer part of the feedback division factor. All integer values from 23 to 255 are allowed. See the Worked Example section.

12-Bit FRAC Value

The 12 FRAC bits set the numerator of the fraction that is input to the Σ-Δ modulator. This, along with INT, specifies the new frequency channel that the synthesizer locks to, as shown in the Worked Example section. FRAC values from 0 to MOD - 1 covers channels over a frequency range equal to the PFD reference frequency.

MOD/R REGISTER (R1)

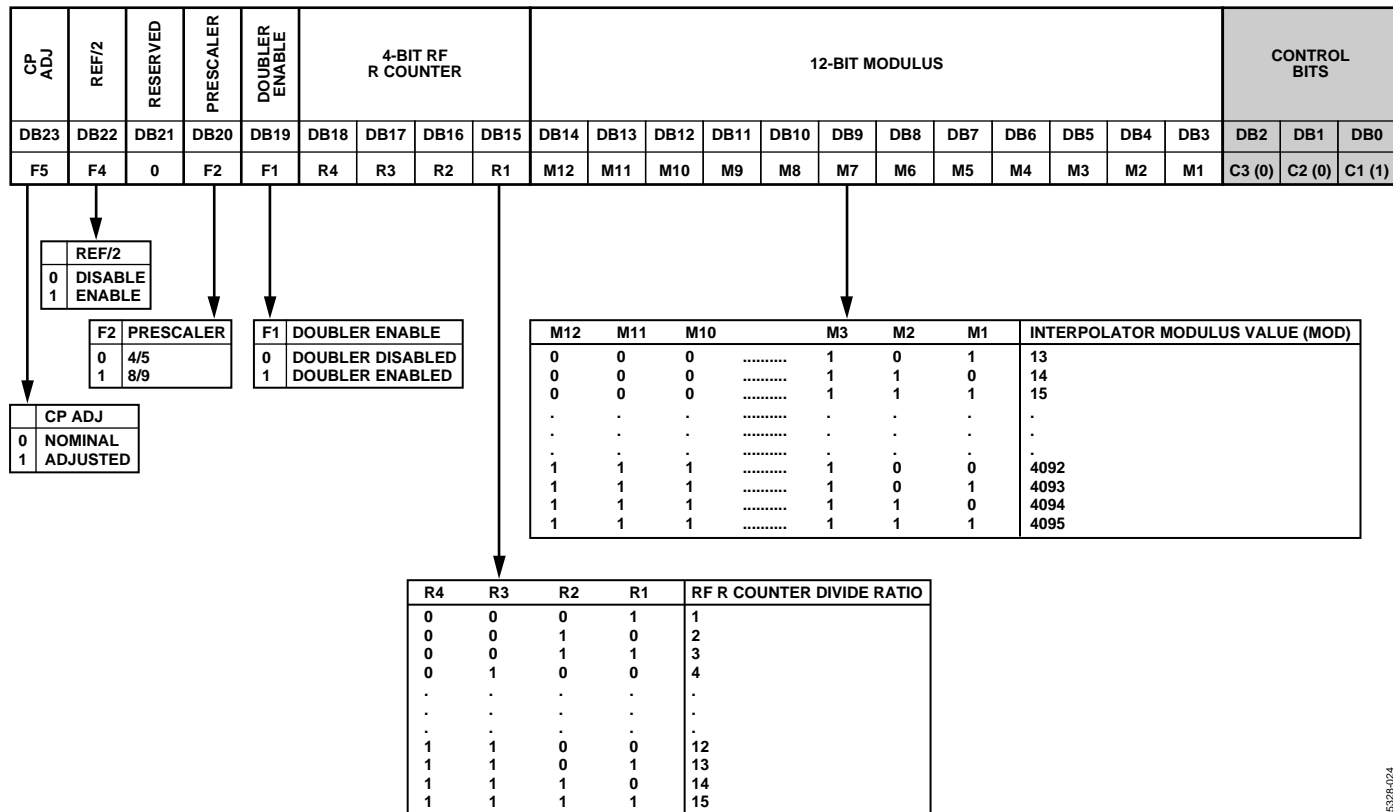


Figure 30.

This register is used to set the PFD reference frequency and the channel step size, which is determined by the PFD frequency divided by the fractional modulus. Note that the MOD, R counter, REF/2, CP Adj, and doubler enable bits are double buffered. They do not take effect until the next write to R0 (FRAC/INT register) is complete.

Control Bits

With C3, C2, and C1 set to 0, 0, 1, the MOD/R register (R1) is programmed.

CP Adj

When this bit is set to 1, the charge pump current is scaled up 25% from its nominal value on the next write to R0. When this bit is set to 0, the charge pump current stays at its nominal value on the next write to R0. See the Programming section for more information on how this feature may be utilized.

REF/2

Setting this bit to 1 inserts a divide by 2 toggle flip-flop between the R counter and PFD, which extends the maximum REF_{IN} input rate.

Reserved Bit

Reserved bit DB21 must be set to 0.

Doubler Enable

Setting this bit to 1 inserts a frequency doubler between REF_{IN} and the 4-bit R counter. Setting this bit to 0 bypasses the doubler.

4-bit RF R Counter

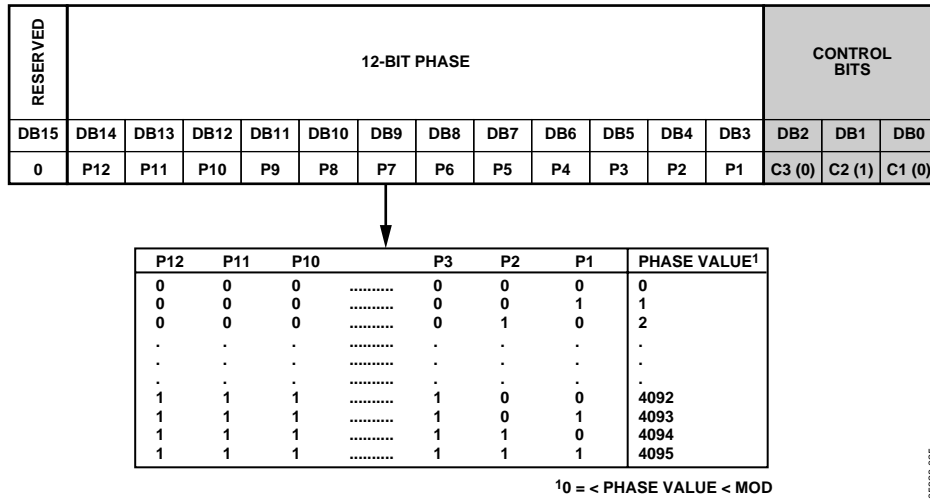
The 4-bit RF R counter allows the REF_{IN} frequency to be divided down to produce the reference clock to the PFD. All integer values from 1 to 15 are allowed. See the Worked Example section.

12-Bit Interpolator Modulus

For a given PFD reference frequency, the fractional denominator or modulus sets the channel step resolution at the RF output. All integer values from 13 to 4095 are allowed. See the Programming section for a Worked Example and guidelines for selecting the value of MOD.

06328-024

PHASE REGISTER (R2)



05326-025

Figure 31.

12-Bit Phase

The phase word sets the seed value of the Σ - Δ modulator. It can be programmed to any integer value from 0 to MOD. As the phase word is swept from 0 to MOD the phase of the VCO output sweeps over a 360° range in steps of 360°/MOD.

Note that the phase bits are double buffered. They do not take effect until the LE of the next write to R0 (FRAC/INT register). Thus if it is desired to change the phase of the VCO output frequency it is necessary to rewrite the INT and FRAC values to R0, following the write to R2.

The output of a fractional-N PLL can settle to any one of MOD possible phase offsets with respect to the reference, where MOD is the fractional modulus.

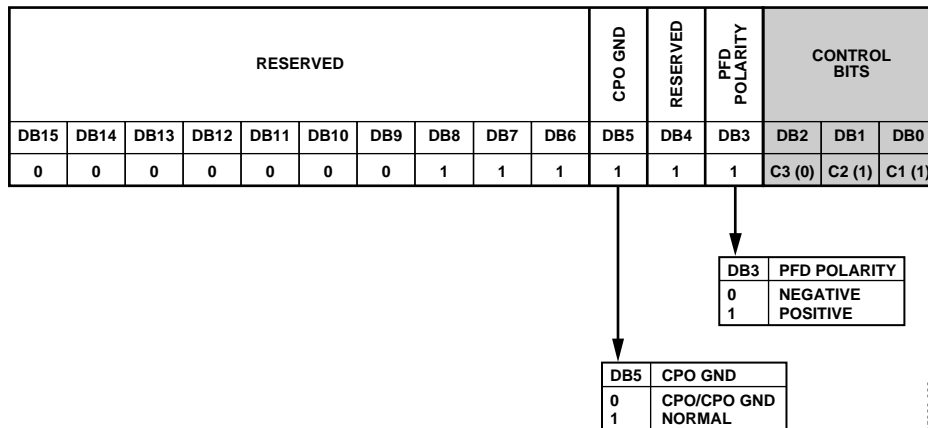
If it is desired to keep the output at the same phase offset with respect to the reference, each time that particular output frequency is programmed, then the interval between writes to R0 must be an integer multiple of MOD reference cycles.

If it is desired to keep the outputs of two ADF4193-based synthesizers phase coherent with each other, but not necessarily with their common reference, then it is only required to ensure that the write to R0 on both chips is performed during the same reference cycle. The interval between R0 writes in this case does not have to be an integer multiple of MOD cycles.

Reserved Bit

The reserved bit, DB15, should be set to 0.

FUNCTION REGISTER (R3)



05328-026

Figure 32.

R3, the function register (Control Bits 0, 1, 1) only needs to be programmed during the initialization sequence (see Table 8).

CPO GND

When CPO GND is low, the charge pump outputs are internally pulled to ground. This is invoked during the initialization sequence to discharge the loop filter capacitors. For normal operation, this bit should be high.

PFD Polarity

This bit should be set to 1 for positive polarity and set to 0 for negative polarity.

Reserved Bits

The DB15 to DB6 reserved bits should be programmed to hex code 007, and reserved bit DB4 should be set to 1.

CHARGE PUMP REGISTER (R4)

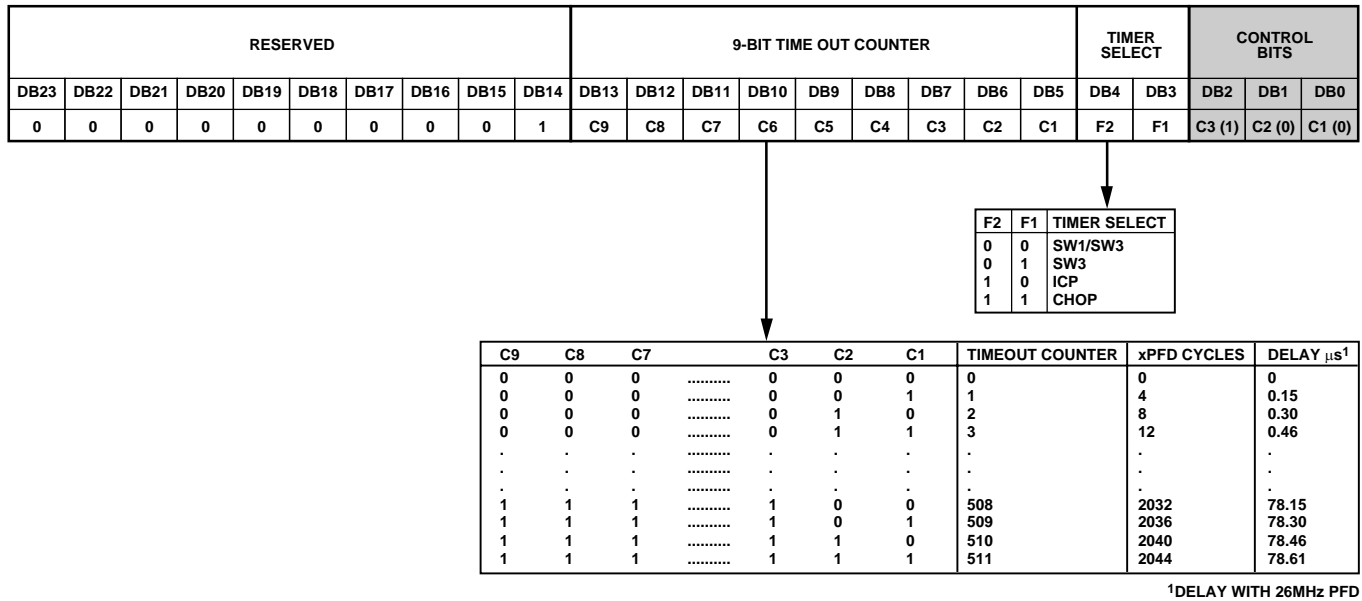


Figure 33.

Reserved Bits

Bits DB23 to DB14 are reserved and should be set to hex code 001 for normal operation.

9-Bit Timeout Counter

These bits are used to program the fast lock timeout counters. The counters are clocked at one-quarter the PFD reference frequency, therefore their time delay scales with the PFD frequency according to the following equation:

$$Delay(s) = (timeout\ counter\ value \times 4) / (PFD\ frequency)$$

For example, if 35 were loaded with timer select (00) with a 13 MHz PFD, then SW1/SW2 would be switched after

$$(35 \times 4) / 13\ MHz = 10.8\ \mu s$$

Timer Select

These two address bits select the timeout counter to be programmed. Note that to set up the ADF4193 correctly requires setup of these four timeout counters, therefore four writes to this register are required in the initialization sequence. Table 6 shows example values for a GSM Tx synthesizer with a 60 kHz final loop BW. See the Applications section for more information.

Table 6. Recommended Values for a GSM Tx LO

Timer Select	Timeout Counter	Value	Time (μ s) with PFD = 13 MHz
11	Chop	13	4
10	ICP	28	8.6
01	SW1/2	35	10.8
00	SW3	35	10.8

On each write to R0, all four timeout counters start. Switch SW3 closes until the SW3 counter times out. Similarly switches SW1/SW2 close until the SW1/SW2 counter times out. When the ICP counter times out, the charge pump current is ramped down from 64x to 1x in six binary steps. It is recommended that both the SW1/SW2 and SW3 timeout counter values are set equal to the ICP timeout counter value plus 7, as is the example of Table 6.

The chop timeout counter is redundant but should set to a value that times out while the PLL is in wide BW mode, for example equal to half the ICP timer value.

POWER-DOWN REGISTER (R5)

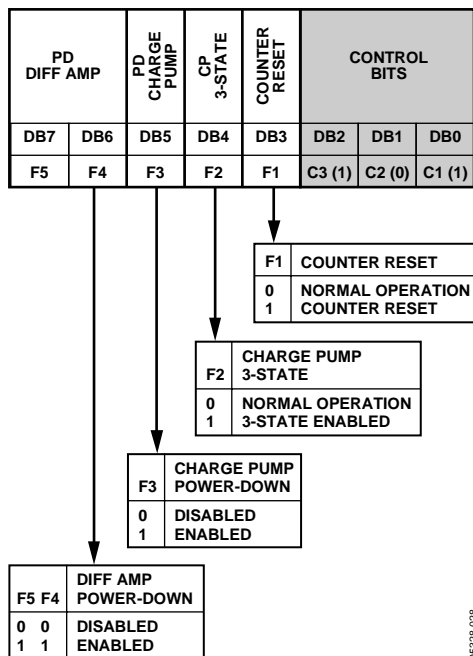


Figure 34.

R5, the power-down register (Control Bits 1, 0, 1) can be used to software power down the PLL and differential amplifier sections. After power is initially applied, there must be writes to R5 to clear the power-down bits and to R2, R1, and R0 before the ADF4193 will come out of power-down.

Power-Down Differential Amplifier

When DB6 and DB7 are set high, the differential amplifier is put into power-down. When DB6 and DB7 are set low, normal operation is resumed.

Power-Down Charge Pump

Setting DB5 high activates a charge pump power-down and the following events occur:

- All active dc current paths are removed, except for the differential amplifier.
- The R and N divider counters are forced to their load state conditions.
- The charge pump is powered down with its outputs in three-state mode.

- The digital lock detect circuitry is reset.
- The RF_{IN} input is debiased.
- The reference input buffer circuitry is disabled.
- The serial interface remains active and capable of loading and latching data.

For normal operation, Bit DB5 should be set to 0, followed by a write to R0.

CP Three-State

When this bit is set high, the charge pump outputs are put into three-state. With the bit set low, the charge pump outputs are enabled.

Counter Reset

When this bit is set to 1, the counters are held in reset. For normal operation this bit should be 0, followed by a write to R0.

MUX REGISTER (R6)

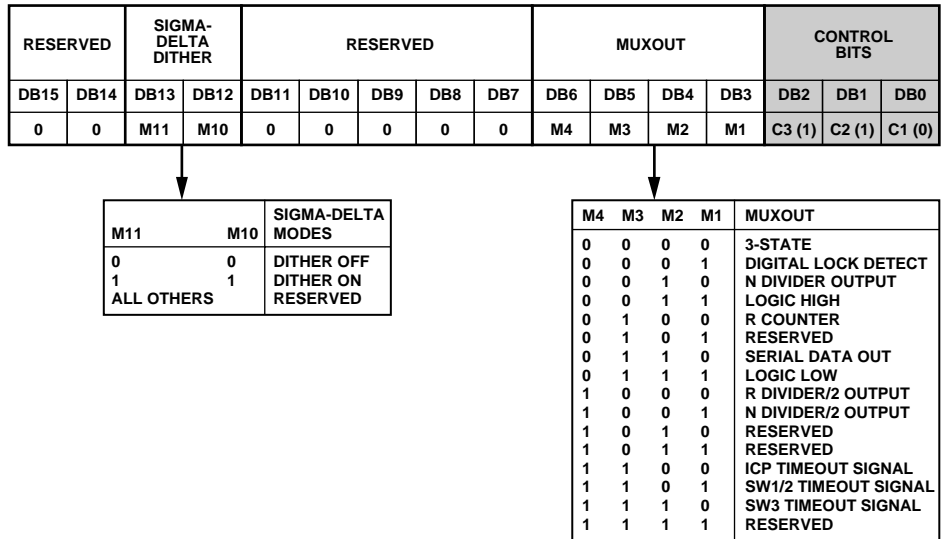


Figure 35.

With C3, C2, and C1 set to 1, 1, 0, respectively, the MUX register is programmed.

Σ - Δ Dither

Bits DB13 and DB12 switch the dithering on and off within the Σ - Δ modulator. When DB13 and DB12 are set high, dither is active. For lowest noise operation, DB13 and DB12 should be set low to disable dither.

Reserved Bits

The reserved bits must all be set to 0 for normal operation.

MUX_{OUT} Modes

The on-chip multiplexer is controlled by these bits. See Figure 35 for the truth table. This pin is useful for diagnosis since it allows the user to look at various internal points of the chip, such as the R divider and INT divider outputs.

In addition, it is possible to monitor the programmed timeout counter intervals on MUX_{OUT}. For example, if the ICP timeout counter was programmed to 65 (with a 26 MHz PFD), then, following the next write to R0, a pulse of width 10 μ s would be observed on the MUX_{OUT} pin.

Digital lock detect is available via the MUX_{OUT} pin.

PROGRAMMING

The ADF4193 can synthesize output frequencies with a channel step or resolution that is a fraction of the input reference frequency. For a given input reference frequency and a desired output frequency step, the first choice to make is the PFD reference frequency and the MOD. Once these are chosen the desired output frequency channels are set by programming the INT and FRAC values.

WORKED EXAMPLE

In this example of a GSM900 RX system, it is required to generate RF output frequencies with channel steps of 200 kHz. A 104 MHz reference frequency input (REF_{IN}) is available. The R divider setting that set the PFD reference is shown in Equation 1.

$$F_{PFD} = REF_{IN} \times [(1+D)/(R \times (1+T))] \quad (1)$$

where

REF_{IN} = input reference frequency

D = doubler enable bit (0 or 1)

R = 4-bit R counter code (0.. 15)

T = REF/2 bit (0 or 1)

The maximum PFD reference frequency of 26 MHz is chosen and the following settings are programmed to give an R divider value of 4:

Doubler enable = 0

R = 2

REF/2 = 1

Next the modulus is chosen to allow fractional steps of 200 kHz:

$$MOD = 26 \text{ MHz}/200 \text{ kHz} = 130 \quad (2)$$

Once the channel step is defined the following equation shows how output frequency channels are programmed:

$$RF_{OUT} = [INT + (FRAC/MOD)] \times [F_{PFD}] \quad (3)$$

where

RF_{OUT} = the desired RF output frequency

INT = integer part of the division

FRAC = numerator part of the fractional division

MOD = modulus or denominator part of the fractional division

For example, the frequency channel at 962.4 MHz is synthesized by programming the following values:

INT = 37

FRAC = 2

SPUR MECHANISMS

The following section describes the three different spur mechanisms that arise with a fractional-N synthesizer and how the ADF4193 can best be programmed to minimize them.

Fractional Spurs

The fractional interpolator in the ADF4193 is a 3rd order Σ-Δ modulator (SDM) with a modulus MOD that is programmable to any integer value from 13 to 4095. If dither is enabled then the minimum allowed value of MOD is 50. The SDM is clocked at the PFD reference rate (f_{PFD}) that allows PLL output frequencies to be synthesized at a channel step resolution of f_{PFD}/MOD.

With dither turned off, the quantization noise from the Σ-Δ modulator appears as fractional spurs. The interval between spurs is f_{PFD}/L, where L is the repeat length of the code sequence in the digital Σ-Δ modulator. For the 3rd order modulator used in the ADF4193 the repeat length depends on the value of MOD, as shown in Table 7.

Table 7. Fractional Spurs with Dither Off

Condition (Dither Off)	Repeat Length	Spur Interval
If MOD is divisible by 2, but not 3	2 × MOD	Channel step/2
If MOD is divisible by 3, but not 2	3 × MOD	Channel step/3
If MOD is divisible by 6	6 × MOD	Channel step/6
Otherwise	MOD	Channel step

With dither enabled, the repeat length is extended to 2²¹ cycles, regardless of the value of MOD, which makes the quantization error spectrum look like broadband noise. This can degrade the in-band phase noise at the PLL output by as much as 10 dB.

Therefore, for lowest noise, dither off is a better choice, particularly when the final loop BW is low enough to attenuate even the lowest frequency fractional spur. The wide loop bandwidth range available with the ADF4193 makes this possible in most applications.

Integer Boundary Spurs

Another mechanism for fractional spur creation involves interactions between the RF VCO frequency and the reference frequency. When these frequencies are not integer related (which is the whole point of a fractional-N synthesizer) spur sidebands appear on the VCO output spectrum at an offset frequency that corresponds to the beat note or difference frequency between an integer multiple of the reference and the VCO frequency.

These spurs are attenuated by the loop filter and are more noticeable on channels close to integer multiples of the reference where the difference frequency can be inside the loop bandwidth, thus the name integer boundary spurs.

ADF4193

The ADF4193's 8:1 loop bandwidth switching ratio makes it possible to attenuate all spurs to sufficiently low levels for most applications. The final loop BW can be chosen to ensure that all spurs are far enough out of band while meeting the lock time requirements with the 8× bandwidth boost.

The ADF4193's programmable modulus and R divider may also be used to avoid integer boundary channels. This option is described in a later section.

Reference Spurs

Reference spurs are generally not a problem in fractional-N synthesizers as the reference offset is far outside the loop bandwidth. However, any reference feedthrough mechanism that bypasses the loop can cause a problem. One such mechanism is feedthrough of low levels of on-chip reference switching noise out through the RF_{IN} pin back to the VCO, resulting in reference spur levels as high as -90 dBc. These spurs can be suppressed below -110 dBc by inserting sufficient reverse isolation, for example, through an RF buffer between the VCO and RF_{IN}. Also, care should be taken in the PCB layout to ensure that the VCO is well separated from the input reference to avoid a possible feedthrough path on the board.

POWER-UP INITIALIZATION

The recommended power-up sequence for the ADF4193 is first to power up the 3 V supplies (AV_{DD}, DV_{DD}, SDV_{DD}), followed by the 5 V supplies (V_{P1}, V_{P2}, V_{P3}). Next, the control registers must be initialized. A 14-step sequence is recommended, as described in Table 8.

The divider and timer setting used in the example in Table 8 is for a DCS1800 Tx synthesizer with a 104 MHz REF_{IN} frequency.

Table 8. Power-Up Initialization Sequence

Step	Register Bits	Hex Codes	Description
1	R5 [7:0]	FD	Set all power-down bits
2	R3 [15:0]	01DB	PD polarity = 1, ground CP _{OUT+} /CP _{OUT-}
Wait 10 ms			Allow time for loop filter capacitors to discharge
3	R7 [15:0]	0007	Clear test modes
4	R6 [15:0]	000E	Digital lock detect on MUX _{OUT}
5	R4 [23:0]	004464	SW1/SW2 timer = 10.8 μs
6	R4 [23:0]	00446C	SW3 timer = 10.8 μs
7	R4 [23:0]	004394	ICP timer = 8.6 μs
8	R4 [23:0]	0041BC	Chop timer = 4 μs
9	R2 [15:0]	00D2	Phase = 26
10	R1 [23:0]	520209	8/9 prescaler, doubler disabled, R = 4, toggle FF on, MOD = 65
11	R0 [23:0]	480140	INT = 144, FRAC = 40 for 1880 MHz output frequency
12	R3 [15:0]	01FB	PD polarity = 1, release CP _{OUT+} /CP _{OUT-}
13	R5 [7:0]	05	Clear all power-down bits
14	R0 [23:0]	480140	INT = 144, FRAC = 40 for 1880 MHz output frequency

The ADF4193 powers up after Step 13. It locks to the programmed channel frequency after Step 14.

CHANGING THE FREQUENCY OF THE PLL AND THE PHASE LOOK-UP TABLE

Once the ADF4193 has been initialized, a write to Register R0 is all that is required to program a new output frequency. The N divider is updated with the values of INT and FRAC on the next PFD cycle following the LE edge that latches in the R0 word. However, as explained later in this section, the settling time and spurious performance of the synthesizer can be further optimized by modifying R1 and R2 register settings on a channel by channel basis. These settings are double buffered by the write to R0. This means that while the data is loaded in through the serial interface on the respective R1 and R2 write cycles, the synthesizer is not updated with their data until the next write to Register R0.

The R2 register can be used to digitally adjust the phase of the VCO output relative to the reference edge. The phase can be adjusted over the full 360° range at RF with a resolution of 360°/MOD. In most frequency synthesizer applications, the actual phase offset of the VCO output with respect to the reference is unknown and does not matter. In such applications the phase adjustment capability of the R2 register can instead be used to optimize the settling time performance as described in the following section.

Phase Look-Up Table

The ADF4193's fast lock sequence is initiated following the write to Register R0. The fast lock timers are programmed so that after the PLL has settled in wide BW mode, the charge pump current is reduced and loop filter resistor switches are opened, to reduce the loop BW. The reference cycle on which these events occur is determined by the values preprogrammed into the timeout counters.

It may be observed from the phase locking plots of Figure 10 and Figure 13 that the lock time to final phase is dominated by the phase swing that occurs when the BW is reduced. Once the PLL has settled to final frequency and phase, in wide BW mode, this phase swing is the same regardless of the size of the synthesizer's frequency jump. The amplitude of the phase swing is related to the current flowing through the loop filter zero resistors on the PFD reference cycle that the SW1/SW2 switches are opened. In an integer-N PLL, this current is zero once the PLL has settled. In a fractional-N PLL the current is zero on average but varies from one reference cycle to the next, depending on the quantization error sequence output from the digital Σ-Δ modulator. Since the Σ-Δ modulator is all digital logic, clocked at the PFD reference rate, for a given value of MOD, the actual quantization error on any given reference cycle is determined by the value of FRAC and the PHASE word that the modulator is seeded with, following the write to R0. By choosing an appropriate value of PHASE corresponding to the

value of FRAC that is programmed on the next write to R0, the size of the error current on the PFD reference cycle the SW1/SW2 switches are opened, and thus the phase swing that occurs when the BW is reduced can be minimized.

With dither off, the fractional spur pattern due to the SDM's quantization noise also depends on the phase word the modulator is seeded with. Tables of optimized FRAC and phase values for popular SW1/SW2 and ICP timer settings can be downloaded from the ADF4193 product page. If making use of a phase table, first write phase to double buffered Register R2, then write the INT and FRAC to R0.

Avoiding Integer Boundary Channels

A further option when programming a new frequency involves a write to Register R1 to avoid integer boundary spurs. If it is found that the integer boundary spur level is too high, an option is to move the integer boundary away from the desired channel by reprogramming the R divider to select a different PFD frequency. For example, if $REF_{IN} = 104$ MHz and $R = 4$ for a 26 MHz PFD reference and $MOD = 130$ for 200 kHz steps, the frequency channel at 910.2 MHz has a 200 kHz integer boundary spur since it is 200 kHz offset from 35×26 MHz. An alternative way to synthesize this channel is to set $R = 5$ for a 20.8 MHz PFD reference and $MOD = 104$ for 200 kHz steps. The 910.2 MHz channel is now 5 MHz offset from the nearest

integer multiple of 20.8 MHz and the 5 MHz beat note spurs are well attenuated by the loop. Setting double buffered Bit R1 [23] = 1 (CP Adj) increases the charge pump current by 25%, which compensates for the 25% increase in N with the change to the 20.8 MHz PFD frequency. This maintains constant loop dynamics and settling time performance for jumps between the two PFD frequencies. The CP Adj bit should be cleared again when jumping back to 26 MHz-based channels.

The Register R1 settings necessary for integer boundary spur avoidance are all double buffered and do not become active on the chip until the next write to Register R0. Register R0 should always be the last register written to when programming a new frequency.

Serial Interface Activity

The serial interface activity when programming the R2 or R1 registers causes no noticeable disturbance to the synthesizers settled phase or degradation in its frequency spectrum. Thus, in a GSM application, it can be performed during the active part of the data burst. Since it takes just 10.2 μ s to program the three registers, R2, R1, and R0 with the 6.5 MHz serial interface clock rate typically used, this programming can also be performed during the previous guard period with the LE edge to latch in the R0 data, delayed until it's time to switch frequency.

APPLICATIONS

LOCAL OSCILLATOR FOR A GSM BASE STATION

Figure 36 shows the ADF4193 being used with a VCO to produce the LO for an GSM1800 base station. For GSM, the REF_{IN} signal can be any integer multiple of 13 MHz, the main requirement is that the slew rate is at least 350 V/μs. The 5 dBm, 104 MHz input sine wave shown, satisfies this requirement.

Recommended parameters for the various GSM/PCS/DCS synthesizers are given in Table 9.

Table 9. Recommended Setup Parameters

Parameter	GSM900		DCS1800/PCS1900	
	Tx	Rx	Tx	Rx
Loop BW	60 kHz	40 kHz	60 kHz	40 kHz
PFDF (MHz)	13	26	13	13
MOD	65	130	65	65
Dither	off	off	off	off
Prescaler	4/5	4/5	8/9	8/9
ICP Timer	28	78	28	38
SW1/2,SW3 Timers	35	85	35	45
VCO K _v	18 MHz/V	18 MHz/V	38 MHz/V	38 MHz/V

Loop BW and PFD Frequency

A 60 kHz loop BW is narrow enough to attenuate the PLL phase noise and spurs to the required level for a Tx low. A 40 kHz BW is necessary to meet the GSM900 Rx synthesizer's particularly tough phase noise and spur requirements at ±800 kHz offsets. To get the lowest spur levels at ±800 kHz offsets for Rx, the Σ-Δ modulator should be run at the highest oversampling rate possible. Thus for GSM900 Rx, a 26 MHz PFD frequency is chosen and MOD = 130 is required for 200 kHz steps. Since this value of MOD is divisible by two, certain FRAC channels have a 100 kHz fractional spur. This is attenuated by the 40 kHz loop filter and therefore is not a concern. However, the 60 kHz loop filter recommended for Tx has a closed-loop response that peaks close to 100 kHz. Hence a 13 MHz PFD with MOD = 65, which avoids the 100 kHz spur, is the best choice for a Tx synthesizer.

Dither

Dither off should be selected for the lowest rms phase error.

Prescaler

The 8/9 prescaler should be selected for the PCS and DCS bands, the 4/5 prescaler allows an N divider range low enough to cover the GSM900 Tx and Rx bands with either a 13 MHz of 26 MHz PFD frequency.

Timer Values For Tx

To comply with the GSM spectrum due to switching requirements, the Tx synthesizer should not switch frequency until the PA output power has ramped down by at least 50 dB. If it takes 10 μs to ramp down to this level then only the last 20 μs of the 30 μs guard period is available for the Tx synthesizer to lock to final frequency and phase.

In fast lock mode the Tx loop BW is boosted 8 times. This results in 480 kHz and therefore the PLL achieves frequency lock for a jump across the entire band in <6 μs. After this, the PA power may start to ramp up again and the loop BW can be restored to the final value. With the ICP timer = 28, the charge pump current reduction begins at ~8.6 μs. When SW1/SW2 and SW3 timers = 35, the current reaches its final value before the loop filter switches open at ~10.8 μs.

With these timer values, the phase disturbance created when the bandwidth is reduced settles back to its final value by 20 μs, in time for the start of the active part of the GSM burst. If faster phase settling is desired with the 60 kHz BW setting, then the timer values may be reduced further but should not be brought less than the 6 μs it takes to achieve frequency lock in wide BW mode.

Timer Values For Rx

The 40 kHz Rx loop BW is boosted 8 times, which results in 320 kHz during fast lock. With the Rx timer values shown, the BW will be reduced after ~12 μs, which allows sufficient time for the phase disturbance to settle back before the start of the active part of the Rx time slot at 30 μs. As in the Tx case, faster Rx settling can be achieved by reducing these timer values, their lower limit being determined by the time it takes to achieve frequency lock in wide BW mode. In addition, the PCS and DCS Rx synthesizers has relaxed 800 kHz blocker specifications and thus can tolerate a wider loop BW, which allows correspondingly faster settling.

VCO K_v

In general the VCO gain, K_v, should be set as low as possible to minimize the reference and integer boundary spur levels that arise due to feedthrough mechanisms. When deciding on the optimum VCO K_v, a good choice is to allow 2 V to tune across the desired band, centered on the available tuning range. With V_{P3} regulated to 5.5 V ± 100 mV, the tuning range available is 2.8 V.

Loop Filter Components

It is important for good settling performance that capacitors with low dielectric absorption are used in the loop filter. Ceramic NPO COG capacitors are a good choice for this application. A 2% tolerance is recommended for loop filter capacitors and 1% for resistors. A 10% tolerance is adequate for the inductor, L1.

ADI SimPLL SUPPORT

The ADF4193 loop filter design is supported on ADI SimPLL v2.7 and later. Example files for popular applications are available for download from the applications section of the

ADF4193 product page. Also available is an application note that outlines a loop filter design procedure that takes full advantage of the new degree of freedom in the filter design that the differential amplifier and loop filter switches provide.

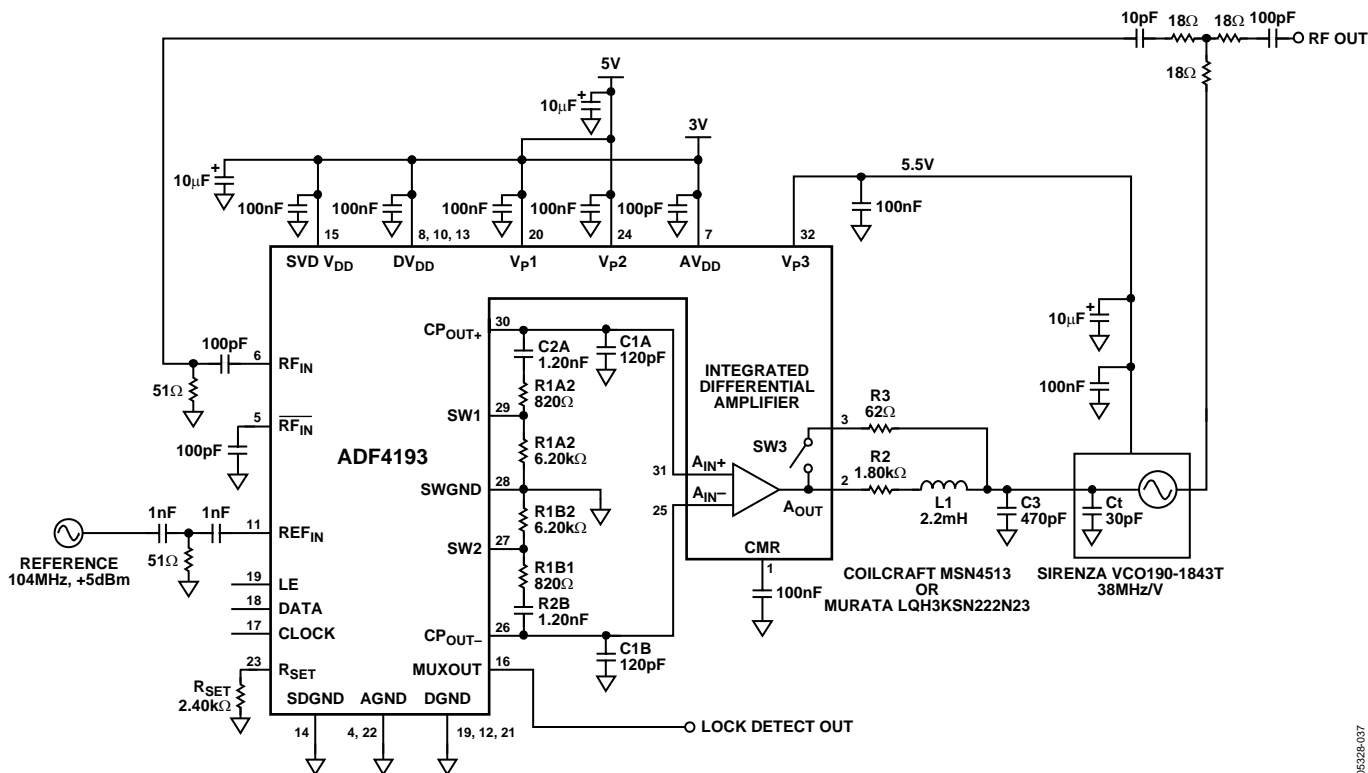


Figure 36. Local Oscillator for DCS1800 Tx Using the ADF4193

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ADF4193

INTERFACING

The ADF4193 has a simple SPI-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When LE goes high, the 24 bits that have been clocked into the input register on each rising edge of CLK are latched into the appropriate register. See Figure 2 for the timing diagram and Table 5 for the register address table.

The maximum allowable serial clock rate is 33 MHz.

ADuC812 Interface

Figure 37 shows the interface between the ADF4193 and the ADuC812 microconverter. Since the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The microconverter is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Some registers of the ADF4193 require a 24-bit programming word. This is accomplished by writing three 8-bit bytes from the microconverter to the device. When the third byte has been written, the LE input should be brought high to complete the transfer.

An I/O port line on the ADuC812 may also be used to detect lock (MUX_{OUT} configured as lock detect and polled by the port input).

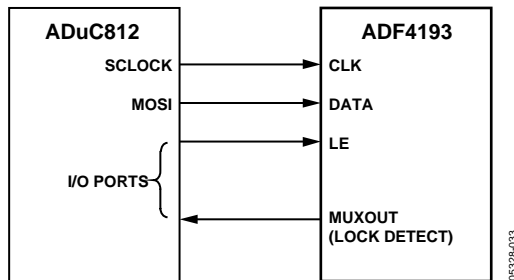


Figure 37. ADuC812 to ADF4193 Interface

ADSP2181 Interface

Figure 38 shows the interface between the ADF4193 and the ADSP21xx digital signal processor. The ADF4193 needs a 24-bit serial word for some writes. The easiest way to accomplish this using the ADSP21xx family is to use the auto-buffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for eight bits and use three memory locations for each 24-bit word. To program each 24-bit word, store the three 8-bit bytes, enable the autobuffered mode, and then write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

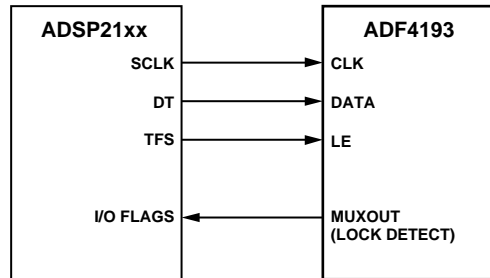


Figure 38. ADSP-21xx to ADF4193 Interface

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

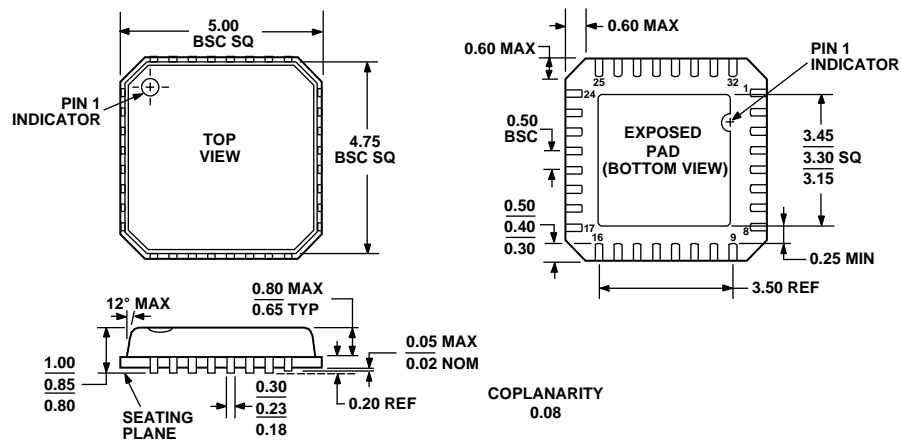
The lands on the chip scale package (CP-32) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the chip scale package has a central thermal pad.

The thermal pad on the printed circuit board should be at least as large as the exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias may be used on the printed circuit board thermal pad to improve the thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm and the via barrel should be plated with 1 oz copper to plug the via.

The user should connect the printed circuit board thermal pad to A_{GND}.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 39. 32-Lead Lead Frame Chip Scale Package [LFCS_P_VQ]
(CP-32-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADF4193BCPZ ¹	-40°C to +85°C	32-Lead LFCS_P_VQ	CP-32-3
ADF4193BCPZ-RL ¹	-40°C to +85°C	32-Lead LFCS_P_VQ	CP-32-3
ADF4193BCPZ-RL7 ¹	-40°C to +85°C	32-Lead LFCS_P_VQ	CP-32-3
EVAL-ADF4193EB1		Evaluation Board (GSM 1800)	
EVAL-ADF4193EB2		Evaluation Board (no VCO or loop filter)	

¹ Z = Pb-free part.

ADF4193

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ADF4193

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